Cypress Semiconductor
Product Qualification Report

QTP# 000505 VERSION 1.2
December, 2002

1 Meg Fast Asynchronous SRAM **R52FD-3 Technology, Fab 4**	
CY7C1021BV33	**64K x 16 Static RAM**
CY7C1019BV33	**128K x 8 Static RAM**

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
001603	New Technology Derivative R52FD-3 / 4Meg MoBL™ , CY62145V18	Jul 00
001208	New 2Meg FCP MoBL2™, CY62136V18, R52FD-3	Jul 00
000505	New 1Meg Asynchronous, CY7C1021BV33, R52FD-3	Oct 00

Note:
Based on using the same design rules and cells to establish a product family, as in JESD-47, Cypress qualifies devices within a product technology by using generic data from that product family to fill out the qualification requirements for those reliability stresses which test intrinsic reliability of the technology. Reliability stresses, such as ESD and Early Life, which are design sensitive are routinely performed in qualifications to ensure the specific design is reliable.

PRODUCT DESCRIPTION (for qualification)		
Qualification Purpose: Qualifies CY7C1021BV33 and CY7C1019BV33 (metal option) in qualified, R52FD Technology , Fab4		
Marketing Part #:	CY7C1021BV33 and CY7C1019BV33 (metal option)	
Device Description:	3.3V-3.6V, Commercial available in 48-ball FBGA, 44-lead TSOP II, 44-lead SOJ package.	
Cypress Division:	Cypress Semiconductor Corporation – Memory Product Division (MPD)	
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. F
What ID markings on Die:	7C1321F	

TECHNOLOGY/FAB PROCESS DESCRIPTION - R52FD-3			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 500Å TiW/6000Å Al-0.5%Cu/300Å TiW Metal 2: 300Å CoTi/8,000Å Al-0.5%Cu/300Å TiW
Passivation Type and Materials:		Oxide - Nitride	
Free Phosphorus contents in top glass layer(%):		0%	
Number of Transistors in Device:		25.2 million	
Number of Gates in Device:		8.4 million	
Generic Process Technology/Design Rule (µ-drawn):		CMOS, Double Metal /0.25 µm/0.3 FETS	
Gate Oxide Material/Thickness (MOS):		SiO_2 / 55 Å	
Name/Location of Die Fab (prime) Facility:		Cypress Semiconductor -- Bloomington, MN	
Die Fab Line ID/Wafer Process ID:		Fab4/R52FD-3	

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
44-pin SOJ (extended qual. to 32-pin)	CSPI-R
44-pin TSOP II	CSPI-R
48-Ball FBGA	TAIWAN-G

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	ZS444
Package Outline, Type, or Name:	44-lead Thin Small Outline Package (TSSOP II)
Mold Compound Name/Manufacturer:	Hitachi CEL 9200
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	>28%
Lead Frame Material:	Copper
Lead Finish, Composition / Thickness:	Solder Plate, 85%Sn, 15%Pb
Die Backside Preparation Method/Metallization:	N/A
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	Ablestik 8361H
Bond Diagram Designation	10-03790
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0um
Thermal Resistance Theta JA °C/W:	47°C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	11-20007
Name/Location of Assembly (prime) facility:	Cypress Philippines (CSPI-R)

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	Cypress Philippines (CSPI-R)
Fault Coverage:	100%

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	1) QTP #000505 Dynamic Operating Condition, 3.8V, 150C, Vcc Max 2) QTP #001603, QTP #001208 Dynamic Operating Condition, 2.875V, 150°C, >Vcc Max ()	P
High Temperature Operating Life Latent Failure Rate	1) QTP #000505 Dynamic Operating Condition, 3.8V, 150C, Vcc Max 2) QTP #001603 Dynamic Operating Condition, 2.875 V, 150°C, >Vcc Max	P
Electrostatic Discharge Human Body Model (ESD-HBM)	1) QTP #000505, QTP #001208, QTP #001603 MIL-STD-883, Method 3015.7 (2,200V)	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	1) QTP #000505, QTP #001208, QTP #001603 Cypress Spec. 25-00020 (500V)	P
Cold Life Test	1) QTP #000505 2) -30°C, 4.3V	P
Dynamic Latch-up Testing	1) QTP #001603 8V	P
Static Latch-up Sensitivity	1) QTP #000505, QTP #001208, QTP #001603 In accordance with JEDEC 17. Cypress Spec. 01-00081 (+/-300mA)	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[4]	Failure Rate[5]
High Temperature Operating Life Early Failure Rate[1]	10,982	1	N/A	N/A	91 PPM
High Temperature Operating Life[2],[3], Long Term Failure Rate	78,800DHRs	0	0.7	170	68 FIT

[1] A production burn-in of 24 Hrs at 150°C, 4.5V is required for the product
[2] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C
[3] Chi-squared 60% estimations used to calculate the failure rate.
[4] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A = The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

[5] **EFR Failure Rate based on QTP 001603, 001208, and 000505**

[5] **LFR Failure Rate based on QTP 001603 and 000505 .**

Reliability Test Data

QTP #: 000505

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERTING LIFE - EARLY FAILURE RATE, 150C, 3.8V, VCC MAX							
CY7C1021BV33-ZSC	4017457	*610038620*	CSPI-R	48H	4891	0	
STRESS: ESD-CDM, 500V							
CY7C1021BV33-ZSC	4017457	*610038620*	CSPI-R	500V	9	0	
CY7C1021BV33-ZSC	4017457	*610038620*	CSPI-R	750V	3	0	
STRESS: ESD-HBM, 2,200V							
CY7C1021BV33-ZSC	4017457	*610038620*	CSPI-R	2200V	9	0	
CY7C1021BV33-ZSC	4017457	*610038620*	CSPI-R	3300V	3	0	
STRESS: HIGH TEMP DYNAMIC OPERTING LIFE-LATENT FAILURE RATE, 150C, 3.8V, Vcc Max							
CY7C1021BV33-ZSC	4028592	*610041228*	CSPI-R	80H	260	0	
STRESS: STATIC LATCH-UP TESTING, +/-300mA							
CY7C1021BV33-ZSC	4017457	*610038620*	CSPI-R	COMP	3	0	

Reliability Test Data

QTP #: 001208

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS:HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 2.875V, Vcc Max							
CY62136V18-BAI	4004343	*610013847*	TAIWN-G	48H	3032	0	
STRESS: ESD-CHARGE DEVICE MODEL, 1,000V							
CY62136V18-BAI	4004343	*610013847*	KOREA-Q	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 3,300V							
CY62136V18-BAI	4004343	*610013847*	KOREA-Q	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 6.5V, +/-300mA							
CY62136V18-BAI	4004343	*610013847*	KOREA-Q	COMP	3	0	

Reliability Test Data

QTP #: 001603

Device	*Fab Lot #*	*Assy Lot #*	*Assy Loc*	*Duration*	*Samp*	*Rej*	*Failure Mechanism*
STRESS: DYNAMIC LATCH-UP TESTING, 8.V							
CY62145V18-BAI	4951635	*610009336*	TAIWN-G	COMP	5	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 6.5V, +/-300mA							
CY62145V18-BAI	4951635	*610009336*	TAIWN-G	COMP	3	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 2.875V, >Vcc Max							
CY62147V18-BAI	4005559	*610015521*	TAIWN-G	48	1500	0	
CY62145V18-BAI	4951635	*610009336*	TAIWN-G	48	1558	1	UNKNOWN, NOT VISUAL
STRESS: ESD-CHARGE DEVICE MODEL, 750V							
CY62145V18-BAI	4951635	*610009336*	TAIWN-G	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY62145V18-BAI	4951635	*610009336*	TAIWN-G	COMP	3	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 2.875V, >Vcc Max							
CY62145V18-BAI	4951635	*610009336*	TAIWN-G	80	116	0	
CY62145V18-BAI	4951635	*610009336*	TAIWN-G	500	116	0	
STRESS: SER TESTING							
CY62145V18-BAI	4951635	*610009336*	TAIWN-G	COMP	5	0	
STRESS: COLD LIFE TEST, -30C, 4.3V							
CYC7C43684AV-AC	4939102	*619933103*	TAIWN-G	500	48	0	
CYC7C43684AV-AC	4939102	*619933103*	TAIWN-G	1000	48	0	