Cypress Semiconductor
Fab Transfer Qualification Report

QTP# 001103 VERSION 2.1
May, 2003

CY2037A Wafer
L28-TSMC Technology in TSMC-2A, Taiwan

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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PRODUCT DESCRIPTION		
Qualification Purpose: To qualify fab transfer of CY2037AWAF/CY2037-2WAF, L28 Technology to TSMC-2A,Taiwan		
Marketing Part #:	CY2037AWAF / CY2037-2WAF	
Device Description:	3V or 5V, with the following configurations: Pad 8 and 9 = Vss1 Pad 1 and 2 = Vcc1 Pad 4, 6 and 7 = Input Only Pins Pad 11 = I/O and Output Pin All remaining = No connect	
Cypress Division:	Cypress Semiconductor Corporation - CPD WA Division	
Overall Die (or Mask) REV:		Rev. A
What ID markings on Die:	7C80380A	

TECHNOLOGY/FAB PROCESS DESCRIPTION - L28-TSMC			
Number of Metal Layers:	2	Metal Composition:	Metal 1: Ti 400Å /TiN1,000Å /AlSiCu 4,700Å /TiN 375Å Metal 2: Ti 1,500Å / AlSiCu 8,000Å / TiN 375Å
Passivation Type and Materials:		SiN 3,000Å /SOG 3,150Å /SiN 12,000Å	
Generic Process Technology/Design Rule (μ-drawn):		CMOS, Single Poly, Double Metal /0.65 μm	
Gate Oxide Material/Thickness (MOS):		SiO_2 / 125 A	
Name/Location of Die Fab (prime) Facility:		TSMC-2A, Taiwan	
Die Fab Line ID/Wafer Process ID:		TSMC-2A /L28-TSMC	

RELIABILITY TESTS PERFORMED

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc = 5.75V, 150°C,Vcc Max	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	1,000V MIL-STD-883,Method 3015.7	P
Ball Shear	Cypress Spec. 24-00024	P
Latch-Up Sensitivity	+/-200mA In Accordance with JEDEC 17. Cypress Spec.01-00081	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Acceleration Factor[3]	Failure Rate[4]
High Temperature Operating Life Early Failure Rate	1000	0	N/A	N/A	0 PPM
High Temperature Operating Life[1, 2] Long Term Failure Rate	181,660HRs	0	0.7	170	30 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

[4]Failure Rate based on L28-TSMC Technology, TMSC-2A qualification, QTP #99285.

RELIABILITY TEST DATA

QTP#: 99285[1]

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: DATA RETENTION (150C)							
CY2280-OC	CSPI-R	2937109	619927291/2/3	500	85	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 3.8V)							
CY2280-OC	CSPI-R	2937109	619927291/2/3	48	335	0	
CY2280-OC	CSPI-R	2937190	619928659/60/61	48	234	0	
CY2280-OC	CSPI-R	2937190	619928659/60/61	48	101	0	
CY2280-OC	CSPI-R	2942829	619933793/4/5	48	349	0	
STRESS: ESD-CHARGE DEVICE MODEL (1000V)							
CY2280-OC	CSPI-R	2937109	619927291/2/3	COMP	3	0	
CY2280-OC	CSPI-R	2937190	619928659/60/61	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2,200V)							
CY2280-OC	CSPI-R	2937109	619927291/2/3	COMP	3	0	
CY2280-OC	CSPI-R	2937190	619928659/60/61	COMP	3	0	
STRESS: HI-ACCEL SATURATION TEST (140C/85%RH/3.63V), PRECOND. 168 HRS 85C/85%RH							
CY2280-OC	CSPI-R	2937109	619927291/2/3	S/RE-FLOW	50	0	
CY2280-OC	CSPI-R	2937109	619927291/2/3	128	50	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 3.63V)							
CY2280-OC	CSPI-R	2937109	619927291/2/3	80	77	0	
CY2280-OC	CSPI-R	2937109	619927291/2/3	168	77	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 3.8V)							
CY2280-OC	CSPI-R	2937109	619927291/2/3	80	120	0	
CY2280-OC	CSPI-R	2937109	619927291/2/3	500	120	0	
CY2280-OC	CSPI-R	2937190	619928659/60/61	80	120	0	
CY2280-OC	CSPI-R	2937190	619928659/60/61	500	120	0	
CY2280-OC	CSPI-R	2942829	619933793/4/5	80	125	0	
CY2280-OC	CSPI-R	2942829	619933793/4/5	500	123	0	
STRESS: LOW TEMPERATURE OPERATING LIFE (-30C/8MHZ)							
CY2280-OC	CSPI-R	2937190	619928659/60/61	500	50	0	
STRESS: PRESSURE COOKER TEST, MSL 1 (121C, 100%RH)							
CY2280-OC	CSPI-R	2937109	619927291/2/3	S/RE-FLOW	53	0	
CY2280-OC	CSPI-R	2937109	619927291/2/3	168	53	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 168 HRS 85C/85%RH (MSL 1)							
CY2280-OC	CSPI-R	2937109	619927291/2/3	S/RE-FLOW	50	0	
CY2280-OC	CSPI-R	2937109	619927291/2/3	300	50	0	

[1] **QTP #99285,L28-TSMC Technology, TMSC-2A qualification.**

Reliability Test Data

QTP #: 001103

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C,5.75V, Vcc Max)							
CY2037A	2949740	*610003291/2/3*	CSPI-R	48	500	0	
CY2037A	2949740	*610003291/2/3*	CSPI-R	48	500	0	
STRESS: ESD-CDM (1000V)							
CY2037A	2949740	*610003291/2/3*	CSPI-R	COMP	3	0	
STRESS: ESD-HBM (2,200V)							
CY2037A	2949740	*610003291/2/3*	CSPI-R	COMP	3	0	
STRESS: STATIC LATCH-UP (12V)							
CY2037A	2949740	*610003291/2/3*	CSPI-R	COMP	6	0	