Low Frequency RFID Card Reader

AN52164

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Application Note Abstract

This application note details the implementation of low frequency RFID Card Reader based on CY8C24x23. The working principle of LF RFID card and CY8C24x23 are explained. The LF RFID card memory construction, the hardware schematic, and the firmware about data decoding algorithm are also described in detail.

Introduction

RFID (Radio Frequency Identification) is a means of identifying a person or object using a radio frequency transmission. This technology is used to identify, track, sort, or detect a wide variety of objects. Communication takes place between a reader (interrogator) and a transponder (silicon chip connected to an antenna). According to international standards, low frequency operates at around 125 KHz, high frequency at 13.56 MHz, and ultra high frequency at 860 to 960 MhZ. LF RFID is typically used in access control, animal tagging, and vehicle immobilizers. Popular design is based on MCU with a LF RFID interface chip such as EM4095 from EM Microelectronic and U2270 from Atmel. This application note takes the LF RFID reader as an example to illustrate the integration design of both reader interface IC and system control MCU into CY8C24x23/CY8C24x33.

Energy is transferred from the reader to the transponder through the magnetic field generated by the reader antenna. The reader antenna is part of a resonant circuit tuned to the RF operating frequency. The magnetic field generated by the reader induces a voltage in the transponder's resonant circuit which supplies power to the transponder. The current in the transponder coil generates a magnetic field, which influences the magnetic field generated by the reader. If the transponder's supply voltage is high enough, it works and transmits data by damping the resonant circuit according to the data stream. The data is modulated into the magnetic field and then transferred from transponder to reader. This results in slight voltage modulation at the reader antenna.

In this example design, CY8C24x23 handles 125 KHz PWM square wave generation, signal amplification and filtration, and data display.

Working Principle of LF RFID Reader

In the LF RFID reader, two devices exist in the system: the RFID reader and the transponder (or the tag). Figure 1 shows the system diagram. Two devices communicate through a 125 KHz RF field.

Figure 1 RFID Reader System

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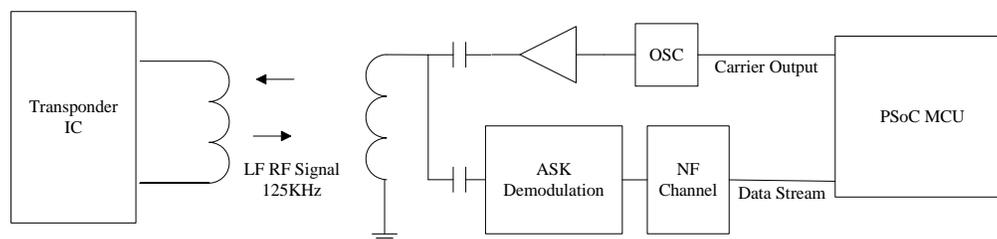
CY8C24x23 Overview

CY8C24x23 is one of the products of the PSoC® family and is compatible with other PSoC devices' architecture as illustrated in Figure 2. It is a programmable system-on-chip with On-Chip Controller device. Each CY8C24x23 PSoC device includes four digital blocks and six analog blocks. Depending on the PSoC package, CY8C22x45 provides up to 24 general-purpose IOs (GPIO) and 4K flash memory and a 256 byte SRAM data memory. Like other PSoC products, CY8C24x23 has some other fixed function on-chip resources such as I2C, UART, and MAC. CY8C24x23 also includes some optimized modules like On-Chip Precision Voltage Reference and User-Configurable Low Voltage Detection.

Figure 2 CY8C24x23 Block Diagram
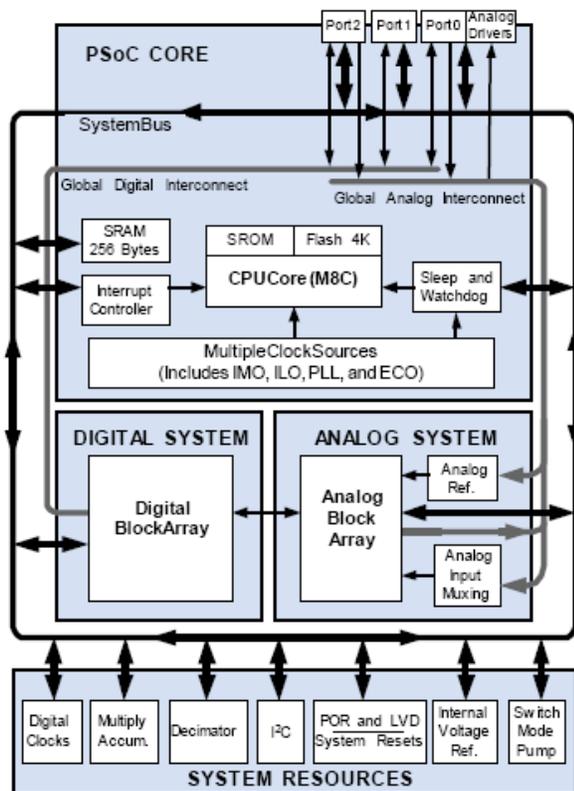
System Features

The LF RDIF demonstration is based on a simple adaptor board which is plugged onto CY3210 kits.

- DC 5V Power Jack

- 2x14 Connector (Female, 0.100 inch pitch)

- 2x8 Connector (Female, 0.100 inch pitch)

- 1x14 Connector for Character LCD

- 5-pin male header (0.100 inch) for I2C

- 5-pin male header for ISSP

- 10K potentiometer for adjusting LCD contrast

- Four red color LEDs indicating data rate

- One power LED

- One UART interface to communicate with PC

Future designs include more advanced features such as:

- Different types of card identification

- I2C communication with PC

System Hardware

The LF RFID reader board has a Low Frequency RF antenna, the ASK demodulation circuit, and the PSoC CY8C24423 chip. Figure 3 shows the block diagram of the main board.

Figure 3 Schematic of LF RFID Reader Adaptor Board
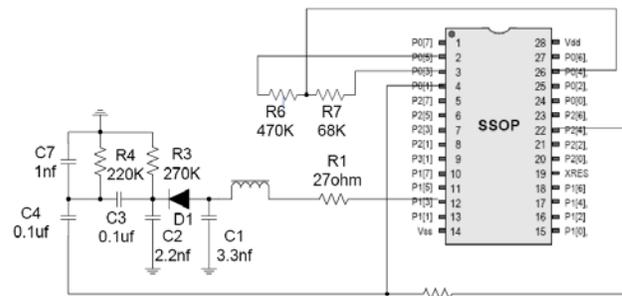
The mother board is the CY3210 kit board, which is responsible for LED lighting and data transmission to PC through UART interface.

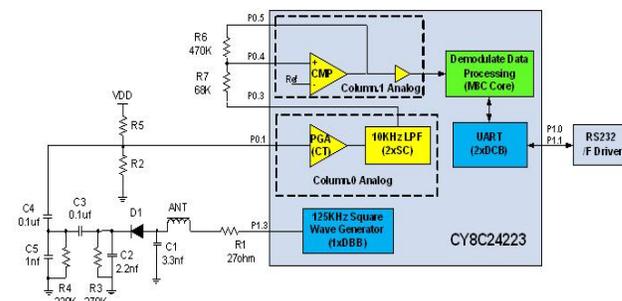Figure 4 Signal Demodulation Block Diagram

Figure 4 shows the method of RF signal energization and demodulation. PSoC internal resources are configured as PGA, low pass filter, and hysteresis comparator for the signal conditioning and data demodulating.

ASK Demodulation

A 125 KHz square wave is generated by a PSoC digital block, and then output through P1.3 to energize the antenna resonant circuit which is tuned at 125 KHz also. The resonant circuit is energized by series resonance. The useful signal appears as a very small amplitude modulation of the reader antenna voltage. D1 is the demodulation diode which is parallel to the high voltage resonant circuit. Figure 5 shows the waveform after D1.

Figure 5 Waveform After D1 Demodulation
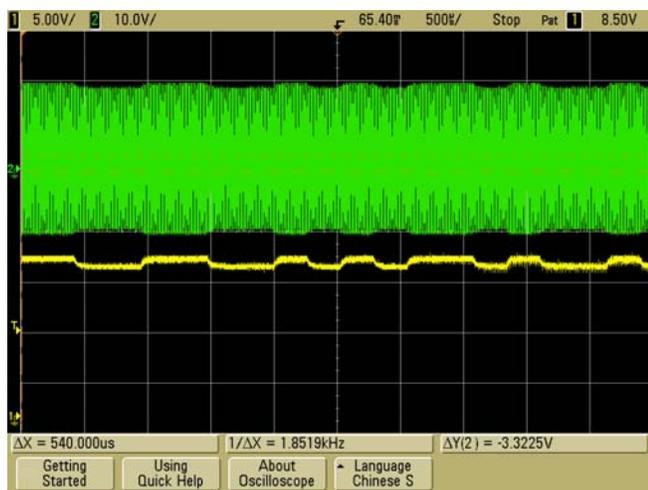
After D1, there is a passive high pass filter by R3, C3, then a low-pass filter by R4 and C5. Figure 6 shows the waveform on C5.

Figure 6 Waveform on C5 (After Passive Filters)
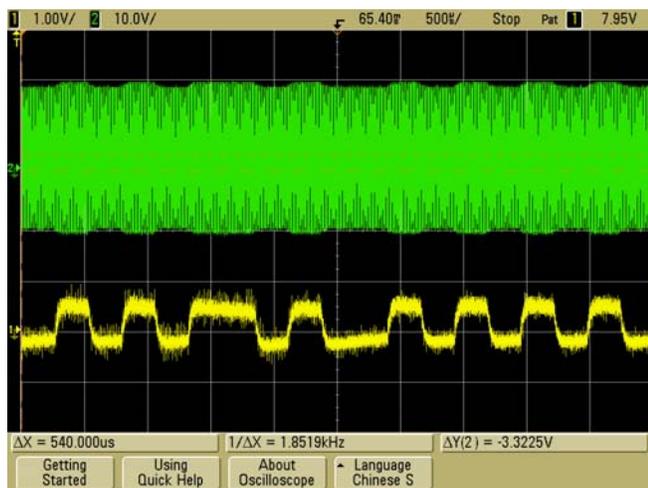
The signal then goes to PSoC through C4 to remove the DC signal and do a voltage shifting to Vdd/2 by P2.4 Port.

Signal Amplification and Noise Removal

A PSoC internal PGA operates the RF signal before it goes into a PSoC internal low-pass filter. You can extend the card detection distance by modifying PGA's gain value. The fully integrated low-pass filter (2-pole Butterworth) removes the remaining carrier signal and high frequency disturbances after demodulation. The upper cut-off frequency of the LPF depends on the customer selected frequency. The corner frequency is 10 KHz, comparing with 2K data rate and 125 KHz carrier waveform frequency.

Signal Reshaping and System Interrupt

PSoC outputs the signal after the LPF to P0.3 through the analog buffer; then it routes back to PSoC P0.4 through a register. The PSoC internal comparator works with two external resisters, R6 and R7, to be a hysteresis comparator. The hysteresis comparator reduces the noise sensitivity of the comparator and helps the comparator avoid oscillation. Thus the data stream is read out easily by the microcontroller. The comparator bus is used to interrupt M8C core. In order to show the ultimate interrupt signal, we output the signal through a temporary digital buffer to an outside pin. Figure 7 shows the signal on the CompBus and the original modulated signal.

Figure 7 Interrupt and the Original Signal

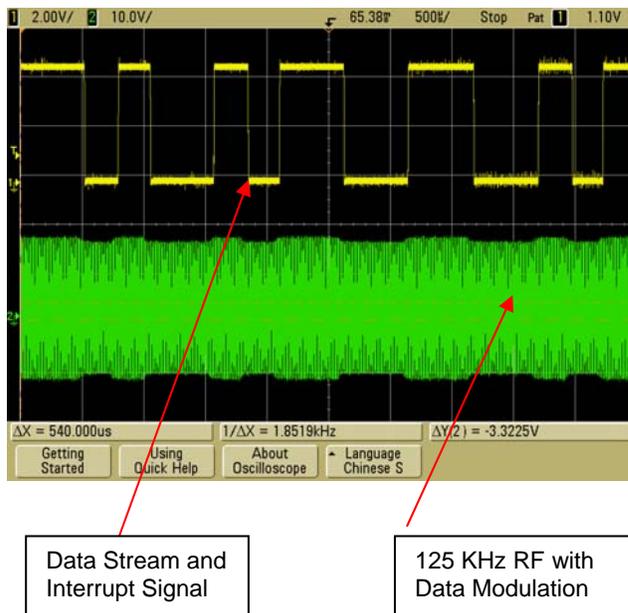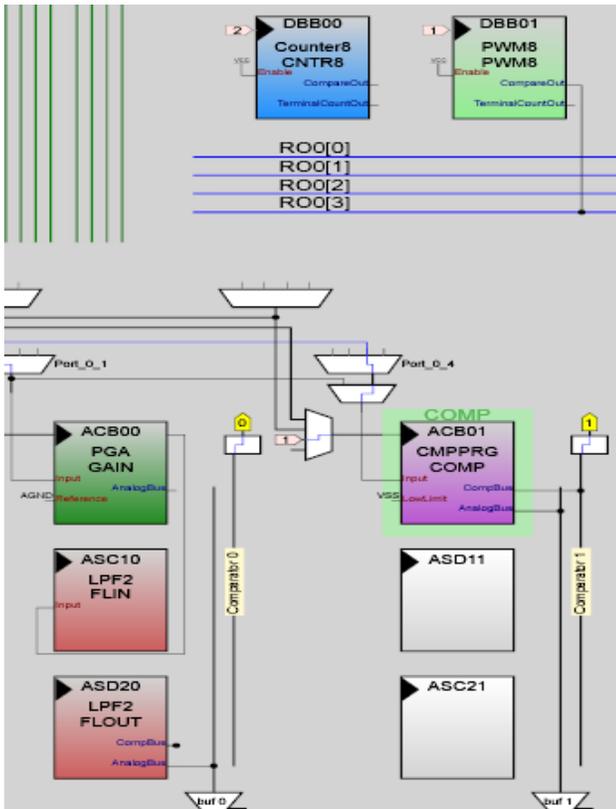Data Stream and Interrupt Signal

125 KHz RF with Data Modulation

Figure 8 PSoC Chip Used Resources

Board Connector Definition and Description

The board connector pins' definition are the same as the CY8C24423 pins' definition.

System Firmware

EM4100 RFID Data Encoding

When the EM4100 RFID card sends data, the output signal is Manchester encoded. It uses a rising edge to send bit 1, and uses a falling edge to send bit 0. Before starting to send the specific data, EM4100 RFID sends 9 bit 1 first. It means that the data stream has 9 consecutive rising edges at first.

Figure 9 Manchester Data Encoding
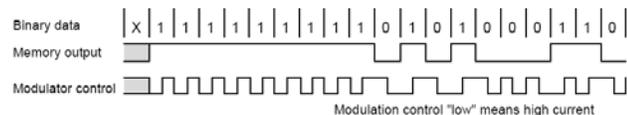
EM4100 Memory Structure

As shown in Figure 9, the EM4100 contains 64 bits divided into five groups of information. The header is composed of nine first bits which are all "1"s. The header is followed by 10 groups of four data bits with one even row parity bit. The last group consists of four even column parity bits without row parity bit. The last bit S0 is a stop bit which is "0".

Figure 10 EM4100 Memory Structure
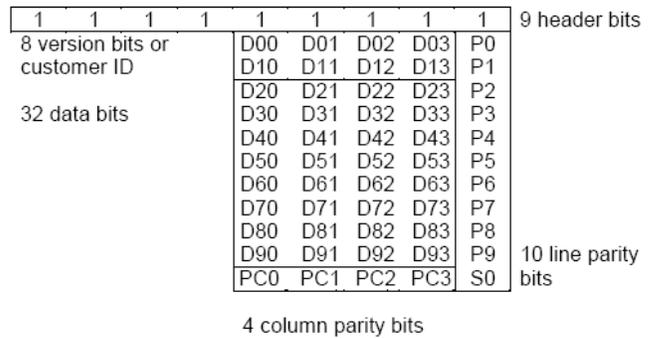
The firmware has four parts: the CompBus Interrupt's time interval measurement mechanism, signal start detection algorithm, the Manchester decoding algorithm, and Parity-bit check procedure. Figure 11 shows the high level firmware flowchart.

Figure 11 Firmware Flowchart
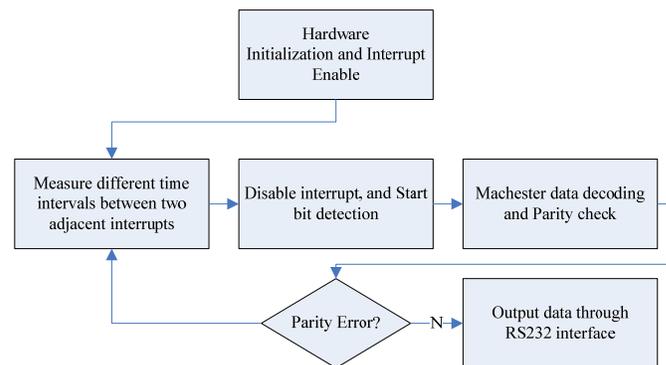
PSoC Digital Block and Analog Resources Consuming

The following table lists the digital blocks, analog blocks, and other resources consumed in the RFID reader system.

Table 1 RFID Reader System Resources

Name	Description
DBB00	Counter8 for CompBus1's Interrupt interval measurement
DBB01	PWM8 for 125 KHz
DCB02	UART TX and RX
DCB03	
ACB00	PGA for Signal Amplification
ACB01	Hysteresis Comparator and Interrupt Source
ASC10	2-pole Butterworth low pass filter
ASC20	

Figure 12 System Interconnection
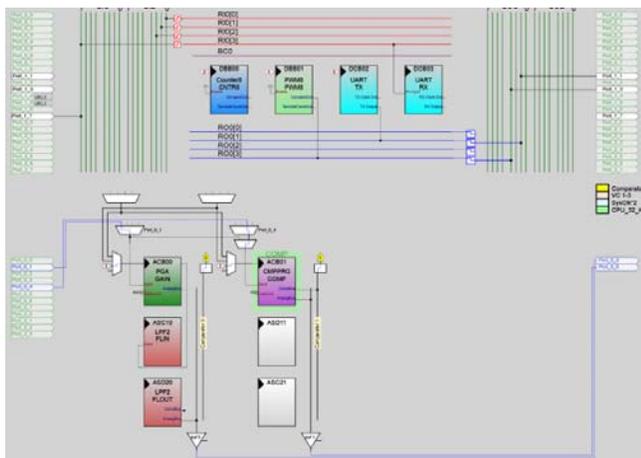
CompBus 1's Interrupt Time Interval Measurement

In the AnalogColumn1's interrupt procedure, we record the down counter's temporary value when the interrupt happens. For the worst case, when the data are all zeros, there are 55 signal falling edges in the data stream. To ensure that a start signal bit can be found in the recorded data sequence, at least 119 (55*2+9) data records are needed. The time interval between two rising edge interrupts is measured by subtracting two adjacent counter values.

The following is the main source code to measure time intervals:

Global Variables:

```
unsigned char Value_Valid=0;
unsigned char Temp_Count=0;

In the interrupt procedure:
void PSoC_COMP_ROUTINE(void)
{
Temp_Count=Counter8_bReadCounter();
Value_Valid=1;
}
```

In the main procedure:

```
while(i<121){
    while(Value_Valid==0);
    Value_Valid=0;
    Count_Value[i++]=Temp_Count;
}
for(i=0;i<120;++i){
    Count_Value[i]-=Count_Value[i+1];
}
```

Data Start Bit Detection

For the output data sequence, there are four different types of waveform between two adjacent rising interrupts.

- Type A:

The time interval is about 530 us, so the counter value is around 0x42. Note that the input clock's period is 8 us.

- Type B:

The time interval is about 800 us, so the counter value is around 0x64.

- Type C:

The time interval is also about 800 us, so the counter value is around 0x64.

- Type D:

The time interval is about 1060 us, so the counter value is around 0x84.

Because the start signal is characterized by one "0" and nine consecutive "1"s in the data sequence, we must find one Type C or D waveform followed by eight consecutive Type A waveforms to identify the start signal. This way, the possible data bit start position is detected. Note that when there is one "1" followed by ten or more "0"s in the data sequence, the waveform is the same as the start signal waveform. To check out this error, use the parity bit. If there is a parity error when decoding the data bit stream from the specified position, use the next possible data bit start position.

Figure 13 Flowchart of Start Bit Detection

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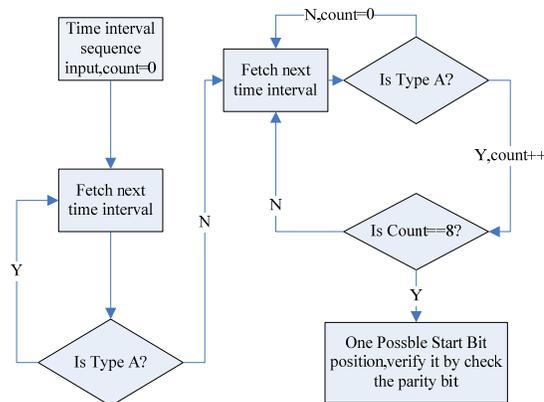
Manchester Data Decoding Algorithm

From the start position, the default data bit value is "1". Note that there must be one Type B waveform in between two consecutive Type C waveforms, and vice versa. In order to distinguish Type B and Type C, set a type flag to identify, and the default value for this flag is "0".

For waveform type A, only one data bit has been sent. The value is the default data value.

For waveform type B, only one data bit has been sent, but the value has been changed. If the previous default value is 1, this sent value is 0, and vice versa. Then we change the type flag to 1 and change the default value to its opposite value.

For waveform type C, two data bits have been sent. The first data bit value is the default data value, and the second is the opposite of the default value. Then we change the type flag to be 0 and change the default value to be its opposite value.

For waveform type D also, two data bits have been sent. The first data bit value is the opposite of the default data value, and the second is the default value.

After we decode 55 data bits, we can use the parity bit to identify whether we found the correct start signal.

Figure 14 Flowchart of Manchester Data Decoding
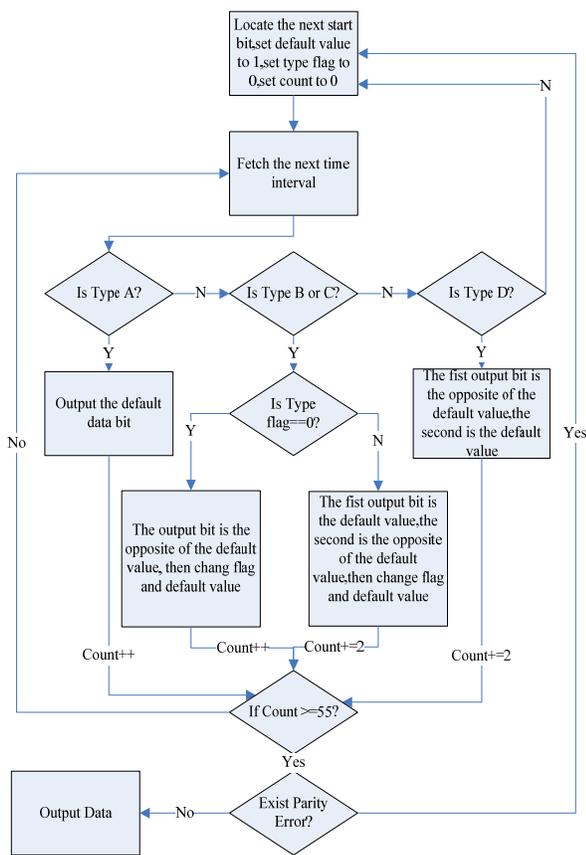
Summary

This application note describes the low frequency RFID card reader system based on PSoC chip CY8C24x23. CY8C24x23 can replace the low frequency RFID card reader interface IC and show the PSoC integration value. The experiment circuit can read the EM4100 RFID card at a range about 5 to 6cm, which is almost the same as EM4905 performance. The reachable distance can be extended by optimizing the antenna driving circuit.

Appendix1: Hardware Schematics

Figure 15 Schematic Drawing of LF RFID Reader Main Board

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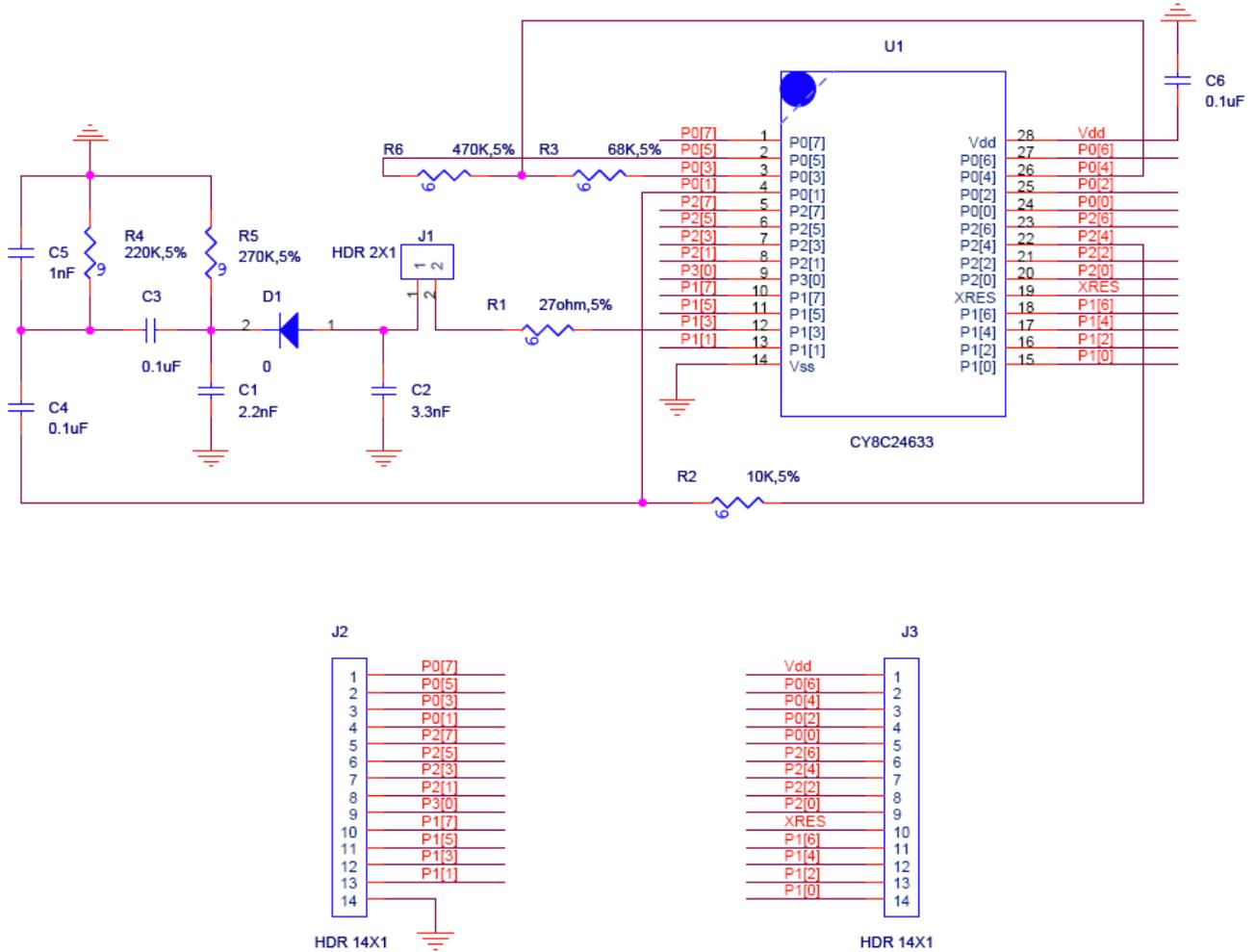
Figure 16 Schematic Drawing of CY3210 Kit Board (UART Interface and LED CY3210 Kit Board)
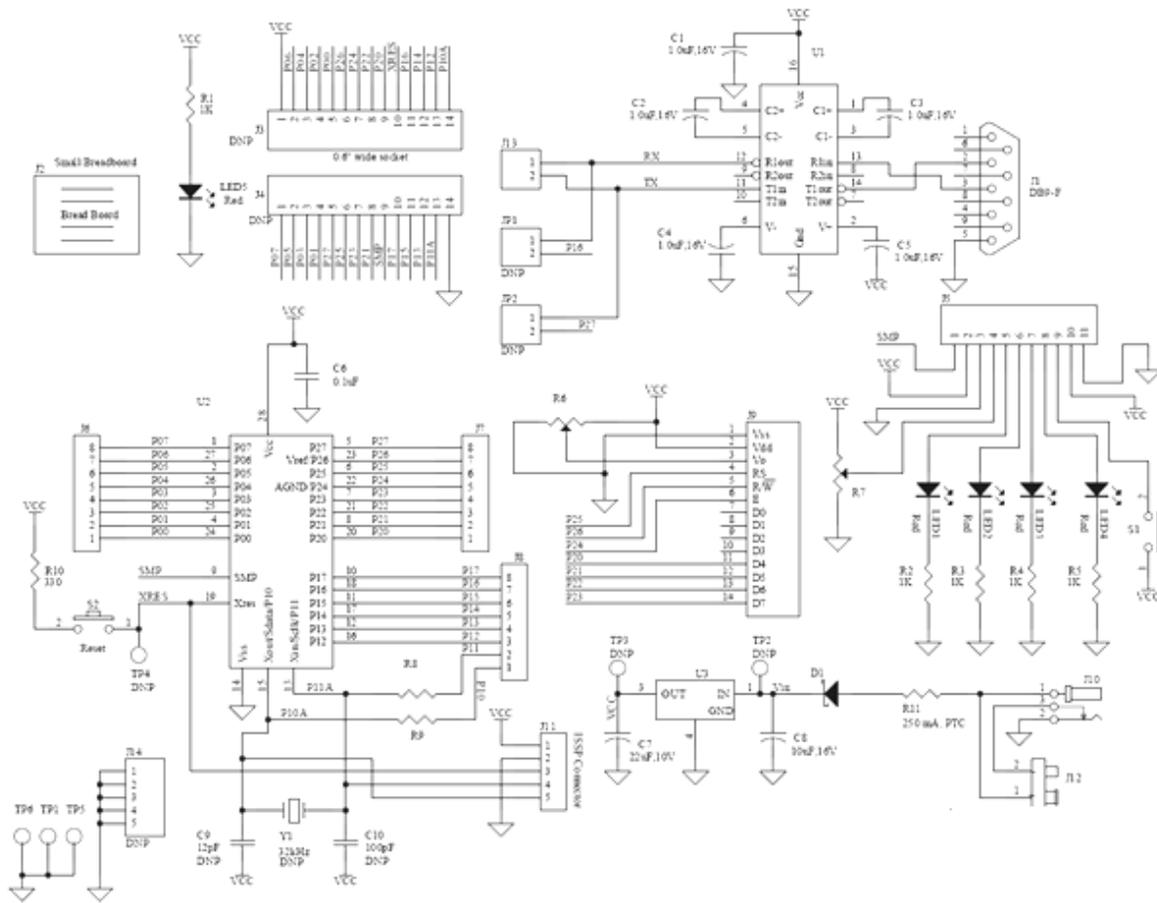
Appendix2: Board Photograph

Figure 17 LF RFID Reader Demo Board Photograph
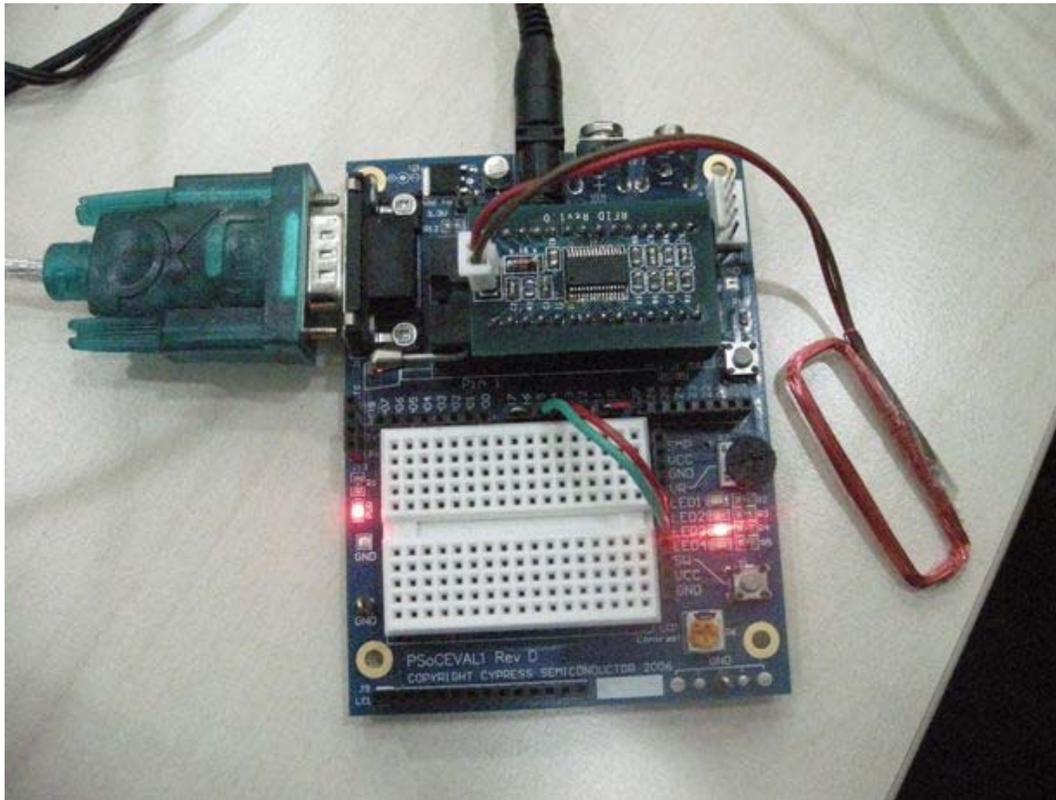
Figure 18 LF RFID Reader Test Experiment Photograph
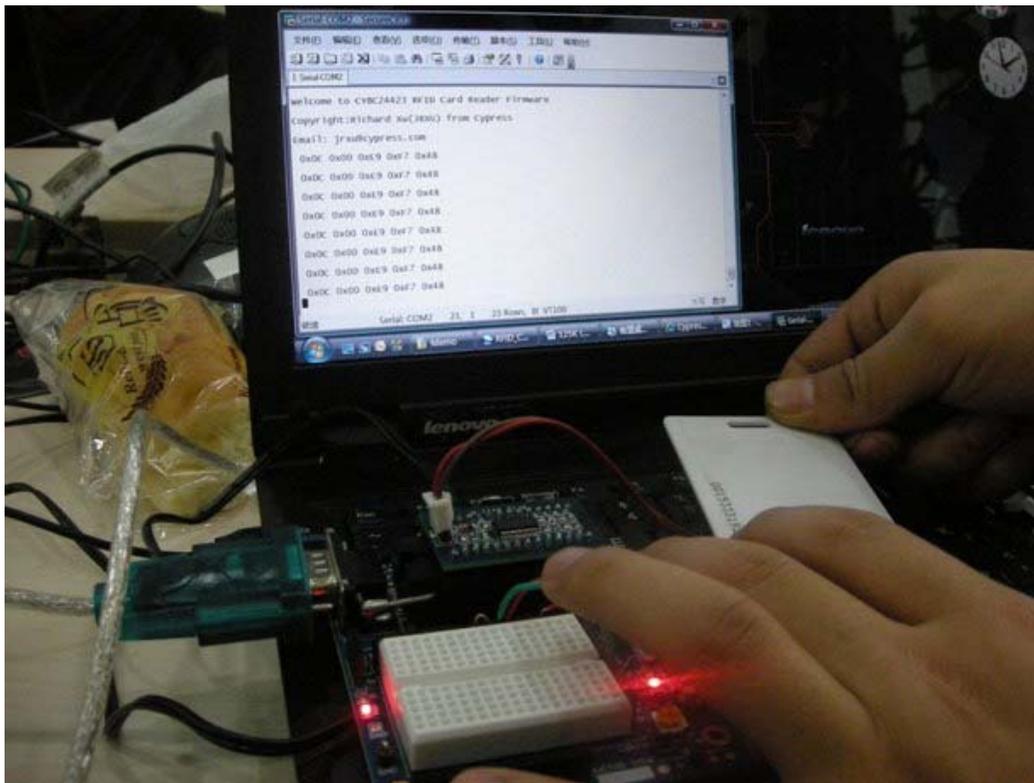
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