Ceramic Resonators Ease Space Constraints when Designing High-Speed USB into Handsets

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Executive Summary

With an increasing number of consumers carrying and transferring large multimedia files such as MP3 and MPEG into their portable devices, leading consumer electronics manufacturers are rushing to design HS-USB into their products. Any designer looking at adding HS-USB will immediately run into the common hurdles of optimizing size, power, and cost. Currently, few application processors and baseband processors integrate HS-USB due to the difficulty of integrating the PHY onto small process technologies, so designers must add a separate HS-USB controller to their designs. One large component that always accompanies a HS-USB peripheral controller is a crystal. This article will discuss the use of small foot-print, price-comparable ceramic resonators that make designing HS-USB into space-constrained applications a less daunting task.

Multimedia and Its Impact on Handset Requirements

Cell phones today are equipped with more multimedia capabilities than ever. Our favorite phones boast cameras up to the 2-3 mega pixel range, making them very suitable for capturing photos and videos on the go – no more missing a baby's first steps or first words. Phones are also doubling as portable media players and consumers can now download music via services like Verizon's Vcast on the road and take them home to their computers. To support these bandwidth intensive multimedia features, many phones come with the ability to add 2GB-8GB of expandable storage in the form of flash or disk based mass storage like Secure Digital or CE-ATA. This enables users to accumulate a considerable amount of multimedia before offloading onto their computers. New photos, videos, and music are created or downloaded, while older files are moved onto the computer for archiving. With standalone Digital Still cameras (DSCs) and Portable Media Players (PMPs), consumers are already accustomed to fast transfers via high-speed USB (HS-USB 480Mbps).

Most cell phones today, however, support full-speed USB (FS-USB 12Mbps), which only provides enough throughput for simple synchronization of address book and calendar. To compare the difference between full-speed USB and high-speed USB in terms of the end user experience, consider how long it takes to transfer ~100MB of music, which is 25 songs at 4MB per MP3. Full-speed USB takes 13 minutes to transfer 25 songs while high-speed USB takes a mere 33 seconds. The impact of transfer speeds on the end user experience is clear and with the growing usage model of cell phones acting as both camera and PMP, cell phone designers are responding quickly by adding high-speed USB into existing phones.

The Problem Facing Adding High-Speed USB

Challenge to Integrate

There are few application processors and baseband processors on the market that fully integrate HS-USB. Some baseband vendors have no plans to ever fully integrate HS-USB. With phones packing more features in the same space or smaller, the basebands and applications processors are quickly adopting smaller process technology. This presents distinct challenges when integrating the HS-USB PHY because the high-speed analog signaling does not scale easily. As a result, the fastest route to adding high-speed USB phones today is by either adding a UTMI transceiver (USB 2.0 Transceiver Macrocell Interface) or ULPI transceiver (UTMI+ Low Pin Interface) to basebands that integrate the HS-USB SIE, or offloading HS-USB control completely to a USB 2.0 HS-USB peripheral controller. Both of these approaches are available on the market today, but one caveat to adding such devices to a cell phone design is that a 6,12,or 24Mhz crystal is required.

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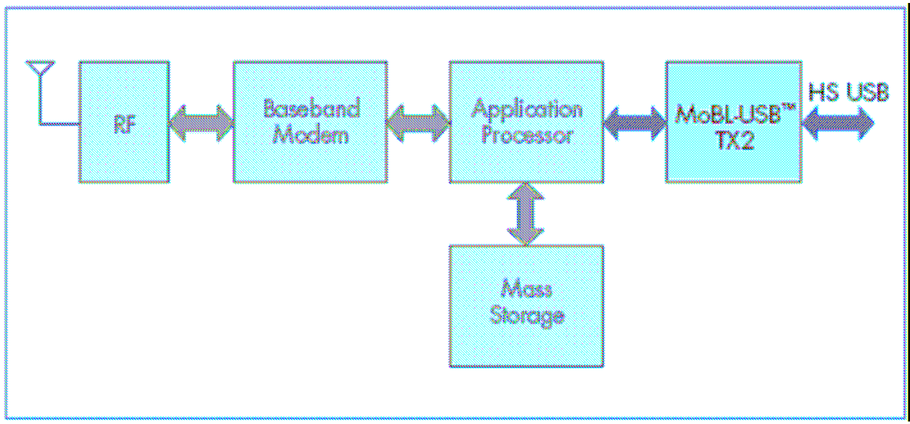
Size Constraints

Consider the following usage models and architectures for adding HS-USB to a cell phone design:

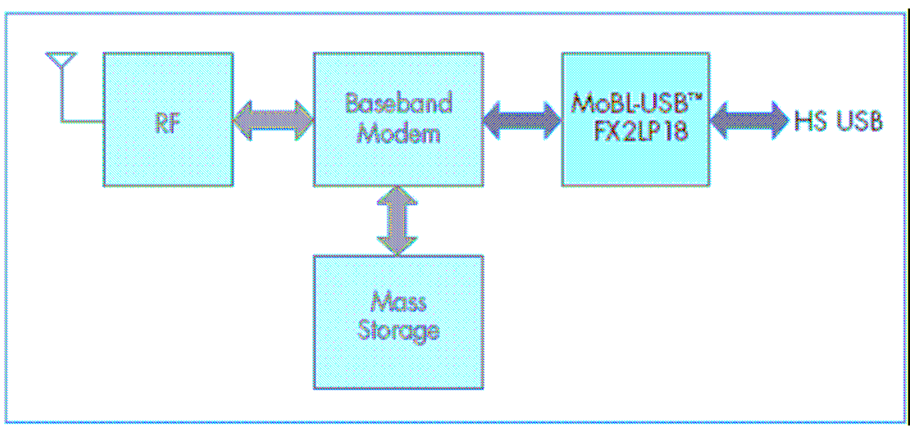
Architecture A: This approach is well-suited for cell phone designs using baseband or applications processors that integrate all of HS-USB except for the UTMI / ULPI Transceiver.

Figure 1: Architecture A using Cypress's MoBL-USB TX2 UTMI/ULPI Transceiver



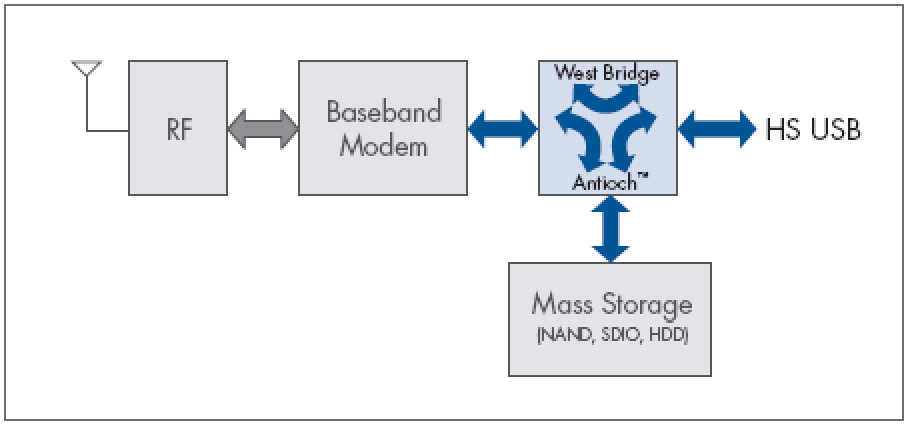
Architecture B: This architecture completely offloads HS-USB control from the baseband processor. This is the fastest and easiest way to add HS-USB to any cell phone design.

Figure 2: Architecture B using Cypress's MoBL-USB FX2LP18 high-speed USB 2.0 programmable microcontroller



Architecture C: This approach not only offloads all HS-USB control from the baseband processor, but also manages control for expandable mass storage. The benefit of this architecture is for a simultaneous usage model between the 3 ports, which allows a cell phone to remain operational for other functions during data transfer.

Figure 3: Architecture C using Cypress's West Bridge Antioch peripheral controller



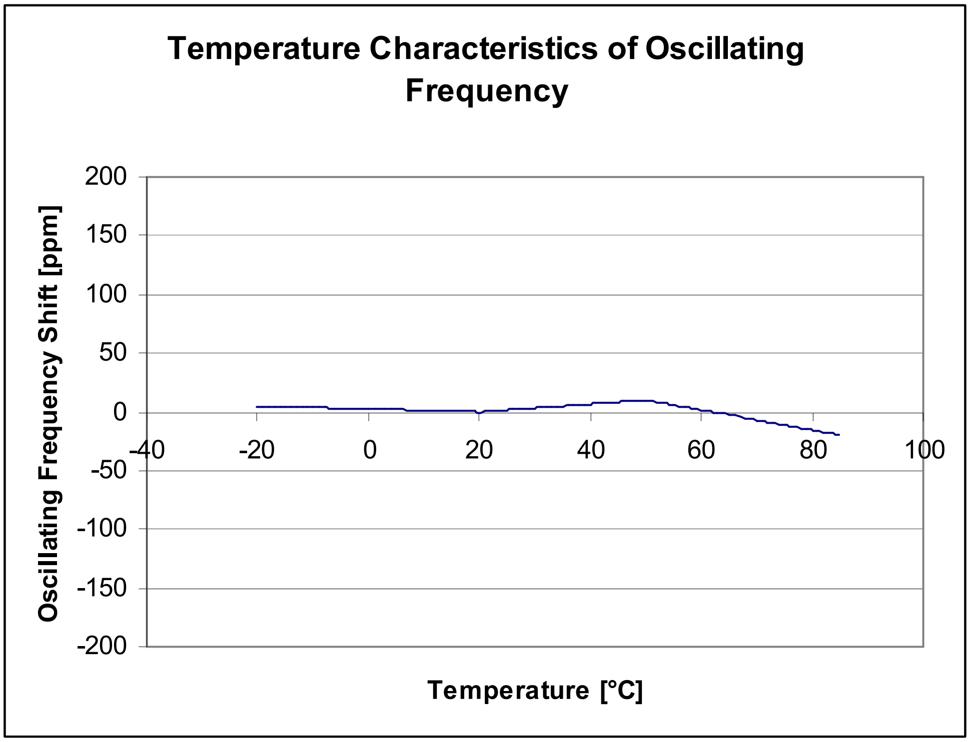
Despite the very different architectures and usage models illustrated above, open any HS-USB device and you will often find one commonality: a clunky crystal measuring 11.35 x 4.65 x 3.5mm. Given the tight space requirements in cell phones (consider the very popular Motorola Razr measuring 13.9mm thick and many upcoming competitors already going or planning on going thinner), such a large crystal makes adding HS-USB a challenging task. Fortunately, there exists at least one ceramic resonator solution on the market today measuring 3.2 x 1.3 x 1.0mm, which provides a 90% board area savings and 70% reduction in thickness over the traditional quartz crystal. While USB is ubiquitous, not all HS-USB devices are created equal and have different tolerances for oscillators. Therefore, it is important to evaluate whether your HS-USB design can take advantage of these small resonators.

Design Considerations with a Ceramic Resonator

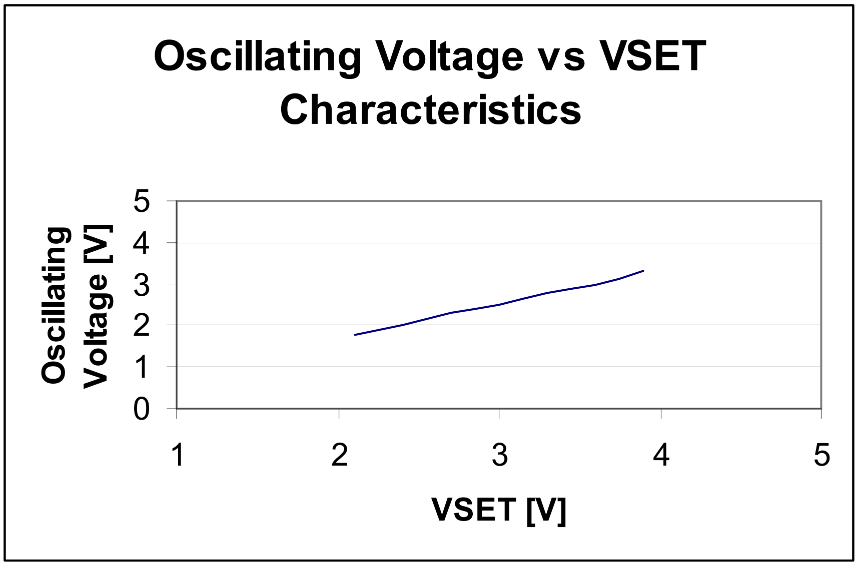
For most high-speed USB devices, the basic crystal requirements are driven by the USB specification for bit rate stability. The clock input is the primary control of this parameter. The USB 2.0 specification requires that the bit rate accuracy be within +/- 500 ppm when the design is running at high speed USB data rates. Factors that contribute to this are the ppm accuracy of the clock, the effects of aging on the source of the clock, the tolerance of the load capacitors used, and the effects of the USB chip itself on the accuracy.

When designing a device for high speed USB with resonators or crystals, the overall design must keep the frequency bit rate within the USB specification of +/- 500ppm. This must be insured over the operating temperature, and voltage range of the USB device. In addition it is necessary to check the design for aging. Both crystal and resonators will age with time. This ageing will affect the PPM rating on the parts.

Most resonators will compromise the PPM characteristics over these three parameters for the sake of cost. Very few of them will maintain a tight enough control to be useful with current USB parts. The Murata CSTCE24M0K2 series is one of the few resonators that control these parameters to maintain compatibility to the USB High-Speed data rates. When the device being designed has an operating temperature range of 0 to 70°C the variation from this part due to temperature has been measured below 10 ppm (see chart below).



The voltage characteristics of this part affect the amplitude and not the frequency of oscillation. The amplitude will drop approximately 0.6 volts when a V_{CC} of 3.3 volts is used. The USB device being used in the design should have sufficient input range to accommodate this voltage drop. The output voltage curve is shown in the chart below.



One added benefit of this part is that the load capacitors are internal to the resonator and keep a tighter control on the variations of this part. In crystal designs the load capacitors are typically external and have a variation of +/- 20%. This means that there will be a given amount of offset from the desired frequency to that being generated. This offset must be considered in the design for it will appear as a data bit rate error. If the frequency is off by 50 ppm then 50 ppm of the bit rate error budget is used by this offset.

To maintain the USB bit rate tolerance, the sum of all the contributing variations must be within the USB specification of +/- 500ppm. Resonators used in this application must have a tight enough specification that aging, frequency offsets due to temperature or voltage and the initial designed tolerance must add up to less than the specification's limits. This specific example used has an initial tolerance of -250 to +200 ppm over temperature and voltage with an aging specification of -100 to +150 ppm for a total variation of -350 to +350 ppm over a 10 year time period. This allows for the use of a small resonator with lower overall cost to drive the USB design.

Conclusion

At the time of this article, HS-USB is already being designed into numerous cell phone models and the first of these HS-USB enabled multimedia phones are slated to release in 2007. There are a number of architectures for designers to choose from when looking to add HS-USB into a cell phone. While some future HS-USB devices will take clock inputs from other sources in a cell phone design, few solutions yet can escape the need for a big crystal to drive the HS-USB. Fortunately, ceramic resonator solutions exist today that solve this problem. To be successful, designers simply need to choose a HS-USB device that can take advantage of the resonators and keep in mind the considerations discussed in this article.

References

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