Bridge Architecture Solves Performance, Design, Cost Problems In New Portables

By Danny Tseng, Senior Applications Engineer, Cypress Semiconductor Corp.

The market for portable electronics has bloomed and prospered in the past decade, as a plethora of new products were introduced and made affordable to the general consumers. Many "killer applications" have emerged in this market space, and they have improved quickly to fulfill growing demands. Launched in the late 1990's, the MP3 player is one of the earliest portable consumer electronics that led the technology evolution. Stemming from the portable, battery-operated device that offers simple digital music playback, designers have since reinvented the "MP3 player" concept to offer more complex functionalities. Consequently, integrated products like the Personal Media Players (PMP) and music-enabled mobile handsets were created. The Apple iPod, for example, has transformed from a basic MP3 player into a family of sophisticated PMP and handset products. The latest iPod Touch supports not only picture/video playback but also advanced features like built-in WiFi for mobile Internet browsing. Other consumer electronics such as Personal Navigation Devices (PND), portable game consoles, electronic dictionaries, and digital photo frames are also adhering to similar integration trends; however, several challenges still exist in today's portable consumer electronics designs.

Integrating the Latest Technologies

At the same time that consumer electronics are offering more features and becoming integrated, embedded processor vendors are also jumping onto the integration band-wagon in attempt to differentiate their products from their competitors. The newest processors in the market include many of the "popular" features that cater to the targeted applications; however, many of the latest mass storage and peripheral standards are still left unsupported. This is due to the fact that the evolution of mass storage and peripheral technologies moves at much faster rates than processor core technology. By the time a processor has gone through its typical 2-year design cycle, new mass storage and peripheral standards have already been released. It is simply impractical and impossible for a processor to keep up with the latest standards. Thus system designers need to adopt an external bridge to supplement the embedded processor with support for the latest mass storages and peripherals.

As technologies evolve rapidly, the success of a vendor depends heavily on its ability to address the fast-changing consumer demands. The key is to keep the brand name fresh in the market by introducing new products periodically, while it is also important to have a portfolio of products that can cater to the different customer bases. Not only is it important to roll out products quickly, it is even more vital to do it in an efficient manner. The system designers must adopt components that are both flexible and expandable, and leverage reusable design architectures to cut down cost and shorten design cycle.

Minimizing Bill of Material (BoM) and manufacturing costs is critical to market success. As each product model is expected to drive a high volume during its lifetime, even the slightest cost difference can determine the profitability and success of the product in the market. However, in the process of balancing performance, integration, and cost, it is a common pitfall to become overly preoccupied in picking a processor that offers the most features while failing to realize the importance of their quality. Therefore, the system designer must manage the trade-off between the number of integrated features and their performance on an embedded processor. Oftentimes, products with many features but suboptimal system performance fail miserably in the fiercely competitive market.

West Bridge Architecture

In attempt to keep processors, mass storage, and peripherals connected, developers are introducing the West Bridge to architectures. Just like the North and South Bridges in the PC world, the West Bridge is designed to interconnect the main processor in an embedded system to external peripherals. An architectural example of a West Bridge is illustrated in Figure 1.

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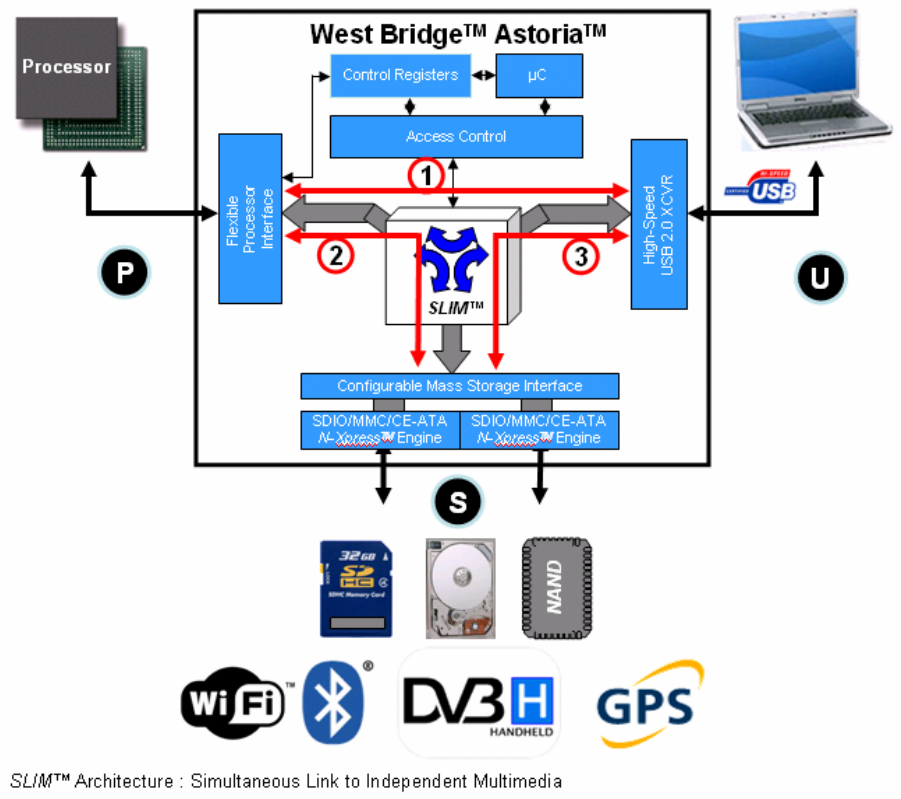
Figure 1: West Bridge Architectural Block Diagram



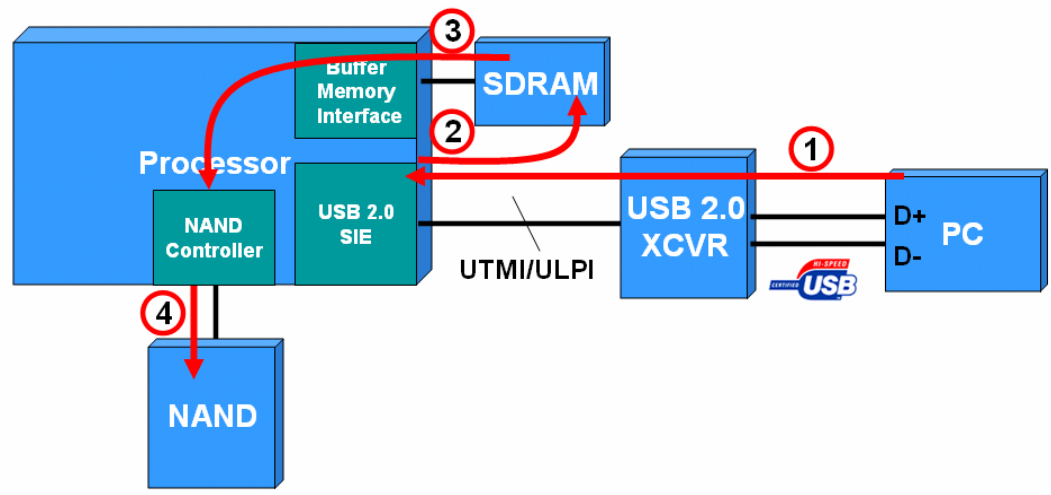
The West Bridge has 3 interfaces: a processor “P” port, a High-Speed USB “U” port, and a mass storage “S” port. The “P” port provides embedded processor connectivity, and it also supports hardware DMA access. A flexible and configurable “P” port can support various standard interfaces available on different processors. The “U” port provides a USB2.0 High-Speed USB link, and the “S” port can be configured to support a variety of mass storage devices, such as SD/SDHC, SDIO, MMC, CE-ATA, and SLC/MLC NAND devices. The red arrows in Figure 1 show the possible data paths among the three ports which allow all three data paths to operate concurrently, enabling multi-tasking of mass storage and peripheral functionalities.

Supporting the Latest Standards

As mentioned previously, embedded processors in the market today do not provide adequate support, if at all, for the latest mass storage and peripheral standards. The West Bridge enables new peripheral connectivity such as USB 2.0 High-Speed, and support new mass storage devices like SLC/MLC NAND, SD2.0 SDHC/SDIO, MMC4.2, and CE-ATA. The design cycle for West Bridge devices is also much shorter than a full-fledged processor; therefore, just like the North and South Bridges in the PC world, it is envisioned that West Bridge will complement processors in embedded systems to provide support for the latest technology standards.

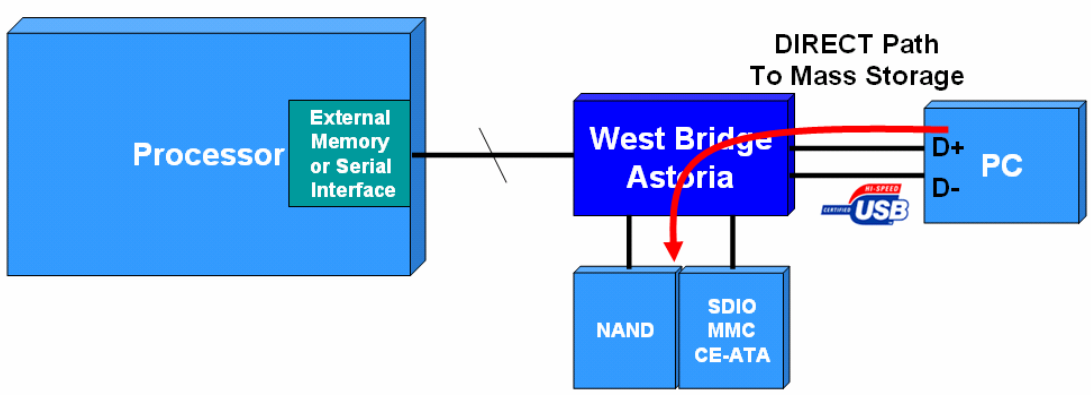
Figure 2 shows a typical example of an USB 2.0 High-Speed implementation, where the embedded processor has integrated High-Speed USB SIE and an external transceiver. The data from the PC first passes through the USB2.0 High-Speed pipe and gets buffered into the SDRAM. The processor then reads the data from SDRAM and writes it into the mass storage device. Not only does the series of intermediate transfers prevent the system to take full advantage of the High-Speed USB link, it can also drastically slow down the overall system if the software is not carefully optimized. Consequently, implementing this architecture often does not yield the best consumer experience.

Figure 2: Data Flow for Systems with Integrated High-Speed USB Controller



In contrast to the architecture shown in Figure 2, Figure 3 shows the West Bridge architecture, where mass storage devices are attached directly to West Bridge. The transfer of data is completely offloaded from the processor, as the processor is no longer in the data path. This frees up processing bandwidth on the processor and enables it to be used for more important tasks.

Figure 3: Direct Data Path from PC to Mass Storage through the West Bridge



The direct path from PC to mass storage dramatically improves effective throughput. Cypress has benchmarked the USB throughput of different consumer electronic devices in the market today. The benchmarking has been done in a controlled environment, and the results are tabulated in Table 1. The names of these devices have been removed hidden for confidentiality.

Table 1: PC to Mass Storage via USB Transfer Speeds Benchmarking

Device	USB Type	Architecture	Storage Type	Observed Throughput
West Bridge	High-Speed	West Bridge	1GB SanDisk Extreme III SD	17.1MBps
			60GB Seagate CE-ATA HDD	26.9MBps
Smart-Phone "R"	Full-Speed	See Figure 3, but with Full-Speed USB	1GB PNY MicroSD	1.0MBps
Music Phone "M"	High-Speed	See Figure 2	1GB SanDisk Extreme III SD	5.7MBps
MP3 Player "A"	High-Speed	See Figure 3	8GB Built-In NAND	4.3MBps

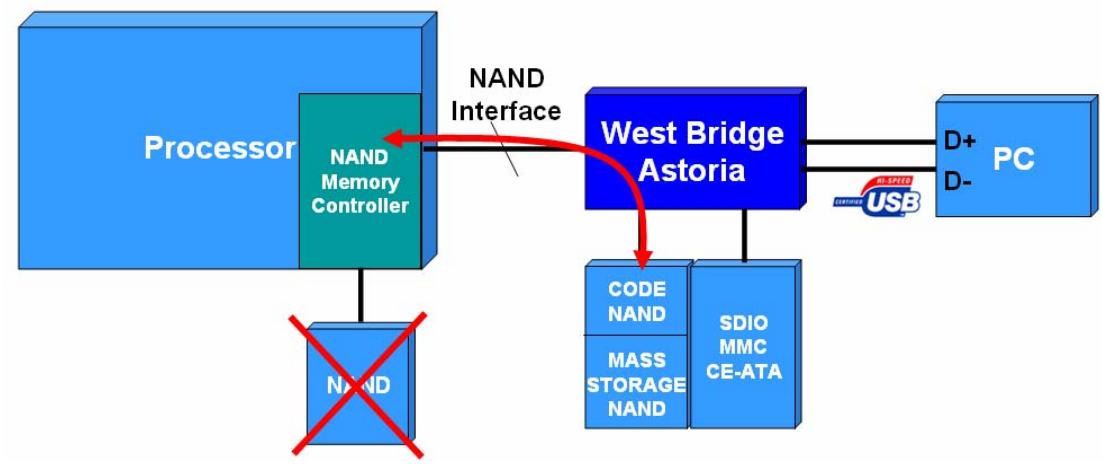
As Table 1 shows, the West Bridge architecture significantly increases the effective throughput between PC and mass storage. This makes the West Bridge very attractive for performance critical systems, as it tremendously improves the consumer experience.

Another benefit of adopting a West Bridge is to enhance design flexibility and enable expandability. Dual SDIO ports, for example, allow seamless peripheral connectivity such as WiFi, Bluetooth, GPS, and many others. Designers can take advantage of dual SDIO ports to quickly spin off derivative products without a complete architectural redesign. For example, one can simply add a DVB-H module to an existing MP3 player design to create a PMP that supports mobile television.

A West Bridge also enables architectures to support the latest MLC NAND technology for cost sensitive applications. MLC NAND cost is approximately 1/3 of SLC NAND, while MLC NAND devices are also available in much higher densities. Thus, in applications like PMPs and digital photo frames where high capacity non-volatile memory is required, the cost advantage of adopting MLC instead of SLC NAND is substantial.

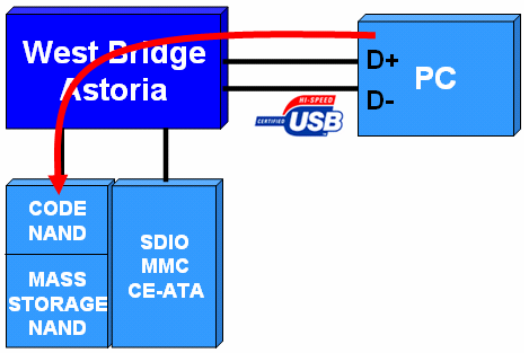
The BoM can be further reduced when the West Bridge is used to facilitate processor booting. A typical embedded design has two non-volatile flash memories: a high-density NAND for mass storage and a NOR or a smaller NAND for boot code storage. A West Bridge can consolidate these by allowing the processor to boot directly from the NAND attached to the West Bridge (Figure 4). The processor boot code is migrated into the West Bridge NAND, hence eliminating the need for a separate flash. Note that the "P"-port is configured to support a NAND interface, thus this migration is seamless and transparent to the processor. The West Bridge NAND is divided into two partitions: one for the processor boot code and another for mass storage. This usage model offers both BOM and board space reductions.

Figure 4: Processor Booting Through the West Bridge (NAND Booting)



Apart from the Bill of Material cost, utilizing a West Bridge can also streamline the manufacturing process of a product. As each model of consumer electronics is manufactured in millions of units' quantity, manufacturing process efficiency becomes exceedingly important. Time is money, and one of the most time-consuming tasks in the manufacturing flow is pre-programming of the NAND with processor boot code. Traditionally, these NAND devices are programmed with gang programmers, then mounted onto the product PCB. The shortcoming of this methodology is slow programming speed; it typically takes 20 minutes to program a single batch of NAND devices. With a West Bridge architecture, programming can be done in-system using a USB host such as a PC (Figure 5). Code can be transferred directly into the NAND via High-Speed USB after the NAND is mounted onto the PCB. The sustained speed of this direct download is considerably higher and more reliable than using gang programmers.

Figure 5: Boot Code Download during Manufacturing Mode



A West Bridge architecture supports the latest mass storage and peripheral standards that complement embedded processors, bringing out best-in-class mass storage performance while offering immense flexibility and expandability that greatly reduces product design time. Support for processor booting and manufacturing mode cuts down overall cost tremendously, thus giving West Bridge-enabled products an enormous competitive advantage. Examples of the West Bridge chip include Cypress Semiconductor's Antioch (CYWB0124AB), in mass production since last year, and the Astoria (CYWB0224AB), which is expected to be available in the first half of 2008.

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709
Phone: 408-943-2600
Fax: 408-943-4730
http://www.cypress.com