



## Optimize Inter-processor Communication in Dual Baseband Dual Mode Handsets

By (Ming Hoong Chong, Product Marketing Engineer, Cypress Semiconductor Corp.)

### Executive Summary

The onset of HSPA capable handsets, combined with improved video and data content quality, brews a perfect storm for many inter-processor communication architectures. Traditional interconnects can no longer support data throughputs in line with baseband processor capabilities and future mobile communication standards. Here's why multi-port interconnects may be a viable solution.

With the onset of globalization, world travel today is prevalent be it for business or leisure; and with travel comes the process of planning to carry the basic essentials and gadgets for the trip. Today's mobile handsets, thankfully, make it redundant to carry such other gadgets as MP3 players, portable navigation devices, cameras and handheld video games. With more than 1 billion units shipped annually, a mobile handset is now one of the basic necessities that people cannot leave home without. However, the phone is not of much use when it does not work in the destination country.

For example, Japan and Korea support a different standard (CDMA and FOMA) than most of Europe, which only supports GSM. Many other countries support both standards (GSM and CDMA) and it depends on the carrier subscribed to. A single handset, therefore, cannot be used worldwide. Many travelers carry two phones or buy a new Subscriber Identification Module (SIM) card at the airport whenever they are on travel, emailing the new number to their friends and colleagues.

This disconnect has given rise to Dual Baseband Dual Mode (DBDM) handsets that promise true operability worldwide as handset manufacturers compete to provide their users with the desired "global" roaming ability. A DBDM handset is a single handset that has 2 separate baseband processors. These handsets usually contain 2 slots for inserting a SIM card for use with GSM channels and Removable User Identification Module (RUIM) for use with CDMA channels. Phones that already have CDMA capabilities on board, however, might only provide one slot for inserting a GSM SIM card. Current major handset manufacturers that tout "World Phones" include Research In Motion (RIM), Samsung, LG, Motorola, and others.

Figure 1

World Phone Manufacturers and Models*			
Samsung	Motorola	LG	RIM
SCH-W531	A840	SH-100	Blackberry 8830
SCH-W579	Z6c	KT-1000	
SCH-839			
SCH-A790			
SPH-325			
SCH-W399			

\*Not complete list

Apart from processing their intended CDMA or GSM signals, each baseband processor is also given specific tasks to perform in the phone. These range from such simple applications as operating the keypad and LEDs to such complex functionalities as operating the LCD screen, camera, and video processing. With two separate processors receiving signals and various other applications split between them, data must be transferred between the processors in an efficient way to prevent delays for the end user, and have little or no impact on battery life. With the introduction of high resolution handset cameras and video streaming in handsets, we see larger file sizes and higher data rates that further amplify the need for efficient data handling between separate processors. How often have we been frustrated by our handsets "freezing" when accessing stored pictures or videos?

With telecommunication technology improving by leaps and bounds, no longer is air data transfer in the Kbps range as the 2.5/2.75G phones of yesteryears. Today's 3.5G HSPA capable phones require data transfer in the Mbps range. Future mobile communication standards that are currently in trials like WiMax, WiBro, LTE and UMB will further push the boundaries of data transfer. To match the increased speed dictated by these new standards, processors have increased in processing power and cellular networks have been upgraded to handle this exponential increase in data transfer.

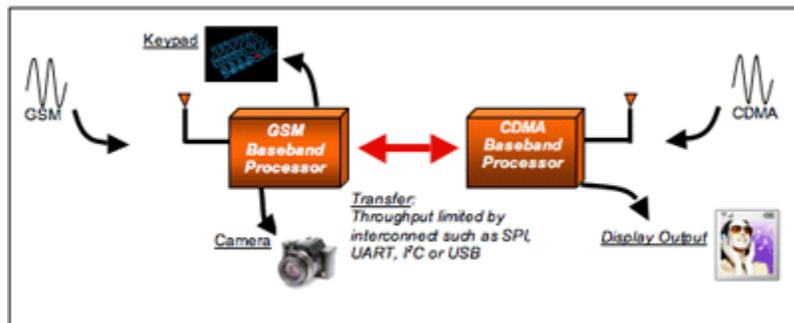
Figure 2

Mobile Communication Standards		
Technology	Generation	Data Rate
EDGE	2.5G	474 Kbps
CDMA2000	2.5G	307 Kbps
EV-DO	3G	3.1 Mbps
HSDPA	3G	14.4 Mbps
WiBro	4G	50 Mbps
WiMax	4G	70 Mbps
UMB	4G	280 Mbps
LTE	4G	277 Mbps

Nevertheless, with the increase in processing power of baseband processors and the increase data capabilities of cellular networks, there remains an antiquated architecture within the handset that is limiting the handset's capability to perform at an optimum - the interprocessor communication architecture. This portion of the telecommunication ecosystem has been lagging behind compared to the exponential technological growth of the cellular handset industry. Currently, we have baseband and application processors that are capable of many Million Instructions per Second (MIPS) and data rates achieving 10Mbps or more for HSPA capable phones. However, with all the focus placed on processor capabilities and wireless data rates, the communication between processors has been a high profile bottleneck. This problem is faced by numerous handset designers that have the latest and greatest processors and chipsets to work with but cannot seem to increase the performance of their devices.

### Current Solutions and their shortcomings

Figure 3



Current handset architectures today use various means of interprocessor communication. The popular direct interfaces currently in use include SPI, I2C, UART, and USB.

Although SPI is capable of data rates of above 20Mbps, there is no uniform specification for SPI and thus it is very dependent on the processor used. Typical SPI of baseband processors are approximately 16Mbps. With various baseband manufacturers producing their own proprietary products, the diverse SPI interfaces on separate baseband processors pose a daunting challenge for designers to pair two baseband processors successfully and achieve the optimum SPI speeds.

On the other hand, although the latest I2C specification calls for a high speed mode with throughputs up to 3.4Mbps, most devices available today are only capable of supporting data rates of between 400Kbps and 1Mbps. At these speeds, I2C is slow for telecommunication needs of today.

The third type of interconnect used in handsets is UART. UART typical data rate is approximately 1.5Mbps and a High Speed UART is capable of up to 5Mbps. However, such data rates are insufficient for high bandwidth interprocessor communication.

One of the more popular interconnect method is via USB (Universal Serial Bus). Most processors are equipped with Full Speed USB (FS-USB) device capability. FS-USB has a maximum data rate of 12Mbps that is in reality closer to 6Mbps throughput due to the high packet overhead necessary in the USB protocol. Furthermore, most baseband processors are not

equipped with USB host capability which is necessary in a USB solution. Thus an additional USB host will have to be built in. Besides being inadequate for today's HSPA data rates, this also increases power consumption due to the USB host being constantly active even when no data is transmitted. The number of USB ports available on a baseband processor is also usually limited as it is the de-facto mode of connecting handsets to the PC.

**Figure 4**

Interconnect	Disadvantages
SPI	- No uniform specification, compatibility issues
PC	- Low speed
UART	- Low speed
FS-USB	- Power consumption, low 3G speeds

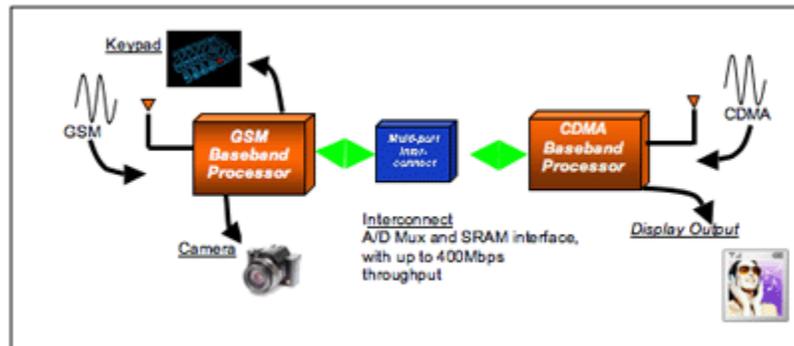
Previously, for text messaging and simple data transfers on slower networks, interconnection methods mentioned might have been sufficient. With HSPA capable handsets attempting to reach 14.4Mbps and beyond, all of the current popular interfaces as seen above are unable to sustain the necessary throughput efficiently and at an optimum.

So how can designers address today's need for increase data throughput in handsets?

### Alternate Solutions and Advantage

One potential solution to the interprocessor connection problem, as used by many DBDM architectures today is the use of multi-port interconnects. In this architecture, a buffered multi-port device acts as an interconnect between two CPUs and enables high-speed data transfer between the two and also helps to reduce the power consumption during inter processor communication (IPC).

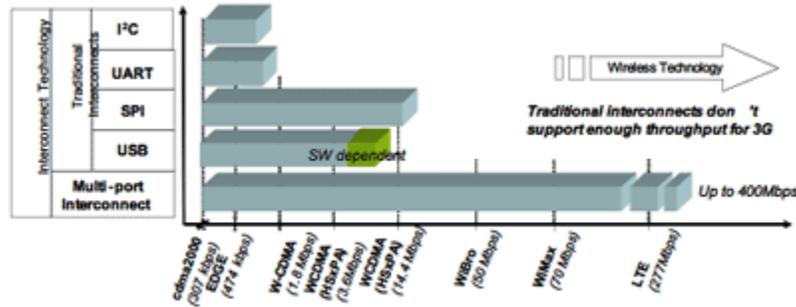
**Figure 5**



### Speed

The most apparent benefit of using multi-port interconnects is speed. With access times as fast as 40ns, dual port memories can support up to 400Mbps. This does not only provide adequate support for HSPA capable handset requirements today, but also sets the groundwork for future increase in throughput needs (eg LTE). As handsets increase in sophistication, increasing data sizes transferred between processors is inevitable. With multi-port interconnects, handset designers are no longer faced with the interprocessor communication bottleneck.

Figure 6



## Power consumption

Besides high speed, low power consumption is another key requirement for DBDM handsets. If both basebands are required to be active all the time during IPC (like in the case of SPI, UART, I2C or USB) battery life takes a hit. Apart from that, active communication between processors requires dedicated resources from each and thus decreases their performance.

A multi-port solution enables passive communication between the processors. A processor can write to the multi-port interconnect when it needs to and go into sleep mode. The other baseband processor can access that data whenever needed at its own convenience. With the multi-port interconnect acting as a buffer, the receiving processor can be in sleep mode until it receives the interrupt from the multi-port interconnect before going active.

Let's look at an example comparing a multi-port IPC solution with a FS-USB based IPC solution. A FS-USB solution with an effective throughput of 6Mbps will take 1 minute and 20 seconds to transfer 480Mb (60MB) or 10 MP3 songs. Similar amount of data using a multi-port interconnect solution will only require 5 seconds at 100Mbps (effective throughput assumed).

A typical baseband processor with a 1.2V core runs at ~120mW active and ~0.24mW in sleep mode. If both processors are active during transfer for 80 seconds, 5.33mWH  $[(120 \times 2) \times 80 / 3600]$  of current is consumed in the USB case. In the case of a multi-port, only one of the processors is active during data transfer. The total battery life consumed by the processors coupled with the multi-port interconnect (~27mW) is only 0.743mWH  $[(120 + 0.24) \times 2 + 27] \times 10 / 3600]$ . This represents around 85% power savings during a single instance of IPC, which is a huge value as more and more people download music, pictures, email, and browse the internet over their phones.

## Flexibility

Another advantage of an interconnect buffer is that there is no software driver required to implement IPC with a multi-port device. This allows handset manufacturers to come up with different models for different regions with little changes to their overall software IPC architecture. This provides more flexibility to the manufacturers to use different operating systems running on different processors and select a processor based on the system needs than IPC limitations.

## Single Chip Solutions

The recent introduction of single chip solutions that encompass select GSM and CDMA bands is an interesting development. Typically in such solutions due to the necessity to fit all the needed functionality onto one single chip, most often there is a compromise on features and performance. These processors are also new and not proven completely in the market yet. Most manufacturers still prefer to go with the tried and tested solutions and often don't like to make many compromises with their feature requirements. Dual processor architectures are also a more likely candidate for the evolving network speeds and feature requirements.



## **Conclusion**

The onset of HSPA capable handsets coupled with the improvement of video and data content quality, brews a perfect storm in the near future for many interprocessor communication architectures. The traditional interconnects can no longer support the necessary data throughputs in line with baseband processor capabilities and future mobile communication standards. Some handset designers have already begun to realize this impending problem and have switched to using low power multi-port interconnects for their DBDM handsets. Multi-port interconnects do not only provide the high bandwidth and low power consumption needed in today's handset design but also provides the flexibility for designers to produce better handsets at lower costs and faster time to market.



## References

Cypress Semiconductor  
198 Champion Court  
San Jose, CA 95134-1709  
Phone: 408-943-2600  
Fax: 408-943-4730  
<http://www.cypress.com>

© Cypress Semiconductor Corporation, 2007. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

PSoC Designer™, Programmable System-on-Chip™, and PSoC Express™ are trademarks and PSoC® is a registered trademark of Cypress Semiconductor Corp. All other trademarks or registered trademarks referenced herein are property of the respective corporations.

This Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.