Non-Volatile Static Random Access Memory (NVSRAM) - High Speed Nonvolatility

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Introduction

Memories are an integral part of any electronic system/application. They can be broadly classified as volatile memories (lose memory contents on power loss) and nonvolatile memories (retain memory contents on power loss). Popular volatile memories include SRAM (Static Random Access Memory), DRAM (Dynamic RAM) etc. Popular nonvolatile memories include EEPROM, Flash etc.

Memories that offer a combination of SRAM features along with nonvolatility have several advantages in a system. Many of today's applications require a fast memory device which can also offer nonvolatility. Several memory technologies offer such solutions. These include NVSRAM, BBSRAM, FRAM and MRAM.

This article explains in brief the features and working of NVSRAM and also compares NVSRAM with other memories offering similar solutions. This can provide a designer an insight into deciding which memory technology is suitable for his design. Before getting into the technical and application details of NVSRAM, we briefly compare the different competing technologies.

NVSRAMs offer nonvolatility by transferring the contents of SRAM to the corresponding nonvolatile cells integrated with each SRAM, on power loss. BBSRAM (Battery Backed-up SRAM) on the other hand, retains the data in SRAM by switching over to a Li Battery source on power-down. FRAM (Ferroelectric RAM) retains data by applying electric field in the right direction to a Ferroelectric crystal. MRAM (Magnetoresistive RAM) uses magnetic polarization to store data permanently.

Table 1: A comparison of important parameters between nvSRAMs and competing technologies

Parameters	*Measurement*	*NVSRAM*	*BBSRAM*	*FRAM*	*MRAM*
Performance	Access Time (ns)	15 – 25	70 - 100	100 - 150	35
Reliability	Years of Retention	20	10	10	10
Current / Power	Active @ 100 ns (mA)	20	22	22	30
	Typical Standby (uA)	750	200	20	9000
Density	Max Density Today (Mb)	4	16	1	4
Packaging	Board Space Rqrm'ts	Small	Large	Small	Small
	KGD Support	Yes	No	Yes	
Environmental	RoHS	Yes	No	Yes	Yes

Nonvolatile Static Random Access Memory (NVSRAM) is a high-speed, high-performance nonvolatile memory that combines the performance characteristics of a high-speed SRAM with that of a nonvolatile cell. The data is retained in the nonvolatile cell integrated with each SRAM cell.

NVSRAMs are available in the density range of 16Kbit to 4Mbit. These NVSRAMs are offered in the industry's fastest access speeds of 15ns – 45ns and can operate in both commercial and industrial temperature range. The NVSRAMs are offered in small footprint SSOP, SOIC and TSOP packages.

Published in Electronics For You June 2007

Figure 1: NVSRAM Block Diagram

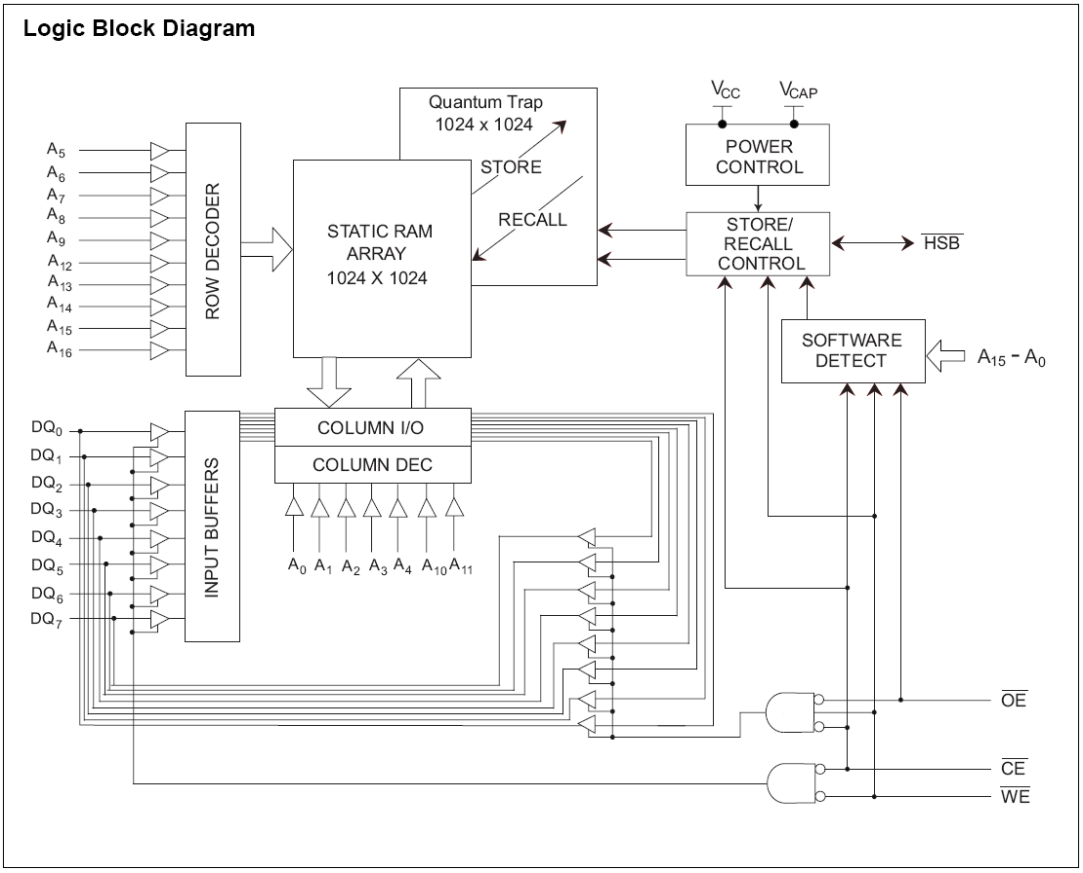


Figure 1 shows the block diagram of a 1Mbit NVSRAM. As can be seen from the figure, the Address lines (A0–A16), the Data lines (DQ0–DQ7) and the control lines (/OE, /CE, and /WE) provide exactly the same interface as a high-speed SRAM. The Power Control block is used to detect variations on the Power supply VCC for AutoStore™ operation. The STORE/RECALL Control block is used for Hardware STORE operation using /HSB pin and for RECALL operation. The Software Detect Block is used for software STORE and RECALL operations.

The only external component required for NVSRAM operation is a capacitor connected to the VCAP pin. This capacitor gets charged by the supply voltage during the power-on condition. This charge provides the energy required for an AutoStore operation (transferring the contents of SRAM to nonvolatile elements on power down).

Device Interface

The interface to NVSRAM is similar to standard asynchronous SRAMs apart from a few extra pins exclusive to the device. For normal Read and Write operations, the NVSRAM is accessed in exactly the same way as an SRAM. The three control signals /CE (Chip Enable), /OE (Output Enable) and /WE (Write Enable) are used in the same way as in SRAMs for normal Read and Write operations to the device.

Figure 2: Comparison between NVSRAM and SRAM interface

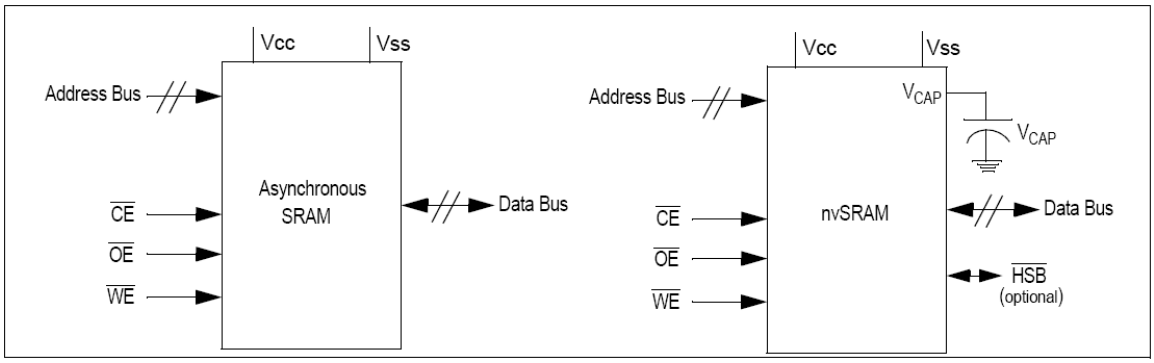


Figure 2 shows the similarity in the interface between NVSRAM and SRAM. As can be seen, VCAP and /HSB are the only additional pins in NVSRAM as compared to an Asynchronous SRAM.

Device Operation

The NVSRAM is made up of two functional components paired up in the same physical cell. These are the SRAM memory cell and the nonvolatile cell. Data in the SRAM can be transferred to the nonvolatile cell (the STORE operation), or from the nonvolatile cell to the SRAM (the RECALL operation). This unique architecture allows all cells to be stored and recalled in parallel. During the STORE and RECALL operation, SRAM Read and Write operations are inhibited. The NVSRAM supports unlimited reads and writes just like a typical SRAM. In addition it provides unlimited RECALL operations and 500,000 STORE operations.

SRAM Read

The NVSRAM performs a READ cycle whenever /CE and /OE are low while /WE and /HSB are high. The address specified on the address pins determines which of the data bytes will be accessed. The data outputs will repeatedly respond to address changes within the access time without the need for transitions on any control input pins, and will remain valid until another address change or until /CE or /OE is brought HIGH, or /WE or /HSB are brought LOW.

SRAM Write

A WRITE cycle is performed whenever /CE and /WE are low and /HSB is high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either /CE or /WE goes high at the end of the cycle.

STORE Operations

Data in SRAM can be stored into the nonvolatile elements using one of the three storage operations. These operations are:

1) AutoStore, initiated on device Power-down.
2) Hardware STORE, activated by /HSB.
3) Software STORE, activated by an address sequence.

AutoStore Operation

AutoStore operation is a unique feature of NVSRAMs and is enabled by default on the device.

During normal operation, the device will draw current from VCC to charge a capacitor connected to the VCAP pin. This stored charge will be used by the chip to perform a single STORE operation. If the voltage on the VCC pin drops below the device minimum operating voltage, the part will automatically disconnect the VCAP pin from VCC. A STORE operation will be initiated with power provided by the VCAP capacitor. The AutoStore operation is completed in 12.5ms (Max.).

Hardware STORE Operation

The NVSRAM provides the /HSB pin for controlling and acknowledging the STORE operations. The /HSB pin can be used to request a hardware STORE cycle. When the /HSB pin is driven low, the NVSRAM will conditionally initiate a STORE operation. An actual STORE cycle will only begin if a WRITE to the SRAM took place since the last STORE or RECALL cycle. The /HSB pin also acts as an open drain driver that is internally driven low to indicate a busy condition while the STORE (initiated by any means) is in progress.

During any STORE operation, regardless of how it was initiated, the NVSRAM will continue to drive the /HSB pin low, releasing it only when the STORE is complete.

Software STORE Operation

Data can be transferred from the SRAM to the nonvolatile memory by a software address sequence. The NVSRAM software STORE cycle is initiated by executing sequential /CE-controlled READ cycles from six specific address locations in exact order. During the STORE cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. Once a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

RECALL Operations

Data backed-up in the nonvolatile elements can be transferred to the SRAM elements using one of the two RECALL operations:

1) Auto RECALL, initiated on Power-up.
2) Software RECALL, activated by an address sequence.

Auto RECALL (Power-up RECALL) Operation

During power-up, or after any low-power condition, an internal RECALL request will be latched. When VCC once again exceeds the minimum operating voltage, a RECALL cycle will automatically be initiated.

Software RECALL Operation

Data can be transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation.

Endurance (No. of STORE cycles to the nonvolatile elements)

The SRAM elements of the NVSRAM provide unlimited Read and Write Cycles.

The NVSRAM guarantees a minimum of 500,000 STORE cycles to the nonvolatile elements.

Data Retention

The nonvolatile elements of the NVSRAM can hold the stored data for a minimum of 20 years.

Target Applications

1. RAID Controller
2. Mobile Data Terminal
3. POS Terminal
4. Printer/Copier
5. Power/Energy Meters
6. Industrial Automation (Remote Terminal Units)
7. Dashboard/Instrument Panel Clusters
8. Single Board Computers
9. Routers
10. WAN Interface Card

Let us consider a sample application and see what performance advantage NVSRAM can deliver.

Industrial Automation (RTUs)

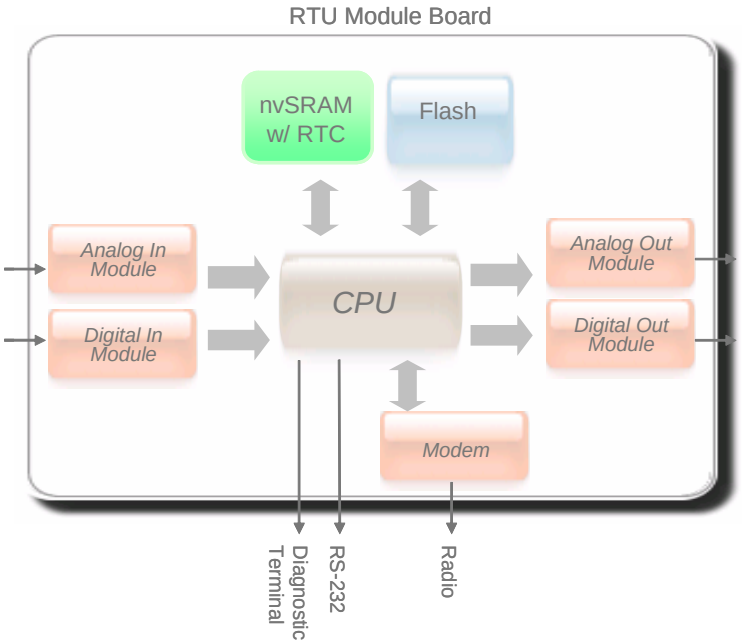
Electric power stations, water management stations, oil refineries and other industrial plants all contain lots of machinery spread out over a large area.

Remote Terminal Units, or RTUs are usually located at different sites around the plants and are part of the SCADA system which stands for *Supervisory Control And Data Acquisition.* The object of the RTU is to measure things such as pressure, flow, voltage or current. For example, if it is used in a water management station, the RTU module might be measuring the water level in a holding tank and decide to fill or empty the tank depending on the water level. But it will also realize when a dangerous point is triggered and an alarm will be sent to the Master station.

Figure 3: A typical RTU

RTUs are CPU-based modules which require both Flash and SRAM memories for normal processing. However, these modules also use an onboard Real Time Clock and watchdog to track real-time events. For example, if the holding tank must maintain above a certain water level for 3 hours, the watchdog timer could be used to alert someone about a situation where that is not met.

Figure 4: A block diagram of a CPU-based RTU Module Board



By using the Cypress nvSRAM solution in place of the standard SRAM, the real-time clock and watchdog timer are already provided. No extra parts are necessary and the system can save on both board space as well as bill of material costs. In addition, these modules may be used in very harsh environments. The Cypress nvSRAM is very resistant to ESD (or electrostatic discharge) and can be used in environments from –40 to 85 degrees Celsius.

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