



nvSRAMs Eclipse Battery-backed Memory

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Executive Summary

Battery-backed Static RAMs have been an industry standard solution for protecting data from power interruption for decades, but they have always had intrinsic flaws related to battery reliability, additional manufacturing steps, and high total costs of ownership. More recently, environmental concerns for the materials used in batteries have pushed the industry towards seriously considering viable alternatives. nvSRAMs, built using a robust SONOS (Silicon-Oxide-Nitride-Oxide-Silicon) process and a high-performance nvSRAM architecture, provide the functionality of traditional battery-backed solution while providing higher reliability, efficient manufacturing, and true RoHS compliance while eliminating batteries altogether. This paper will describe nvSRAM products and how they replace traditional battery-backed solutions for memory and real-time-clock applications.

For three decades, engineers have combined batteries and static RAMs to protect data during intended and unexpected power outages. Initially, discrete implementations were built with low-density memory circuits and crude battery technologies using discrete power sensing and switching circuits. Performance proved to be a challenge, and batteries had limited capacity with questionable reliability. To meet the low power required for extended battery-backed operation memories were designed with slow access times.

Fortunately, a significant improvement became available as clever engineers combined discrete parts by assembling modules, first using dual-in-line, through-hole and later with surface mount packages. By putting the memory and control circuits in the same package with the battery, or by making a two-package implementation where the battery snaps onto the integrated circuit, the burdens of good circuit design, manufacturing, and reliability were shifted from the systems designer to the component supplier. One additional feature became almost synonymous with battery-backed SRAMs; the Real-Time-Clock. Since many applications needed to display time and date information along with time-stamping system events, it was only natural to combine these capabilities with the battery-backed SRAM, since the battery supply was already there.

Unfortunately, even as memory densities, integrated control circuits, and battery technologies improved, the same fundamental deficiencies remained. Whether in modular packages or discretely assembled on the printed circuit board (yes, many applications still use this technique) battery-backed SRAM continues to suffer from low reliability, complex manufacturing, a large footprint, slow performance and, now with greater environmental awareness, difficulty in keeping with the intent of moving towards completely "green" solutions. Let's examine each of these points.

The typical battery-backed SRAM implementation is made up of 4 components; the SRAM, the voltage monitor/controller, the battery and a battery socket, although the socket can be eliminated in modules. Simply multiplying the failure rate of each component would provide a reasonable first-level approximation of the system's reliability, but one should also consider the number of traces and connections required for all of the interconnects between devices, while taking special note of the battery connection which is frequently socketed, allowing the greater possibility of contact corrosion and intermittent connections from vibration. Battery life is a big variable, dependent upon how often the system cycles to battery power, temperature, and the type of battery used. Nominally, an SRAM operating with 5 μ A of standby current and a 165-mAh battery will last less than four years. Put this system through temperature extremes, whether while operating or in storage, and this number may degrade dramatically.

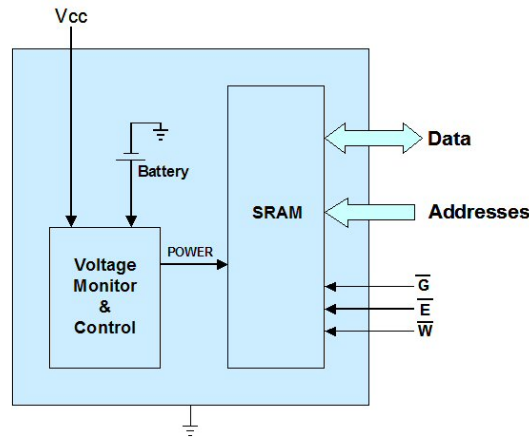
Manufacturing with batteries has been difficult primarily because of battery's inability to withstand the extreme temperatures used for re-flow soldering, which is only exacerbated with the higher temperature profiles being introduced for lead-free solder. This condition initially required the battery or the module to be assembled as a secondary manufacturing operation; that is, after the printed circuit board was assembled the battery was added in a manual step. Later, modules were built with the SRAM and control IC embedded in a surface-mount package that went through the normal re-flow cycle, then having a separate molded package containing the battery "snapped" onto it as a secondary operation. The molded battery was attached with plastic clips and the electrical connections were simply pressure connections subject to the same corrosion and vibration concerns of the socketed battery.

The board space required to support battery-backed SRAM has changed with the evolution of technologies but still remains inefficient. Discrete implementations have always required more area, largely because of the battery. Even with today's high-density packaging, a 44-pin TSOPII for the memory, a μ DFN for the controller, and a 20 mm coin cell require at least 555 mm² without yet accounting for routing and manufacturing tolerances. A popular battery-backed SRAM module today is packaged in a 27mm x 27mm BGA package, taking 729 mm² of board space. No battery-backed SRAM implementation today can claim the combined footprint and height of a standard single package monolithic memory.

High-speed access wasn't critical in the early life of battery-backed SRAMs, since system speeds were modest and in many cases these memories weren't used for real-time processing. Since very low-power SRAMs were required to conserve battery power, it was convenient that low power designs were also slow. Today, most battery-backed implementations are rated at 100 nsec access times, although some perform as fast as 55 nsec. Again, these specifications require balancing system speed requirements against data retention time, which is a function of standby current and battery capacity.

This brings us to an issue getting more attention than all the previous issues combined...that of being "green." When speaking of battery-powered systems of any kind this issue is highly charged, and battery-backed SRAMs can be especially sensitive because the memories are usually deeply embedded in systems and can't be easily inspected, repaired, or most importantly, properly disposed of. Within the industry there is much ado about complying with the European Union's Restriction of Hazardous Substances Directive or RoHS. RoHS restricts the use of six substances; lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls, and polybrominated diphenyl ether. In the semiconductor industry we generally think of this as the "lead-free" initiative. It is not commonly understood, however, that batteries, except as they might use some of the restricted materials above, are exempt from the RoHS directive. However, the Directive on Batteries and Accumulators and Waste Batteries is targeting the use of less hazardous substances in the manufacture of batteries, and improving waste management of these batteries. Other countries, including the United States with the EPA's 1996 Battery Act, are implementing similar initiatives to control the environmental impact of batteries. These initiatives will put increasing pressure on battery users and, by adding environmental-awareness pressures and costs related to monitoring and disposal, will force electronics manufacturers to look for viable alternatives. Although it is impractical to eliminate the use of batteries altogether, these movements will continue to add restrictions to the materials used as well as increase requirements on recycling and collection of batteries. The direct cost impact of these actions will vary by country and time, since each has freedom in their methods employed to improve waste management, but there are direct and indirect costs in the form of creating and managing disposal facilities as well as incremental taxes that will be imposed on suppliers of equipment using batteries.

Figure 1: Batter-Backed SRAM Blocked Diagram



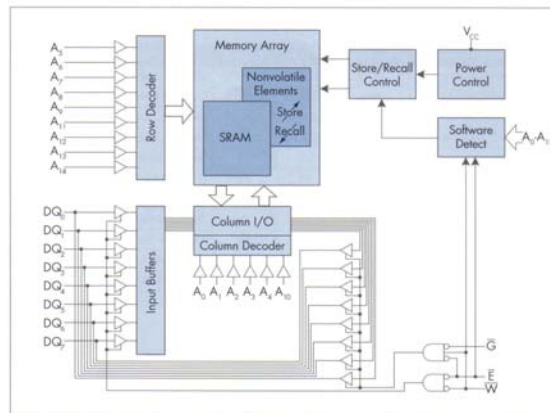
Alternatives to battery-backed SRAMs have been elusive. Some applications combine separate SRAM and EEPROM or SRAM and FLASH devices, which move the data into the non-volatile device when power is lost. These have obvious shortcomings because of the limited amount of data that can be transferred over the data bus in the amount of time a back-up power source, such as a high value capacitor, can provide. Exotic new technologies are also possible solutions in the long term. Ferroelectric, magnetic, and phase-change memories are all experiencing some success in developing nonvolatile capabilities that may in the future become commercially viable, but so far these have been constrained by limited performance, expensive manufacturing, and specialized materials.

Non-Volatile SRAMs

In order to address the shortcomings of battery-backed SRAMs, the electronics industry has introduced non-volatile SRAMs. These parts integrate a high-speed SRAM cell with non-volatile elements to provide powered-off back up while eliminating batteries altogether. The nvSRAM block diagram illustrates how the system interface is identical to any traditional high performance asynchronous SRAM. In either the x8 or x16 configuration, the address and data lines along with /CE, /OE, and /WE control signals, are familiar to the system designer. In normal operation, data are written to and read from the SRAM portion of the cell.

The non-volatile function is enabled when system power is lost or when the user initiates a store command. When system power is sensed to be dropping below the minimum operating level by the nvSRAM's power monitor circuit, the chip's I/Os are disabled to prevent corrupting the data in the SRAM, and then a store function is initiated within the chip. Energy from a small capacitor (typically 22µf to 68µf) is used to copy the data state from the SRAM portion of the memory cell into its nonvolatile elements. These non-volatile elements are tightly coupled with each SRAM bit cell and all data bits are transferred in one parallel operation. When power is restored, the power monitor initiates a recall function, restoring data states of the non-volatile elements into the SRAM. When the system supply is stable and ready to operate, the data are available for use as if no event had occurred. Depending on the device selected, the store operation can also be initiated by hardware or software command.

Figure 2: nvSRAM Block Diagram



A Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) process is used to integrate nonvolatile elements into high performance SRAM memory cells, and low erase/program currents and electric fields store charge into a silicon nitride insulating material. Low currents are possible because charge is pumped through a thin oxide layer, resulting in high reliability and the ability to store the entire memory array simultaneously. Stored charge in an insulating silicon nitride layer, as compared to a conducting floating polysilicon gate, is also far less susceptible to failures from contact spiking, oxide ruptures, or manufacturing defects. The SONOS process has been used for decades in discrete memories as well as in embedded systems, proving to be highly reliable, manufacturable, and scalable. Most important, the process requires no unusual materials or equipment and has been integrated with standard CMOS processes in many high-volume production wafer fabrication facilities.

Since nvSRAM nonvolatile storage is not dependent on a battery source for data retention, it is highly predictable. Writes to the SRAM are infinite, while non-volatile endurance is guaranteed for 200,000 store cycles. Recalls from the non-volatile elements do not exercise endurance cycles. Data retention is specified for 20 years after the last store cycle, even over the industrial temperature range.

nvSRAMs can also support expected on-chip RTC functions combining the high-performance reliability of a monolithic non-volatile memory with a full-featured clock. For example, real-time clock functions provide an accurate clock with leap year tracking and a programmable, high accuracy oscillator. An alarm function is programmable for one-time alarms or periodic seconds, minutes, hours, or days. A programmable watchdog timer can be available for process control. Clock and timer functions are accessed through dual-port registers that overlay the upper 16 address spaces in the nvSRAM memory array. Extremely low oscillator current at 32.768 KHz allows capacitor operation during system power-off operation. No power is required for the nvSRAM array, guaranteeing reliable nonvolatile data storage.



The nvSRAM is a single, monolithic device and, therefore, has all the efficient assembly and high reliability attributes of a standard SRAM, with similar package options. Cypress currently offers nvSRAMs from 256Kb through 4 Mb densities and will continue to develop higher density versions. Access times are available to 15 nsec. Surface mount SSOP, SOIC, TSOPII and BGA packages are all lead-free, so with no battery and RoHS compliant packages the nvSRAM eliminates current and future concerns presented by battery-backed SRAMs.



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