Taking Novel Si Ideas from Lab to Fab: the Emergence of the Technology Development Foundry

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Over the last decade, the semiconductor industry has gone through a fundamental change of supply chain disintegration. In response to increasing process development and manufacturing costs, the foundry business model emerged and gave rise to the fabless business model. This model allowed enterprises to focus on product development, while relying on its manufacturing partners for process technology development and manufacturing execution. As revenues for this industry segment grew, integrated device manufacturers (IDMs) started adopting the model as well, to varying degrees, to strategically manage wafer capacity and optimize associated capital expenditures. The underlying economic principle for foundry success is the pooling of resources, creating economies of scale and allowing shared access to those resources at a reduced cost.

The ever-increasing costs of semiconductor research and development (R&D), now coupled with slower revenue growth, will not only drive the further expansion of the fabless model, but it will also cause new everlasting changes in the industry. The so-called R&D funding gap is forcing the emergence of new business and collaboration models, while the continual scaling of CMOS is becoming the work of a few select, very sizeable IDMs and foundries. Most of us, however, will need to find new business vehicles to pursue new silicon-based innovation.

New Trends

As demand for memory storage, computing power and bandwidth continues to rise over the next decade, ambient intelligence will become a reality, and life science and energy solutions will change our way of life, requiring that traditional silicon chips do more than scale along Moore's Law and be an electronic computing miracle. They will need to morph into more capable and dynamically reconfigurable programmable devices that use less power or generate their own power, sense their environment, act on those environmental stimuli, and become structurally and intelligently compatible with biological and other media.

The technology behind these products will incorporate radical new concepts, materials and architectures to spur new functionality and value on the silicon wafer. By making very small, yet significant changes in the silicon chip fabrication process, costs are minimized, advances of the mainstream silicon process are leveraged, and completely new product functionalities are delivered.

As a result of driving Moore's Law over the last few decades, phenomenal baseline technologies are available today. Many established and start-up companies are building derivative technologies of these baselines to innovate in the silicon space without having to spend millions on capital equipment and basic process development. For example, engineers re-use existing investments and process modules by using unified memory schemes, microelectromechanical systems (MEMS) and image sensors to enable commercialization of a new breed of silicon chips, not necessarily at the most advanced technology nodes. Additionally, the aggressively pursued commercialization of nanotechnology is driving new concepts out of the lab environment and into the realm of established semiconductor capabilities where integration with CMOS technologies is desired (and feasible), and where superior technology and equipment capabilities are available (versus 4-inch and 6-inch environments) along with a huge manufacturing infrastructure that will become underutilized with the continued push to 300mm in the sub-65 nanometer regime. As a consequence of these trends, tremendous business opportunities exist for companies to not only innovate in the design space, but also in the process technology space. Under the design-centric fabless model, this task is typically left to the manufacturing partner. However, the demand for custom process development has grown to a level where the foundry cannot reliably support and commit to all the necessary requests. To enable an enterprise with capabilities for process development, one would need access to a fab environment that would allow independent intellectual property (IP) development, rapid cycles of learning and a mechanism for reliable transfer to manufacturing.

Traditional Approach

One approach an enterprise could take to conduct process development would be to build a prototype "fab" itself. Not only would this drain cash in an undesired core competency, but it would also take time away from focusing on accelerating time-to-market, manufacturing and revenue growth. In response, an obvious choice is to fragment the supply chain, reduce capital expenditure spending and increase cycle time to manage the complexities of tying together sub-optimal processing shops. A better, but not optimal, solution would be to partner with a world-class foundry and develop the technology within the walls of their manufacturing environment. Depending on the foundry utilization levels and R&D resource availability, a deal could be negotiated. Caution must be taken with respect to IP sharing and manufacturing rights, two desired attributes for a manufacturing partner willing to divert from its core competency. Depending on the utilization levels and the cyclicality thereof, commitments to R&D projects in such an environment may impact cycle time and project progress. Government-sponsored consortia may provide another alternative, yet these entities typically lack a commercial orientation, have an IP ownership-centric business model, and focus more on pre-competitive R&D for mainstream silicon processing.

A New Business Model

An alternative that goes back to the fundamental principle of foundry model success is recommended: Give people access to a pooled and shared fab environment – an environment focused on process technology development, rather than manufacturing.

The role of the technology development foundry is to be the bridge between the lab and fab in bringing novel silicon technologies and products to market in the nanotechnology era. The development foundry model provides a cost-competitive process development infrastructure in a manufacturing-like fab environment, enabling the accelerated commercialization of proof-of-concepts into real, manufacturing-ready technology solutions.

Under the business model umbrella, enterprises can acquire development time, capability and a business process infrastructure in a commercially oriented open-access facility. Services are provided without a membership fee, without the requirement to share IP, and without the need for developing technology in a research environment – a losing proposition when manufacturing is the end goal.

The business model is an open model where customer engineers reside on-site, are certified to work in the fab, and take control over their own project. To do so, they will rely on an operational infrastructure provided by the development foundry in the form of a clean, stable and available toolset. Together with a focused operations team, this will provide the customer with fast cycles of learning when introducing a new product. In a way, the customer uses the fab as their fab without having to buy, build and manage it.

In any shared development environment, a stereotypical concern is IP and IP protection. IP protection can be ensured through the implementation of a variety of tools and business processes. Solutions start with the deployment of a strong IP policy, a broad workforce training program and proper contractual obligations. In addition, hardware and software solutions can be implemented to further protect the valuable content of processing run cards and recipes.

Embracing this concept will allow an enterprise to focus on its core competencies of product and technology development. The funding agents behind today's high-tech products are in search of management teams that have the vision and capability to leverage advanced outsourcing mechanisms.

Case Study

Matrix Semiconductor (now SanDisk 3D LLC since its acquisition by SanDisk in 2005) proofed the concept of a new memory architecture at Stanford laboratories. To take their new antifuse-based, one-time programmable (OTP) technology to the prerecorded applications market (e.g. game cartridges and digital music albums), they needed to characterize their technology beyond the 4-inch technology capabilities and the limited yield environment of Stanford. Because the gap from 4-inch to 8-inch manufacturing in Asia proved to be too big, they asked Silicon Valley Technology Center (SVTC) to further develop and "productionize" their novel silicon technology before qualification at TSMC.

Conclusions

Tomorrow's traditional silicon chips will continue to be driven by the relentless pursuit of Moore's Law in sub-65 nanometer technologies, which is an unaffordable regime for most of us. Derivative technology development will bring about a new breed of silicon chips, as the silicon platform expands beyond its historical computing, memory and bandwidth applications. Few remedies currently exist to adequately address the fundamental challenges associated with bringing novel silicon technologies from the lab environment into mainstream manufacturing. The fabless community is continually challenged to find an acceptable vehicle to characterize their new technologies once the technologies have graduated from a university lab. The development foundry model is one way the future entrepreneur will be able to turn his silicon ideas into real products cost effectively. He will expand his manufacturing foundry model to include a development foundry, allowing him to independently develop technology and product IP without being distracted by the business of running fabs. ■

About the Author

Bert Bruggeman is the managing director of SVTC, a division of Cypress Semiconductor focused on providing third-party engineering groups access to its advanced semiconductor fab in San Jose, California. SVTC positions itself as the bridge between the lab and the fab to enable the efficient development of novel silicon ideas, from prototyping into real manufacturing. Mr. Bruggeman holds an MSEE from the Catholic University of Leuven, Belgium and joined Cypress Semiconductor from IMEC, Belgium in 1996. Since then, he has held various management positions in technology, operations and business management. He has authored and co-authored over 20 publications in the field of process development and semiconductor operations.