Cypress' CapSense Sigma-Delta Algorithm

Cypress Semiconductor White Paper

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Executive Summary

CapSense Sigma Delta algorithm (CSD) is Cypress' latest capacitive sensing algorithm for the CY8C21x34 and CY8C24x94 PSoC® device family.

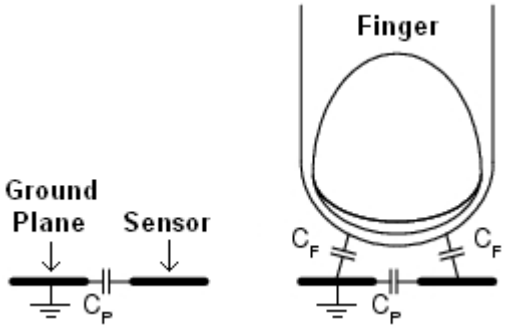
CSD enables the implementation of an array of capacitive sensors through switched capacitor circuitry, an analog multiplexer, digital counting, and PWM functions.

The hardware configuration works in conjunction with high level software routines from the CSD User Module found in PSoC Designer™ to compensate for environmental and physical sensor variations

What is Capacitive Sensing?

A capacitive sensor is a pair of adjacent electrodes (Figure 1). When a conductive object is placed in proximity of the two electrodes, the capacitance changes sending a signal from the sensor to the microcontroller, allowing the planned action to occur. The base capacitance is often referred to as the parasitic capacitance (C_P). The physical sensor itself is typically a copper trace constructed on a PCB, although sensors can be any conductive material. For example, one could use the transparent conductor indium tin oxide (ITO) and print the pattern on a transparent substrate.

Figure 1: Capacitive Sensor



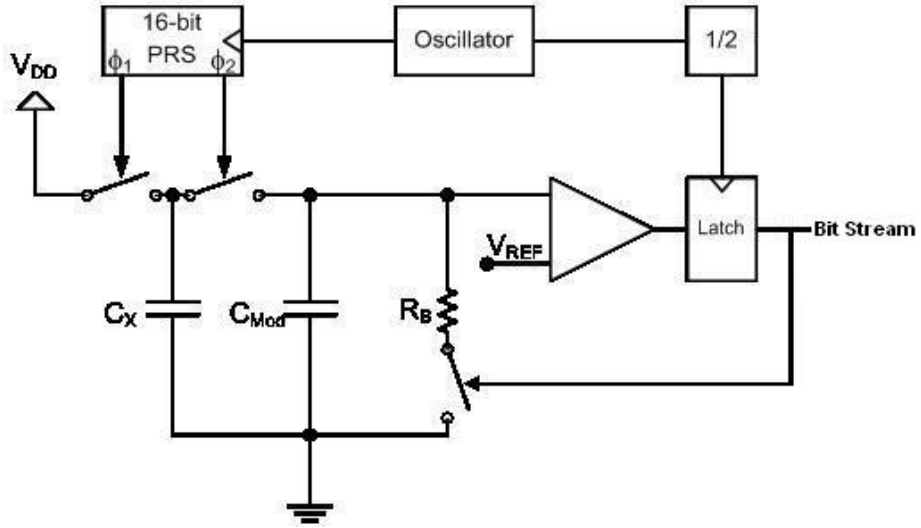
Each sensor is a capacitor with one contact grounded, and the other contact connected to the PSoC's analog global bus. The result is an active variable capacitor, C_X ($C_X = C_P + C_F$). The presence of a conductive object (such as a finger) increases the capacitance of the sensor with reference to ground. Determining sensor activation is then a matter of measuring the change in capacitance.

What is Sigma-Delta?

The CSD algorithm, developed by Cypress, uses the switched capacitor circuitry to convert the sensor capacitance into a voltage, which is compared to a reference voltage. When the capacitor voltage reaches the reference voltage, the comparator triggers a bleed resistor discharging the capacitor. After the capacitor voltage discharges below the reference voltage, the bleed resistor is left floating to allow the capacitor to continue charging. The comparator output becomes a bit-stream as it toggles the bleed resistor and manipulates its input voltage. This bit stream is ANDed with a PWM to provide consistent stream framing. The number of counts in each frame is analyzed to determine if the capacitive sensor was activated.

CSD requires the use of an external modulation capacitor (C_{Mod}) and bleed resistor (R_B) in addition to the sensor capacitor (C_X). Figure 2 shows the input stage for CSD.

Figure 2: CSD Input Stage Block Diagram



Input Stage (Sigma Delta Modulation)

The input stage of the CSD algorithm starts with a switch capacitor network. The network starts with a switch capacitor block connected to V_{DD}. The sensor capacitor (C_X) is connected to the bus and in parallel with the required external modulation capacitor (C_{Mod}). The switch capacitor block is controlled by a 16-bit Pseudo Random Sequencer (PRS). A PRS is used instead of fixed clock source to attenuate emitted noise on C_X by reducing the amount of EMI created by a fixed frequency source and to increase EMI immunity from other sources and their harmonics.

Figure 3: Close Up of C_{Mod} Waveform

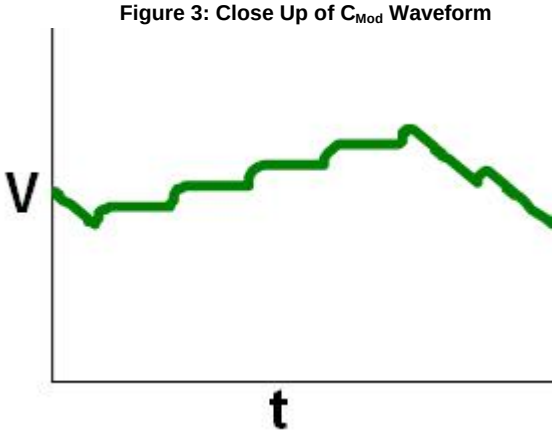
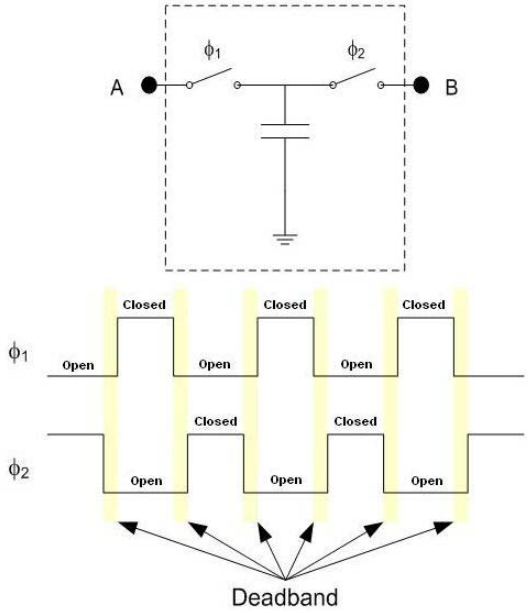


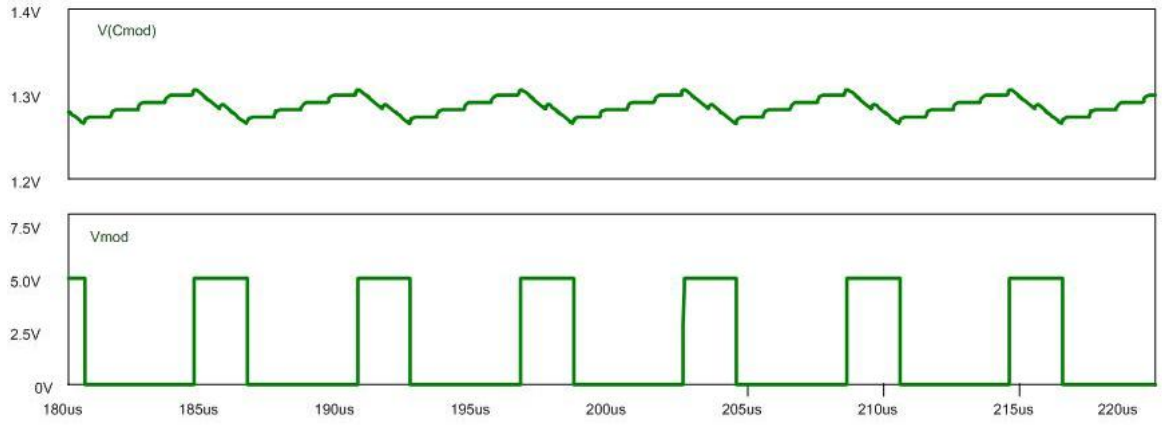
Figure 4: Timing Diagram for Switch Capacitor



The voltage on the external modulation capacitor C_{Mod} is continually charged in small increments due to continuous operation of the switch capacitor as shown by Figure 3. The switch capacitor causes these small voltage increments instead of a smooth increase due to its functional nature. As Figure 4 shows, phase 1 (Φ_1) and phase 2 (Φ_2) of the switch capacitor are never closed at the same time. Therefore, as phase 1 of the switch capacitor closes, it charges C_X. As phase 1 opens, the charge on C_X is held until phase 2 closes, sharing charge from C_X with C_{Mod}. Because the switch capacitor is controlled by the PRS, each incremental step is not uniform in voltage or duration. These minute inconsistencies do not affect CSD algorithm the performance.

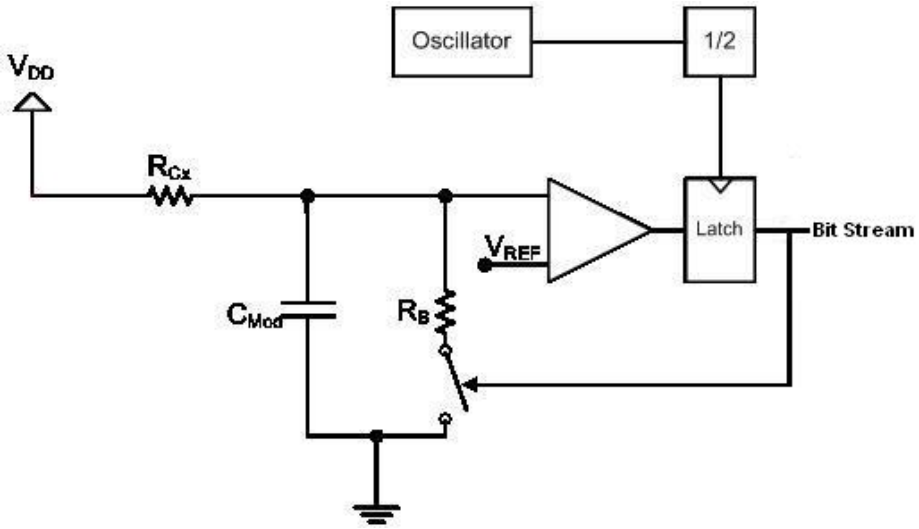
When the voltage reaches V_{REF} the comparator trips, but the latch does not toggle until two clock cycles later. This is due to the latching being clocked at half the speed of the oscillator, which also clocks the PRS. It is known that the latch toggles two cycles after the comparator trips since phase 2 of the switch capacitor and the checking of the latch start on the same cycle. Therefore, the latch waits two cycles before checking again after the comparator trips. This allows for a known time between the tripping point and the latch toggle. This two cycle delay is illustrated in Figure 5.

Figure 5: Comparator Input vs. Latch Output



When the latch output goes high, the switch is closed, connecting the bleed resistor (R_B) to ground which discharges C_{Mod}. Note that the waveform in Figure 3 shows that C_{Mod} is actually charged for several short moments during the discharge phase. This happens because the switch capacitor continues to operate and is dumping charge on C_{Mod} as it is being discharged. Once again, this does not adversely affect operation. After C_{Mod} discharges beyond V_{REF}, the latch does not toggle until after two clock cycles. Therefore, two known times exist: two clock cycles after C_{Mod} increases over V_{REF} and two clock cycles after C_{Mod} decreases beneath V_{REF}; the difference between these two times allows the user to know of a finger's presence. This charging and discharging with a comparator and latch is a form of Sigma-Delta modulation and is where CSD derives its name.

Figure 6: CSD Input Stage Effective Resistance Block Diagram



The switch capacitor block, when running, functions as a resistor as shown in Figure 6. The equivalent resistance is calculated by:

$$R_{Equivalent} = \frac{1}{f_S C_X} \qquad \textbf{(1)}$$

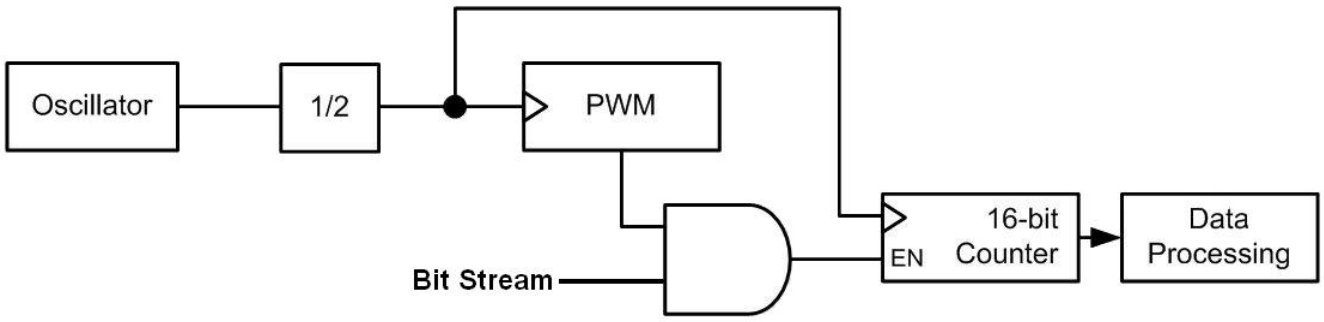
- f_S is the switching frequency of phases 1 and 2
- C_X is the sensor capacitance

When a finger is present on C_X, the equivalent resistance decreases. This decreased resistance causes an increase in the current flowing through R_{Cx}. To maintain the voltage on C_{Mod} near V_{REF}, the switch connecting the bleed resistor (R_B) to ground is closed with a higher duty cycle. Discharging takes longer because the voltage is still applied as it is discharging.

Bit Stream Filter

The opening and closing of the latch by the output of the comparator creates a variable duty cycle bit stream used to determine the presence of a finger on C_X. Figure 7 shows a block diagram of a bit stream filter that takes the output from the latch and processes it.

Figure 7: CSD Bit Stream Filter



The bit stream is first ANDed with a PWM, which is clocked at the same frequency as the latch, to create measurement windows as shown in Figure 8. These measurement windows are fed directly into the enable input in a counter, which is also clocked at the same frequency as the latch. As each bit from a measurement goes into the enable input, the counter records the number of clock cycles that occur during its length. Since the duty cycle of the bit stream increases with higher capacitance, more counts are measured when a finger is present, as shown in Figure 9. The counter only records the number of clock cycles for one measurement window at a time as the PWM resets the counters by setting an interrupt when transitioning from high to low.

Figure 8: Counts Window as Created by ANDing Bit Stream with PWM

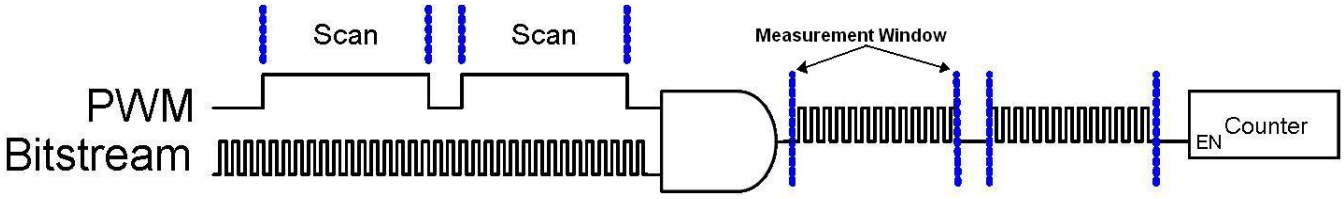
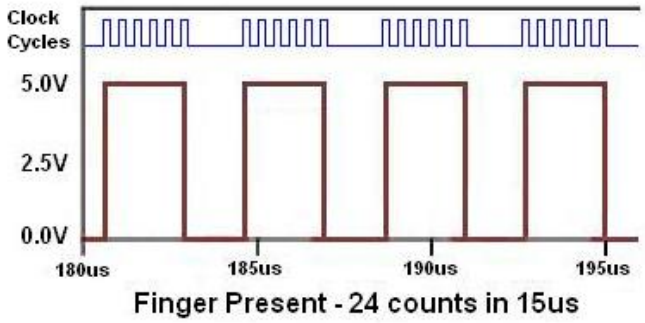
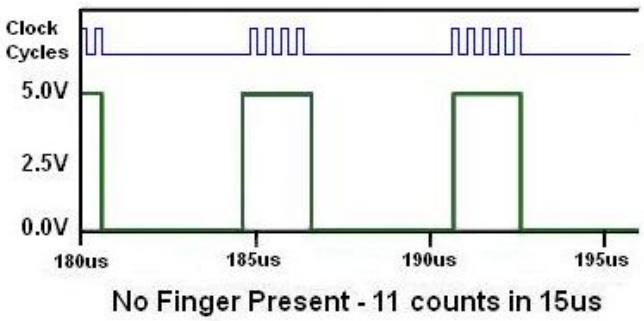


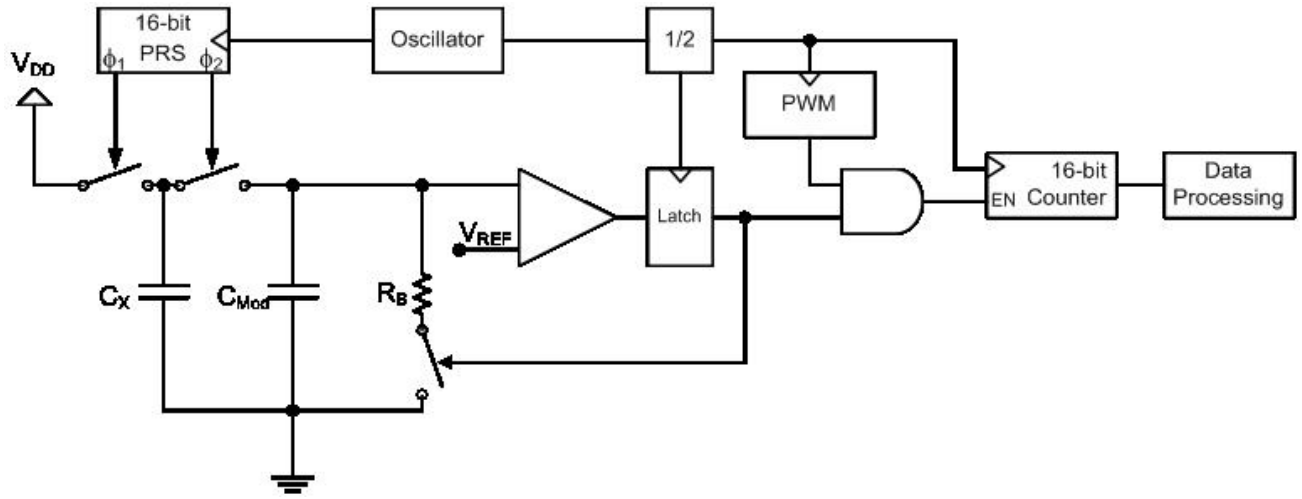
Figure 9: Finger Present Counts vs. No Finger Present Counts as Recorded by the Counter





The raw number of clock cycles (referred to as 'counts') from the counter are updated to a register used by the CSD algorithm for determining a finger's presence, as well as setting the baseline and adapting to environmental conditions. The CSD algorithm looks at several measurement windows for each sensor depending on user settings.

Figure 10: Complete Schematic for CSD



Summary

The PSoC Mixed Signal Array is a configurable array of digital and analog resources, flash memory, RAM, an 8-bit microcontroller and several other features. These features allow PSoC to implement innovative capacitive sensing techniques in its CapSense portfolio. PSoC's intuitive development environment can be used to configure and reconfigure the device to meet design specifications and specification changes. CapSense Sigma Delta exhibits exceptional sensitivity and noise immunity, low power consumption and a fast update rate, along with the flexible design process inherent to the PSoC.

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