White Paper

Developing Low-Cost Modular Handset Architectures Using Dual-Port Interconnects

The time to introduce a new handset into the market is shrinking. Along with a shorter time-to-market window, the complexity of the features necessary for a successful product is increasing. As the handset market has evolved, so have the functions supported by a handset: cameras, internet browsing, streaming video, MP3, gaming and PDA functionality are all being added to the basic voice handset functionality.

These market requirements force handset designers to take an incremental approach to handset system design—they add functionality to their existing designs, trying to keep the redesign of both hardware and software to a minimum. They also rely on some of these emerging features being integrated into hardware as they become widely acceptable. However, the hardware integration cycle is much longer (18 to 24 months) than the time available to introduce the feature to the market.

Under these conditions, system designers rely on merely upgrading existing architectures with dedicated hardware that are capable of supporting new functionalities.

Quickly Upgrading an Existing Architecture

An existing architecture centered around a main processor—for example, a baseband modem—can be enhanced by adding an additional processing element (ASIC, DSP, GPP) to it—for example, a general-purpose processor running games or video compression. The new processing element has to interface with the existing architecture with as little change as possible. The interface further needs to offer enough throughput to support high-bandwidth connectivity.

The existing memory bus, connected to a dual-port interconnect, serves as a perfect candidate for a simple, high throughput interface. This approach causes limited changes to the existing system since the existing processor only perceives additional memory (see *Figure 1*).

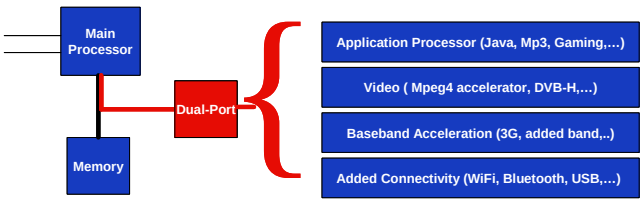

Figure 1. Upgrading an Architecture by Connecting a Dual-Port on an Existing Memory Bus

A dual-port interconnect is a piece of shared memory with two fully independent SRAM interfaces. It allows two processing elements to connect via their memory buses and to communicate at high bandwidth. In the case of a handset, it provides an easy way to add functionality to an existing architecture. One port is connected to the existing processor's memory bus and the other port is connected to any type of device with an SRAM interface. These devices include any type of processor (adding gaming, MP3, video, or even PDA functionality), or modem (adding a new communication band, 3G acceleration, 802.11 connectivity or Video Broadcast).

Modular Architecture Strategy

Handset product life cycles are shrinking, which means that system houses cannot afford to invest their R&D budgets on platforms that will last for only one product life cycle. They have to create platforms that can evolve from one generation of handsets to the next, thereby amortizing the R&D investment over multiple product cycles.

This can only be accomplished by creating platforms with modular architectures that enable subsystems to be upgraded independently, with shorter development time and at lower costs. Modular architectures provide a very flexible platform that can keep pace with the market requirements.

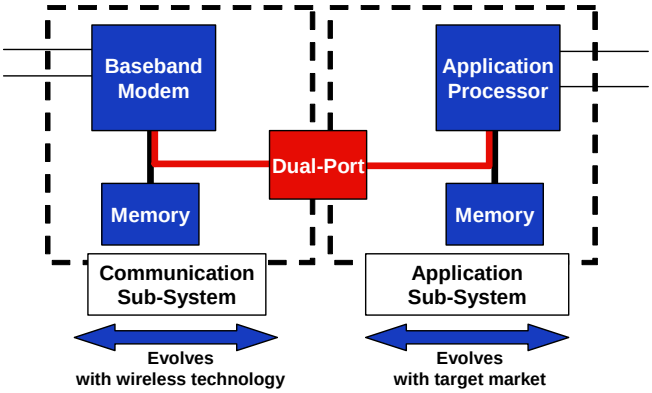

Figure 2. Defining Different Subsystems with Independent Evolution using a Dual-Port

In addition to quick development and shorter debugging time, a modular architecture further allows the re-use of similar subsystems across handsets that are targeted at different markets. The cost of each solution can be adapted by picking different processing elements—for instance, choosing from the simplest to the cutting-edge of multimedia application processors, interfacing with the same baseband modem. Dual-ports also allow for the simplest communication mechanism (read and writes to memory) between two subsystems. This implies that the software overhead on each subsystem is reduced to a minimum.

A dual-port interconnect contributes directly to creating a modular platform, by offering a simple and standard memory-mapped interface, and therefore allowing a given

sub-system to interface to any other subsystem, present or future. This enables the newly created platform to elegantly evolve to future market requirements.

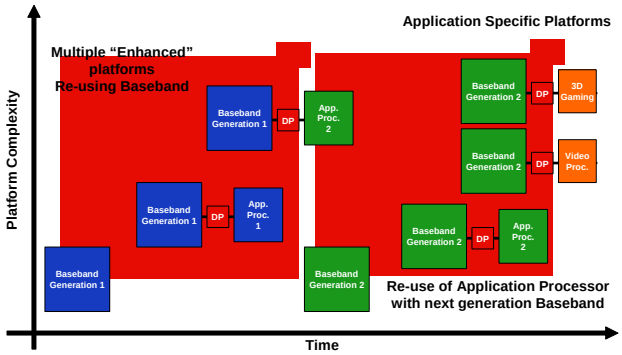

Figure 3. Example of a Portfolio using a Modular Architecture Strategy

Figure 3 describes the evolution of a handset OEM's portfolio. The OEM has a modular system strategy: a single baseband chip is used in the simplest designs; it is then enhanced multiple times to create several new products by the addition of different application processors via a dual-port interconnect. The dual-port interconnect enables two completely different applications processors to be added to the baseband processor with minimal changes. This architecture allows the OEM to continue to introduce competitive products into the market while the next generation baseband processor is still under development. This platform can be further upgraded with the next generation baseband processor via the same dual-port interface.

The Dual-Port Interconnect

A dual-port is the most flexible interprocessor interconnect available today. By offering a standard SRAM interface that connects with the existing memory bus, it allows an existing processor to interface with almost any other processing element. It also simplifies and reduces the communication software overhead.

Cypress Semiconductor Corporation combined its expertise in dual-port architecture and low-power technology to build the low-cost MoBL® (More Battery Life™) Dual-Port, designed and priced specifically for mobile platforms. The Cypress MoBL Dual-Port also solves several other needs of advanced handset architectures.

In terms of power, the Cypress MoBL low-leakage technology allows the dual-port's standby power consumption to be below 3.6 µW at 1.8V. This makes the Cypress MoBL Dual-Port the lowest-power dual-port available in the market today. With the wide variety of baseband and other processors on the market, it also supports multiple I/O voltage (1.8V, 2.5V and 3V).

Further, the bandwidth requirements on wireless systems continue to increase. Wireless systems are also now required to support non-cellular technologies, such as 802.11b, with data rates up to 11 Mbps. Standard low-speed serial interconnects, when available on some processors, cannot usually provide the required bandwidth. The Cypress MoBL Dual-Port offers fast access, 35 ns, over an x16 bus, allowing over 400 Mbps of throughput, which exceeds the data rate requirements of 3G, WiFi or Video Broadcast.

Small footprint being another requirement, the Cypress MoBL Dual-Port is available as die or packaged in a small 6x6 mm 0.5 mm-pitch BGA.

In terms of functionality, the Cypress MoBL Dual-Port behaves as any other Cypress asynchronous dual-port. A busy signal is asserted when both ports try to access the same memory space at the same time, providing built-in arbitration. A mailbox functionality allows the two processors to send each other interrupts, simply by writing to a specific location. This can be used as a way to signal to the other processor that data is available for download.

Handset system designers want to minimize the number of GPIO pins that drive very simple functionality, such as reading external DIP switches or lighting up LEDs. The Cypress MoBL Dual-Port allows some of these signals to be external to the processor by incorporating input read registers and output drive registers into its features. The Input Read Register (IRR) captures in a specific memory space the status of two external binary devices such as DIP switches. By simply reading from the Dual-Port, either processor can monitor the status of these two devices. The Output Drive Registers (ODR) can drive up to five interrupts signals. This allows either processor to control up to five external devices by just writing onto a specific location in the dual-port.

Conclusion

Embedded applications on handsets change quickly and therefore the time available between two generations of handset platforms is shrinking. This causes OEMs to pick modular architectures for their systems that can adapt to the accelerated pace of the market. Dual-Ports play a key role in these modular designs by enabling the incremental evolution of multiple subsystems, which communicate at high bandwidth via a standard memory bus interface. To answer this emerging need, Cypress has designed and priced the new MoBL Dual-Port specifically for this type of application, making it the lowest power Dual-Port available.