CYPRESS SEMICONDUCTOR

FINAL PRODUCT CHANGE NOTIFICATION

PCN: PCN030013 **DATE:** March 26, 2003

Subject: SRAM, 8 Meg, 1.8V, Slow Asynchronous Die Change

To:

Description of Change:

The part numbers listed below have been qualified to be transferred from R7, 0.15m CMOS process, to R8, a 0.13m CMOS process in Cypress's Bloomington, MN, Fab 4. This will result in a die shrink. The new die revision is D and is marked on the device after the date code.

Data Sheet Changes:
1.- The ordering part number has been revised to contain the letter "D" to designate the new die. (EX: CY62157DV18*)

2.-Some electrical parameter limits have changed as described in the "Benefits of Change' section at the bottom of this page.

New datasheets have been issued to reflect these changes and can be downloaded from the following link:

http://www.cypress.com/sram/datasheets.html#MoBLÔ

The new device has the same fit, form, and function. The Qualification report QTP# is attached.

Benefit of Change: This change will increase the number of good die per wafer resulting in shorter lead-times and improved availability.

Part Numbers Affected:
Affected Parts: 04

Affected Part	Description
CY62155CV18*	
CY62157CV18*	
CG5802ATT	
CG6060ATT	

Customer Part Numbers Affected:
Affected Parts: 00

CYPRESS SEMICONDUCTOR

FINAL **PRODUCT CHANGE NOTIFICATION**

Qualification Status:
Completed- QTP#031102

Sample Status:
Available Now

Approximate Implementation Date:
Production release of the new product will be phased in WW0314 or as agreed per your contract terms and conditions. We encourage conversion to the new revision product as quickly as possible. The old revision product has been discontinued and is available in limited quantities only. Please contact your local sales representative for availability information.

Response Required:
Your company requires written approval of changes prior to the shipment of changed product. There is no time limitation. If you have current orders pending, this form must be signed and returned as soon as possible. If acceptance is not received, delays in shipment may occur unless you have special agreement with our sales office.

Change accepted by_____________________ Print Name____________________
Title_____________________ Date_____________________

Fax signed approval to Banjie Bautista at 408-943-2165 or reply by E-mail to pcn_adm@cypress.com

Sincerely,

Banjie Bautista
PCN Process Manager

John Quist
Director of Quality Systems

Cypress Semiconductor
Technology Qualification Report

QTP# 031102 VERSION 1.0
March 2003

R8LD-1.8V Technology, Fab4	
High Performance Static SRAM	
CY62155DV-2XWI **CY62155DV18** **CY62157DV18** **CY62157DV20**	**512K x 16** **Static RAM**

MoBL2™ and More Battery Life™ is trademark of Cypress Semiconductor

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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Reliability Director
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TECHNOLOGY QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
031102	New Technology R8LD-1.8V / New Device, 8Meg, MoBL Static RAM CY62155DV* and family	Mar 03

PRODUCT DESCRIPTION (for qualification)		
Qualification Purpose: Qualify New Technology R8LD-1.8V, Fab 4 and CY62155DV* device and family.		
Marketing Part #:	CY62155DV* / CY62157DV18, CY62157DV20	
Device Description:	1.65V – 2.2V, Industrial available in 48-ball FBGA package.	
Cypress Division:	Cypress Semiconductor Corporation –Memory Product Division (MPD)	
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. D
What ID markings on Die:	7C62355D	

TECHNOLOGY/FAB PROCESS DESCRIPTION – R8LD-1.8V			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 150Å Ti / 3,000Å Al 0.5%Cu/ 300Å TiW Metal 2: 300Å Ti/8,000Å Al 0.5%Cu / 300Å TiW
Passivation Type and Materials:	1000Å TEOS / 9000Å Nitride		
Free Phosphorus contents in top glass layer(%):	0%		
Number of Transistors in Device	48 million		
Number of Gates in Device	48 million		
Generic Process Technology/Design Rule (µ-drawn):	CMOS, Double Metal /0.13 µm		
Gate Oxide Material/Thickness (MOS):	SiO_2, 32Å		
Name/Location of Die Fab (prime) Facility:	Cypress Semiconductor -- Bloomington, MN		
Die Fab Line ID/Wafer Process ID:	Fab4/R8LD-1.8V		

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
48-ball FBGA	**TAIWN-G, QTP #011102**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	BA48
Package Outline, Type, or Name:	48-ball Fine Pitch Ball Grid Array (FBGA)
Mold Compound Name/Manufacturer:	PLASKON SMT-B1-LAS
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	>28%
Substrate Material:	BT Resin
Lead Finish, Composition / Thickness:	Solder Ball, 63%Sn, 37%Pb
Die Backside Preparation Method/Metallization:	N/A
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	Ablestik 8355F
Die Attach Method:	Epoxy
Bond Diagram Designation:	10-04689
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0um
Thermal Resistance Theta JA °C/W:	55°C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	49-41020
Name/Location of Assembly (prime) facility:	ASE Taiwan

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	**USA-C, CML-R**
Fault Coverage:	100%

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max = 2.4V, 125°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max = 2.4V, 150°C	P
High Temperature Steady State Life	Static Operating Condition, Vcc Max = 2.2V, 150°C	P
High Accelerated Saturation Test (HAST)	130°C, 2.2V,85%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30C/60%RH+3IR-Reflow, 235°C+5, 0°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity MSL3 192 Hrs, 30C/60%RH+3IR-Reflow, 235°C+5, 0°C	P
Pressure Cooker	121°C, 100%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30C/60%RH+3IR-Reflow, 235°C+5, 0°C	P
High Temperature Storage	150°C ± 5°C no bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Age Bond Strength	200C, 4HRS MIL-STD-883, Method 883-2011	P
Low Temperature Operating Life	-30C, 2.35V, 8MHZ	P
Acoustic Microscopy, MSL 3	Cypress Spec. 25-00104	P
Dynamic Latch-up	125C, 3.55V	P
Static Latch-up	125C, 6.5V, ± 300mA In accordance with JEDEC 17. Cypress Spec. 01-00081	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[4]	Failure Rate
High Temperature Operating Life Early Failure Rate	6,485	2	N/A	N/A	154 PPM
High Temperature Operating Life[1,2,] Long Term Failure Rate	573,280 DHRs	0	0.7	170	9 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A = The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 031102

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC-MSL3							
CY62157DV20 (7C62357D)	4151609	*610205573N*	*TAIWN-G*	COMP	20	0	
CY62157DV20 (7C62357D)	4205767	*610210027*	*TAIWN-G*	COMP	20	0	
CY62157DV20 (7C62357D)	4210625	*610216786N1*	*TAIWN-G*	COMP	20	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 2.4V, Vcc Max							
CY62157DV20 (7C62357D)	4247883	*610303398*	*TAIWN-G*	96	1390	0	
CY62157DV20 (7C62357D)	4230988	*610240982N*	*TAIWN-G*	96	1191	0	
CY62157DV20 (7C62357D)	4151609	*610205573N*	*TAIWN-G*	72	1109	0	
CY62157DV20 (7C62357D)	4205767	*610210027*	*TAIWN-G*	72	858	1	1-GF SINGLE BIT
CY62157DV20 (7C62357D)	4210625	*610216786N1*	*TAIWN-G*	72	1103	1	1-NONE VISUAL
CY62157DV20 (7C62357D)	4214343	*610221185*	*TAIWN-G*	72	834	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 2.4V, Vcc Max							
CY62157DV20 (7C62357D)	4222101	*610234320*	*TAIWN-G*	80	416	0	
CY62157DV20 (7C62357D)	4222101	*610234320*	*TAIWN-G*	500	383	0	
CY62157DV20 (7C62357D)	4230988	*610240982N*	*TAIWN-G*	80	418	0	
CY62157DV20 (7C62357D)	4230988	*610240982N*	*TAIWN-G*	500	415	0	
CY62157DV20 (7C62357D)	4214343	*610221185*	*TAIWN-G*	80	410	0	
CY62157DV20 (7C62357D)	4214343	*610221185*	*TAIWN-G*	500	330	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 2.2V, Vcc MAX							
CY62157DV20 (7C62357D)	4151609	*610205573N*	*TAIWN-G*	80	80	0	
CY62157DV20 (7C62357D)	4151609	*610205573N*	*TAIWN-G*	180	74	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY62157DV20 (7C62357D)	4151609	*610205573*	*TAIWN-G*	COMP	9	0	
CY62157DV20 (7C62357D)	4205767	*610210027*	*TAIWN-G*	COMP	9	0	
CY62157DV20 (7C62357D)	4210625	*610216786*	*TAIWN-G*	COMP	9	0	
CY62157DV20 (7C62357D)	4215571	*610222767N*	*TAIWN-G*	COMP	9	0	
CY62157DV20 (7C62357D)	4216781	*610223553*	*TAIWN-G*	COMP	9	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY62157DV20 (7C62357D)	4215571	*610222767N*	*TAIWN-G*	COMP	9	0	
CY62157DV20 (7C62357D)	4214343	*610221278*	*TAIWN-G*	COMP	9	0	
CY62157DV20 (7C62357D)	4216781	*610223553*	*TAIWN-G*	COMP	9	0	
STRESS: DYNAMIC LATCH-UP TESTING, 125C, 3.55V							
CY62157DV20 (7C62357D)	4205767	*610210027*	*TAIWN-G*	COMP	3	0	

Reliability Test Data

QTP #: 031102

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: STATIC LATCH-UP TESTING, 125C, 6.5V, ±300mA							
CY62157DV20 (7C62357D)	4151609	*610205573*	*TAIWN-G*	COMP	3	0	
CY62157DV20 (7C62357D)	4205767	*610210027*	*TAIWN-G*	COMP	3	0	
CY62157DV20 (7C62357D)	4210625	*610216786*	*TAIWN-G*	COMP	3	0	
STRESS: LOW TEMPERATURE OPERATING LIFE, -30C, 2.35V							
CY62157DV20 (7C62357D)	4151609	*610205573*	*TAIWN-G*	500	50	0	
STRESS: HIGH TEMPERATURE STORAGE, 150C							
CY62157DV20 (7C62357D)	4151609	*610205573N*	*TAIWN-G*	500	50	0	
CY62157DV20 (7C62357D)	4151609	*610205573N*	*TAIWN-G*	1000	50	0	
STRESS: AGE BOND STRENGTH							
CY62157DV20 (7C62357D)	4151609	*610205573*	*TAIWN-G*	COMP	5	0	
CY62157DV20 (7C62357D)	4205767	*610210027*	*TAIWN-G*	COMP	5	0	
CY62157DV20 (7C62357D)	4210625	*610216786*	*TAIWN-G*	COMP	5	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, PRE COND 192 HR 30C/60%RH, MSL3							
CY62157DV20 (7C62357D)	4151609	*610205573N*	*TAIWN-G*	176	50	0	
CY62157DV20 (7C62357D)	4205767	*610210027*	*TAIWN-G*	176	50	0	
CY62157DV20 (7C62357D)	4210625	*610216786N1*	*TAIWN-G*	168	50	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 1.98V, PRE COND 192 HR 30C/60%RH, MSL3							
CY62157DV20 (7C62357D)	4151609	*610205573*	*TAIWN-G*	128	50	0	
CY62157DV20 (7C62357D)	4205767	*610210027*	*TAIWN-G*	128	48	0	
CY62157DV20 (7C62357D)	4210625	*610216786*	*TAIWN-G*	128	59	0	
STRESS: TC COND. C -65C TO 150C, PRECONDITION 192 HRS 30C/60%RH, MSL3							
CY62157DV20 (7C62357D)	4151609	*610205573N*	*TAIWN-G*	300	40	0	
CY62157DV20 (7C62357D)	4205767	*610210027*	*TAIWN-G*	300	50	0	
CY62157DV20 (7C62357D)	4210625	*610216786N1*	*TAIWN-G*	300	50	0	