

# AIROC™ CYW20835 Bluetooth® LE system on chip hardware design guidelines

## About this document

This document discusses the hardware design guidelines for the AIROC™ CYW20835 Bluetooth® LE system on chip kit.

## Scope and purpose

This document provides basic guidelines on layout for AIROC™ CYW20835 Bluetooth® LE system on chip.

## Intended audience

This document provides hardware guidance on how to design with CYW20835.

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**Basic layout guidelines**

# 1 Basic layout guidelines

Most Bluetooth® devices use four-layer boards to minimize thickness. Components are placed on the top layer; the bottom layer is a solid ground fill. Most signal traces are routed on the top layer.

For RF traces, use a 50-ohm transmission line to minimize mismatch losses and reflections, and therefore maximize the power transferred to the load.

There are two types of transmission lines: microstrip and stripline. The reference design uses the microstrip design.

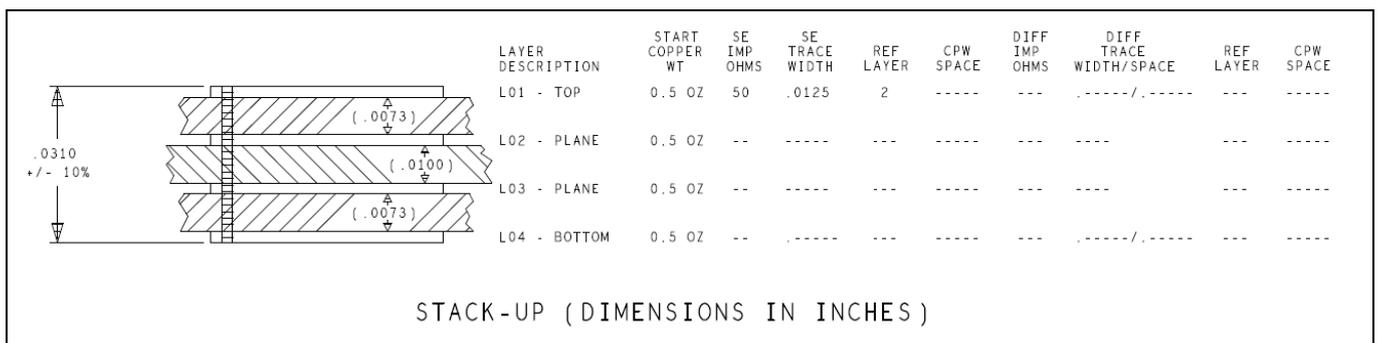
Transmission lines require a proper geometry. Some parameters are highly dependent on the dielectric material – trace width, vertical distance to ground plane, and a solid ground plane of sufficient width. Different height and width solutions perform differently.

For the microstrip layer and its reference ground layer selections, two things should be considered:

1. Thinner traces have higher insertion loss – PCB fabrication requires adequate trace width for reliability and repeatability. The heights between the microstrip and ground should be thick enough to guarantee adequate trace width for the microstrip.
2. For microstrip lines, avoid sharp corners; use a smooth radius to change directions. The coplanar ground follows the contour of these traces with a clearance of two to three line widths (2 W to 3 W). Connect the outer layer to the reference ground plane using vias so that they surround the microstrip trace.

The microstrip is used in this reference design is on Layer 1. The reference ground is Layer 2. This reference design uses a four-layer PCB with a stack up as shown in **Figure 1**.

- Layer 1: Main signal layer
- Layer 2: Solid ground layer
- Layer 3: Power signal layer
- Layer 4: Digital signal layer. Additional power signals that could not be routed on Layer 3 can be routed here as well. However, you must ensure that they do not overlap any of the power signals on Layer 3.



**Figure 1 Typical board stackup used for CYW20835**

**Component placement**

## 2 Component placement

As a rule, follow the receive signal flow from the antenna to the antenna matching and filter circuits, then to the low-noise amplifier (LNA) chip input. Keep the radio front end (RF), power management unit (PMU), and baseband (BB) decoupling capacitors next to CYW20835 pin pads.

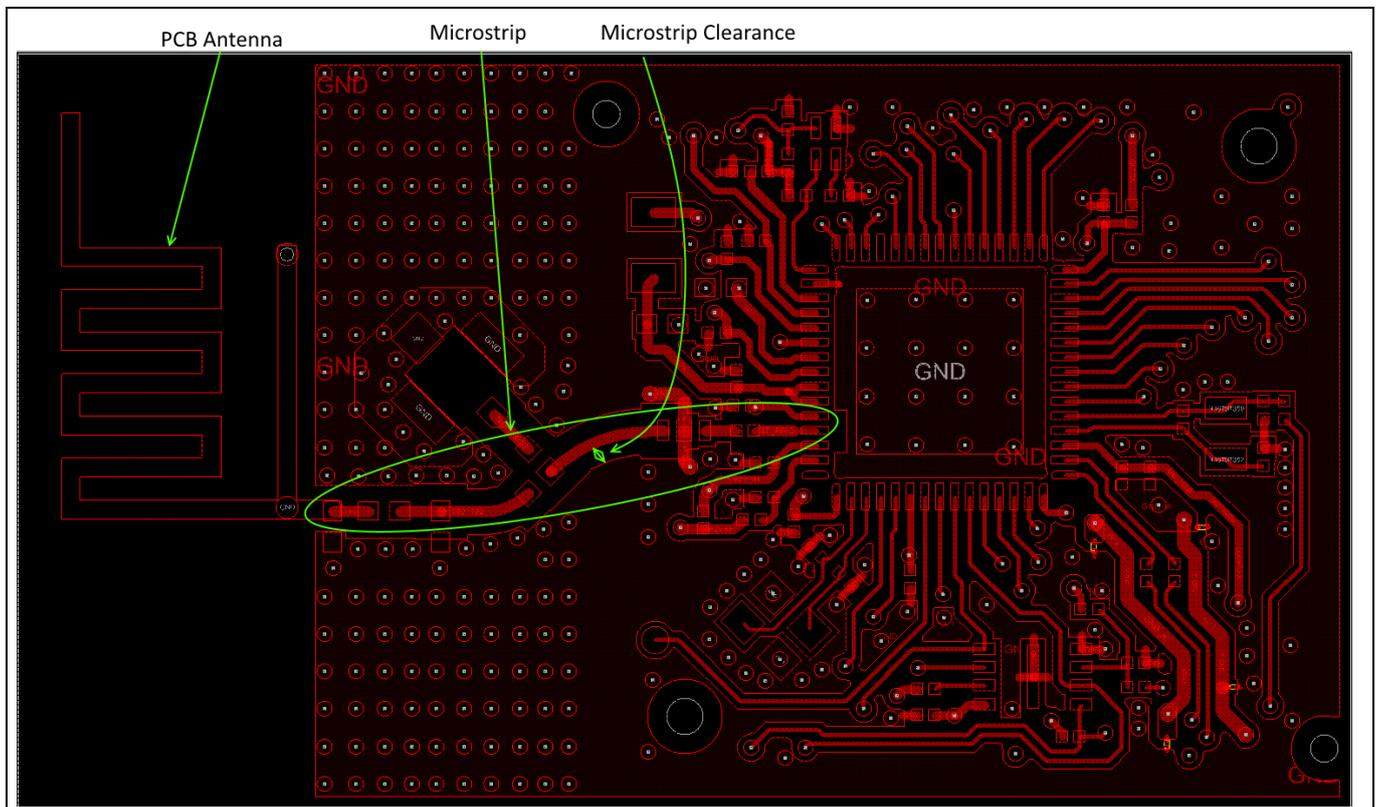
### 2.1 Antenna placement

Keep the antenna connection to the device as short as possible. Maintain a solid ground near the antenna and adequate ground clearance for the layers beneath the antenna.

In the reference design, the antenna is on the top layer on the left of the board next to the CYW20835 chip.

### 2.2 PCB antenna

For more details on PCB antennas, see [AN91445 - Antenna design and RF layout guidelines](#). For the associated Gerber file, visit <https://www.cypress.com/go/AN91445>.



**Figure 2** Antenna placement and microstrip clearance

### 2.3 Crystal placement

Protect the crystal and related traces from noise sources, and use a solid ground to separate the crystal from RF traces. The crystal ground plane should have direct vias to the reference ground plane.

You can find the crystal specification requirements in the CYW20835 datasheet. See the reference design BOM for the recommended vendor part numbers.

## Component placement

### 2.4 Decoupling capacitors

See the reference schematic for decoupling capacitor usage and values on different power domains. Infineon recommends that you use the vendor and part numbers shown in the reference design BOM. Decoupling capacitors must be placed as close to its associated pin as possible.

### 2.5 Ground vias

Do not use long thin traces to connect components to ground vias; doing so adds inductance that can significantly alter circuit performance.

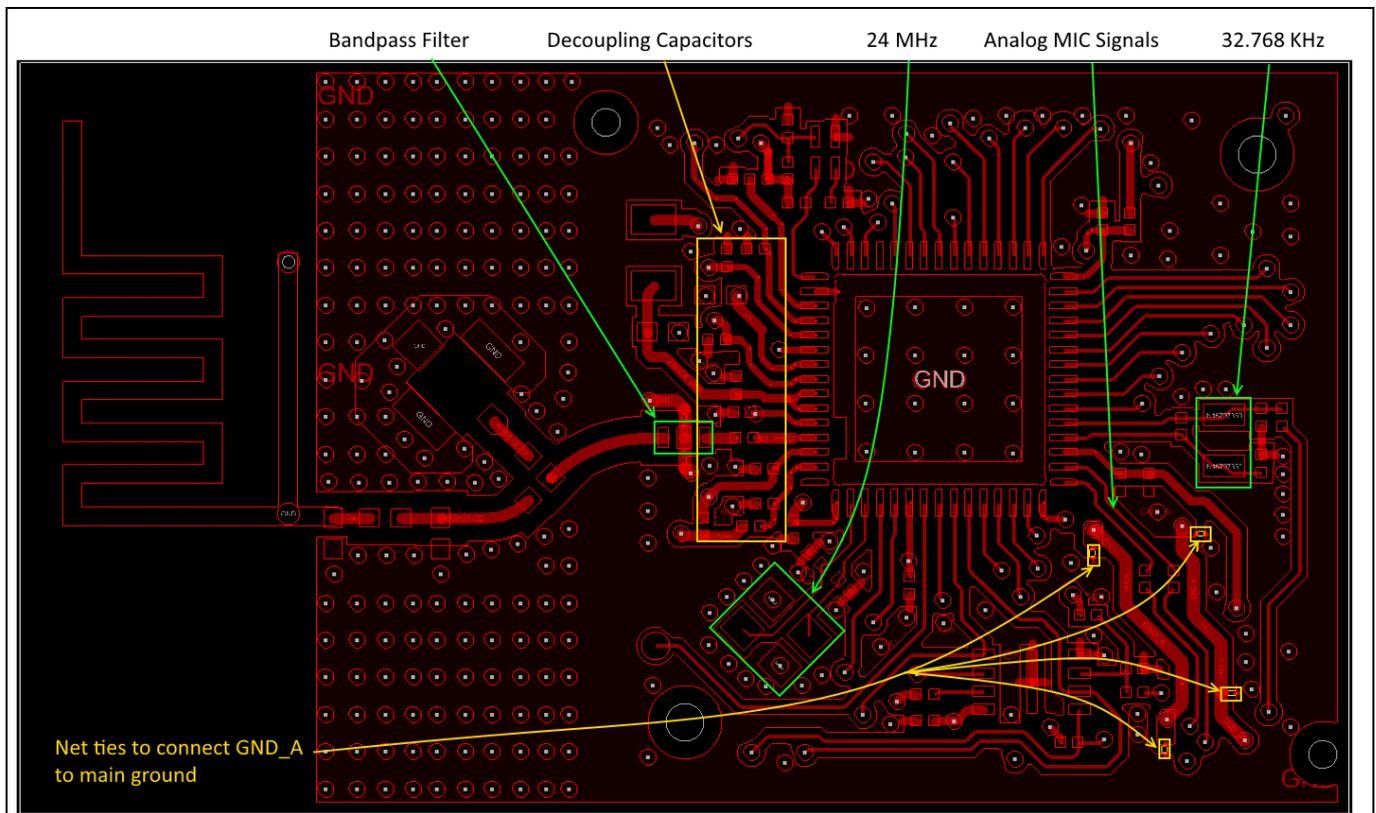
### 2.6 Bandpass filter

Place a chip bandpass filter between the antenna matching components and the CYW20835 device to attenuate harmonics from CYW20835. The chip band pass filter part used in the CYW20835 reference design is Murata, LFB182G45CL3D178.A microstrip is used for all connections of the bandpass filter.

Insertion loss and out-of-band attenuation performance depend on PCB component layouts and tolerances. Filter layout should follow general RF layout rules.

### 2.7 Analog mic signals

Place a series 0.1- $\mu$ F capacitor for each of the analog MIC signals, MIC\_P and MIC\_N. MIC\_P and MIC\_N should also be routed within the analog ground (GND\_A) area as shown in **Figure 3**. Use net ties to shown in **Figure 3** to stitch GND\_A to the main ground. The analog MIC is powered by the CYW20835's MIC\_BIAS pad by default.



**Figure 3** Bandpass filter and decoupling capacitors

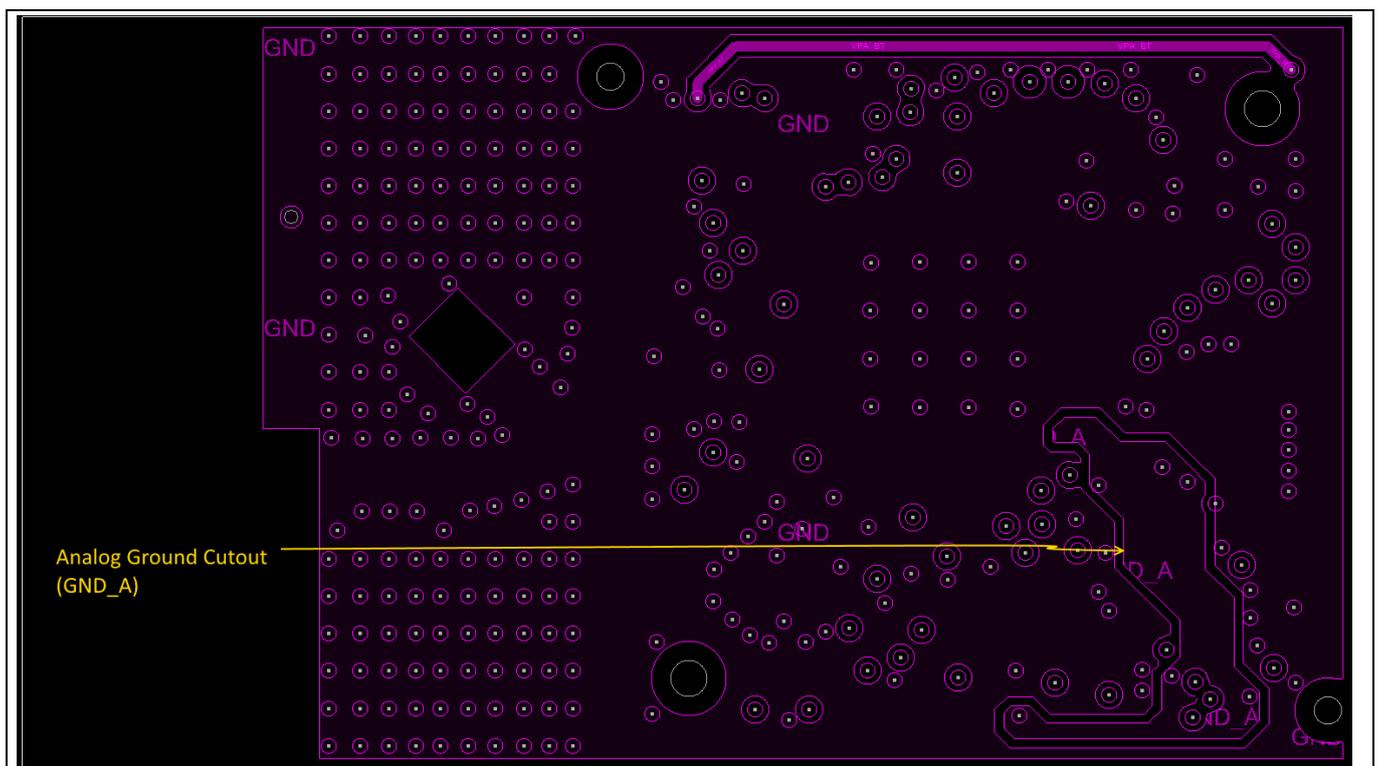
## Component placement

### 2.8 Serial flash

The CYW20835 kit uses the GD25WD80C serial flash from GigaDevice. Place the flash device on the same side as pins 35–40 of the CYW20835 device so that serial flash signals are relatively short; this helps to minimize unnecessary crossing with other signals.

### 2.9 Layer 2, solid ground fill

Fill the layer immediately below the layer where CYW20835 is located (Layer 2), with solid ground for optimal ground return path. An analog ground (GND\_A) cutout for the analog MIC is necessary. The GND\_A cutout should cover all of the analog MIC signal and power traces on Layer 1.



**Figure 4** Layer 2, solid ground fill

### 2.10 Power traces

- Use wide traces for power supply lines. You should calculate the maximum current to be carried on each trace and make the trace width proportionate to the current
- Route the main DC power supply line up the middle of the board like a spine, branching off left and right as needed

### 2.11 Avoid routing DC power in a loop

- Protect the RF power supply from main power, noisy signals, and digital power by separating with ground fill
- Ensure that adequate power trace width and vias are available (or present) to minimize parasitic impedance
  - CBUCK\_OUT → Minimum 12 mils trace width
  - CBUCK\_OUT to DIGLDO\_VDDIN (pin 25) → Minimum 8 mils trace width
  - VDDIO → Minimum 12 mils trace width

## Component placement

- VDDIO to LHL\_VDDO (pin 60)/BT\_VDDO (pin 36) → Minimum 8 mils trace width
- BT\_VDDC → Minimum 10 mils trace width
- BT\_VDDC (pin 37) → Minimum 8 mils trace width
- VBAT to SR\_VDDBAT3V (pin 22) → Minimum 12 mils trace width
- CBUCK\_OUT to RFLDOIN (pin 24) → Minimum 8 mils trace width
- RFLDO\_VDDOUT (pin 12) to 1P2VRF → Minimum 8 mils trace width
- VPA\_BT → Minimum 12 mils trace width
- PALDO\_VDDOUT3V (pin 20) to BT\_PAVDD2P5 (pin 26) → Minimum 8 mils trace width
- 1P2VRF → Minimum 8 mils trace width
- 1P2VRF to IFVDD1P2 (pin 19)/PLLVDD1P2 (pin 21) / VCOVDD1P2 (pin 20) → Minimum 8 mils trace width
- MIC\_AVDD (pin 48) → Minimum 8 mils trace width
- MIC\_BIAS (pin 45) → Minimum 8 mils trace width

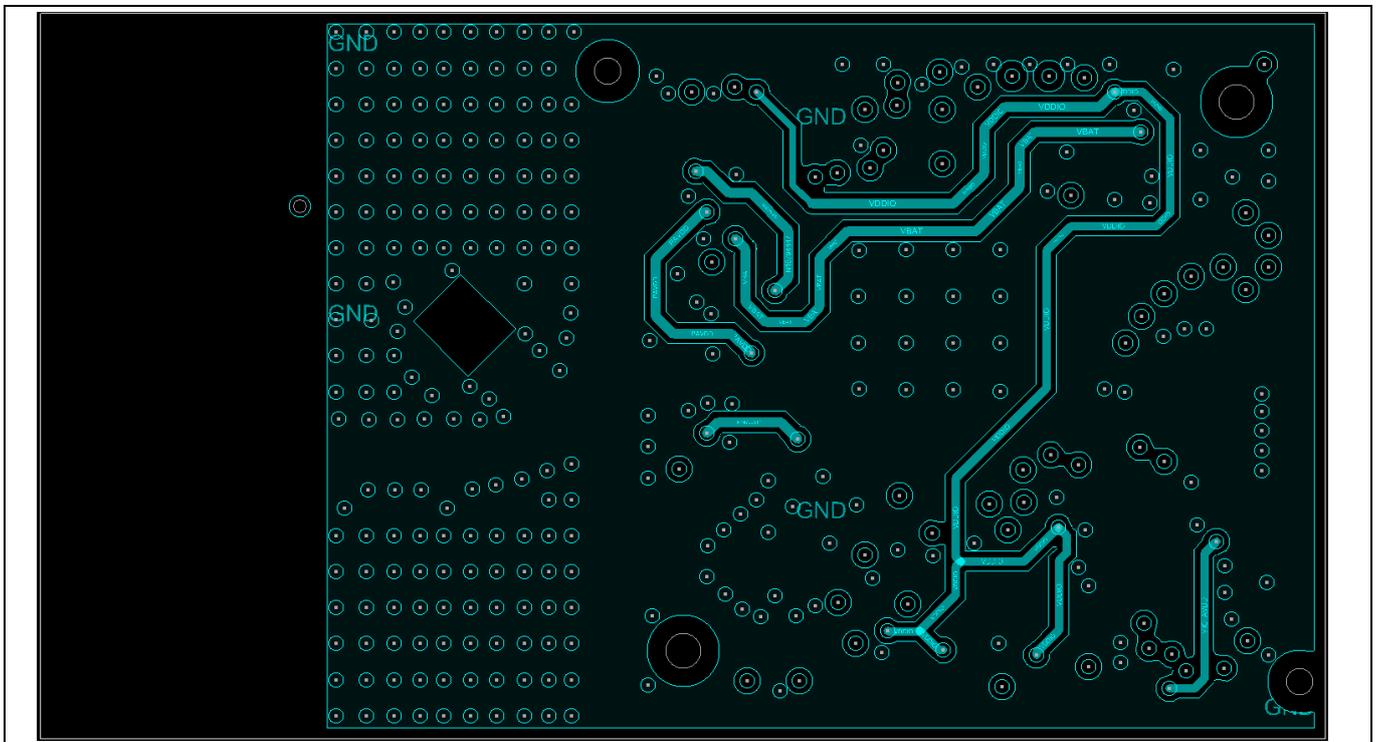


Figure 5 Power supply traces

## 2.12 Power inductor

Ensure that there is ground isolation between the power inductor and the RF area. The power inductor should also be placed as close to CBUCK pins as possible. See the “Recommended component” section in the CYW20835 datasheet, and reference design files for the recommended component.

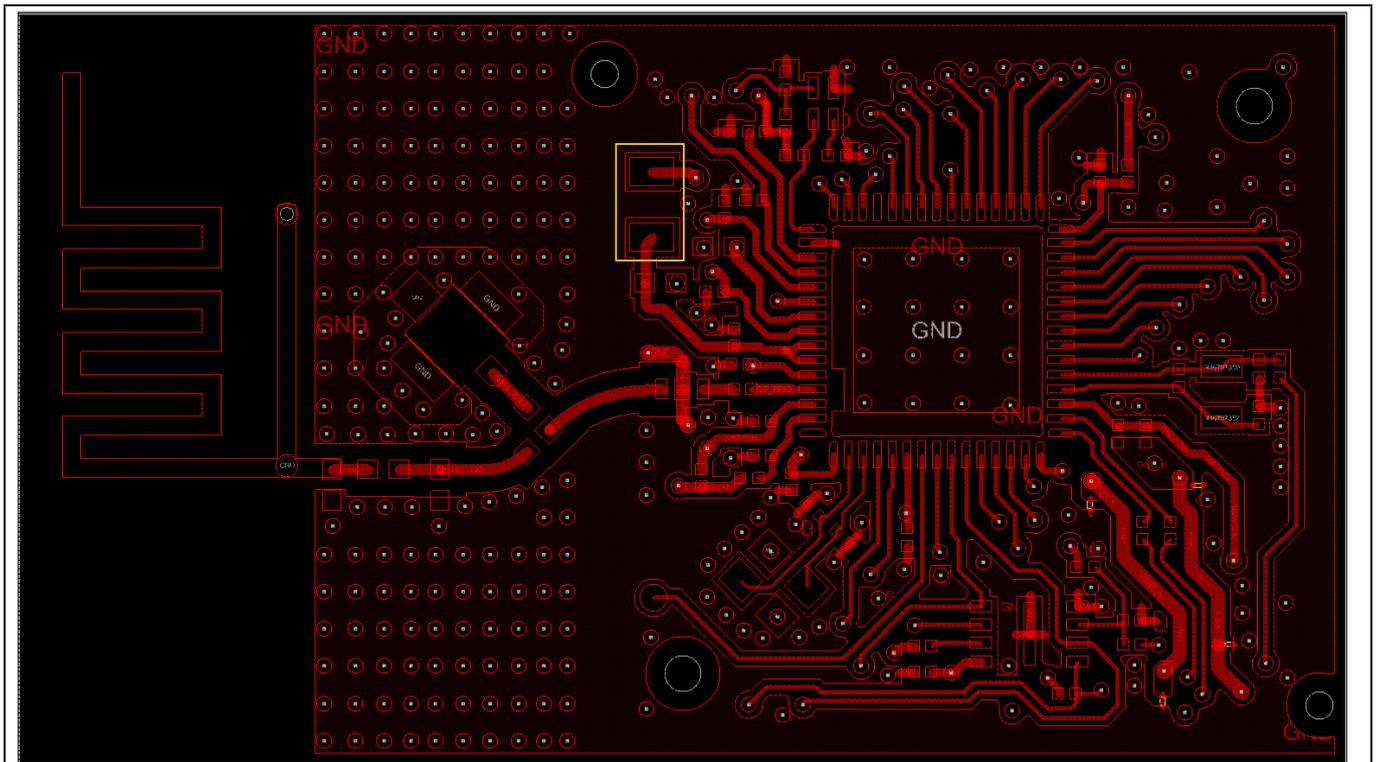


Figure 6 Power inductor routing

### 2.13 Layer 4

Use Layer 4 for all non-critical signal routing.

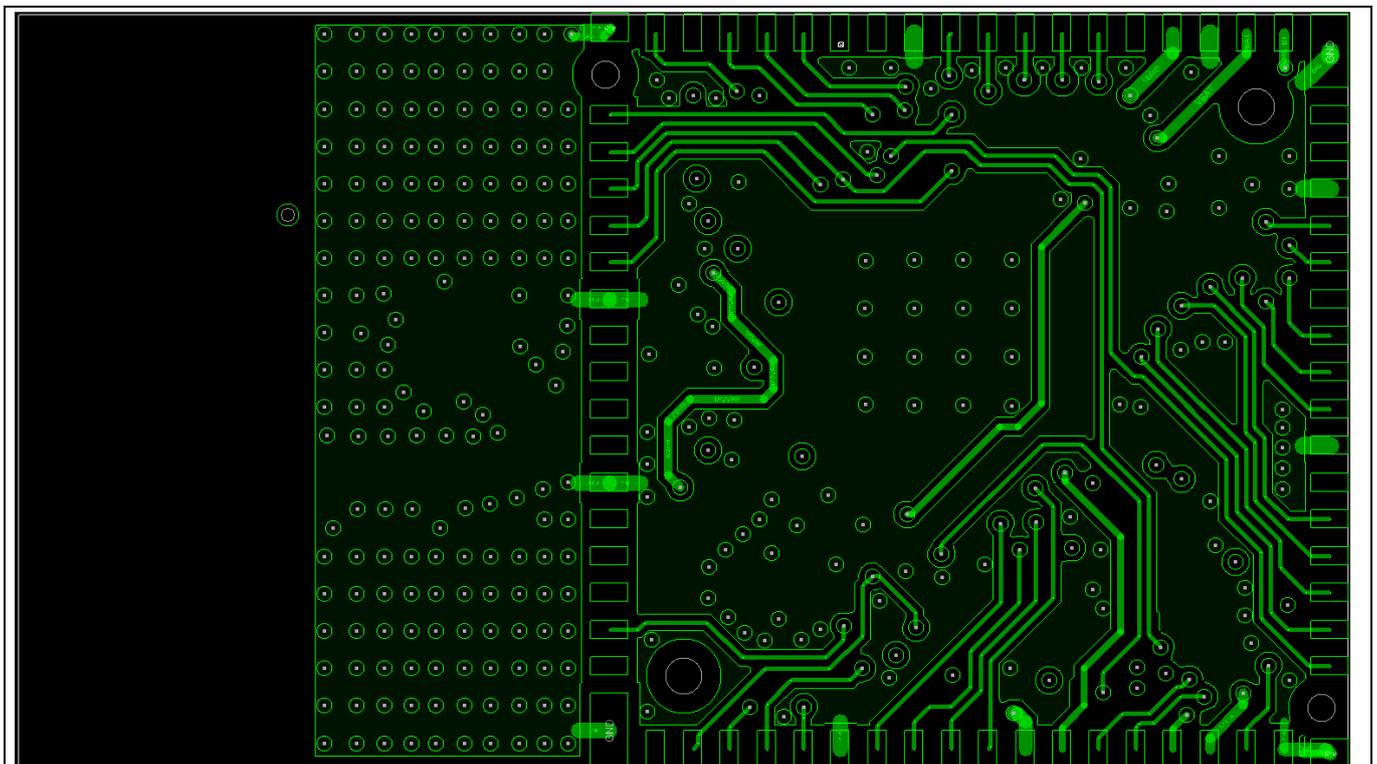


Figure 7 Layer 4

### 2.14 Assembly instructions

CYW20835 is an Infineon standard QFN (quad flat no-lead) package. For additional assembly instructions and reflow profiles, see [AN72845 - Design guidelines for quad flat no-lead \(QFN\) packaged devices](#).

### Revision history

#### Major changes since the last revision

Date	Version	Description
2021-10-05	**	Initial release.

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