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Heavy Ion, Single Event Effects (SEE) Final Report for Cypress Semiconductor CYRS16B256 Serial NOR Flash 256-Mbit

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Prepared By: _____ 27 Oct 2020
JD Instruments Date

1.0 Test Overview

Heavy ion radiation testing was performed on Oct 26-27, 2020 at the Texas A&M Cyclotron facility (TAMU).

Previous SEE/SEL testing on commercial versions of these parts (S25FL256L) established static upset curves and some latchup regimes.

Tests during this campaign were to compare static upset behavior between these parts and previous testing, further refine latchup safe operating conditions and test for upsets during dynamic (ERASE/WRITE) operations.

These parts are 256Mb NOR Flash Floating Gate devices packaged in 36 pin, ceramic flat-packs.

Single Event Upset testing was conducted at minimum supply voltage (V_{DD_Min} = 2.7V) and room temperature whereas Single Event Upset Testing was conducted at the maximum supply voltage (V_{DD_Max} = 3.6V) and elevated temperature.

These Rad Tolerant parts use slightly different ERASE/WRITE parameters than the commercial equivalents. This resulted in noticeably lower static bit upset cross sections.

No latchup occurred when parts were exposed at 85^0C to 10^7 ions/cm2 with ions having an LET of 42.3 MeVcm^2/mg. Parts did not experience latchup up to 8e6 ions/cm2 at 85^0C to ions with an LET of 60 MeVcm^2/mg. However, the erase capability was damaged by exposure to these high fluences.

2.0 Test Procedure

Four types of tests were performed on these parts:

1) Memory was loaded with a pattern, the part irradiated to some fluence, and the pattern read out of the part to see how many bits had been upset.
2) For some radiations a "Vt profile" test was performed on stored memory. This is a test where the READ discrimination voltage was varied to determine the distribution of charge states across all memory cells. This type of test will reveal changes in charge state distribution due to radiation even when changes are not sufficient to cause a memory bit upset.
3) Memory was loaded with a pattern and continuously READ while being irradiated.
4) Memory was repeatedly ERASED/WRITTEN while being irradiated.
5) Parts were heated to some level and irradiated to a high fluence while Idd was continuously monitored to see if the parts latched.

Figure 1 shows the block diagram for this part. These parts are packaged in 36 pin ceramic flat-packs which are contained in plastic frames for ease in handling. Pictures of the front and back side of these parts in their carriers are shown in figure 2. The DUT was heated by installing a heater strip underneath the carrier. DUT temperature was monitored using an RTD placed

between the heater strip and the bottom of the DUT. Actual DIE temperature was measured using an IR temperature sensor as shown in figure 3.

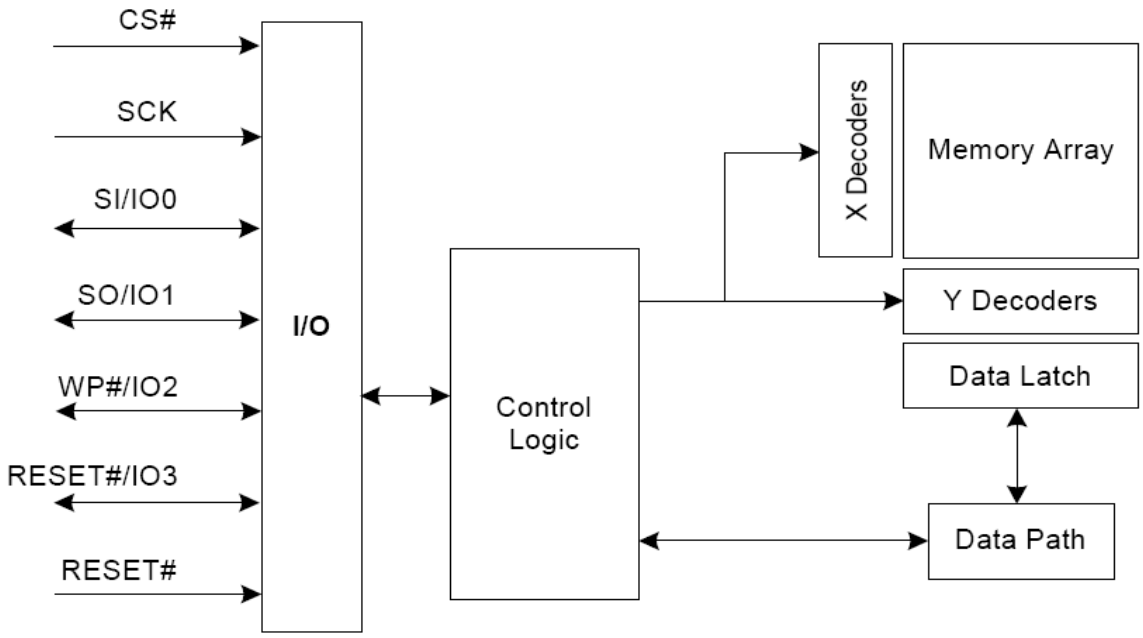

Figure 1. Cypress CYRS16B256, 256Mb SNOR

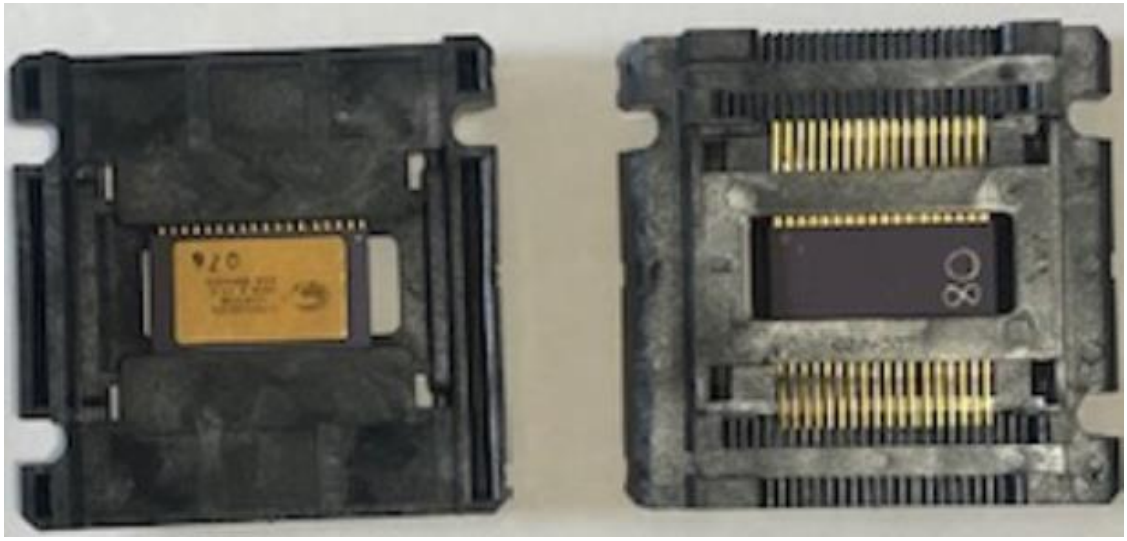

Figure 2. 32 Pin Ceramic Flat-Packs in Plastic Carriers

Figure 3. I.R. Temperature Sensor

2.1 Parts Identification

Parts were provided with serial numbers printed on their metal lid. The serial numbers were also hand written on the underbody of the ceramic package. Serial numbers were entered in the test run log for traceability and reporting.

2.2 Parts Handling and Storage

All parts are considered sensitive to electrostatic discharge (ESD) and were handled accordingly.

2.3 Test Facility

An overview of the TAMU cyclotron facility is shown in figure 4. Devices were mounted to a test board positioned in air in front of the beam exit at the “radiation effects facility” location shown in the figure.

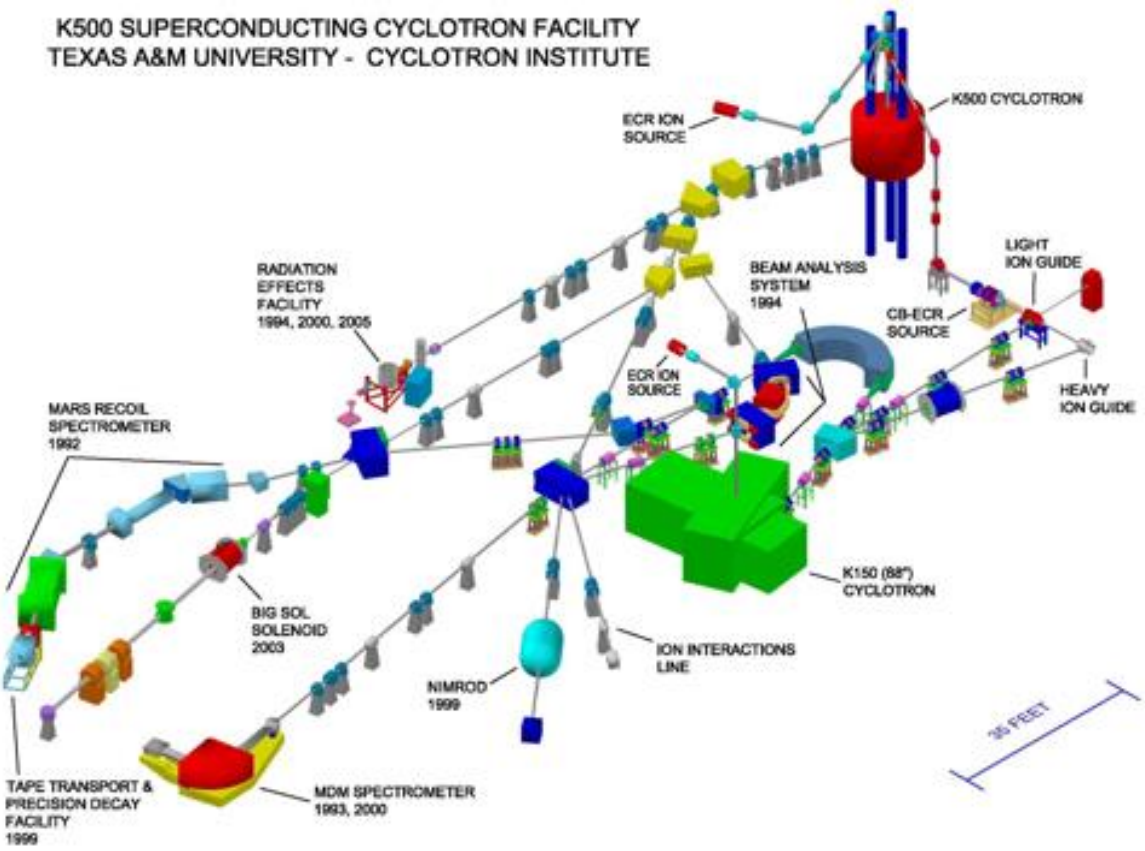

Figure 4. Overview of Texas A&M Cyclotron Facility (TAMU)

All irradiations were performed using the 25MEV tuning of the cyclotron. Figure 5 shows all ions available for this tuning. For this test the following ions were used:

ION	LET ($MeVcm^2/mg$)
^{129}XE	42.3 -> 60
^{84}KR	20 -> 40

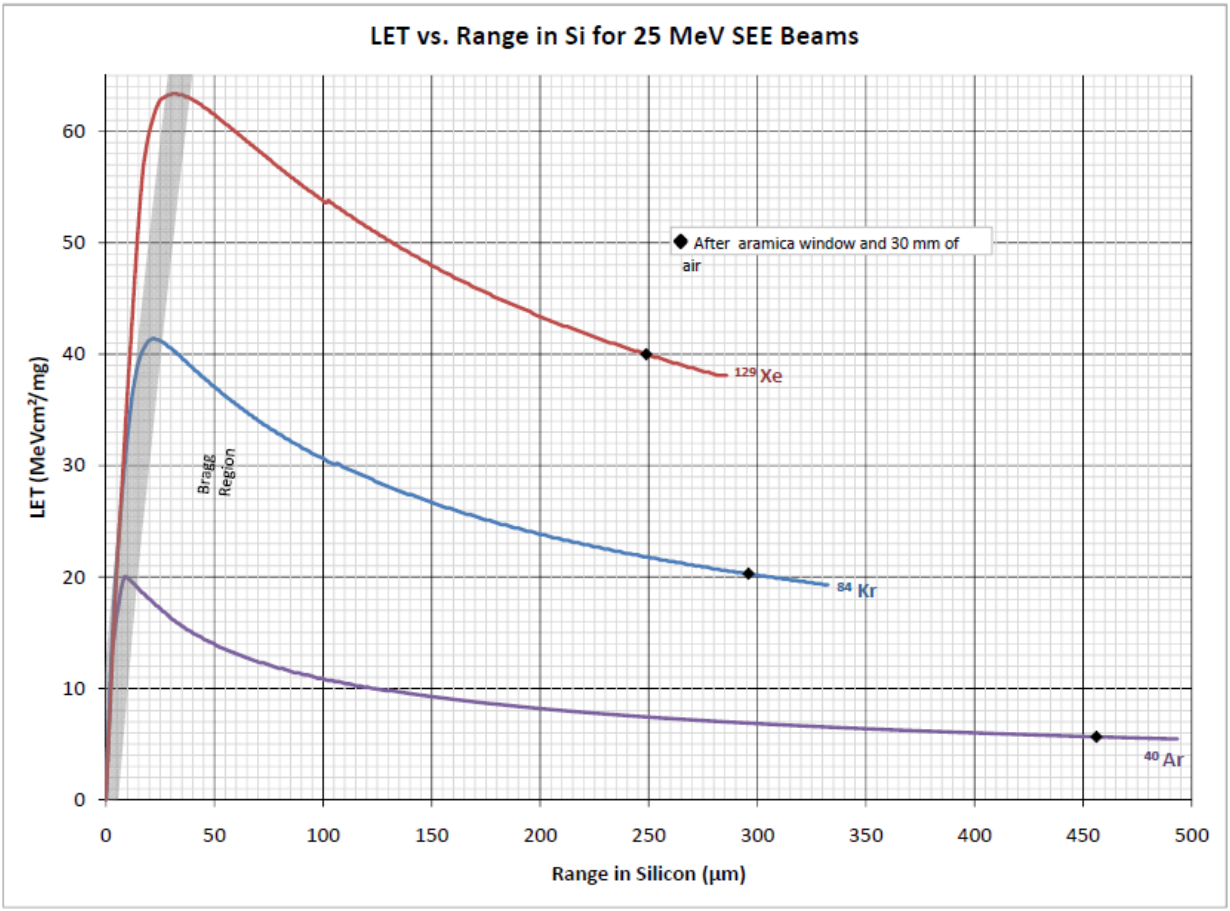

Figure 5. TAMU Ions Available with 25MeV Tuning

2.4 Specific Test Requirements

2.4.1 Test Fixtures

For this testing the metal lid of each device was removed to expose the die. The part was installed in a socket with the die exposed as open top DUT to the heavy ion beam. To achieve device heating a strip heater was mounted between the socket and the bottom side of the plastic carrier. A hole in the bottom side of the plastic carrier was filled with Type 44 Heat Sink Compound to conduct heat from the heater strip to the DUT.

2.4.2 Cabling

Cabling was provided to supply power to the DUT. A USB cable connected to special circuitry on the test board for functional testing of the DUT.

2.4.3 Test Procedure

Testing was performed at various temperatures between 20.2^0C of 85^0C. DUT temperature was measured using an IR thermometer before and after each run with elevated temperature.

2.4.4 Data Collection

Major test information was recorded in a "run log" spreadsheet. The complete run log is shown in attachment A.

Detailed failure results were also collected as ascii text. Figure 6 shows a portion of the detailed failure log for run 5. In this log note that all memory upsets were single bit which could be corrected using EDAC circuitry.

```
Addr = 0x022B5FD, Exp = 0XAA, Read = 0XEA, BitFails = 1
Addr = 0x02505A3, Exp = 0XAA, Read = 0XAE, BitFails = 1
Addr = 0x026FCC1, Exp = 0XAA, Read = 0XEA, BitFails = 1
Addr = 0x0274A3B, Exp = 0XAA, Read = 0XAE, BitFails = 1
Addr = 0x0292AF4, Exp = 0X55, Read = 0XD5, BitFails = 1
Addr = 0x02C13D9, Exp = 0XAA, Read = 0XEA, BitFails = 1
Addr = 0x02E87C7, Exp = 0XAA, Read = 0XAB, BitFails = 1
Addr = 0x02F631D, Exp = 0XAA, Read = 0XAE, BitFails = 1
Addr = 0x030F62C, Exp = 0X55, Read = 0X57, BitFails = 1
Addr = 0x030FF9A, Exp = 0X55, Read = 0X57, BitFails = 1
Addr = 0x033A695, Exp = 0XAA, Read = 0XAB, BitFails = 1
Addr = 0x03B8385, Exp = 0XAA, Read = 0XEA, BitFails = 1
Addr = 0x03D4F67, Exp = 0XAA, Read = 0XBA, BitFails = 1
Addr = 0x03E946F, Exp = 0XAA, Read = 0XBA, BitFails = 1
```

Figure 6. Portion of Detailed Error Log for Run 5, Static Upsets

3.0 Test Results

3.1 SEL

Four tests were performed to evaluate latchup vs. temperature and LET. Figure 7 shows the portion of the run log containing data for these runs. The ion used for all latchup tests was ^{129}XE. The column containing this information was not shown in this figure so other information could be enlarged an read more easily.

RUN#	DUT #	Duration (Sec)	LET	Fluence	# Errs	# Pwr Cycles	Temp	Latch?	DOSE	Comment
1	133	681	42.3	2.60E+06	76	1	>95	Yes	2300	Current "Ratched Up" causing self heating. Latched to 125mA. Held too long, damaged part
8 & 9	113	4572	42.3	1.00E+07	41	0	85	No	3256	Fully Functional
10	"	3748	60	8.50E+06	2217	0	85	Yes	8166	Latch at 8.5e6 ions/cm^2, Problem with socket?
11	130	1706	60	1.00E+07	5147	0	85	No	9607	Current jumped up as high as 100mA & then dropped back to 5mA. Would READ correctly, but NOT ERASE after run. Non Functional!

Figure 7. Latchup Portion of Run Log

Run #1 was performed at an LET of 42.3 MeVcm^2/mg and a starting temperature of 85^{0}C. During the exposure Idd was observed to gradually increase in a step-wise manner.

Unfortunately DUT temperature was not closely monitored over the course of irradiation and was constantly increasing due to self-heating in the part. Eventually the part latched and the power supplies were left on too long, resulting in the part being damaged. When the part latched the DUT temperature was noted to be greater than 95^0C. DUT temperature was rapidly increasing at that point due to self heating from the latch condition.

The next latchup test was performed over runs #8 and #9. Run #8 was accidentally stopped prematurely and the beam was re-started as run #9. Results were tabulated at the conclusion of run #9. These runs used the same conditions as Run #1 (85^0C , LET = 42.3 MeVcm^2/mg) except current to the heat strip was constantly adjusted to keep DUT temperature at of 85^0C. During this exposure the DUT was exposed to 10^7 ions/cm^2 and no latchup was observed. Idd did increase over the course of radiation, but the part was fully functional after completion of the radiation.

Runs #10 and #11 were performed with a die temperature of 85^0C and an LET of 60. MeVcm^2/mg. During run #10 the DUT latched at a fluence of $8.5x10^6$ ions/cm^2. During run #11 the DUT did not latch during an exposure to 10^7 ions/cm^2 , but was not able to perform an ERASE operation after the exposure.

These results show that latchup in these parts is very temperature sensitive. Irradiations with 42.3 MeVcm^2/mg ions at 85^0C did not latch. Irradiations with 60 MeVcm^2/mg ions latched and/or damaged the parts. Based on these results it is recommended that the parts not be used at temperatures above 85^0C or in environments where they might be subjected to ions with LETs above 42.3 MeVcm^2/mg at elevated temperatures.

3.2 Static Upsets

Commercial versions of this part were characterized for upset cross-sections in 2016. Limited upset cross-section testing was performed in this campaign. Figure 8 compares bit upset cross-sections from this testing vs. that measured in 2016.

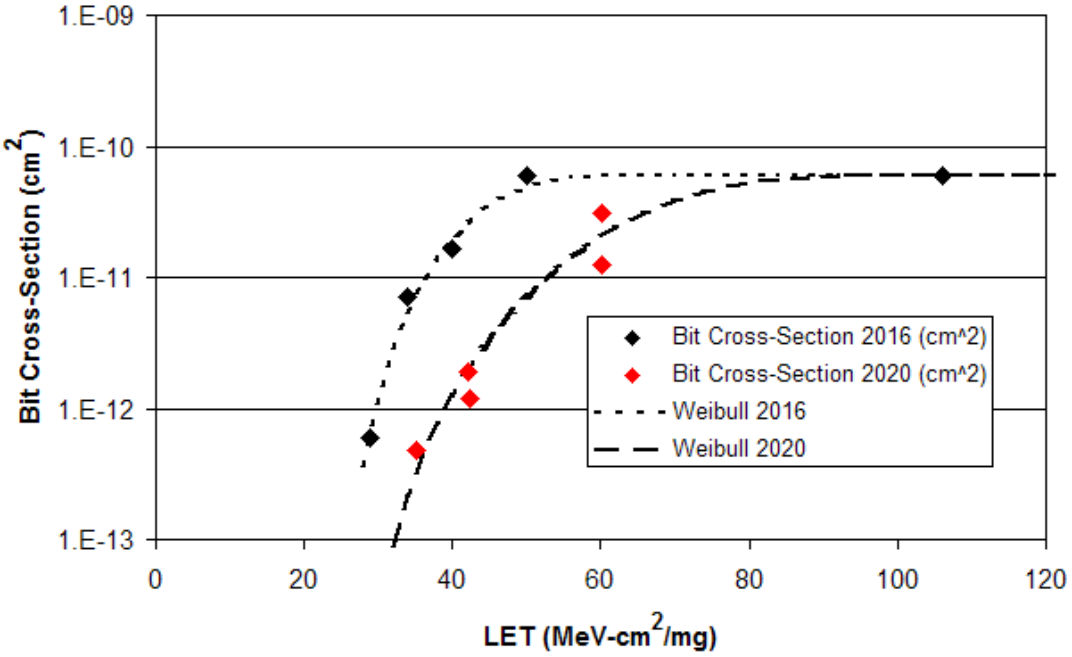

Figure 8. Bit Upset Cross-Section, 2016 vs 2020

This graph clearly shows that bit upset cross-sections in radiation tolerant parts were consistently lower than for the commercial parts. These results were as expected because the radiation tolerant version of the parts use different ERASE/WRITE parameters compared to the standard commercial parts. Figure 9 shows the distribution of threshold voltages (Vt's) over the population of bits tested.

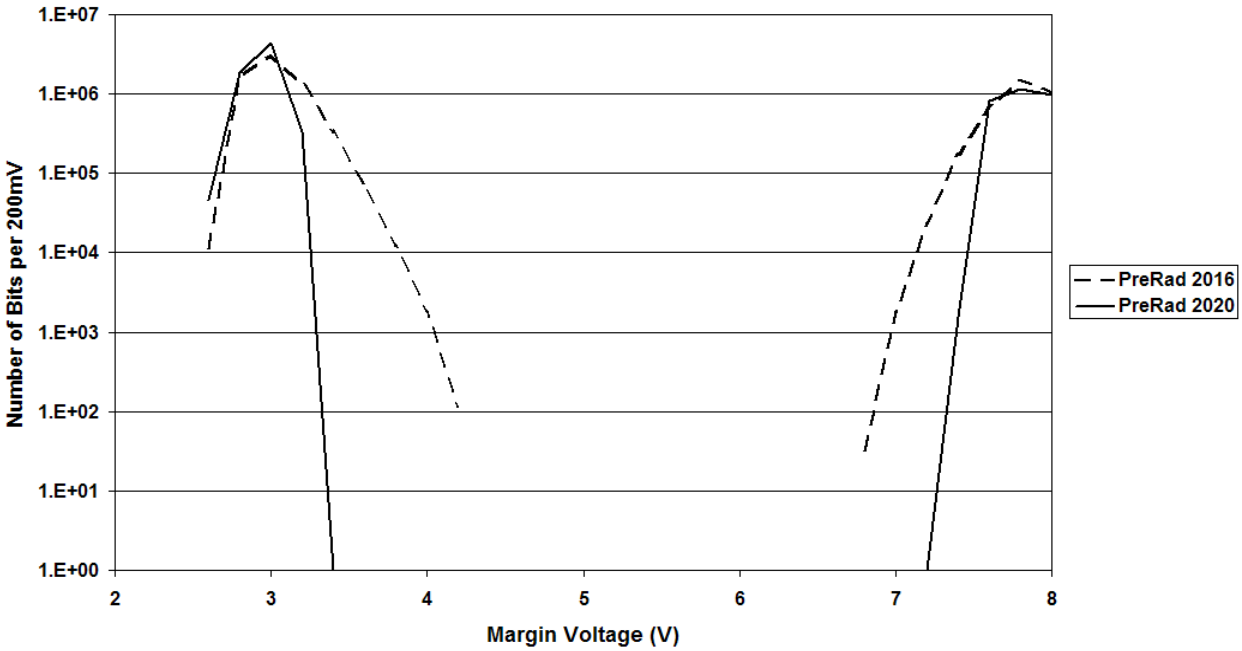

Figure 9. Pre-Radiation Vt Distributions, 2016 vs 2020

In this figure the population of ERASED bits is in the left half of the plot and programmed bits in the right half. Note that the distribution of Vt's is much more tightly grouped in the radiation tolerant version of the parts and that the separation between the lower portions of the ERASED vs PROGRAMMED bits is much further apart. Since the Vt of memory bits struck by heavy ions is shifted towards the center of the graph it is reasonable to expect fewer bits to be shifted sufficiently to change their READ state if the pre-radiation populations are further apart.

Figure 10 shows the Weibull parameters for the curves shown in figure 8.

	2016	2020
Width (MeV-cm^2/mg)	22	45
Saturation (u^2/bit)	6.00E-11	6.00E-11
Onset (MeV-cm^2/mg)	24	25
Pwr	3	3.5

Figure 10. Weibull Parameters, 2016 vs 2020

Using these parameters, figure 11 shows CREME96 calculations for bit upsets per device per day for "Space Station Solar Minimum" and "Geo-Synchronous Solar Minimum" conditions using. Note that upset rates for both orbits improved by approximately 1 order of magnitude for both orbits using the 2020 Weibull parameters.

	2016	2020
Space Station Solar Min	1.38E-09	1.47E-10
Geo-Synchronous Solar Min	2.80E-08	2.45E-09

Figure 11. Upsets/Dev/Day,
Space Station Solar Min and Geo-Synchronous Solar Min

3.3 Continuous Read

Continuous READ tests were performed on 2 DUTs over a range of LETs from 35 to 60 MeVcm^2/mg. Figure 12 shows the portion of the run log containing data for these runs.

RUN	DUT #	Duration (Sec)	Test Type	Ion	LET	Fluence	Flux	# Errs	# SEFIs	DOSE	Comment
4	113	717	Continuous Read	Xe	42.3	1.00E+05	139	1	1	67	Read Continuous works FINE at this flux, ERASE Function failed after exposure, recovered after power cycle
5	113	616	Continuous Read	Xe	60	6.77E+04	110	14	2	65	20,444 errors after 6.77e4 ions, 16 True upsets, SEFI. ERASE non-functional, Fully functional after power cycle
16	105	82	Continuous Read	Kr	35	2.22E+05	2688	2	0	124	Burst read error. Cleared on re-read. Flux too high?
17	105	358	Continuous Read	Kr	35	1.00E+05	279	0	0	56	No Errs, fully functional. Erases fine

Figure 12. Continuous READ Portion of Run Log

During 2 irradiations with LETs of 35 MeVcm^2/mg the parts remained fully functional although there was one occurrence of a "Burst Read" error. Memory in these parts is read by issuing a "Page Read" command and then receiving a return of 512 bytes of data. During the burst read

error all addresses were returned as containing 0x00 instead of the actual values. On a successive READ operation the correct data was returned.

During the 60 MeVcm^2/mg irradiation the part was operating fine until it suddenly began returning burst read errors. Figure 13 shows the error patterns that were returned once this SEFI occurred. Note that the last 2 positions in the address were a repeating pattern of 74, AA, FD and that the data patterns read also followed a repeating cycle of 3 entries. This probably indicates some error in decode logic. This SEFI persisted until power was cycled at which point the part could again be read properly.

```
Addr = 0x0200074, Exp = 0X55, Read = 0X75, BitFails = 1
Addr = 0x02000AA, Exp = 0X55, Read = 0X5D, BitFails = 1
Addr = 0x02000FD, Exp = 0XAA, Read = 0XEA, BitFails = 1
Addr = 0x0200174, Exp = 0X55, Read = 0X75, BitFails = 1
Addr = 0x02001AA, Exp = 0X55, Read = 0X5D, BitFails = 1
Addr = 0x02001FD, Exp = 0XAA, Read = 0XEA, BitFails = 1
Addr = 0x0200274, Exp = 0X55, Read = 0X75, BitFails = 1
Addr = 0x02002AA, Exp = 0X55, Read = 0X5D, BitFails = 1
Addr = 0x02002FD, Exp = 0XAA, Read = 0XEA, BitFails = 1
          "
          "
          "
Addr = 0x0217674, Exp = 0X55, Read = 0X75, BitFails = 1
Addr = 0x02176AA, Exp = 0X55, Read = 0X5D, BitFails = 1
Addr = 0x02176FD, Exp = 0XAA, Read = 0XEA, BitFails = 1
```

Figure 13. SEFI, Continuous Burst Read Errors

After irradiations at both 42.3 and 60 MeVcm^2/mg the ERASE function failed. After power cycling the ERASE function was again operating properly. These were both considered to be SEFIs. Thus, when irradiated with ions having LETs of 60 MeVcm^2/mg the DUT actually had 2 types of SEFIs, both of which were cleared by power cycling.

The "Stuck" Burst READ condition only occurred once at a fluence of 6.77x10^4 ions/ cm^2 and an LET of 60 MeVcm^2/mg. This single data point would indicate this SEFI has a device cross-section around 1.477x10-5 cm^2.

Discussion of SEFIs where ERASE functionality stopped working will be included in the following section which analyzes continuous ERASE/WRITE operations.

3.4 Continuous Erase/Write

Continuous ERASE/WRITE tests were performed on 2 DUTs over a range of LETs from 35 to 60 MeVcm^2/mg. Figure 14 shows the portion of the run log containing data for these runs.

RUN	DUT #	Duration (Sec)	Test Type	Ion	LET	Fluence	Flux	# SEFIs	DOSE	Comment
6	113	330	Cont. ERASE/WRITE	Xe	60	3.60E+04	110	1	34	Erase started taking 20 seconds/page ! SEFI. Fully functional after power cycle.
7	113	689	Cont. ERASE/WRITE	Xe	42.3	1.00E+05	145	1	67	Erase functional but doubld in time at 9e3 ions/cm^2. NO ERASE SEFI
18	105	105	Cont. ERASE/WRITE	Kr	35	2.30E+04	218	1	12.8	ERASE SEFI, Erases changed to 20 sec timeout. Cleared after power cycle. Fully functional
19	105	1384	Cont. ERASE/WRITE	Kr	35	4.00E+05	288	1	224	Erase time changed from ~1 sec to ~0.6 sec. Some bits could not be erased. Cleared with power cycle

Figure 14. ERASE/WRITE Portion of Run Log

In each of these 4 runs the ERASE time per sector changed. Sector erases are performed by sending an ERASE command to the DUT and then repeatedly polling the part to see when the operation is complete. Normally this ERASE time is slightly more than 1 second per sector.

Two types of SEFI errors were detected during this testing. Both types could be cleared by cycling power.

The first type of SEFI was that the DUT stopped performing ERASE functions. When this occurred the test program began reporting a 20 second timeout after every ERASE command. This SEFI occurred both for ^{129}XE ions at an LET of 60 MeVcm^2/mg and ^{84}KR ions at an LET of 35 MeVcm^2/mg. This type of SEFI was also observed during continuous READ testing when devices were ERASED/WRITTEN at the conclusion of each irradiation. Figure 15 shows device cross-sections for this type of SEFI using data from both types of tests.

Test Type		LET	FLUENCE	Device X-Section
READ	ERASE/WRITE	(MeVcm^2/mg)	(ions/cm^2)	(cm^2)
X		60	6.77E+04	1.48E-05
	X	60	3.60E+04	2.78E-05
X		42.3	1.00E+05	1.00E-05
	X	35	2.30E+04	4.35E-05

Figure 15. Loss of ERASE Functionality SEFI

Figure 15 does not show any clear variation in device cross-section vs. LET. The most that can be said is that the device cross-section for this type of SEFI is below ~1.0x10^{-5} cm^2.

The second type of SEFI was a sudden change in the time reported for the ERASE operation. In one case the time doubled to 2 seconds and in the second case it reduced to 0.6 seconds. This SEFI occurred both for ^{129}XE ions at an LET of 42.3 MeVcm^2/mg and ^{84}KR ions at an LET of 35 MeVcm^2/mg. Figure 16 shows device cross-sections calculated for both of these runs. In this case there was a significant difference in cross-section between the 2 LETs indicating there may be an onset slightly below 35 MeVcm^2/mg. More testing would be required to validate this.

LET ($MeVcm^2/mg$)	FLUENCE ($ions/cm^2$)	Device X-Section (cm^2)
42.3	9.00E+03	1.11E-04
35	4.00E+05	2.50E-06

Figure 16. Change in ERASE Time SEFI

Both types of SEFIs were interpreted as upsets in digital logic. The first type could be an upset in state machine circuitry causing the part to get "stuck". The second type was most likely an upset in a latch containing timing information for the ERASE operation. Both types of SEFIs were restored after a power cycle.

3.5 Changes in Vt Distributions With Heavy Ion Radiation

A large portion of memory was written once and then not ERASED/WRITTEN again. Figure 17 shows Vt distribution in this portion of memory for DUT SN105 after the conclusion of all irradiations. Note that this consisted of ~$3x10^6$ $ions/cm^2$ having a range of LETs between 20 and 42 $MeVcm^2/mg$.

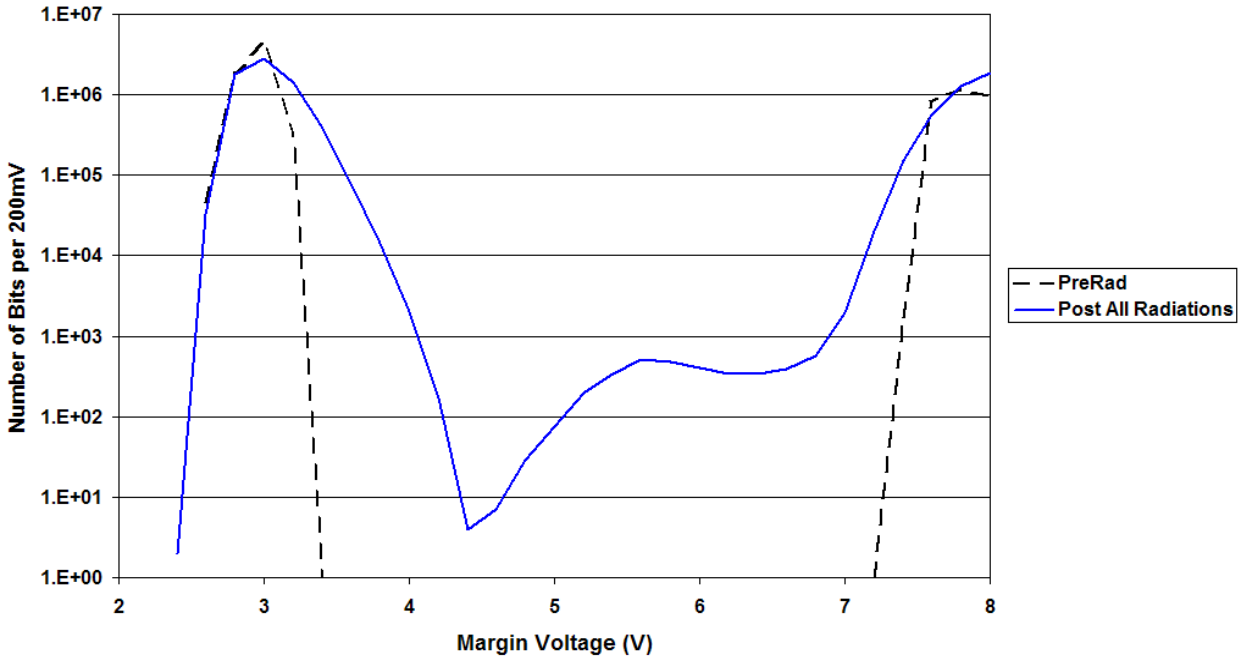

Figure 17. Vt Distribution in SN105 after all Irradiations

No exact conclusions can be drawn from this plot but it is obvious that the distribution of ERASED and PROGRAMMED bits spread out. Also, the "bump" in the distribution just "to the left" of programmed bits is the result of heavy ion strikes on memory cells.

Vt distribution in the portion of the memory that was used for dynamic ERASE/WRITE testing was significantly different. Figure 18 shows the Vt distribution in this portion of memory for SN105. Note that the distribution of programmed bits was restored to pre-radiation values whereas the distribution of erased bis became much more widely spread. It is suspected that the ERASE operation in these parts is not applied to memory cells that read as erased. Thus, cells

with Vt's below some value will never be erased. The only way to reset the original distribution would be to first program all memory bits and then erase them.

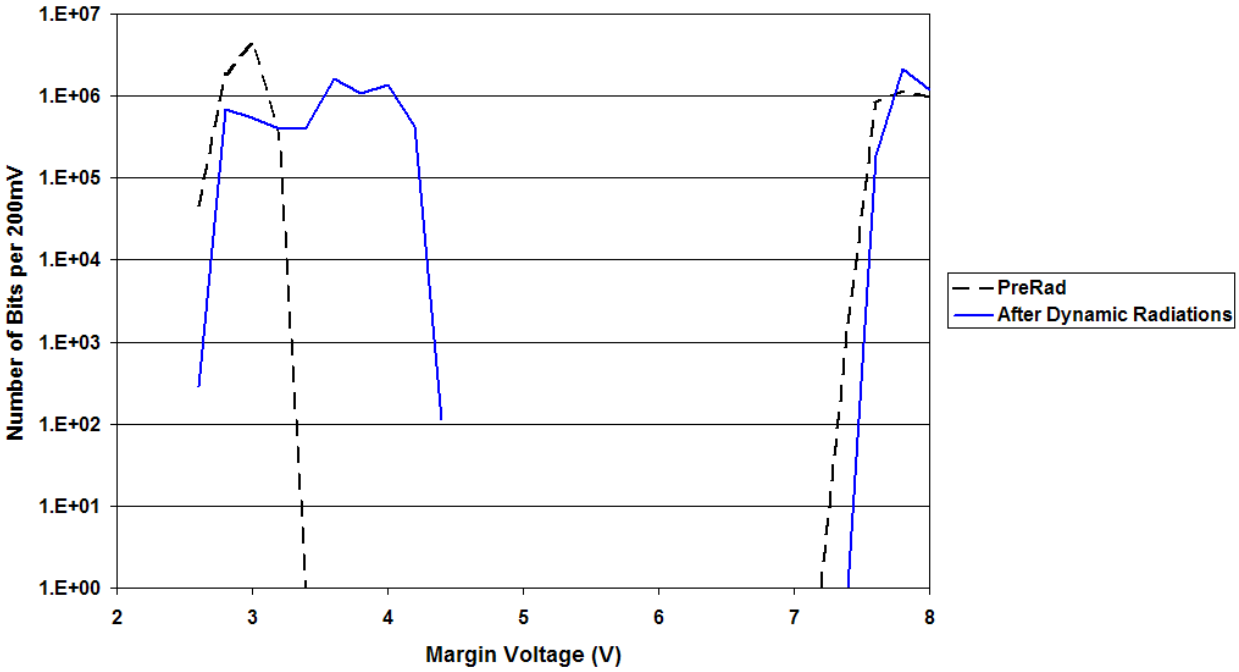

Figure 18. Vt Distribution in SN105 after all Dynamic Radiations

4.0 Conclusions

The 256M NOR Flash appear to be latchup immune up to a temperature of 85^0C when irradiated with 10^7 ions/cm^2 with ions having an LET of 42.3 MeV-cm^2/mg and to $8*10^6$ with ions having an LET of 60 MeV-cm^2/mg, respectively.

Memory cells are very resistant to heavy ion radiation up to an LET of 28 MeVcm^2/mg and did not show any bit upset. At higher LET values the bit upset cross-section was always <1e-10 err/cm^2 which is sufficiently low so as to not be of any concern.

All observed memory upsets were single bit errors, which can be easily corrected by System Hamming codes.

Attachment A. Run Log

RUN	DUT #	Duration (Sec)	Test Type	Ion	LET	Fluence	Flux	# Errs	# SERs	#Pwr Cycles	Temp	Latch?	DOSE	Comment
1	133	681	Latchup	Xe	423	2.60E+06	5000	76		1	85	Yes	2300	Latched to 125mA. Held to long, damaged part
2	113	88	Static Upset	Xe	423	2.00E+05	2100	4			22		128	
4	"	717	Continuous Read Upset	Xe	423	1.00E+05	139	1	1	0	22	No	67	Read Continuous works FINE at this flux. ERASE Function failed after exposure, recovered after power cycle
5	"	616	Continuous Read Upset	Xe	60	6.77E+04	110	14	2	1	22	No	65	20,444 errors after 6.77e4 ions, 16 True upsets, SEFI. ERASE non-functional. Fully functional after power cycle
6	"	330	Continuous ERASE	Xe	60	3.60E+04	110	---	1	1	22	No	34	Erase started taking 20 seconds/page! "SEFI. Fully functional after power cycle.
7	"	689	Continuous ERASE	Xe	423	1.00E+05	145	---	1	0	22	No	67	Erase functional but doubld in time at 9e3 ions/cm^2. NO ERASE SEFI
8	"	1958	Latchup	Xe	423	4.80E+06	2457		1		85		3256	
9	"	2514	Latchup	Xe	423	5.00E+06	1913	41			85		3385	Continuation of run 8. NO LATCH to 1e7, 41 errs at 1E7. Fully functional
10	"	3748	Latchup	Xe	60	8.50E+06	2270	2217			85	Yes		Problem with socket
11	130	1706	Latchup	Xe	60	1.00E+07	5858	5147		0	85	No	9607	Current jumped up as high as 100mA & then dropped back to 5mA. Would NOT ERASE after run. Non Functional!
12	105	205	Static Upset	Kr	20	9.87E+04	479	0			22		31	Fully Functional
13	"	230	Static Upset	Kr	28	1.00E+05	434	0			22		44	Fully Functional
14	"	640	Static Upset	Kr	28	3.00E+05	705	0			22		134	Continuation of run 13. No errs at 4e5 ions/cm^2
15	"	181	Static Upset	Kr	35	5.00E+05	2753	4	1		22		280	Erase SEFI, had to cycle power to enable erase. Fully functional after pwr cycle
16	"	82	Continuous Read Upset	Kr	35	2.22E+05	2688	2			22		124	Burst read error. Cleared on re-read. Flux too high?
17	"	358	Continuous Read Upset	Kr	35	1.00E+05	279	0			22		56	No Errs, fully functional. Erases fine
18	"	105	Continuous ERASE	Kr	35	2.30E+04	218		1		22		12.8	ERASE SEFI, Erases changed to 20 sec timeout. Cleared after power cycle. Fully functional
19	"	1384	Continuous ERASE	Kr	35	4.00E+05	288		1		22		224	Erase time changed from ~1 sec to ~0.6 sec. Some bits could not be erased. Cleared with power cycle
20	"	215	Static Upset	Kr	40	3.00E+05	1387	63			22		191	Erase SEFI, after static upset run. Timed out. Worked after pwr cycle.
20A	"		Static Upset VT Profile Area	Mix	20-40	2.04E+06		22						Performed normal READ over sectors 4-29
21	"	907	Static Upset VT Profile Area	Kr	42	1.00E+06	1102	32			22		676	Incremental errs due to LET=42