AN INFINEON TECHNOLOGIES COMPANY

2020 Q4 Quarterly Reliability Report

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1. Introduction

Cypress's Reliability Monitor Program (RMP) is used to measure the reliability of all process technologies on a regular basis. This is an extensive effort that is aimed at providing generic fab process coverage for all fab process technologies.

The Reliability Monitor Program has two purposes:

1. Improved Reliability Performance

   Each reject is analyzed to its root cause in order to drive continuous improvement through the implementation of corrective actions.

2. Generation of Reliability Data

   RMP test results are used to assess the benefits of burn-in, provide estimates of typical lifetimes, model field applications, and determine suitability of plastic packaging in various temperature and humidity environments.

A number of process technology groupings are established for the purpose of reliability assessment. These groupings result in larger sample sizes so that the reliability analysis is statistically significant. Process similarity guidelines are used to define these process groupings.

Cypress Semiconductor has established aggressive reliability objectives. The quality standard at Cypress is zero defects, driven by a culture requiring continuous improvement in quality and reliability.

Product reliability is assured by a total quality management system. The quality management system is described in detail in Cypress Semiconductor Quality Manual. Key reliability related programs of the total quality management system are: (1) design rule review and approval; (2) control of raw materials and vendor quality; (3) manufacturing statistical process controls; (4) “Maverick Lot” yield limits; (5) formal training and certification of manufacturing personnel; (6) qualification of new products and manufacturing processes; (7) continuous reliability monitoring; (8) formal failure analysis and corrective action; and (9) competitive benchmarking.

Product Reliability data is accumulated as a result of new product qualification test plan activities as well as from the reliability monitor program. All reliability test samples are obtained from standard production material. Sample selection is based on generic product families. These generic products are designed with very similar design rules and manufactured from a core set of processes. Sampling of device is not limited to in-house Cypress facilities but also includes certified external subcontractor foundries.

Reliability strategy requires that every failure that occurs during reliability testing be subjected to failure analysis to determine the failure mechanism. Corrective action is then implemented to prevent future failures, resulting in continuous improvement in product reliability.

Sabbas Daniel

Executive Vice-President, Quality

2. Reliability Tests and Test Conditions

The results of the RMP testing for the past six quarters are summarized in this document. The stress tests employed and the typical test conditions used are shown in the Table 2.1.

Table 2.1 Reliability Monitor Stress Conditions

Stress	Ambient Condition	Typical Read Point
Early Life	150°C, 125°C, 105°C	48, 96 hours
Inherent Life	150°C, 125°C, 105°C	408, 500, 1000 hours
Data Retention	150°C, 125°C	1000 hours
HAST	110°C, 85% RH 130°C, 85% RH	264 hours 96 hours
Temperature Cycle	-40°C to 150°C (Condition M) -55°C to 125°C (Condition B) -65°C to 150°C (Condition C)	1000 cycles 1000 cycles 500 cycles
Unbiased HAST	110°C, 85% RH, no bias 130°C, 85% RH, no bias	264 hours 96 hours
Pressure Cooker Test	121°C, 15 PSIG, no bias	96, 168 hours
High Temperature Storage	150°C, 125°C	1000 hours

Package level reliability testing refers to the assessment of the overall reliability of the device in packaged form. This consists of subjecting packaged samples to reliability tests that exposed the sample sets to different stress conditions, after which the samples are tested for any degradation.

At Cypress, plastic surface mount devices are pre-conditioned prior to undergoing Temperature Cycling, Pressure Cooker Test/Unbiased HAST, and HAST. Pre-conditioning per JEDEC Standard JESD22-A113 is required in order to simulate the stresses to which the packaged parts are subjected to during shipping, storage, board assembly and cleaning operations. Package reliability tests are performed as part of the qualification processes and as part of the standard reliability monitor program. The reliability test employed is chosen based on the failure mechanism, as different stress tests accelerate different failure mechanisms. These reliability tests utilize one or more of the following stress factors such as: temperature, moisture or humidity, voltage and pressure, to accelerate failure. Figure 2.1 shows Cypress package reliability stress flow. Packages are soaked and reflowed based on their shipping moisture sensitivity classification. The samples are tested (acoustic and electrical) after preconditioning, failures from which are considered as preconditioning failures and not reliability failures. Preconditioning failures should be taken seriously, since these imply that the samples are not robust enough to withstand the board mounting process.

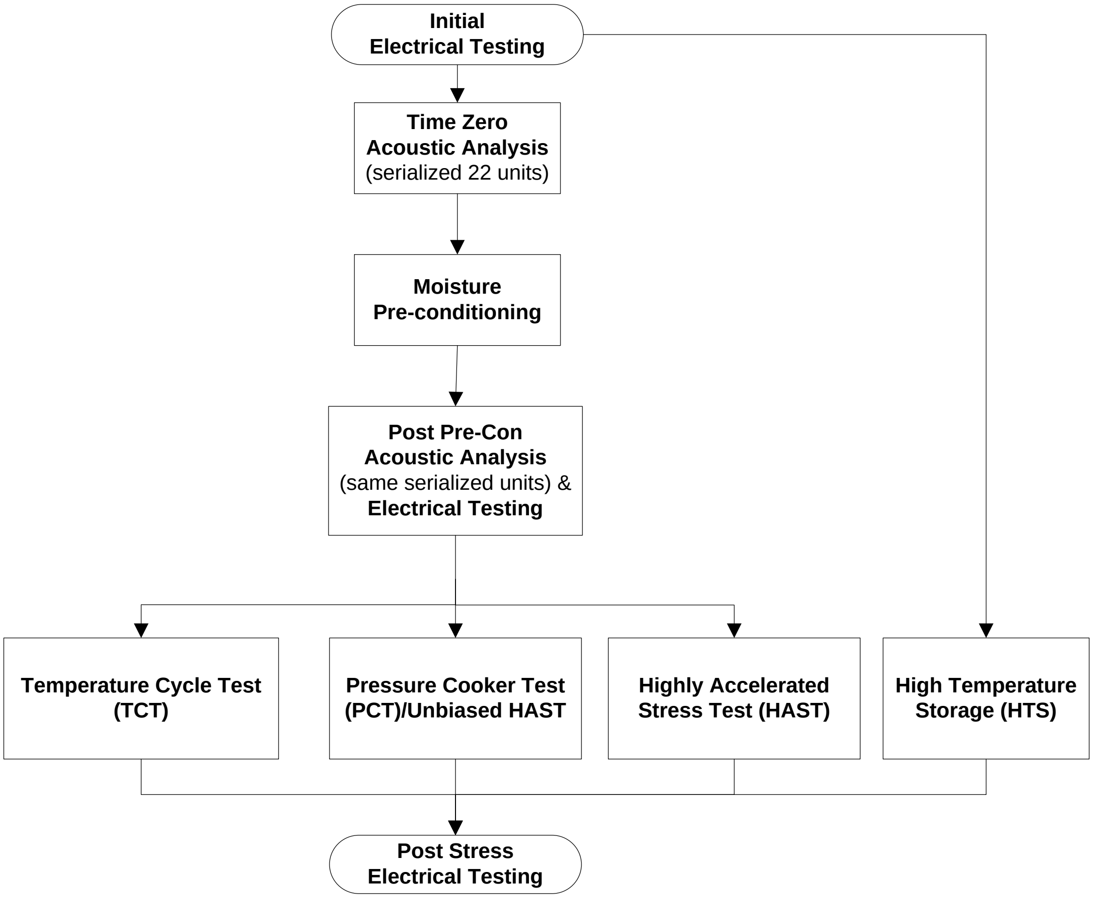


Figure 2.1 Cypress Package Reliability Stress Flow

3. Reliability Data/Analysis

The reliability data generated from the Reliability Monitor Program is presented in this section along with a detailed description of the modeling procedure used for estimating reliability under field conditions.
Also included is a summary of environmental stress results for each process technology grouping by package types.

3.1 The Exponential Distribution

The exponential distribution is simple to use, well understood and as valid as any for life tests with large sample sizes and few failures. No actual distribution can be implied as there is seldom enough data to determine one. The exponential distribution, characterized by a constant failure rate, is a special case of the Weibull. The average failure rate is the same as the instantaneous failure rate for the exponential distribution because the failure rate is constant.

The exponential distribution is the only one for which a MTTF (mean time to failure) value may easily be estimated and it is simply the reciprocal of the failure rate (λ). In addition, it is the only one for which a confidence level may be readily assigned to the failure rate calculation.

The conventional expression for the failure rate, λ, is

$$\lambda = \chi^2(2n + 2, 1 - \alpha)*10^9/(2*SS*t*AF)$$

where λ is the failure rate in FITs (failures per billion unit-hours), $\chi^2(2n+2,1-\alpha)/2$ is the upper confidence value for "**n**" failures and upper confidence limit, (expressed as a decimal value), **SS** is the sample size, t is the test duration in hours, and **AF** is the acceleration factor relating the life test junction temperature to a assumed field junction temperature.

The χ^2(chi square) value for 2n+2 degrees of freedom and the probability, 1-α, can be obtained from a table or calculated using Microsoft® Excel chi squared inverse function [=CHIINV(1-α,2n+2)].

The best way to understand the concept of confidence levels is to consider this example. Assume that a life test on a 100-part sample from a certain product population had one failure and a 60% confidence level was desired. The chi square value corresponding to one failure at 60% confidence is 2.02. This means that one has a 60% confidence that the "true" value of the population's defect rate is between zero (or some very small value) and 2.02%.

3.2 Failure Distributions

The lognormal and Weibull CDF's are the distributions most often used to represent reliability failure mechanisms. The exponential distribution, characterized by a constant failure rate, is a special case of the Weibull. The lognormal distribution is specified by two parameters: T_{50}, the median time to failure, and sigma, the shape parameter. Similarly, the Weibull distribution, which can be written in closed form as

$$F(t) = 1 - \exp[-(t/c)^m],$$

is characterized by a characteristic life c and a shape parameter m. The value of the shape parameter determines whether the failure rate is increasing (m>1), decreasing (m<1), or constant (m=1). The exponential distribution, is specified completely by the one parameter c which is called the mean time to failure (MTTF). Figures 1 and 2 show failure rates for several values of the scale parameters of the lognormal and Weibull distributions, respectively.

$$F(t) = 1 - \exp[-(t/c)],$$

Figure 1. Lognormal Distribution

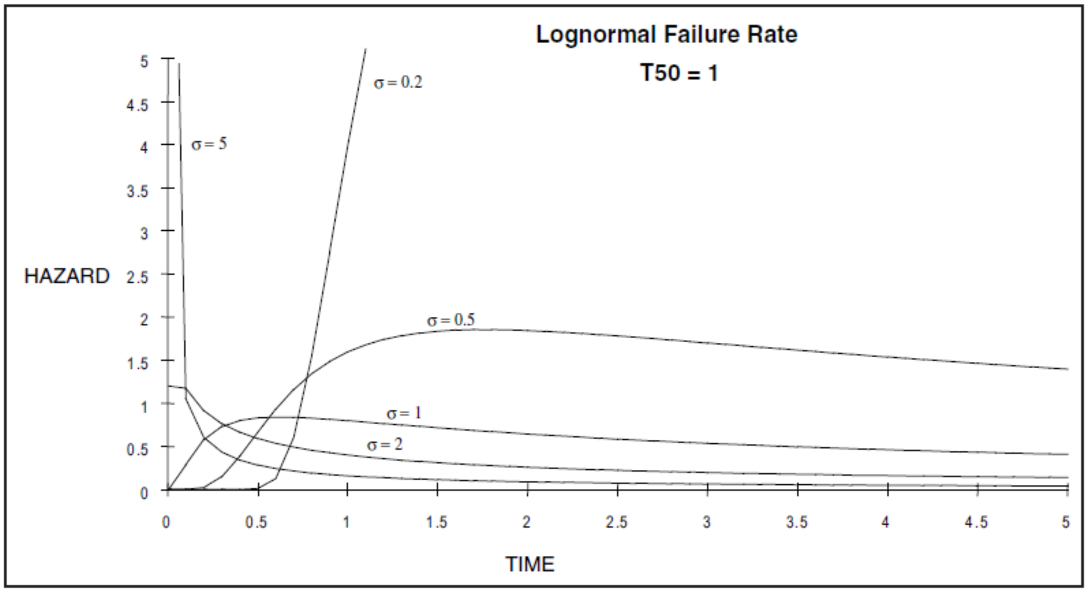
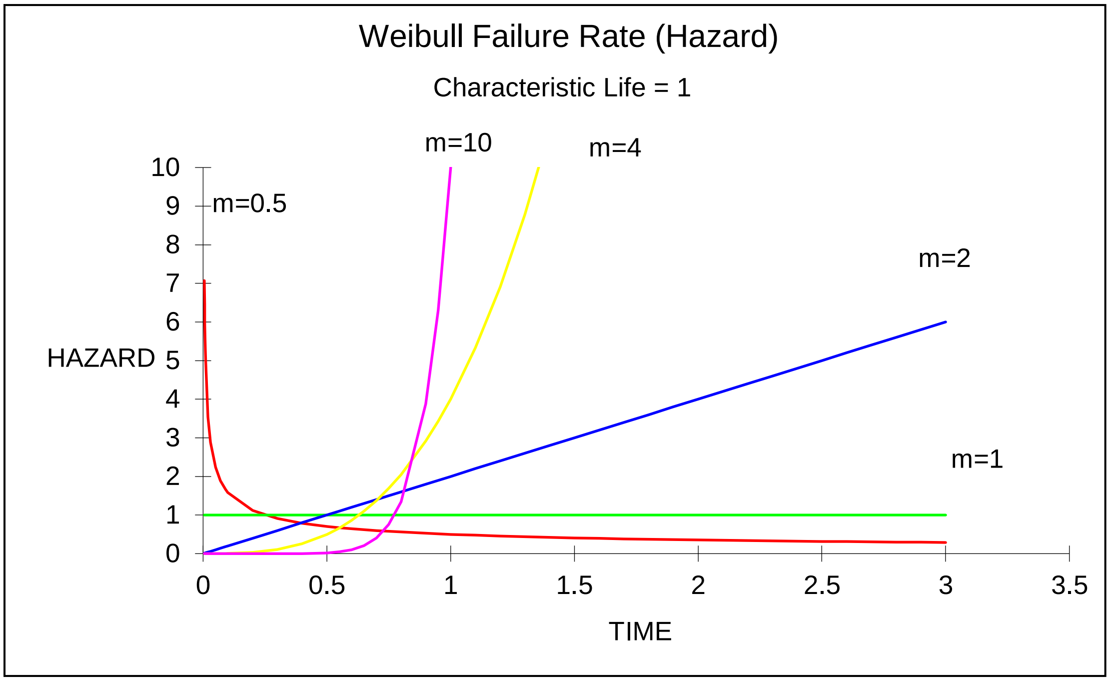


Figure 2. Weibull Distribution



3.3 Calculations of Failure Rates

To estimate field failure rates from reliability studies, many factors must be considered. One primary requirement is the identification of individual failure mechanisms in order to ascribe the failures to the proper categories used in the Cypress reliability model.

3.3.1 Considerations and Assumptions

1. Defective subpopulations and Early Life failures:

   In any production lot, a defective subpopulation may exist. These are devices that fail by a mechanism that is not common to the general population and is usually the result of some processing error or defect. These failures usually occur early and consequently called Early Life failures. Early life reliability is reported in terms of ppm defective expected during the first year of use under typical use conditions. No upper confidence bound will be used for this estimate. The ppm defective is the ration of the number of rejects to the number of samples and expressed in ppm.

   PPM = (Total Reject / Total samples) * 1,000,000

2. Inherent Life failures:

   Failures that occur in later life reliability are usually caused by mechanisms related to defects that could occur in any product of this type. These are known here as Inherent Life failures. Inherent life reliability is reported in using the exponential model, in terms of FITs (failures per billion unit-hours) with a 60% upper confidence bound for zero failure.

3. Estimation of thermal acceleration factors:

   The best-known activation energies for each mechanism are used in calculating the thermal acceleration using the standard Arrhenius equation for thermal acceleration. For each process group/ package combination, representative acceleration factors were estimated based on the weighted average of acceleration factors of individual devices in that group.

4. Voltage acceleration factor is not included in failure rate calculation even though voltage acceleration may be used during stress.

5. It is common in reliability literature to see failure rates stated at a specified level of confidence:

   For example, a 60% upper confidence limit on the failure rate indicates that unless a 4 in 10 chances (40%) has occurred, the true population failure rate is less than the stated limit. The summation of individual failure rate components, each at 60% confidence, will however, result in an overall failure rate at an unknown confidence level that may dramatically exceed 60%. The failure rates quoted in the Quarterly Reliability Report are at a 60% upper confidence level.

4 Data Summaries by Process Technology

Technology	Products Family	Inherent Life (FITS)
CS 69S, CS 69LS	S29CD-J, S29NS-J, S29PL-J, S71NS-J, S71PL-J Product Families	6
CS 69SS, CS 69LSS	S29AL-J, S29AS-J, S29JL-J Product Families	5
CS 119S, CS 119LS	S29GL-N, S29NS-N, S29PL-N, S29WS-N, S70PL-N, S71GL-N, S71NS-N, S71PL- N, S71WS-N Product Families	6
CS 129, CS 129L, CS 129AL	S29FL-P, S25FL-P, S29GL-P, S29NS-P, S29WS-P, S70FL-P, S70GL-P, S71GL-P, S71NS-P, S71WS-P, S72NS-P Product Families	7
CS239, CS239L, CS 239LS	S29GL-S, S25FL-S S25FS-S, S26KL-S, S26KS-S, S29VS-R, S29WS-R, S70GL-S, S70-FL-S, S70FS-S, S79FL-S, S79FS-S Product Families	12
CS 340L	S29GL-T, S70GL-T, S26HL-T, S26HS-T Product Families	19
90 nm SPI Floating Gate	S25FL1-K, S25FL2-K Product Families	5
65nm SPI Floating Gate	S25FL-L Product Families	6
C8	HSLS_USB (CY7C64713*, CY7C68013A*) Product Families	29
LL65	ASYNC (CY62147G30*, CY62148G*, CY62157G30*, CY62167EV30LL*, CY62187EV30LL*, CY62177EV30LL*) Product Families	12
R8	ASYNC (CY62167DV30LL*) Product Families	31
R9	SYNC (CY7C1470BV33*, CY7C1472BV33*) Product Families	30
R95	ASYNC (CY62126EV30LL*, CY62128ELL*, CY62146ESL*, CY62147EV30LL*, CY62167EV30LL*) Product Families	8
S40	PSOC (CY8C624AAZI*, CY8C6247BZI*, CY8C6245AZI*, CY7CS40T3A*) Product Families	28
S8	NVSRAM (CY14B101*, CY14B104*, CY14V101*); AUTOPSOC (CY8C4147*, CYAT81688*); PSOC (CY8C4024*, CY8C4124*, CY8C4125*, CY8C4148*, CY8C4245*); TYPE-C (CYAC1126*, CYPD2134*, CYPD2154*, CYPD3184*, CYPD4225*, CYPD6128*, CYPD6227*); HSLS_USB (CY7C652157*) Product Families	3
130nm TI F-RAM	F-RAM (CY15B102*, CY15B104*, CY15B108*, CY15V102*, FM24CL64B8*, FM25CL64B8*, FM25V20A*) Product Families	29
BD500HC1C	TYPE-C (CYPAP111A0*, CYPAP111A1*, CYPAP111A2*, CYPAP111A3*, CYPAP112A3*) Product Families	20
180nm PMICs	S6AXXXX, S6BXXXX Product Families	19
40 nm MCU (FLASH)	S6J33X, S6J34X, S6J35X, CYT2B, CYT4B Product Families	1
55nm MCU (FLASH)	S6J31X, S6J32X Product Families	17
90nm MCU (FLASH)	S6E1XXX, S6E2XXX, CY(MB)9AFXXX, CY(MB)9BFXXX, CY(MB)9DFXXX, CY(MB)9EFXXX, CY(MB)91F52X Product Families	10
180nm MCU (FLASH)	CY(MB)90FXXX, CY(MB)91FXXX, CY(MB)95F5XX, CY(MB)95F6XX Product Families	6
350 nm MCU (FLASH)	CY(MB)90F3XX, CY(MB)91F3XX, CY(MB)95F1XX Product Families	6
65 nm Wireless	Bluetooth, Wi-Fi (65nm) Product Families	28
40 nm Wireless	Bluetooth, Wi-Fi (40nm) Product Families	22

4.1 S29CD-J, S29NS-J, S29PL-J, S71NS-J, S71PL-J Product Families

CS 69S, CS 69LS

This 0.11 micron CMOS Flash technology was introduced in December 2003 and utilizes a tunnel oxide, polysilicon floating gate, silicided poly word line and interconnections are three metal layers with contact plugs and barrier metal.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	**Read Point / Test Result**		**Modeling Parameters @ 55°C**					**Average Failure Rate**	
	Early Life (hrs)	**Inherent Life (hrs)**	**Ea eV**	**TAF**	**VAF**	**OAF**	**MTTF (yrs)**	**Early Life (PPM)**	**Inherent Life (FITS)**
	48	**1000**							
Sample Size	2000	750							
150C, Zero fails, Process ave. Ea	0	0	0.7	217	1	217	20303	0	6

Data Retention Bake - 150°C

Reliability Stress	**Sample Size**	**Reject**	**PPM**	**FITS**
1000	1000	0	0	<1

4.2 S29AL-J, S29AS-J, S29JL-J Product Families

CS 69SS, CS 69LSS

This 0.11 micron CMOS Flash technology was introduced in February 2008 and utilizes a tunnel oxide, polysilicon floating gate, silicided poly word line and interconnections are three metal layers with contact plugs and barrier metal.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	**Read Point / Test Result**		**Modeling Parameters @ 55°C**					**Average Failure Rate**	
	Early Life (hrs)	**Inherent Life (hrs)**	**Ea eV**	**TAF**	**VAF**	**OAF**	**MTTF (yrs)**	**Early Life (PPM)**	**Inherent Life (FITS)**
	48	**1000**							
Sample Size	2000	770							
150C, Zero fails, Process ave. Ea	0	0	0.7	227	1	227	21805	0	5

Data Retention Bake - 150°C

Reliability Stress	**Sample Size**	**Reject**	**PPM**	**FITS**
1000	1078	0	0	<1

4.3 S29GL-N, S29NS-N, S29PL-N, S29WS-N, S70PL-N, S71GL-N, S71NS-N, S71PL-N, S71WS-N Product Families

CS 119S, CS 119LS

This 0.11 micron CMOS Flash technology was introduced in June 2004 and utilizes a tunnel oxide, Silicon Nitride (SiN) data storage layer, silicided poly word line and interconnections are three or four metal layers with contact plugs and barrier metal.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	**Read Point / Test Result**		**Modeling Parameters @ 55°C**					**Average Failure Rate**	
	Early Life (hrs)	**Inherent Life (hrs)**	**Ea eV**	**TAF**	**VAF**	**OAF**	**MTTF (yrs)**	**Early Life (PPM)**	**Inherent Life (FITS)**
	48	**1000**							
Sample Size	2000	750							
150C, Zero fails, Process ave. Ea	0	0	0.7	196	1	196	18329	0	6

Data Retention Bake - 150°C

Reliability Stress	**Sample Size**	**Reject**	**PPM**	**FITS**
1000	539	0	0	<1

4.4 S29FL-P, S25FL-P, S29GL-P, S29NS-P, S29WS-P, S70FL-P, S70GL-P, S71GL-P, S71NS-P, S71WS-P, S72NS-P Product Families

CS 129, CS 129L, CS 129AL

This 90 nanometer CMOS Flash technology was introduced in Aug 2006 and utilizes a tunnel oxide, Silicon Nitride (SiN) data storage layer, silicided poly word line and interconnections are three copper layers.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	**Read Point / Test Result**		**Modeling Parameters @ 55°C**					**Average Failure Rate**	
	Early Life (hrs)	**Inherent Life (hrs)**	**Ea eV**	**TAF**	**VAF**	**OAF**	**MTTF (yrs)**	**Early Life (PPM)**	**Inherent Life (FITS)**
	48	**1000**							
Sample Size	2000	750							
150C, Zero fails, Process ave. Ea	0	0	0.7	188	1	188	17521	0	7

Data Retention Bake - 150°C

Reliability Stress	**Sample Size**	**Reject**	**PPM**	**FITS**
1000	1078	0	0	<1

4.5 S29GL-S, S25FL-S S25FS-S, S26KL-S, S26KS-S, S29VS-R, S29WS-R, S70GL-S, S70-FL-S, S70FS-S, S79FL-S, S79FS-S Product Families

CS 239, CS 239L, CS 239LS

This 65 nm Mirror bit flash technology was introduced in September 2010 and utilizes a tunnel oxide, Silicon Nitride (SiN) data storage layer, silicided poly word line and interconnections are four metal layers with contact plugs and barrier metal.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 125°C

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	1000							
Sample Size	2000	1090							
125C, Zero fails, Process ave. Ea	0	0	0.7	69	1	69	9351	0	12

Data Retention Bake - 150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
1000	2795	0	0	<1

4.6 S29GL-T, S70GL-T, S26HL-T, S26HS-T Product Families

CS 340L

This 45nm Mirror bit flash technology was introduced in December 2015 and utilizes a tunnel oxide, Silicon Nitride(SiN) data storage layer, silicided poly word and interconnections are four metal layers with contact plu and five metal layers with contact plug and barrier metal.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 125°C

Failure Mechanisms	**Read Point / Test Result**		**Modeling Parameters @ 55°C**					**Average Failure Rate**	
	Early Life (hrs)	**Inherent Life (hrs)**	**Ea eV**	**TAF**	**VAF**	**OAF**	**MTTF (yrs)**	**Early Life (PPM)**	**Inherent Life (FITS)**
	96	**1000**							
Sample Size	2000	1200							
125C, Zero fails, Process ave. Ea	0	0	0.7	40	1	40	5949	0	19

Data Retention Bake - 150°C

Reliability Stress	**Sample Size**	**Reject**	**PPM**	**FITS**
1000	616	0	0	3

4.7 S25FL1-K, S25FL2-K Product Families

90 nm SPI Floating Gate

90 nm SPI (Serial Peripheral Interface) Floating Gate Flash Technology was introduced in May 2012 and utilizes tunnel oxide, polysilicon floating gate and interconnections are three metal layers with contact plugs and barrier metals.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	**Read Point / Test Result**		**Modeling Parameters @ 55°C**					**Average Failure Rate**	
	Early Life (hrs)	**Inherent Life (hrs)**	**Ea eV**	**TAF**	**VAF**	**OAF**	**MTTF (yrs)**	**Early Life (PPM)**	**Inherent Life (FITS)**
	48	**1000**							
Sample Size	2000	900							
150C, Zero fails, Process ave. Ea	0	0	0.7	208	1	208	23376	0	5

Data Retention Bake - 150°C

Reliability Stress	**Sample Size**	**Reject**	**PPM**	**FITS**
1000	539	0	0	<1

4.8 S25FL-L Product Families

65 nm SPI Floating Gate

65nm SPI (Serial Peripheral Interface) Floating Gate Technology was introduced in August 2016 and utilizes tunnel oxide, polysilicon floating gate and interconnections are three metal layers with contact plugs and barrier metals.

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	**Read Point / Test Result**		**Modeling Parameters @ 55°C**					**Average Failure Rate**	
	Early Life (hrs)	**Inherent Life (hrs)**	**Ea eV**	**TAF**	**VAF**	**OAF**	**MTTF (yrs)**	**Early Life (PPM)**	**Inherent Life (FITS)**
	48	**1000**							
Sample Size	2000	640							
150C, Zero fails, Process ave. Ea	0	0	0.7	227	1	227	18124	0	6

Data Retention Bake - 150°C

Reliability Stress	**Sample Size**	**Reject**	**PPM**	**FITS**
1000	693	0	0	<1

4.9 HSLS_USB (CY7C64713*, CY7C68013A*) Product Families

C8 Technology

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature – 125°C

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	1000							
Sample Size	578	578							
125C, Zero fails, Process ave. Ea	0	0	0.7	55	1	55	3982	0	29

4.10 ASYNC (CY62147G30*, CY62148G*, CY62157G30*, CY62167EV30LL*, CY62187EV30LL*, CY62177EV30LL*) Product Families

LL65 Technology

Data Summary and Failure Rate Estimation using Exponential Model
HTOL Stress Temperature - 125°C

Failure Mechanisms	**Read Point / Test Result**				**Modeling Parameters @ 55°C**					**Average Failure Rate**	
	Early Life (hrs)		**Inherent Life (hrs)**		**Ea eV**	**TAF**	**VAF**	**OAF**	**MTTF (yrs)**	**Early Life (PPM)**	**Inherent Life (FITS)**
	48	**96**	**500**	**1000**							
Sample Size		14443		1185						0	12
125C, Zero fails, Process ave. Ea		0		0	0.7	55	1	55			
Sample Size	117		117						9402		
150C, Zero fails, Process ave. Ea	0		0		0.7	170	1	170			

4.11 ASYNC (CY62167DV30LL*) Product Families

R8 Technology

Data Summary and Failure Rate Estimation using Exponential Model
HTOL Stress Temperature – 125/150°C

Failure Mechanisms	**Read Point / Test Result**				**Modeling Parameters @ 55°C**					**Average Failure Rate**	
	Early Life (hrs)		**Inherent Life (hrs)**		**Ea eV**	**TAF**	**VAF**	**OAF**	**MTTF (yrs)**	**Early Life (PPM)**	**Inherent Life (FITS)**
	48	**96**	**500**	**1000**							
Sample Size		415		415						0	31
125C, Zero fails, Process ave. Ea		0		0	0.7	55	1	55			
Sample Size	77		77						3674		
150C, Zero fails, Process ave. Ea	0		0		0.7	170	1	170			

4.12 SYNC (CY7C1470BV33*, CY7C1472BV33*) Product Families

R9 Technology

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	500							
Sample Size	362	362							
150C, Zero fails, Process ave. Ea	0	0	0.7	170	1	170	3831	0	30

4.13 ASYNC (CY62126EV30LL*, CY62128ELL*, CY62146ESL*, CY62147EV30LL*, CY62167EV30LL*) Product Families

R95 Technology

Data Summary and Failure Rate Estimation using Exponential Model
HTOL Stress Temperature – 125/150°C

Failure Mechanisms	Read Point / Test Result					Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	96	408	500	1000							
Sample Size		2561			100						0	8
125C, Zero fails, Process ave. Ea		0			0	0.7	55	1	55			
Sample Size	800		215	1150								
150C, Zero fails, Process ave. Ea	0		0	0		0.7	170	1	170	14715		

4.14 PSOC (CY8C624AAZI*, CY8C6247BZI*, CY8C6245AZI*, CY7CS40T3A*) Product Families

S40 Technology

Data Summary and Failure Rate Estimation using Exponential Model
HTOL Stress Temperature – 125/150°C

Failure Mechanisms	Read Point / Test Result				Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)		Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	96	500	1000							
Sample Size		1559		442						0	28
125C, Zero fails, Process ave. Ea		0		0	0.7	55	1	55			
Sample Size	95		95						4050		
150C, Zero fails, Process ave. Ea	0		0		0.7	170	1	170			

Data Retention Bake – 125°C

Reliability Stress	Sample Size	Reject	PPM	FITS
1000	160	0	0	104

4.15 NVSRAM (CY14B101*, CY14B104*, CY14V101*); AUTOPSOC (CY8C4147*, CYAT81688*); PSOC (CY8C4024*, CY8C4124*, CY8C4125*, CY8C4148*, CY8C4245*); TYPE-C (CYAC1126*, CYPD2134*, CYPD2154*, CYPD3184*, CYPD4225*, CYPD6128*, CYPD6227*); HSLS_USB (CY7C652157*) Product Families

S8 Technology

Data Summary and Failure Rate Estimation using Exponential Model
HTOL Stress Temperature – 125/150°C

Failure Mechanisms	Read Point / Test Result					Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)			Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	96	408	500	1000							
Sample Size		24754			357						0	3
125C, Zero fails, Process ave. Ea		0			0	0.7	55	1	55			
Sample Size	41973		1140	2712								
150C, Zero fails, Process ave. Ea	0		0	0		0.7	170	1	170	41001		

Data Retention Bake – 125/150°C

Reliability Stress	Sample Size	Reject	PPM	FITS
1000 (125)	78	0	0	3
1000 (150)	1625	0	0	

4.16 F-RAM (CY15B102*, CY15B104*, CY15B108*, CY15V102*, FM24CL64B8*, FM25CL64B8*, FM25V20A*) Product Families

130nm TI F-RAM Technology

Data Summary and Failure Rate Estimation using Exponential Model
HTOL Stress Temperature – 125/150°C

Failure Mechanisms	**Read Point / Test Result**			**Modeling Parameters @ 55°C**					**Average Failure Rate**	
	Early Life (hrs)		**Inherent Life (hrs)**	**Ea eV**	**TAF**	**VAF**	**OAF**	**MTTF (yrs)**	**Early Life (PPM)**	**Inherent Life (FITS)**
	48	**96**	**1000**							
Sample Size		9083	570						0	29
125C, Zero fails, Process ave. Ea		0	0	0.7	55	1	55			
Sample Size	800									
150C, Zero fails, Process ave. Ea	0							3927		

Data Retention Bake – 125°C

Reliability Stress	**Sample Size**	**Reject**	**PPM**	**FITS**
1000	1116	0	0	<1

4.17 TYPE-C (CYPAP111A0*, CYPAP111A1*, CYPAP111A2*, CYPAP111A3*, CYPAP112A3*) Product Families

BD500HC1C Technology

Data Summary and Failure Rate Estimation using Exponential Model
HTOL Stress Temperature - 125°C

Failure Mechanisms	**Read Point / Test Result**		**Modeling Parameters @ 55°C**					**Average Failure Rate**	
	Early Life (hrs)	**Inherent Life (hrs)**	**Ea eV**	**TAF**	**VAF**	**OAF**	**MTTF (yrs)**	**Early Life (PPM)**	**Inherent Life (FITS)**
	96	**1000**							
Sample Size	9217	832							
125C, Zero fails, Process ave. Ea	0	0	0.7	55	1	55	5732	0	20

4.18 S6AXXXX, S6BXXXX Product Families

180 nm PMICs

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 125°C

Failure Mechanisms	**Read Point / Test Result**		**Modeling Parameters @ 55°C**					**Average Failure Rate**	
	Early Life (hrs)	**Inherent Life (hrs)**	**Ea eV**	**TAF**	**VAF**	**OAF**	**MTTF (yrs)**	**Early Life (PPM)**	**Inherent Life (FITS)**
	96	**1000**							
Sample Size	855	855							
125C, Zero fails, Process ave. Ea	0	0	0.7	55	1	55	5891	0	19

4.19 S6J33X, S6J34X, S6J35X, CYT2B, CYT4B Product Families

40 nm MCU (FLASH)

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 125/150°C

Failure Mechanisms	Read Point / Test Result				Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)		Inherent Life (hrs)		Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	48	96	500	1000							
Sample Size		616		616						0	1
125C, Zero fails, Process ave. Ea		0		0	0.7	55	1	55			
Sample Size	8094		8094						89894		
150C, Zero fails, Process ave. Ea	0		0		0.7	170	1	170			

4.20 S6J31X, S6J32X Product Families

55 nm MCU (FLASH)

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature – 105/125°C

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	1000							
Sample Size	77	77						0	17
105C, Zero fails, Process ave. Ea	0	0	0.7	20	1	20			
Sample Size	924	924							
125C, Zero fails, Process ave. Ea	0	0	0.7	55	1	55	6561		

4.21 S6E1XXX, S6E2XXX, CY(MB)9AFXXX, CY(MB)9BFXXX, CY(MB)9DFXXX, CY(MB)9EFXXX, CY(MB)91F52X Product Families

90 nm MCU (FLASH)

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 125°C

Failure Mechanisms	**Read Point / Test Result**		**Modeling Parameters @ 55°C**					**Average Failure Rate**	
	Early Life (hrs)	**Inherent Life (hrs)**	**Ea eV**	**TAF**	**VAF**	**OAF**	**MTTF (yrs)**	**Early Life (PPM)**	**Inherent Life (FITS)**
	96	**1000**							
Sample Size	1694	1694							
125C, Zero fails, Process ave. Ea	0	0	0.7	55	1	55	11671	0	10

4.22 CY(MB)90FXXX, CY(MB)91FXXX, CY(MB)95F5XX, CY(MB)95F6XX Product Families

180 nm MCU (FLASH)

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 125°C

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	1000							
Sample Size	2906	2906							
125C, Zero fails, Process ave. Ea	0	0	0.7	55	1	55	20021	0	6

4.23 CY(MB)90F3XX, CY(MB)91F3XX, CY(MB)95F1XX Product Families

350 nm MCU (FLASH)

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 125°C

Failure Mechanisms	**Read Point / Test Result**		**Modeling Parameters @ 55°C**					**Average Failure Rate**	
	Early Life (hrs)	**Inherent Life (hrs)**	**Ea eV**	**TAF**	**VAF**	**OAF**	**MTTF (yrs)**	**Early Life (PPM)**	**Inherent Life (FITS)**
	96	**1000**							
Sample Size	2581	2581							
125C, Zero fails, Process ave. Ea	0	0	0.7	55	1	55	17782	0	6

4.24 Bluetooth, Wi-Fi (65nm) Product Families

65 nm Wireless

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 125°C

Failure Mechanisms	**Read Point / Test Result**		**Modeling Parameters @ 55°C**					**Average Failure Rate**	
	Early Life (hrs)	**Inherent Life (hrs)**	**Ea eV**	**TAF**	**VAF**	**OAF**	**MTTF (yrs)**	**Early Life (PPM)**	**Inherent Life (FITS)**
	96	**1000**							
Sample Size	596	596							
125C, Zero fails, Process ave. Ea	0	0	0.7	55	1	55	4106	0	28

4.25 Bluetooth, Wi-Fi (40nm) Product Families

40 nm Wireless

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 125°C

Failure Mechanisms	Read Point / Test Result		Modeling Parameters @ 55°C					Average Failure Rate	
	Early Life (hrs)	Inherent Life (hrs)	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life (PPM)	Inherent Life (FITS)
	96	1000							
Sample Size	766	766							
125C, Zero fails, Process ave. Ea	0	0	0.7	55	1	55	5277	0	22

5 Data Summaries by Package Family

5.1 BGA (Ball Grid Array)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	1510	0	0
	264hrs	3542	0	0
HIGH TEMP STORAGE	1000hrs	5080	0	0
TEMP CYCLE	500cycle	3875	0	0
	1000cycle	1728	0	0
UNBIASED HAST TEST	96hrs	3322	0	0
	264hrs	1761	0	0

5.2 BGA (Ball Grid Array) – Flip Chip

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	225	0	0
HIGH TEMP STORAGE	1000hrs	250	0	0
TEMP CYCLE	1000cycle	250	0	0
UNBIASED HAST TEST	96hrs	250	0	0

5.3 DFN (Dual Flat no-leads)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	399	0	0
HIGH TEMP STORAGE	1000hrs	580	0	0
PRESSURE COOKER TEST	168hrs	255	0	0
TEMP CYCLE	500cycle	645	0	0
UNBIASED HAST TEST	96hrs	175	0	0

5.4 DIP (Dual-In-line Package)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	308	0	0
	264hrs	75	0	0
HIGH TEMP STORAGE	1000hrs	285	0	0
PRESSURE COOKER TEST	168hrs	161	0	0
TEMP CYCLE	500cycle	692	0	0
UNBIASED HAST TEST	96hrs	75	0	0

5.5 LCC (Leaded Chip Carrier)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HIGH TEMP STORAGE	1000hrs	60	0	0
PRESSURE COOKER TEST	168hrs	30	0	0
TEMP CYCLE	500cycle	30	0	0

5.6 QFN (Quad Flat no-leads)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	3362	0	0
	264hrs	456	0	0
HIGH TEMP STORAGE	1000hrs	3338	0	0
PRESSURE COOKER TEST	96hrs	779	0	0
	168hrs	3474	0	0
TEMP CYCLE	500cycle	6320	0	0
	1000cycle	225	0	0
UNBIASED HAST TEST	96hrs	1183	0	0
	264hrs	231	0	0

5.7 QFP (Quad Flat Package)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	4708	0	0
	264hrs	2659	0	0
HIGH TEMP STORAGE	1000hrs	4359	0	0
PRESSURE COOKER TEST	96hrs	760	0	0
	168hrs	1059	0	0
TEMP CYCLE	500cycle	9164	0	0
UNBIASED HAST TEST	96hrs	6055	0	0
	264hrs	231	0	0

5.8 SOJ (Small Outline J Lead)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	120	0	0
HIGH TEMP STORAGE	1000hrs	107	0	0
PRESSURE COOKER TEST	168hrs	269	0	0
TEMP CYCLE	500cycle	268	0	0
UNBIASED HAST TEST	96hrs	239	0	0

5.9 SOP (Small Outline Gull Wing Lead Package)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	3588	0	0
	264hrs	306	0	0
HIGH TEMP STORAGE	1000hrs	4175	0	0
	2000hrs	45	0	0
PRESSURE COOKER TEST	96hrs	1014	0	0
	168hrs	2765	0	0
TEMP CYCLE	500cycle	5819	0	0
	1000cycle	125	0	0
UNBIASED HAST TEST	96hrs	1663	0	0

5.10 SSOP (Shrink Small Outline Package)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	1189	0	0
HIGH TEMP STORAGE	1000hrs	811	0	0
PRESSURE COOKER TEST	96hrs	387	0	0
	168hrs	609	0	0
TEMP CYCLE	500cycle	1415	0	0
UNBIASED HAST TEST	96hrs	410	0	0

5.11 TSOP (Thin Small Outline Package)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	4174	0	0
	264hrs	130	0	0
HIGH TEMP STORAGE	1000hrs	4900	0	0
PRESSURE COOKER TEST	96hrs	1035	0	0
	168hrs	1863	0	0
TEMP CYCLE	500cycle	5625	0	0
UNBIASED HAST TEST	96hrs	1863	0	0

5.12 WLCSP (Wafer Level Chip Scale Package)

Reliability Stress		Sample Size	Reject	Failure Rate PPM
HAST	96hrs	1192	0	0
	264hrs	18	0	0
HIGH TEMP STORAGE	1000hrs	1531	0	0
TEMP CYCLE	1000cycle	2564	0	0
UNBIASED HAST TEST	96hrs	2217	0	0

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