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## Objective

CE222967 demonstrates accessing the Excelon™ Ultra QSPI F-RAM™ using the Serial Memory Interface (SMIF) block in PSoC® 6 MCU and ModusToolbox™ IDE.

## Requirements

**Tool:** ModusToolbox IDE 1.1

**Programming Language:** C

**Associated Parts:** All PSoC 6 MCU parts

**Related Hardware:** PSoC 6 WiFi-BT Pioneer Kit (CY8CKIT-062-WiFi-BT)

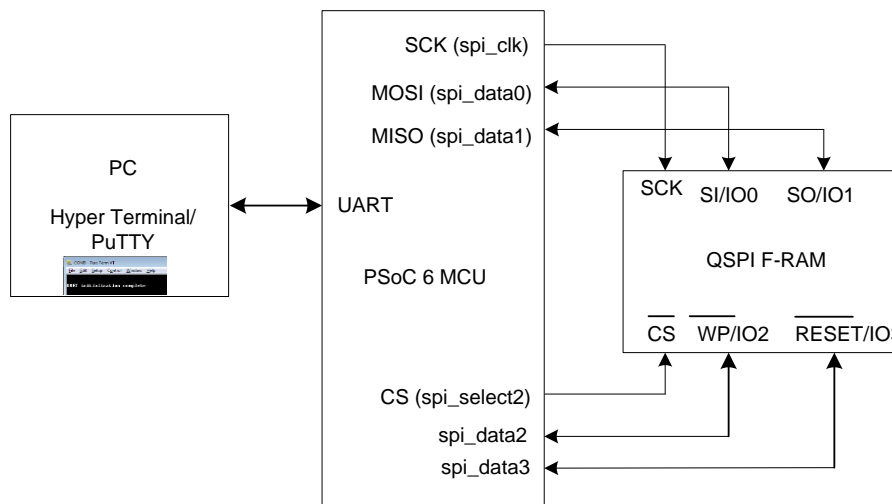
## Overview

CE222967 provides a code example that implements the Quad Serial Memory Interface (QSPI) host controller on the PSoC 6 MCU device using the SMIF resource and demonstrates accessing different features of an external QSPI F-RAM using ModusToolbox IDE. The result is displayed by driving the RGB LED, which turns green when the result is a pass, and turns red when the result is a fail. The code example also enables the UART interface to connect to a PC to monitor the result.

## Hardware Setup

The hardware setup includes connecting the QSPI F-RAM with PSoC 6 MCU as shown in Figure 1. You can use either dedicated hardware as described in the Requirements section or any PSoC 6 MCU DVK connected to an external QSPI F-RAM via jumper wires. This example uses the PSoC 6 WiFi-BT Pioneer kit's default configuration.

Figure 1. Hardware Setup Block Diagram



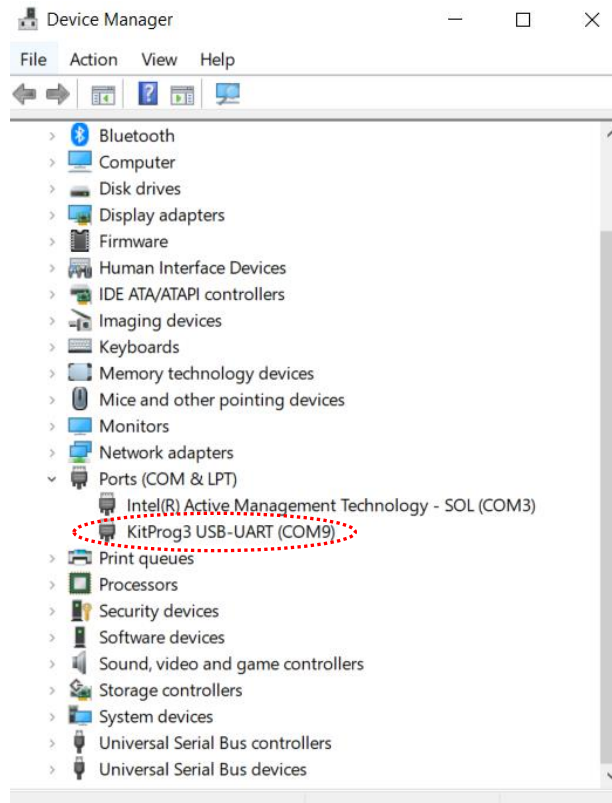
**Note:** PSoC 6 BLE and PSoC 6 WiFi-BT Pioneer kits are shipped with KitProg2. ModusToolbox only works with KitProg3. Therefore, make sure that the kit is upgraded to KitProg3 before using this code example. See ModusToolbox **Help > ModusToolbox IDE Documentation > User Guide**; section “PSoC 6 MCU KitProg Firmware Loader”. If you do not upgrade, you will see an error like “unable to find CMSIS-DAP device” or “KitProg firmware is out of date”.

## Software Setup

This section demonstrates the procedure to set up the serial (UART) connection using PuTTY on PC to communicate with the PSoC 6 Pioneer Kit. PuTTY is a free SSH and Telnet client for Windows. You can download PuTTY from [www.putty.org](http://www.putty.org). Follow these instructions to determine the COM port number and set up PuTTY to monitor the code example outputs on a PC.

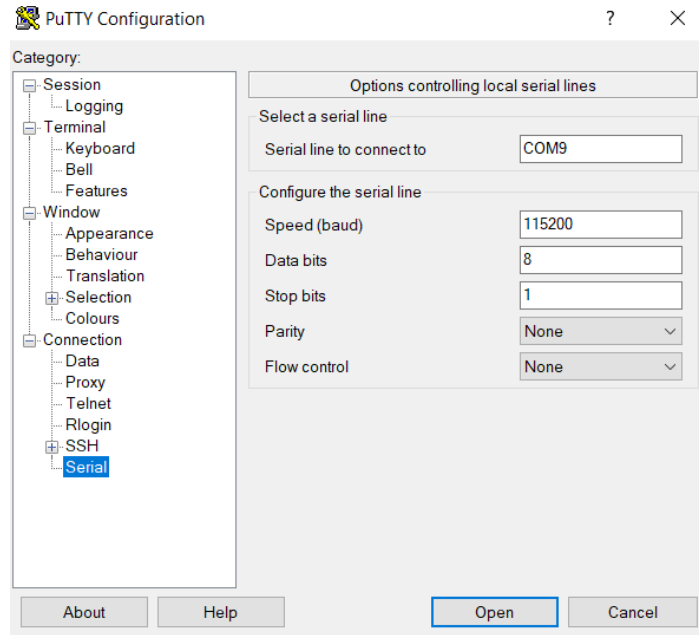
1. Connect PSoC 6 Pioneer Kit to the PC using the USB cable. The kit enumerates as KitProg3 USB-UART and is available under the **Device Manager > Ports (COM & LPT)**. A communication port (COMx) is assigned to KitProg3 USB-UART; for example, COM9 is assigned to PSoC 6 Pioneer Kit on the sample setup, as shown in [Figure 2](#).

Figure 2. KitProg3 USB-UART in Device Manager



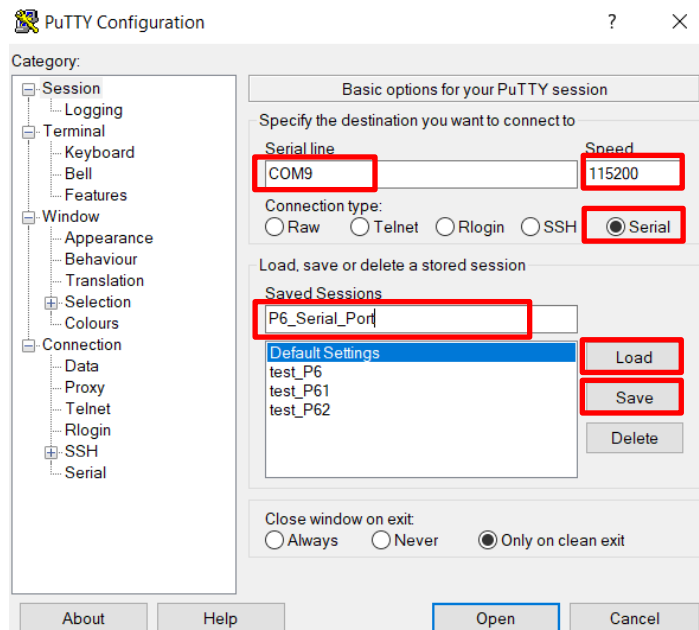
2. After you download and install PuTTY, double-click the PuTTY icon and select **Serial** under **Connection**.
3. A new window, as shown in [Figure 3](#), opens where the communication port can be selected. Do the following in the **Options controlling local serial lines** section:
  - Enter the PSoC 6 MCU Port (COM & LPT), COMx, in **Serial line to connect to**. This code example uses **COM9**. Verify the COM setting for your setup and select the appropriate COMx.
  - Enter **Speed (baud):115200**, **Data bits:8**, and **Stop bits:1**.
  - Set **Parity** and **Flow control** to None.

Figure 3. Open New Connection



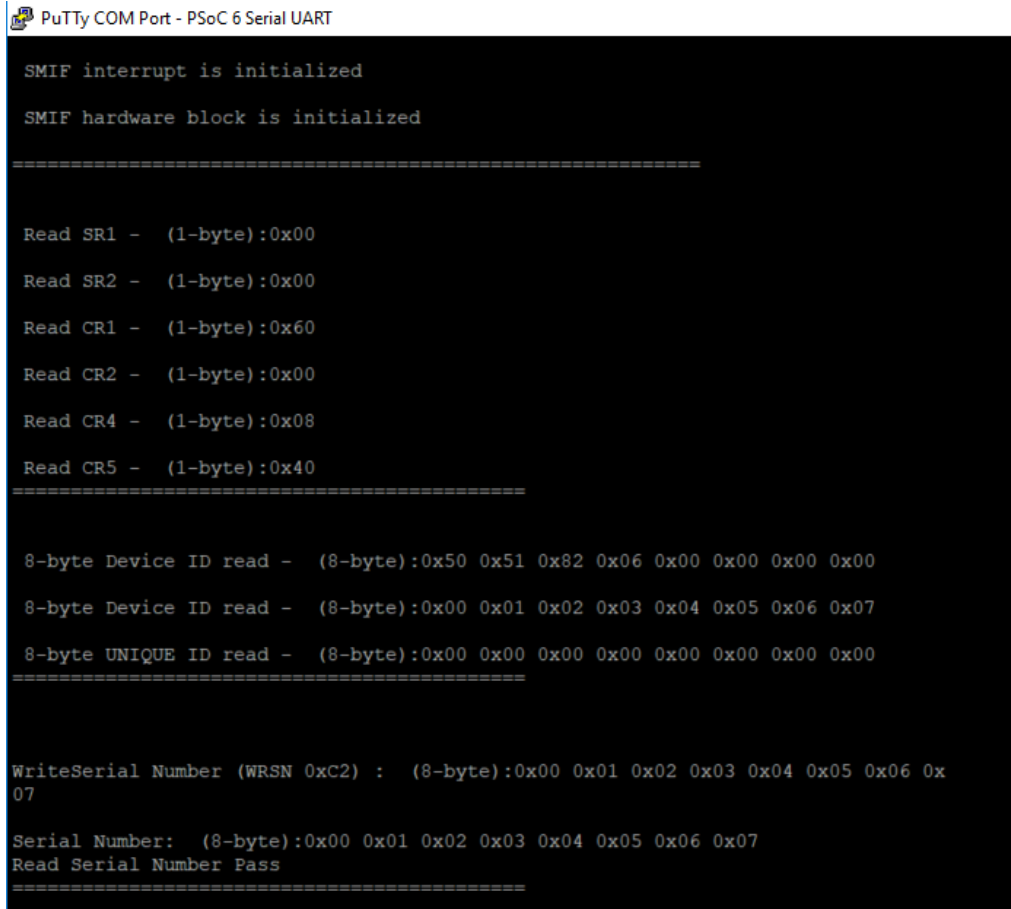
4. Select **Session** under **Category**. Select **Serial** under **Connection type** as shown in Figure 4. You can save this current session and load the settings when required. Enter a name in **Saved Sessions** and click **Save**. Click **Open** to proceed.

Figure 4. Select Communication Type in PuTTY



- The COM terminal window displays the code example results as shown in [Figure 5](#). You may have to reprogram the PSoC 6 MCU device with the code example or reset the PSoC 6 MCU device (already programmed) to restart code execution and monitor the result.

Figure 5. Result Displayed on PC Terminal



```

PuTTY COM Port - PSoC 6 Serial UART

SMIF interrupt is initialized
SMIF hardware block is initialized

=====

Read SR1 - (1-byte):0x00
Read SR2 - (1-byte):0x00
Read CR1 - (1-byte):0x60
Read CR2 - (1-byte):0x00
Read CR4 - (1-byte):0x08
Read CR5 - (1-byte):0x40
=====

8-byte Device ID read - (8-byte):0x50 0x51 0x82 0x06 0x00 0x00 0x00 0x00
8-byte Device ID read - (8-byte):0x00 0x01 0x02 0x03 0x04 0x05 0x06 0x07
8-byte UNIQUE ID read - (8-byte):0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
=====

WriteSerial Number (WRSN 0xC2) : (8-byte):0x00 0x01 0x02 0x03 0x04 0x05 0x06 0x
07

Serial Number: (8-byte):0x00 0x01 0x02 0x03 0x04 0x05 0x06 0x07
Read Serial Number Pass
=====
  
```

Alternatively, you can run HyperTerminal if supported on your PC to monitor the above result.

## Operation

This code example demonstrates the following features of the Excelon Ultra QSPI F-RAM:

- Sets the device access mode to default SPI mode. This ensures that the part starts in a known SPI mode.
- Reads two Status and four Configuration registers (SR1, SR2, CR1, CR2, CR4, CR5)
- Reads the 8-byte device ID
- Writes 256 bytes into F-RAM at a given address, in SPI mode
- Reads 256 bytes from F-RAM at a given address, using the READ (0x02) opcode in SPI, DPI, and QPI mode
- Reads 256 bytes from F-RAM at a given address, using the Fast\_Read (0x0B) opcode in QPI mode
- Writes and read 256 bytes special sector using SSWR and SSRD commands in QPI mode

Do the following to execute the code example project. See the [Design and Implementation](#) section for more details.

- Connect the CY8CKIT-062-WiFi-BT Pioneer Kit to a USB port on your PC. Set the  $V_{DD}$  select either 1.8 V or 3.3 V using the switch SW5 on PSoC 6 Pioneer Kit. The QSPI F-RAM supports wide operating range  $V_{DD} = 1.8$  V to 3.6 V.
- Open a serial port communication program such as PuTTY and select the corresponding COM port. Configure the terminal to match the UART: 115200 baud rate, 8N1, Parity and Flow control: None.

3. Import the application into a new workspace. See [KBA225201](#).
4. Build and program the application into the CY8CKIT-062-WiFi-BT Kit or CY8CKIT-062-BLE Kit which has serial F-RAM mounted on it.
5. Observe the result by monitoring the RGB LED. The LED toggles green when result is a pass and red when result is a fail.
6. Observe the result through UART message printed in the terminal window. [Figure 5](#) shows a snapshot of a sample UART terminal output.

## Debugging

You can debug the example to step through the code. Use the **Debug (KitProg3)** configuration. See [KBA224621](#) to learn how to start a debug session with ModusToolbox IDE.

## Design and Implementation

The Quad Serial Memory Interface (QSPI) resource implements QSPI-based communication for interfacing external Excelon Ultra QSPI F-RAM devices with PSoC 6 MCU. This example executes a burst write of 256-byte data to an external QSPI F-RAM in SPI, DPI, QPI modes respectively. The written data is then read back to check its integrity. The UART resource outputs debug/result information to a terminal window. A user LED (RGB) indicates the status of read and write operation.

## Resources

[Table 1](#) and [Table 2](#) list the PSoC 6 MCU resources and their utilization in this code example.

Table 1. ModusToolbox Resources - Peripherals

Resource	Alias	Purpose	Non-Default Settings
Quad Serial Memory Interface (QSPI) 0	KIT_FRAM	Configured as the SPI host controller to communicate with the SPI F-RAM	<a href="#">Figure 6</a>
Serial Communication Block (SCB) 5	KIT_UART	To print output results on a terminal window	<a href="#">Figure 7</a>

[Table 2](#) lists the resources used in this example, and how they are used in the design.

Table 2. ModusToolbox Resources - Pins

Resource	Port/Alias	Pin Drive Mode	Purpose	Non-Default Settings
GPIO – Port 11	P11[0]/FRAM_CS	Strong Drive, Input buffer off	Sends SPI commands to access the SPI F-RAM	<a href="#">Figure 8</a>
	P11[3]/ QSPI_IO3	Strong Drive, Input buffer on		
	P11[4]/ QSPI_IO2	Strong Drive, Input buffer on		
	P11[5]/ QSPI_IO1	Strong Drive, Input buffer on		
	P11[6]/ QSPI_IO0	Strong Drive, Input buffer on		
	P11[7]/ QSPI_SCK	Strong Drive, Input buffer off		
GPIO – Port 5	P5[0]/ KIT_UART_RX	Digital High-Z, input buffer on	Receives/transmits data packets from/to PC terminal	<a href="#">Figure 9</a>
	P5[1]/ KIT_UART_TX	Strong Drive, Input buffer off		
GPIO – Port 0	P0[3]/RGB_RED	Strong Drive, Input buffer off	Drives the GPIO to glow red of the RGB LED to indicate the fail status	<a href="#">Figure 10</a>
GPIO – Port 1	P1[1]/RGB_GREEN	Strong Drive, Input buffer off	Drives the GPIO to glow green of the RGB LED to indicate the pass status	<a href="#">Figure 11</a>

## Parameter settings

Non-default settings for each resource is outlined in red in the following figures. Figure 6 and Figure 7 show the resource parameter settings for QSPI 0 and SCB 5 blocks for enabling the SPI host and UART.

Figure 6. QSPI 0 (KIT\_FRAM) Resource Parameter Settings

The screenshot shows the 'Parameters' window for the 'Quad Serial Memory Interface (QSPI) 0 (KIT\_FRAM)'. The left pane shows the resource tree with 'Quad Serial Memory Interface (QSPI) 0' selected. The right pane shows the following settings:

- Peripheral Documentation:** Configuration Help (Open SMIF Documentation)
- Clks:**
  - HF Clock: CLK\_HF0 root\_clk [USED]
  - Interface Clock: CLK\_HF2 root\_clk [USED]
  - SPI Clock: P11[7] digital\_inout (QSPI\_SCK) [USED]
- External tools:** QSPI Configurator (Launch QSPI Configurator) - outlined with a dotted red line.
- Data:**
  - SPI Data[0]: P11[6] digital\_out (QSPI\_IO0) [USED]
  - SPI Data[1]: P11[5] digital\_out (QSPI\_IO1) [USED]
  - SPI Data[2]: P11[4] digital\_out (QSPI\_IO2) [USED]
  - SPI Data[3]: P11[3] digital\_out (QSPI\_IO3) [USED]
  - SPI Data[4]: <unassigned>
  - SPI Data[5]: <unassigned>
  - SPI Data[6]: <unassigned>
  - SPI Data[7]: <unassigned>
- Slave Select:**
  - SPI Slave Select 0: <unassigned>
  - SPI Slave Select 1: <unassigned>
  - SPI Slave Select 2: P11[0] digital\_out (FRAM\_CS) [USED]
  - SPI Slave Select 3: <unassigned>
- Interrupt:** <unassigned>

This code example does not use the “QSPI Configurator” external tool, outlined as above with the dotted red line.

Figure 7. SCB 5 (KIT\_UART) Resource Parameter Settings

The screenshot shows the 'Parameters' window for the 'Serial Communication Block (SCB) 5 (KIT\_UART)'. The left pane shows the resource tree with 'Serial Communication Block (SCB) 5' selected. The right pane shows the following settings:

- Peripheral Documentation:** Configuration Help (Open UART (SCB) Documentation)
- General:**
  - Com Mode: Standard
  - Baud Rate (bps): 115200
  - Oversample: 8
  - Bit Order: LSB First
  - Data Width: 8 bits
  - Parity: None
  - Stop Bits: 1 bit
  - Enable Digital Filter:
- Support RS-485:** TX-Enable:
- Flow Control:**
  - Enable Flow Control:
  - CTS Polarity: Active Low
  - RTS Polarity: Active Low
  - RTS Activation Level: 63
- Connections:**
  - Clock: 16 bit Divider 0 clk (KIT\_UART\_Clock) [USED]
  - RX: PS[0] digital\_inout (KIT\_UART\_RX) [USED]
  - TX: PS[1] digital\_inout (KIT\_UART\_TX) [USED]
  - RX Trigger Output: <unassigned>
  - TX Trigger Output: <unassigned>
- Actual Baud Rate:**
  - Actual Baud Rate (bps): 115384
  - Baud Rate Accuracy (%): 0.160
  - Clock Frequency: 923.077 kHz
- Trigger Level:**
  - RX FIFO Level: 63
  - TX FIFO Level: 63

Figure 8 and Figure 9 show the QSPI and UART port pin and drive strength settings. Refer Table 2 for the drive mode setting for each PSoC 6 MCU pin used in this code example.

Figure 8. Port 11 (QSPI Controls) Resource Parameter Settings

Figure 9. Port 5 (KIT\_UART Control) Resource Parameter Settings



Figure 10 and Figure 11 show the RGB LED port pin and drive strength settings to drive the RGB LED red when the code executes with fail output and drives green when the code executes with pass (expected) output.

Figure 10. P0[3] (RGB\_RED) Resource Parameter Settings

The screenshot displays the PSoC Designer interface for configuring the P0[3] (RGB\_RED) resource. On the left, the Resource list shows Port 0 pins P0[0] through P0[5], with P0[3] selected and its personality set to RGB\_RED. The central pin grid shows the physical layout of pins P0.0 through P0.5, with P0.3 highlighted in orange. The right-hand pane, titled 'P0[3] (RGB\_RED) - Parameters', contains the following settings:

Name	Value
<b>Peripheral Documentation</b>	
Configuration Help	<a href="#">Open GPIO Documentation</a>
<b>General</b>	
Drive Mode	Strong Drive, Input buffer off
Initial Drive State	High (1)
<b>Input</b>	
Threshold	CMOS
Interrupt Trigger Type	None
<b>Output</b>	
Slew Rate	Fast
Drive Strength	Full
<b>Internal Connection</b>	
Analog	<unassigned>
Digital Output	<unassigned>
Digital InOut	<unassigned>
<b>Advanced</b>	
Store Config in Flash	<input checked="" type="checkbox"/>

Figure 11. P1[1] (RGB\_GREEN) Resource Parameter Settings

The screenshot displays the PSoC Designer interface for configuring the P1[1] (RGB\_GREEN) resource. On the left, the Resource list shows Port 1 pins P1[0] through P1[5], with P1[1] selected and its personality set to RGB\_GREEN. The central pin grid shows the physical layout of pins P1.0 through P1.5, with P1.1 highlighted in orange. The right-hand pane, titled 'P1[1] (RGB\_GREEN) - Parameters', contains the following settings:

Name	Value
<b>Peripheral Documentation</b>	
Configuration Help	<a href="#">Open GPIO Documentation</a>
<b>General</b>	
Drive Mode	Strong Drive, Input buffer off
Initial Drive State	High (1)
<b>Input</b>	
Threshold	CMOS
Interrupt Trigger Type	None
<b>Output</b>	
Slew Rate	Fast
Drive Strength	Full
<b>Internal Connection</b>	
Analog	<unassigned>
Digital Input	<unassigned>
Digital Output	<unassigned>
Digital InOut	<unassigned>
<b>Advanced</b>	
Store Config in Flash	<input checked="" type="checkbox"/>

Figure 12 and Figure 13 show the 75-MHz SPI clock (CLK\_HF2) setting. Cypress Excelon ultra QSPI F-RAM can operate up to 108 MHz (max) in all the three (SPI, DPI, and QPI) modes.

Figure 12. CLK\_HF2 Resource Parameter Settings – PLL Frequency

Name	Value
Peripheral Documentation	Open PLL Documentation
Configuration Help	Open PLL Documentation
General	
Source Frequency	8 MHz ± 1%
Low Frequency Mode	<input type="checkbox"/>
Configuration	Automatic
Desired Frequency (MHz)	150,000
Optimization	Min Power
Feedback (22-112)	75
Reference (1-18)	2
Output (2-16)	2
Actual Frequency	150 MHz ± 1%

Figure 13. CLK\_HF2 Resource Parameter Settings – Source Clock and Divider

Name	Value
Peripheral Documentation	Open High-Frequency Clocks Documentation
Configuration Help	Open High-Frequency Clocks Documentation
General	
Source Clock	CLK_PATH1
Source Frequency	150 MHz ± 1%
Divider	2
Frequency	75 MHz ± 1%
Clock Output	Quad Serial Memory Interface (QSPI) 0 clock (KIT_FRAM) [UNUSED]

**Note:** The PLL frequency change from its default (144-MHz) may impact the clock for other peripherals and generate clock constrain errors while applying changes through the Peripheral Clocks tab. In that case, clock constrain should be fixed either by changing the **Connections > Clock** option (*8 bit Divider 0 clk, 8 bit Divider 1 clk, ... 16 bit Divider clk 0, ... etc.*) available under the Clock setting of respective peripheral (through **Peripherals** tab of *design.modus*) or adjusting the selected clock *Divider* value through **Peripheral-Clocks** tab of *design.modus*. Errors related to any clock constrain are issued while saving the Device Configurator settings (**File > Save**).

## Reusing This Example

This code example is designed for the CY8CKIT-062-WiFi-BT Pioneer Kit. To use the design on a different PSoC 6 MCU kit, import the application for that kit; see [KBA225201](#). Changing to a different kit may require you to reassign pins. [Table 3](#) lists the target PSoC 6 MCU kits with PSoC 6 MCU manufacturing part no on it.

Table 3. PSoC 6 MCU Kits to PSoC 6 Device Used

PSoC 6 MCU Kit Name	PSoC 6 MCU Device Used
CY8CKIT-062-4343W	CY8C624ABZI-D44
CY8CKIT-062-WiFi-BT	CY8C6247BZI-D54
CY8CKIT-062-BLE	CY8C6347BZI-BLD53
CY8CMOD-062-4343W	CY8C624ABZI-D44
CY8CPROTO-062-4343W	CY8C624ABZI-D44

In some cases, a resource used by a code example (for example, a peripheral) is not supported on another device. In that case, the example will not work. If you build the code targeted at such a device, you will get errors. See the device datasheet for information on specific resource the device supports.

## Related Documents

For a comprehensive list of PSoC 6 MCU resources, see [KBA223067](#) in the Cypress community.

Application Notes	
<a href="#">AN218375</a> - Designing with Cypress Quad SPI (QSPI) F-RAM	Provides functional details, timing, and example code for SPI F-RAMs.
<a href="#">AN221774</a> – Getting Started with PSoC 6 MCU	Describes PSoC 6 MCU devices and how to build your first ModusToolbox application and PSoC Creator project.
<a href="#">AN215656</a> – PSoC 6 MCU: Dual-CPU System Design	Describes the dual-CPU architecture in PSoC 6 MCU and shows how to build a simple dual-CPU design.
Code Examples	
<a href="#">CE220823</a> - PSoC 6 MCU SMIF Memory Write and Read Operation	Demonstrates interfacing with an external NOR flash memory in QSPI mode using the SMIF block in PSoC 6 MCU.
Visit the <a href="#">Cypress GitHub site</a> for a comprehensive collection of code examples using ModusToolbox IDE	
Device Documentation	
<a href="#">PSoC 6 MCU Datasheets</a>	PSoC 61, PSoC 62, PSoC 63 MCU Datasheets
<a href="#">Excelon Ultra 4-Mbit QSPI F-RAM Datasheet</a>	1.8-3.6 V (3.0 V typ.), 108 MHz, 4Mb QSPI F-RAM datasheet
Development Kit Documentation	
<a href="#">CY8CKIT-062-BLE PSoC 6 BLE Pioneer Kit</a>	
<a href="#">CY8CKIT-062-WiFi-BT PSoC 6 WiFi-BT Pioneer Kit</a>	
<a href="#">CY8CPROTO-062-4343W PSoC 6 Wi-Fi BT Prototyping Kit</a>	
<a href="#">CY15FRAMKIT-002 Development Kit</a>	
Tool Documentation	
<a href="#">ModusToolbox</a>	The Cypress IDE for IoT designers

## Document History

Document Title: CE222967 – Excelon-Ultra QSPI F-RAM Access Using PSoC 6 MCU SMIF

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Revision	ECN	Submission Date	Description of Change
**	6667793	09/05/2019	New Code Example

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