

16-Mbit (1M words × 16 bit) Static RAM with Error-Correcting Code (ECC)

Features

- High speed
 - $t_{AA} = 10$ ns
- Temperature range
 - Military: -55°C to 125°C
- Embedded error-correcting code (ECC) for single-bit error correction
- Low active and standby currents
 - $I_{CC} = 90$ -mA typical at 100 MHz
 - $I_{SB2} = 20$ -mA typical
- Operating voltage range: 2.2 V to 3.6 V
- 1.0-V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Available in Pb-free / Leaded Sn/Pb 48-ball VFBGA

Functional Description

CY7C1061G^[1] is a high-performance CMOS fast static RAM part with embedded ECC. ECC logic can detect and correct single-bit error in read data word during read cycles.

This device has single chip enable input and is accessed by asserting the chip enable input (CE) LOW.

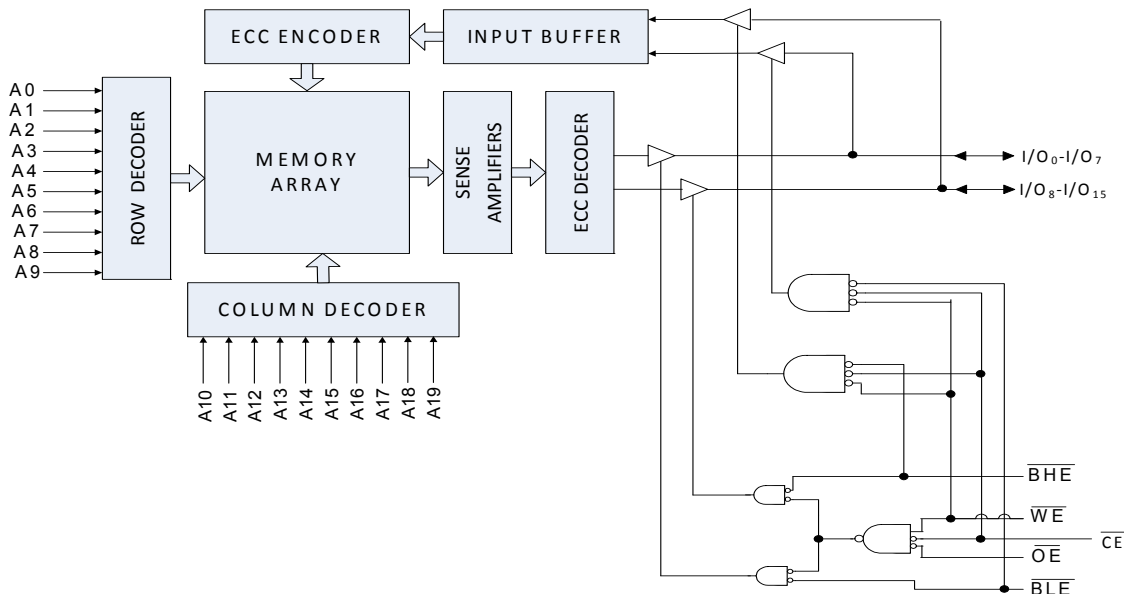
To perform data writes, assert the Write Enable (\overline{WE}) input LOW and provide the data and address on the device data pins (I/O_0 through I/O_{15}) and address pins (A_0 through A_{19}) respectively. The Byte High Enable (\overline{BHE}) and Byte Low Enable (\overline{BLE}), inputs control byte writes and write data on the corresponding I/O lines to the memory location specified. \overline{BHE} controls I/O_8 through I/O_{15} and \overline{BLE} controls I/O_0 through I/O_7 .

To perform data reads, assert the Output Enable (\overline{OE}) input and provide the required address on the address lines. Read data is accessible on I/O lines (I/O_0 through I/O_{15}). You can perform byte accesses by asserting the required byte enable signal (\overline{BHE} or \overline{BLE}) to read either the upper byte or the lower byte of data from the specified address location.

All I/O s (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), or control signals are de-asserted (\overline{OE} , \overline{BLE} , \overline{BHE}). Refer to the below logic block diagram.

The CY7C1061G military device is available in 48-ball VFBGA packages.

Logic Block Diagram – CY7C1061G



Note

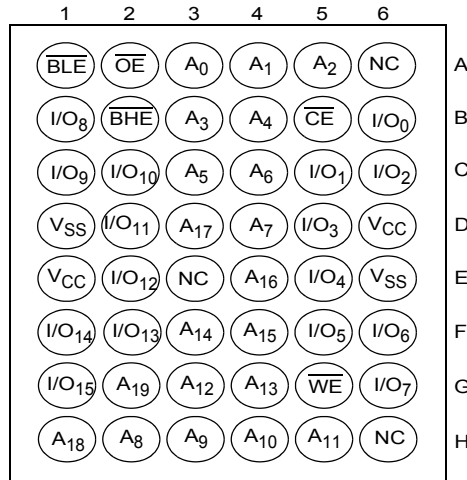
1. The device does not support automatic write-back on error detection.

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Pin Configurations

Figure 1. 48-ball VFBGA (6 × 8 × 1.0 mm) pinout [2]



Product Portfolio

Product	Range	V _{CC} Range (V)	Speed (ns)	Current Consumption			
				Operating I _{CC} (mA)		Standby, I _{SB2} (mA)	
				f = f _{max}			
				Typ [3]	Max	Typ [3]	Max
CY7C1061G30	Military	2.2 V–3.6 V	10	90	160	20	50

Notes

- 2. NC pins are not connected internally to the die.
- 3. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature	-65 °C to +150 °C
Case temperature with power applied	-55 °C to +125 °C
Supply voltage on V _{CC} relative to GND	-0.5 V to +6.0 V
DC voltage applied to outputs in High-Z State ^[4]	-0.5 V to V _{CC} + 0.5 V

DC input voltage ^[4]	-0.5 V to V _{CC} + 0.5 V
Current into outputs (LOW)	20 mA
Static discharge voltage (MIL-STD-883, Method 3015)	> 2001 V
Latch-up current	> 140 mA

Operating Range

Grade	Ambient Temperature	V _{CC}
Military	-55 °C to +125 °C	2.2 V to 3.6 V

DC Electrical Characteristics

Over the operating range of -40 °C to 125 °C

Parameter	Description	Test Conditions	10 ns			Unit		
			Min	Typ ^[5]	Max			
V _{OH}	Output HIGH voltage	2.2 V to 2.7 V	V _{CC} = Min, I _{OH} = -1.0 mA		2.0	-	-	V
		2.7 V to 3.0 V	V _{CC} = Min, I _{OH} = -4.0 mA		2.2	-	-	
		3.0 V to 3.6 V	V _{CC} = Min, I _{OH} = -4.0 mA		2.4	-	-	
V _{OL}	Output LOW voltage	2.2 V to 2.7 V	V _{CC} = Min, I _{OL} = 2 mA		-	-	-	V
		2.7 V to 3.6 V	V _{CC} = Min, I _{OL} = 8 mA		-	-	0.4	
V _{IH} ^[4]	Input HIGH voltage	2.2 V to 2.7 V	-	-	2.0	-	V _{CC} + 0.3	V
		2.7 V to 3.6 V	-	-	2.0	-	V _{CC} + 0.3	
V _{IL} ^[4]	Input LOW voltage	2.2 V to 2.7 V	-	-	-0.3	-	0.6	V
		2.7 V to 3.6 V	-	-	-0.3	-	0.8	
I _{IX}	Input leakage current	GND ≤ V _{IN} ≤ V _{CC}		-5.0	-	+5.0	μA	
I _{OZ}	Output leakage current	GND ≤ V _{OUT} ≤ V _{CC} , Output disabled		-5.0	-	+5.0	μA	
I _{CC}	Operating supply current	V _{CC} = Max, I _{OUT} = 0 mA, CMOS levels	f = f _{MAX} = 1/t _{RC}		-	90.0	160.0	mA
I _{SB1}	Automatic CE power down current – TTL inputs	Max V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		-	-	60.0	mA	
I _{SB2}	Automatic CE power down current – CMOS inputs	Max V _{CC} , $\overline{CE} \geq V_{CC} - 0.2$ V, V _{IN} ≥ V _{CC} - 0.2 V or V _{IN} ≤ 0.2 V, f = 0		-	20.0	50.0	mA	

Notes

- V_{IL} (min) = -2.0 V and V_{IH} (max) = V_{CC} + 2 V for pulse durations of less than 20 ns.
- Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V, T_A = 25 °C.

Capacitance

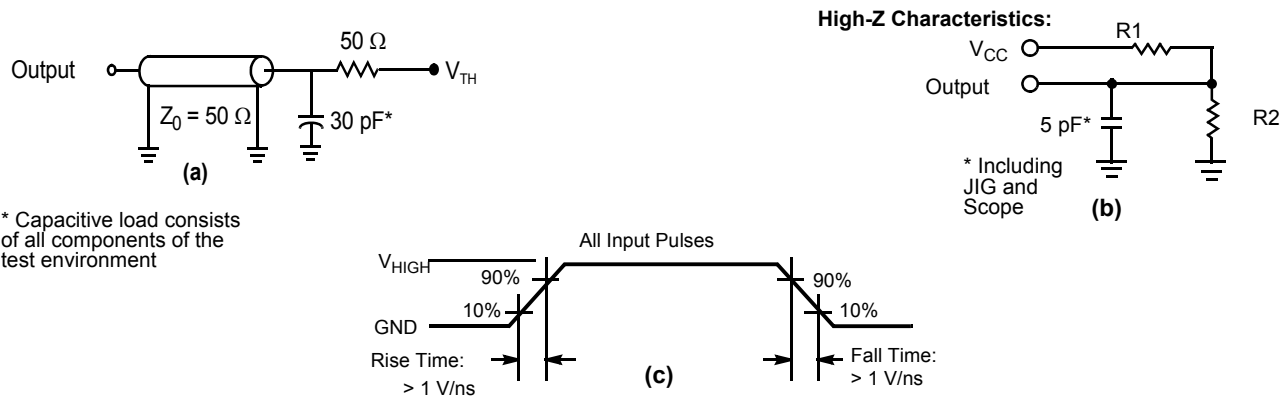
Parameter ^[6]	Description	Test Conditions	All Packages	Unit
C_{IN}	Input capacitance	$T_A = 25\text{ }^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = V_{CC}(\text{typ})$	10	pF
C_{OUT}	I/O capacitance		10	pF

Thermal Resistance

Parameter ^[6]	Description	Test Conditions	48-ball VFBGA	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3×4.5 inch, four-layer printed circuit board	31.50	$^\circ\text{C/W}$
θ_{JC}	Thermal resistance (junction to case)		15.75	$^\circ\text{C/W}$

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms ^[7]



Parameters	3.0 V	Unit
R1	317	Ω
R2	351	Ω
V_{TH}	1.5	V
V_{HIGH}	3	V

Notes

- Tested initially and after any design or process changes that may affect these parameters.
- Full-device AC operation assumes a $100\text{-}\mu\text{s}$ ramp time from 0 to $V_{CC}(\text{min})$ and $100\text{-}\mu\text{s}$ wait time after V_{CC} stabilizes to its operational value.

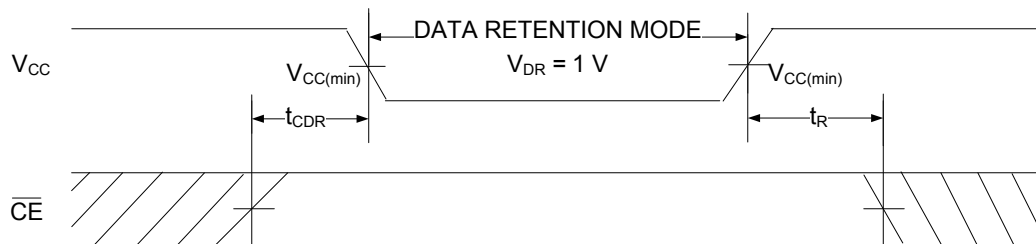
Data Retention Characteristics

Over the operating range of $-55\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention	–	1.0	–	V
I_{CCDR}	Data retention current	$V_{CC} = V_{DR}$, $\overline{CE} \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	50.0	mA
$t_{CDR}^{[8]}$	Chip deselect to data retention time	–	0	–	ns
$t_R^{[8]}$	Operation recovery time	$V_{CC} \geq 2.2\text{ V}$	10.0	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform ^[9]



Notes

- 8. Tested initially and after any design or process changes that may affect these parameters.
- 9. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)}$ $\geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(min)}$ $\geq 100\text{ }\mu\text{s}$.

AC Switching Characteristics

 Over the operating range of $-55\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$

Parameter ^[10]	Description	10 ns		Unit
		Min	Max	
Read Cycle				
t_{POWER}	V_{CC} (stable) to the first access ^[11]	100.0	–	μs
t_{RC}	Read cycle time	10.0	–	ns
t_{AA}	Address to data	–	10.0	ns
t_{OHA}	Data hold from address change	3.0	–	ns
t_{ACE}	$\overline{\text{CE}}$ LOW to data	–	10.0	ns
t_{DOE}	$\overline{\text{OE}}$ LOW to data	–	5.0	ns
t_{LZOE}	$\overline{\text{OE}}$ LOW to low-Z ^[12, 13]	0	–	ns
t_{HZOE}	$\overline{\text{OE}}$ HIGH to high-Z ^[12, 13]	–	5.0	ns
t_{LZCE}	$\overline{\text{CE}}$ LOW to low-Z ^[12, 13]	3.0	–	ns
t_{HZCE}	$\overline{\text{CE}}$ HIGH to high-Z ^[12, 13]	–	5.0	ns
t_{PU}	$\overline{\text{CE}}$ LOW to power-up ^[14]	0	–	ns
t_{PD}	$\overline{\text{CE}}$ HIGH to power-down ^[14]	–	10.0	ns
t_{DBE}	Byte enable to data valid	–	5.0	ns
t_{LZBE}	Byte enable to low-Z ^[12, 13]	0	–	ns
t_{HZBE}	Byte disable to high-Z ^[12, 13]	–	6.0	ns
Write Cycle^[15, 16]				
t_{WC}	Write cycle time	10.0	–	ns
t_{SCE}	$\overline{\text{CE}}$ LOW to write end	7.0	–	ns
t_{AW}	Address setup to write end	7.0	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{\text{WE}}$ pulse width	7.0	–	ns
t_{SD}	Data setup to write end	5.0	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{LZWE}	$\overline{\text{WE}}$ HIGH to low-Z ^[12, 13]	3.0	–	ns
t_{HZWE}	$\overline{\text{WE}}$ LOW to high-Z ^[12, 13]	–	5.0	ns
t_{BW}	Byte Enable to write end	7.0	–	ns

Notes

10. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{\text{CC}} \geq 3\text{ V}$) and $V_{\text{CC}}/2$ (for $V_{\text{CC}} < 3\text{ V}$), and input pulse levels of 0 to 3 V (for $V_{\text{CC}} \geq 3\text{ V}$) and 0 to V_{CC} (for $V_{\text{CC}} < 3\text{ V}$). Test conditions for the read cycle use the output loading shown in part (a) of Figure 2 on page 5, unless specified otherwise.
11. t_{POWER} gives the minimum amount of time that the power supply is at stable V_{CC} until the first memory access is performed.
12. t_{HZOE} , t_{HZCE} , t_{HZWE} , and t_{HZBE} are specified with a load capacitance of 5 pF, as shown in part (b) of Figure 2 on page 5. Hi-Z, Lo-Z transition is measured $\pm 200\text{ mV}$ from steady state voltage.
13. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
14. These parameters are guaranteed by design and are not tested.
15. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{\text{IL}}$, $\overline{\text{CE}} = V_{\text{IL}}$ and $\overline{\text{BHE}}$, or $\overline{\text{BLE}} = V_{\text{IL}}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
16. The minimum write pulse width for Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) should be sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 4. Read Cycle No. 1 of CY7C1061G (Address Transition Controlled) [17, 18]

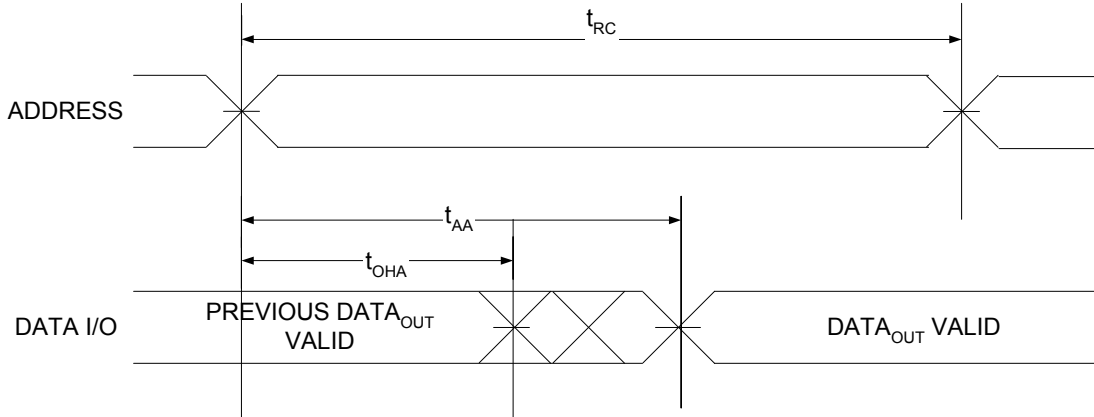
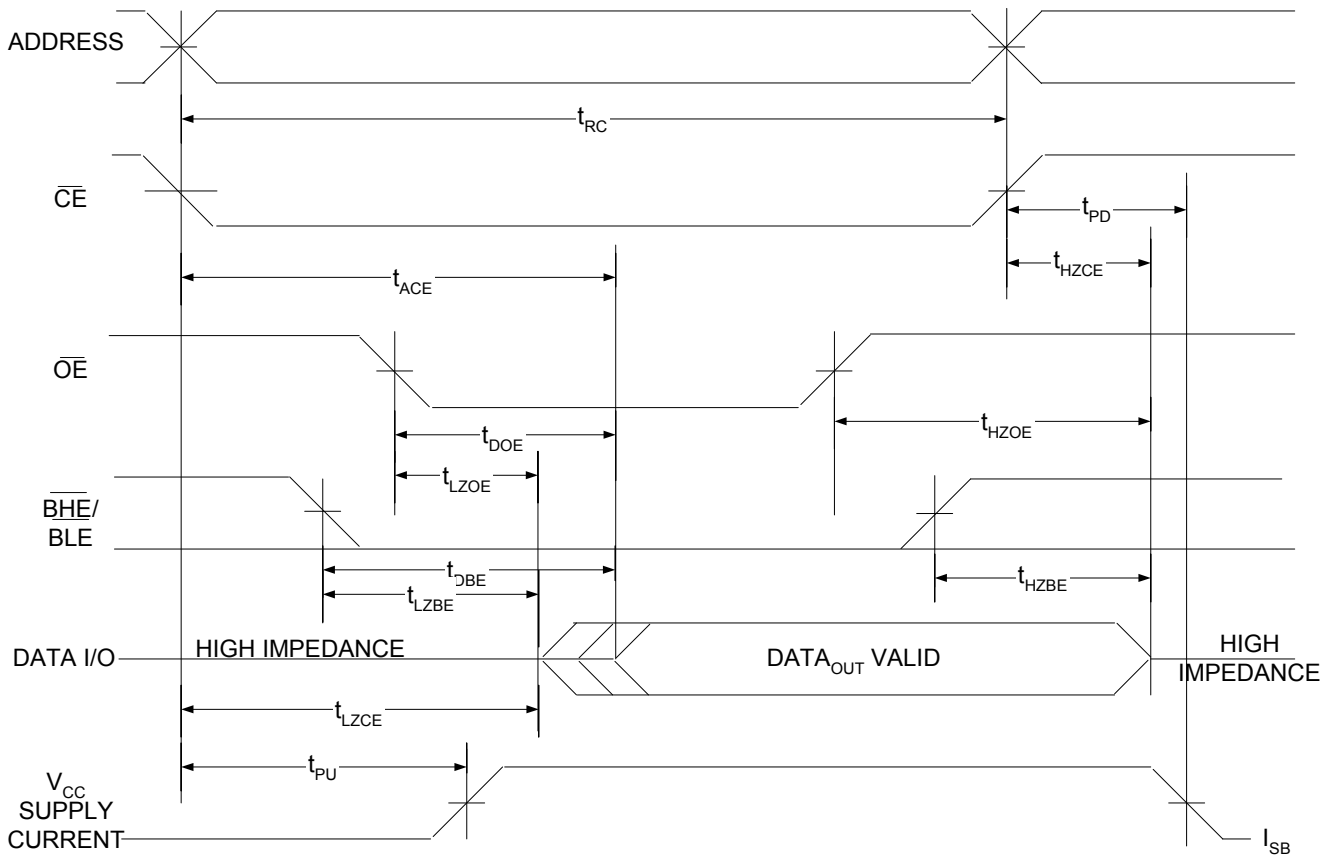


Figure 5. Read Cycle No. 2 (\overline{OE} Controlled) [18, 19]



Notes

- 17. The device is continuously selected, $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$, \overline{BHE} or \overline{BLE} or both = V_{IL} .
- 18. \overline{WE} is HIGH for read cycle.
- 19. Address valid prior to or coincident with \overline{CE} LOW transition.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [20, 21]

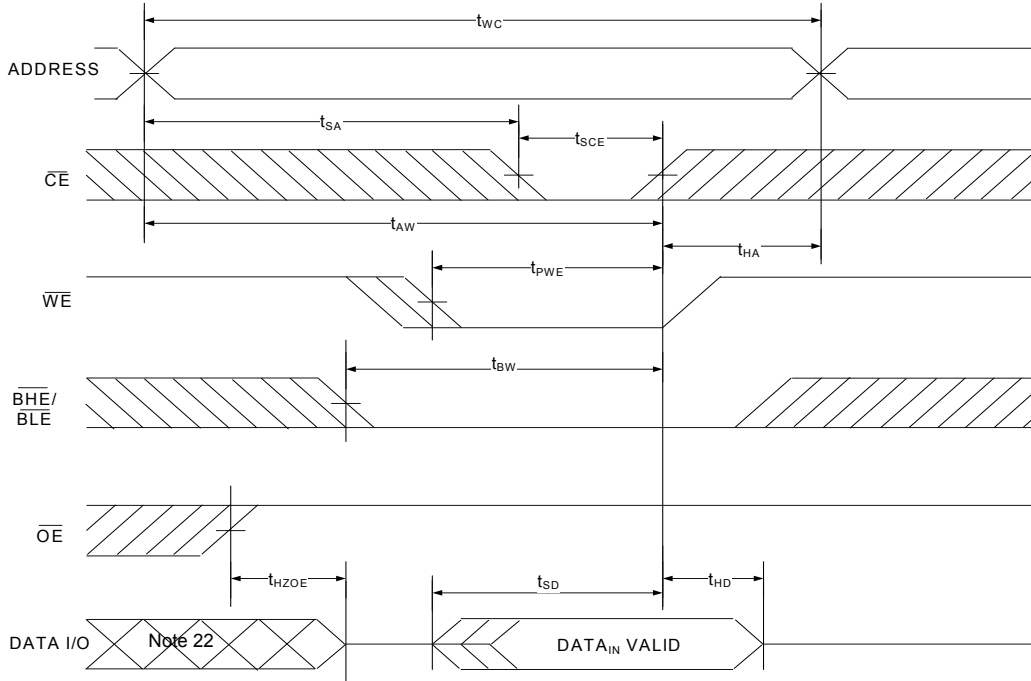
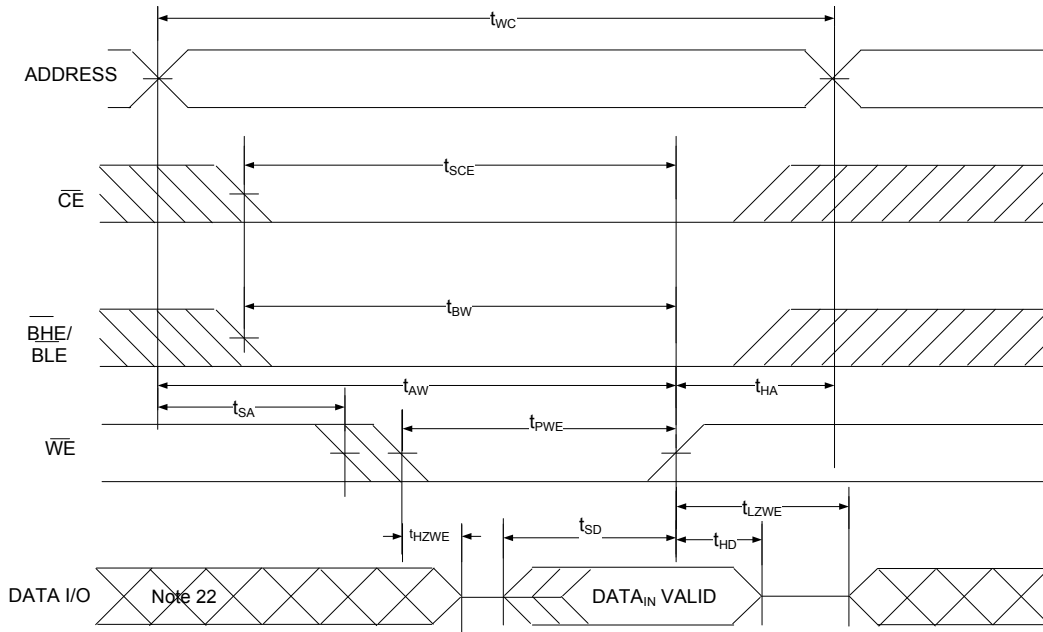


Figure 7. Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [20, 21, 23]

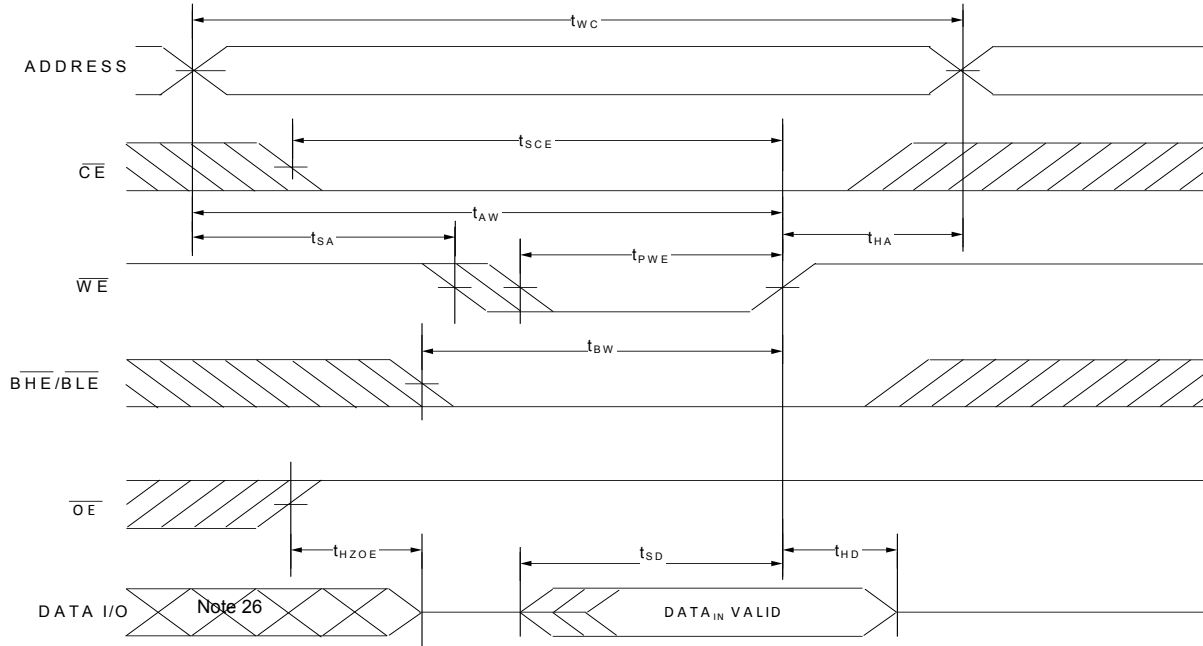


Notes

- 20. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{IL}$, $\overline{\text{CE}} = V_{IL}$, and $\overline{\text{BHE}}$ or $\overline{\text{BLE}} = V_{IL}$. These signals must be LOW to initiate a write and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 21. Data I/O is in high-impedance state if $\overline{\text{CE}} = V_{IH}$, or $\overline{\text{OE}} = V_{IH}$ or $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}} = V_{IH}$.
- 22. During this period, the I/Os are in output state. Do not apply input signals.
- 23. The minimum write pulse width for Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) should be sum of t_{HZWE} and t_{SD} .

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 (\overline{WE} Controlled) [24, 25]



Notes

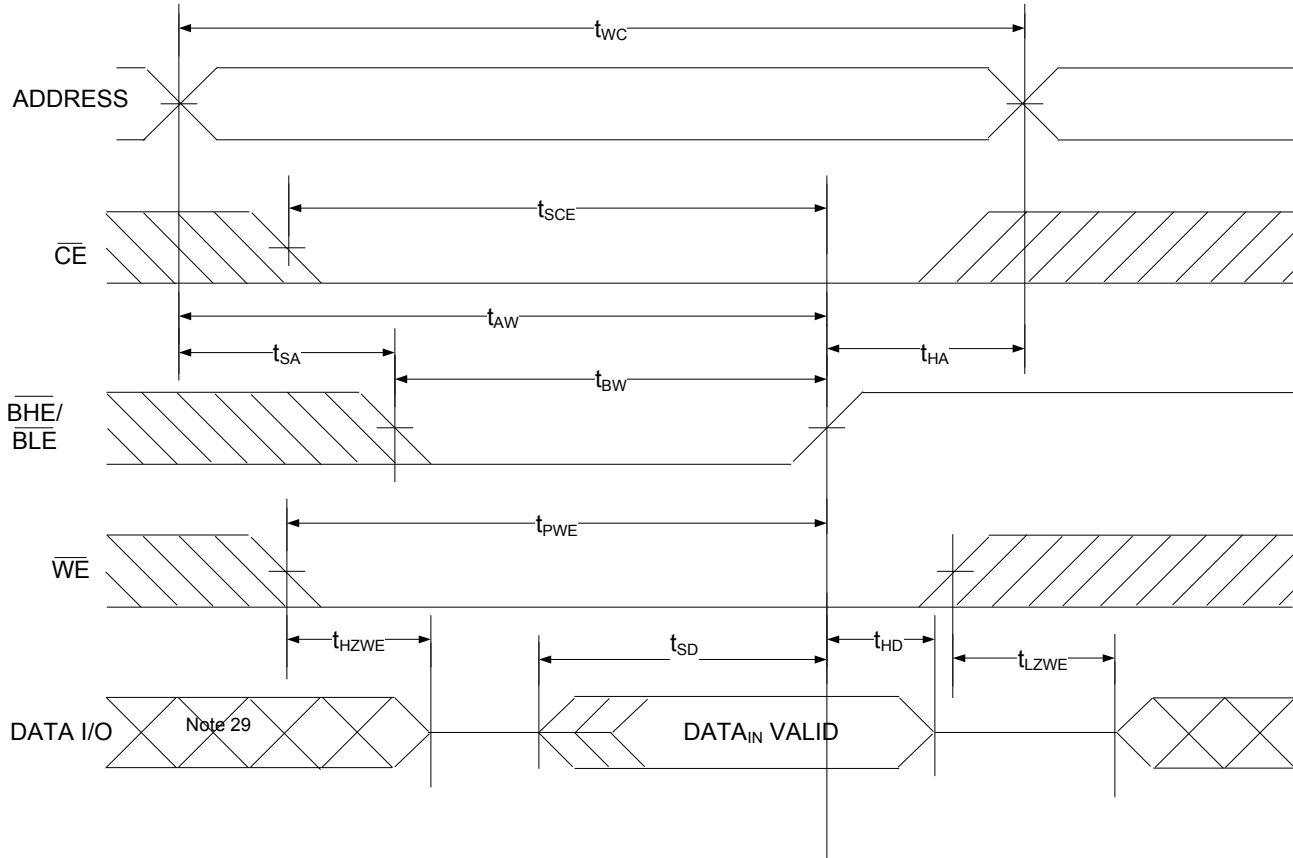
24. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$, and \overline{BHE} or $\overline{BLE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

25. Data I/O is in high impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or \overline{BHE} , and/or $\overline{BLE} = V_{IH}$.

26. During this period the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled) [27, 28]



Notes

- 27. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{IL}$, $\overline{\text{CE}} = V_{IL}$, and $\overline{\text{BHE}}$ or $\overline{\text{BLE}} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 28. Data I/O is in high-impedance state if $\overline{\text{CE}} = V_{IH}$, or $\overline{\text{OE}} = V_{IH}$ or $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}} = V_{IH}$.
- 29. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	\overline{BLE}	\overline{BHE}	I/O ₀ –I/O ₇	I/O ₈ –I/O ₁₅	Mode	Power
H	X ^[30]	X ^[30]	X ^[30]	X ^[30]	High Z	High Z	Power down	Standby (I _{SB})
L	L	H	L	L	Data out	Data out	Read all bits	Active (I _{CC})
L	L	H	L	H	Data out	High Z	Read lower bits only	Active (I _{CC})
L	L	H	H	L	High Z	Data out	Read upper bits only	Active (I _{CC})
L	X	L	L	L	Data in	Data in	Write all bits	Active (I _{CC})
L	X	L	L	H	Data in	High Z	Write lower bits only	Active (I _{CC})
L	X	L	H	L	High Z	Data in	Write upper bits only	Active (I _{CC})
L	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I _{CC})
L	X	X	H	H	High Z	High Z	Selected, outputs disabled	Active (I _{CC})

Note

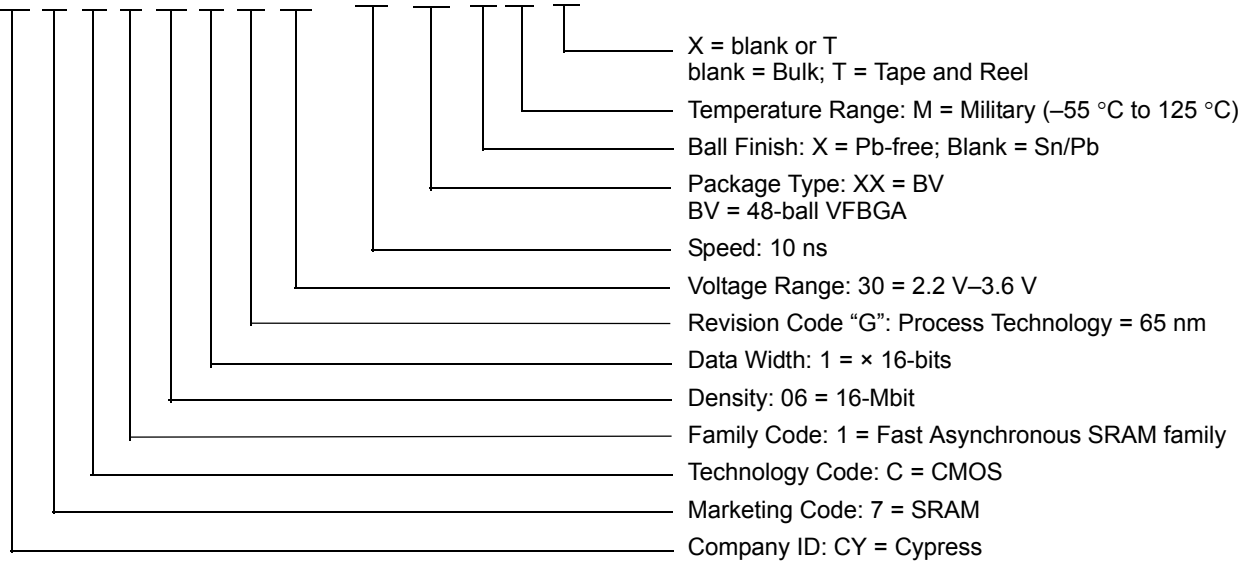
³⁰. The input voltage levels on these pins should be either at V_{IH} or V_{IL}.

Ordering Information

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (all Pb-free)	Operating Range
10	2.2 V–3.6 V	CY7C1061G30-10BVM	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm)	Military
		CY7C1061G30-10BVXM			

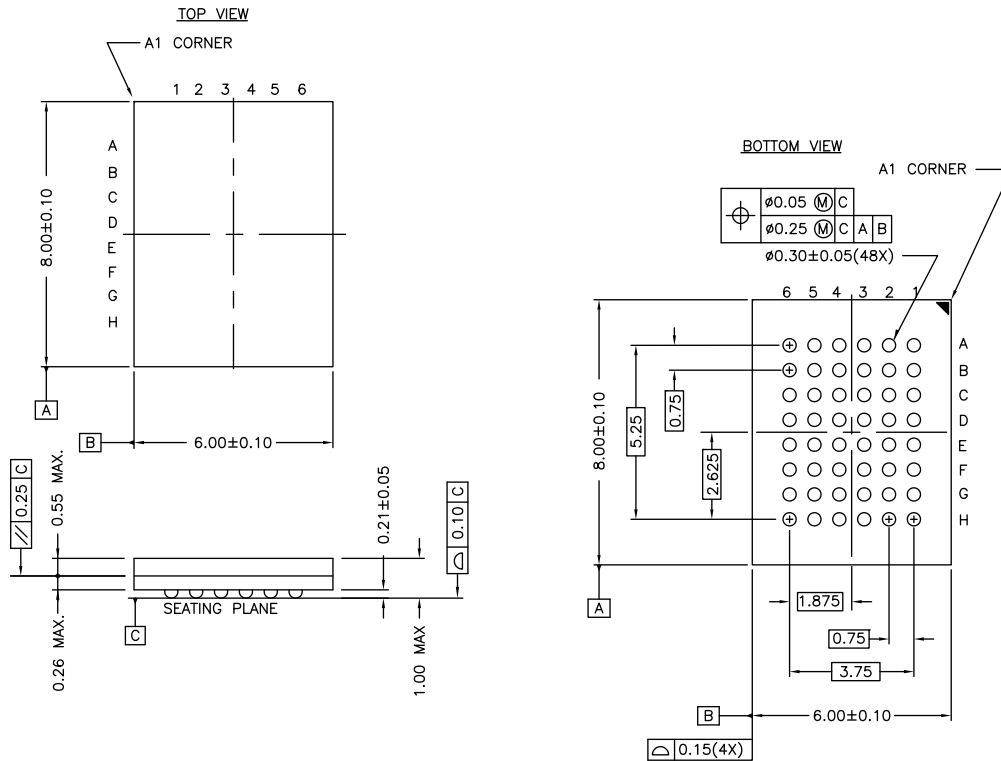
Ordering Code Definitions

CY 7 C 1 06 1 G XX - 10 BV X M X



Package Diagrams

Figure 10. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:
 PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD)
 posted on the Cypress web.

51-85150 *H

Acronyms

Table 1. Acronyms Used in this Document

Acronym	Description
BHE	Byte High Enable
BLE	Byte Low Enable
CE	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
OE	Output Enable
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
VFBGA	Very Fine-Pitch Ball Grid Array
WE	Write Enable

Document Conventions

Units of Measure

Table 2. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1061G Military, 16-Mbit (1M words × 16 bit) Static RAM with Error-Correcting Code (ECC)				
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**	5652941	VINI	03/07/2017	New data sheet.

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