PSoC 64 Secure Boot MCU

General Description

PSoC® 6 MCU is a high-performance, ultra-low-power and secure MCU platform, purpose-built for IoT applications. The PSoC 64 Secure Boot MCU line, based on the PSoC 6 MCU platform, features out-of-box security functionality, providing an isolated root-of-trust with true attestation and provisioning services. In addition, it delivers a pre-configured secure execution environment which supports system software for various IoT platforms; and enables TLS authentication, secure storage, and secure firmware management. PSoC 64 also includes a rich execution environment for application development, with RTOS support that communicates with the secure execution environment.

Features

32-bit Dual CPU Subsystem

Note: In PSoC 64 the Cortex M0+ is reserved for system functions, and is not available for applications.

- 150-MHz Arm® Cortex®-M4F (CM4) CPU with single-cycle multiply (Floating Point and Memory Protection Unit)
- 100-MHz Cortex-M0+ (CM0+) CPU with single-cycle multiply and MPU
- User-selectable core logic operation at either 1.1 V or 0.9 V
- Active CPU power slope with 1.1-V core operation
  - Cortex-M4: 40 µA/MHz
  - Cortex-M0+: 20 µA/MHz
- Active CPU power slope with 0.9-V core operation
  - Cortex-M4: 22 µA/MHz
  - Cortex-M0+: 15 µA/MHz
- Three DMA controllers

Memory Subsystem

- 448-KB application flash, 32-KB auxiliary flash (AUXflash), and 32-KB supervisory flash (Sflash); read-while-write (RWW) support. Two 8-KB flash caches, one for each CPU.
- 152-KB SRAM with programmable power control and retention granularity
- One-time-programmable (OTP) 1-Kb eFuse array

Hardware-Based Root-of-Trust (RoT)

- RoT based on immutable boot-up code, Flash content hash, and Cypress public key that ensures firmware integrity prior to provisioning
- Supports trusted RoT handover to maintain chain of trust and establish OEM trust anchor for secure boot
- Device generates a unique device ID and a device secret key during the provisioning process, which can be used for attestation and signing

Immutable Secure Boot Support

- Flexible chain of trust can use different signatures for different images
- ECC-based image signature validation

Cypress Secure Bootloader

- Open Source MCUBoot[1] based bootloader optimized for the PSoC 64 family
- Pre-built bootloader binary capable of validating, launching and updating signed user application images
- Tightly integrated with provisioned debug and boot policies to inherit and implement security policies

Low-Power 1.7-V to 3.6-V Operation

- Six power modes for fine-grained power management
- Deep Sleep mode current of 7 µA with 64-KB SRAM retention
- On-chip DC-DC Buck converter, <1 µA quiescent current
- Backup domain with 64 bytes of memory and Real-Time Clock

Flexible Clocking Options

- On-chip crystal oscillators (4 to 35 MHz, and 32 kHz)
- Phase-locked Loop (PLL) for multiplying clock frequencies
- 8 MHz Internal Main Oscillator (IMO) with ±2% accuracy
- Ultra-low-power 32-kHz Internal Low-speed Oscillator (ILO)
- Frequency Locked Loop (FLL) for multiplying IMO frequency

Quad-SPI (QSPI)/Serial Memory Interface (SMIF)

- Execute-In-Place (XIP) from external Quad SPI Flash
- On-the-fly encryption and decryption
- 4-KB cache for greater XIP performance with lower power
- Supports single, dual, quad, dual-quad, and octal interfaces w/ throughput up to 640 Mbps

Segment LCD Drive

- LCD segment direct block support up to 59 segments and up to 8 commons.
- Operates in System Deep Sleep mode

Note
1. For details, refer to https://mcuboot.com/.

Serial Communication

- Seven run-time configurable serial communication blocks (SCBs)
  - Six SCBs: configurable as SPI, I^2C, or UARTs
  - One Deep Sleep SCB: configurable as SPI or I^2C
- USB Full-Speed device interface
- One SD Host Controller/eMMC/SD controller
- One CAN FD block

Timing and Pulse-Width Modulation

- Twelve Timer/Counter Pulse-Width Modulator (TCPWM)
- Center-aligned, Edge, and Pseudo-random modes
- Comparator-based triggering of Kill signals

Programmable Analog

- 12-bit 1-Msps SAR ADC with differential and single-ended modes and 16-channel sequencer with signal averaging
- Two low-power comparators available in Deep Sleep and Hibernate modes
- Built-in temp sensor connected to ADC

Up to 53 Programmable GPIOs

- Two Smart I/O ports (8 I/Os) enable Boolean operations on GPIO pins; available during system Deep Sleep
- Programmable drive modes, strengths, and slew rates
- Two overvoltage-tolerant (OVT) pins

Capacitive Sensing

- Cypress CapSense Sigma-Delta (CSD) provides best-in-class SNR, liquid tolerance, and proximity sensing
- Enables dynamic usage of both self and mutual sensing
- Automatic hardware tuning (SmartSense™)

Cryptography Accelerators

- Hardware acceleration for symmetric and asymmetric cryptographic methods and hash functions
- True Random Number Generator (TRNG) function

Package

- 68 QFN

Contents

Development Ecosystem

PSoC 6 MCU Resources

Cypress provides a wealth of data at www.cypress.com to help you select the right PSoC device and quickly and effectively integrate it into your design. The following is an abbreviated, hyperlinked list of resources for PSoC 6 MCU:

- **Overview**: PSoC Portfolio, PSoC Roadmap
- **Product Selectors**: PSoC 6 MCU
- **Application Notes** cover a broad range of topics, from basic to advanced level, and include the following:
  - AN221774: Getting Started with PSoC 6 MCU
  - AN218241: PSoC 6 MCU Hardware Design Guide
  - AN213924: PSoC 6 MCU Device Firmware Update Guide
  - AN215656: PSoC 6 MCU Dual-CPU System Design
  - AN219528: PSoC 6 MCU Power Reduction Techniques
  - AN85951: PSoC 4, PSoC 6 MCU CapSense Design Guide
- **Code Examples** demonstrate product features and usage, and are also available on Cypress GitHub repositories.
- **Technical Reference Manuals (TRMs)** provide detailed descriptions of PSoC 6 MCU architecture and registers.
- PSoC 6 MCU Programming Specification provides the information necessary to program PSoC 6 MCU nonvolatile memory
- Development Tools
  - ModusToolbox™ enables cross platform code development with a robust suite of tools and software libraries
  - CY8CPROTO-064B0S3 PSoC 64 Secure Boot Prototyping Kit: a low-cost hardware platform that enables design and debug of the PSoC 64 CYB06445LQI-S3D42 product line.
  - PSoC 6 CAD libraries provide footprint and schematic support for common tools. BSDL files are also available.
- **Training Videos** are available on a wide range of topics including the PSoC 6 MCU 101 series
- **Cypress Developer Community** enables connection with fellow PSoC developers around the world, 24 hours a day, 7 days a week, and hosts a dedicated PSoC 6 MCU Community

ModusToolbox™ IDE and the PSoC 6 SDK

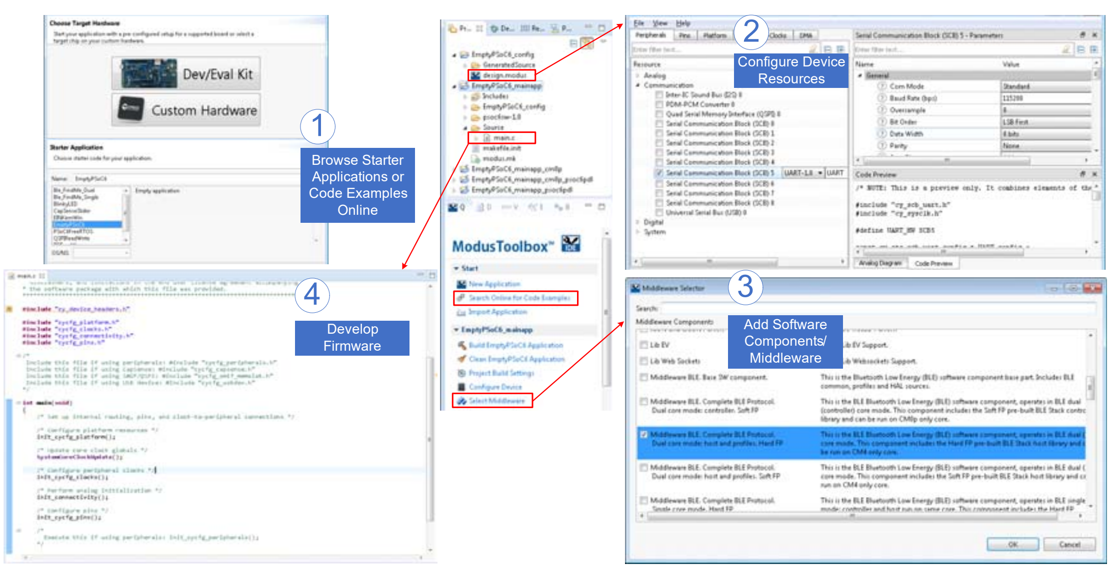
ModusToolbox is an Eclipse-based development environment on Windows, macOS, and Linux platforms that includes the ModusToolbox IDE and the PSoC 6 SDK. The ModusToolbox IDE brings together several device resources, middleware, and firmware to build an application. Using ModusToolbox, you can enable and configure device resources and middleware libraries, write `C/C++/assembly` source code, and program and debug the device.

The PSoC 6 SDK is the software development kit for the PSoC 6 MCU. The SDK makes it easier to develop firmware for supported devices without the need to understand the intricacies of the device resources.

For additional detail on using the Cypress tools, refer to AN221774: Getting Started with PSoC 6 MCU and the documentation and help integrated into ModusToolbox. As Figure 1 shows, with the ModusToolbox IDE, you can:

1. Create a new application based on a list of starter applications, filtered by kit or device, or browse the collection of code examples online.
2. Configure device resources in *design.modus* to build your hardware system design in the workspace.
3. Add software components or middleware.
4. Develop your application firmware.

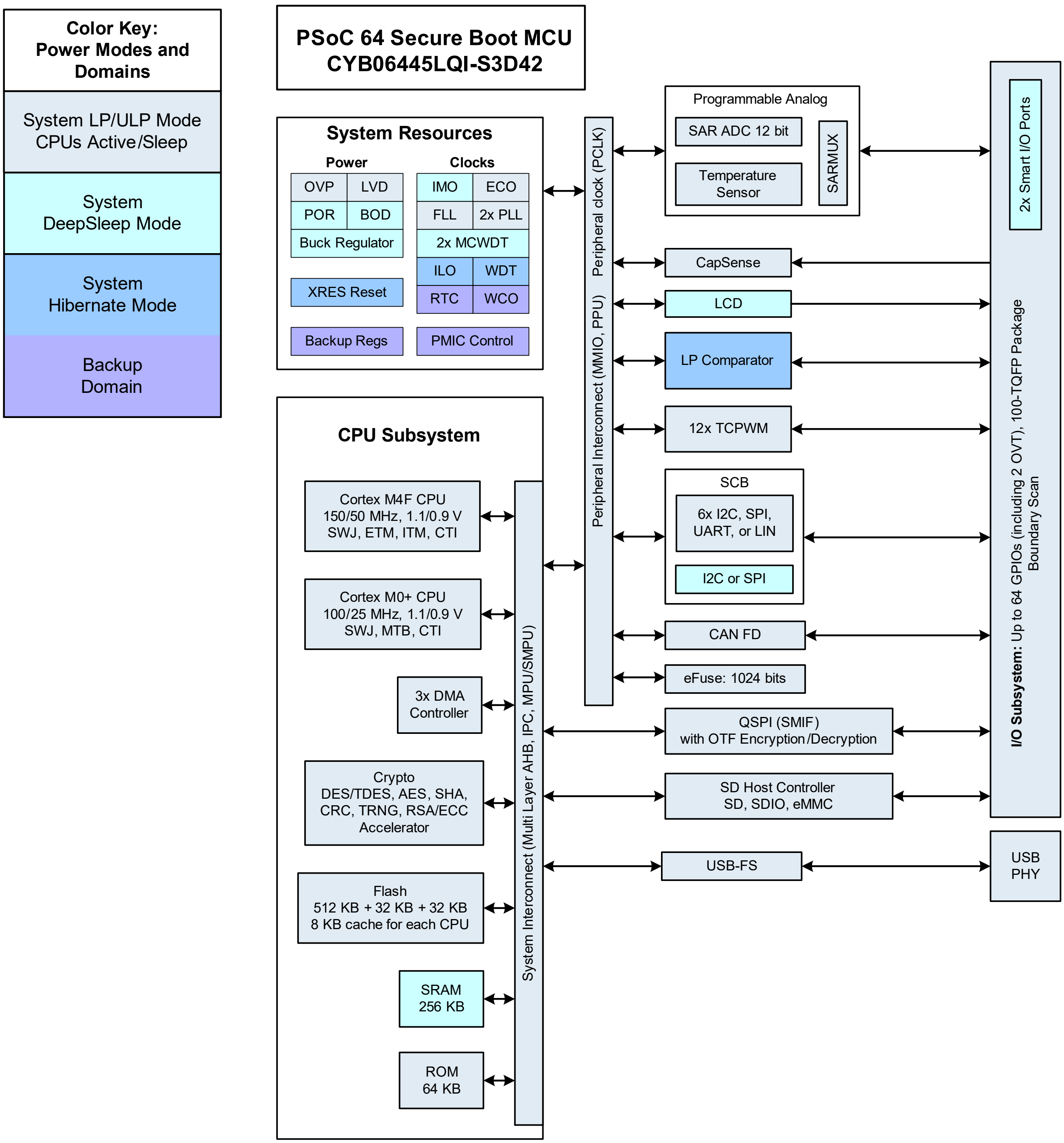
Figure 1. ModusToolbox IDE Resources and Middleware



Blocks and Functionality

Figure 2 shows the major subsystems and a simplified view of their interconnections. The color coding shows the lowest power mode where the particular block is still functional (for example, the Opamps are functional down to DeepSleep mode).

Figure 2. Block Diagram



This product line has up to 512 KB of flash; however 64 KB is reserved for system usage, leaving 448 KB for applications. It also has up to 256 KB of SRAM; however 104 KB is reserved for system usage, leaving 152 KB for applications.

The PSoC 64 devices offer an immutable, RoT-based boot-up process, which allows only signed applications to be booted up. In addition, secure user assets such as keys and debug policies can be securely provisioned on the device in an HSM environment and made immutable The PSoC 64 line of Secure MCUs also allow for secure Root-of-Trust based cryptography services which can be accessed using System calls.

There are three debug access ports, one each for CM4 and CM0+, and a system port. All debug and test interfaces can be permanently disabled during final production provisioning to avoid any malicious reprogramming or reading of flash and register contents.

The PSoC 6 devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware. All device interfaces can be permanently disabled (device security) for applications concerned about attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. The security level is settable by the user.

Complete debug-on-chip functionality enables full device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The ModusToolbox Integrated Development Environment (IDE) provides fully integrated programming and debug support for these devices. The SWJ (SWD and JTAG) interface is fully compatible with industry-standard third party probes. With the ability to disable debug features, with very robust flash protection, and by allowing customer-proprietary functionality to be implemented in on-chip programmable blocks, PSoC 6 provides a very high level of security.

Functional Description

The following sections provide an overview of the features, capabilities and operation of each functional block identified in the block diagram in Figure 2. For more detailed information, refer to the following three references.

- Peripheral Driver Library (PDL) Application Programming Interface (API) Reference Manual.

  PDL provides low-level drivers for each resource in the device, and supports the entire PSoC 6 MCU portfolio. PDL is an element of the PSoC 6 SDK, which is installed as part of ModusToolbox. With ModusToolbox installed, you can access the PDL API reference manual either from the Documentation tab of the Quick Panel, or you can navigate directly to it at *<install_directory>\ModusToolbox_<version>\libraries\psoc6sw-<version>\docs*. Using PDL should be the primary means of interacting with the PSoC 6 MCU hardware.

- Architecture Technical Reference Manual (TRM)

  The architecture TRM provides the detailed description of each resource in the device. This is the next reference to use if it is necessary to understand the operation of the hardware below the software provided by PDL. It describes the architecture and functionality of each resource and explains the operation of each resource in all modes. It provides specific guidance regarding the use of associated registers.

- Register Technical Reference Manual

  The register TRM provides the complete list of all registers in the device. It includes the breakdown of all register fields, their possible settings, read/write accessibility, and default states. All registers that have a reasonable use in typical applications have functions to access them from within PDL. Note that ModusToolbox and PDL may provide software default conditions for some registers that are different from and override the hardware defaults.

CPU and Memory Subsystem

PSoC 6 has multiple bus masters, as Figure 2 shows. They are: CPUs, DMA controllers, SD Host controllers, and a Crypto block. Generally, all memory and peripherals can be accessed and shared by all bus masters through multi-layer Arm AMBA high-performance bus (AHB) arbitration. Accesses between Cores can be synchronized using an inter-processor communication (IPC) block.

CPUs

There are two Arm Cortex CPUs:

The Cortex-M4 (CM4) has single-cycle multiply, a floating-point unit (FPU), and a memory protection unit (MPU). It can run at up to 150 MHz. This is the main CPU, designed for a short interrupt response time, high code density, and high throughput.

CM4 implements a version of the Thumb instruction set based on Thumb-2 technology (defined in the *Armv7-M Architecture Reference Manual*).

The Cortex-M0+ (CM0+) has single-cycle multiply, and an MPU. It can run at up to 100 MHz; however, for CM4 speeds above 100 MHz, CM0+ and bus peripherals are limited to half the speed of CM4. Thus, for CM4 running at 150 MHz, CM0+ and peripherals are limited to 75 MHz.

CM0+ is the secondary CPU; it is used to implement system calls and device-level security, safety, and protection features. CM0+ provides a secure, uninterruptible boot function. This guarantees that post boot, system integrity is checked and memory and peripheral access privileges are enforced.

CM0+ implements the Armv6-M Thumb instruction set (defined in the *Armv6-M Architecture Reference Manual*).

The CPUs have the following power draw, at V_{DD} = 3.3 V and using the internal buck regulator:

Table 1. Active Current Slope at V_{DD} = 3.3 V Using the Internal Buck Regulator

		System Power Mode	
		ULP	LP
CPU	Cortex-M0+	15 µA/MHz	20 µA/MHz
	Cortex-M4	22 µA/MHz	40 µA/MHz

The CPUs can be selectively placed in their Sleep and Deep Sleep power modes as defined by Arm.

Both CPUs have nested vectored interrupt controllers (NVIC) for rapid and deterministic interrupt response, and wakeup interrupt controllers (WIC) for CPU wakeup from Deep Sleep power mode.

The CPUs have extensive debug support. PSoC 6 has a debug access port (DAP) that acts as the interface for device programming and debug. An external programmer or debugger (the “host”) communicates with the DAP through the device serial wire debug (SWD) or Joint Test Action Group (JTAG) interface pins. Through the DAP (and subject to device security restrictions), the host can access the device memory and peripherals as well as the registers in both CPUs.

Each CPU offers debug and trace features as follows:

- CM4 supports six hardware breakpoints and four watchpoints, 4-bit embedded trace macrocell (ETM), serial wire viewer (SWV), and printf()-style debugging through the single wire output (SWO) pin.
- CM0+ supports four hardware breakpoints and two watchpoints, and a micro trace buffer (MTB) with 4 KB dedicated RAM.

PSoC 6 also has an Embedded Cross Trigger for synchronized debugging and tracing of both CPUs.

Interrupts

PSoC 6 has 122 system and peripheral interrupt sources and supports interrupts and system exception on both CPUs. CM4 has 122 interrupt request lines (IRQ), with the interrupt source ‘n’ directly connected to IRQn. CM0+ has eight interrupts IRQ[7:0] with configurable mapping of one or more interrupt sources to any of the IRQ[7:0]. CM0+ also supports eight internal (software only) interrupts.

Each interrupt supports configurable priority levels (eight levels for CM4 and four levels for CM0+). Up to four system interrupts can be mapped to each of the CPUs' non-maskable interrupts

(NMI). Up to 39 interrupt sources are capable of waking the device from Deep Sleep power mode using the WIC. Refer to the technical reference manual for details.

Direct Memory Access (DMA) Controllers

PSoC 64 has three DMA controllers, which support CPU-independent accesses to memory and peripherals. Two of them have 22 channels each and the third has 2 channels. The descriptors for DMA channels can be in SRAM or flash. Therefore, the number of descriptors are limited only by the size of the memory. Each descriptor can transfer data in two nested loops with configurable address increments to the source and destination. The size of data transfer per descriptor varies based on the type of DMA channel. Refer to the technical reference manual for detail.

Cryptography Accelerator (Crypto)

This subsystem consists of hardware implementation and acceleration of cryptographic functions and random number generators. The Crypto subsystem supports the following:

- Encryption/Decryption Functions
  - Data Encryption Standard (DES)
  - Triple DES (3DES)
  - Advanced Encryption Standard (AES) (128-, 192-, 256-bit)
  - Elliptic Curve Cryptography (ECC)
  - RSA cryptography functions
- Hashing functions
  - Secure Hash Algorithm (SHA)
  - SHA1
  - SHA224/256/384/512
- Message authentication functions (MAC)
  - Hashed message authentication code (HMAC)
  - Cipher-based message authentication code (CMAC)
- 32-bit cyclic redundancy code (CRC) generator
- Random number generators
  - Pseudo random number generator (PRNG)
  - True random number generator (TRNG)

Protection Units

PSoC 64 has multiple types of protection units to control erroneous or unauthorized access to memory and peripheral registers. CM4 and CM0+ have Arm MPUs for protection at the bus master level. Other bus masters use additional MPUs. Shared memory protection units (SMPUs) help implement memory protection for memory/ resources that are shared among multiple bus masters. Peripheral protection units (PPU) are similar to SMPUs but are designed for protecting the peripheral register space.

Protection units support memory and peripheral access attributes including address range, read/write, code/data, privilege level, secure/non-secure, and protection context.

Protection units are configured at secure boot to control access privileges and rights for bus masters and peripherals.

Up to eight protection contexts (secure boot is in protection context 0) allow access privileges for memory and system resources to be set by the secure boot process per protection context by bus master and code privilege level. Multiple protection contexts are supported on a single CPU.

Memory

In the PSoC 64 line of processors, the SMPUs are set up by default and cannot be modified by the user. See section 8 in the Architecture TRM for the protection context assignment.

PSoC 6 contains flash, SRAM, ROM, and eFuse memory blocks.

- Flash

  This product line has up to 512 KB of flash; however 64 KB is reserved for system usage, leaving 448 KB for applications that is organized in 256-KB sectors. There are also two 32-KB flash sectors:

  - Auxiliary flash (AUXflash), typically used for EEPROM emulation
  - Supervisory flash (Sflash). Data stored in Sflash includes device trim values, Flash Boot code, and encryption keys. After the device transitions into the Secure lifecycle stage, Sflash can no longer be changed.

  The flash uses 128-bit-wide accesses to reduce power. Write operations can be performed at the row level. A row is 512 bytes. Read operations are supported in both System Low Power and Ultra-Low Power modes, however write operations may not be performed in System Ultra-Low Power mode.

  The flash controller has two caches, one for each CPU. Each cache is 8 KB, with 4-way set associativity.

- SRAM

  It also has up to 256 KB of SRAM; however, 104 KB is reserved for system usage, leaving 152 KB for applications. Power control and retention granularity is implemented in 32 KB blocks allowing the user to control the amount of memory retained in Deep Sleep. Memory is not retained in Hibernate mode.

- ROM

  The 64-KB ROM, also referred to as the supervisory ROM (SROM), provides code (ROM Boot) for several system functions. The PSoC 6 MCU ROM contains device initialization, flash write, security, eFuse programming, and other system-level routines. ROM code is executed only by the CM0+ CPU, in protection context 0. A system function can be initiated by either CPU, or through the DAP. This causes an NMI in CM0+, which causes CM0+ to execute the system function.

- eFuse

  A one-time-programmable (OTP) eFuse array consists of 1024 bits, of which 512 are reserved for system use, such as die ID, device ID, initial trim settings, device life cycle, and security settings. The remaining bits are available for storing security key information, hash values, unique IDs or similar custom content.

  Each fuse is individually programmed; once programmed (or “blown”), its state cannot be changed. Blowing a fuse transitions it from the default state of 0 to 1. To program an eFuse, V_{DDIO0} must be at 2.5 V ±5%, at 14 mA.

  Because blowing an eFuse is an irreversible process, programming is recommended only in mass production programming under controlled factory conditions. For more information, see PSoC 6 MCU Programming Specifications.

Boot Code

Two blocks of code, ROM Boot and Flash Boot, are pre-programmed into the device and work together to provide device startup and configuration, basic security features, life-cycle stage management and other system functions.

- ROM Boot

  On a device reset, the boot code in ROM is the first code to execute. This code performs the following:
  - Integrity checks of flash boot code
  - Device trim setting (calibration)
  - Setting the device protection units
  - Setting device access restrictions for secure life-cycle states

  ROM cannot be changed and acts as the Root of Trust in a secure system.

- Flash Boot

  Flash boot is firmware stored in SFlash that ensures that only a validated application may run on the device. It also ensures that the firmware image has not been modified, such as by a malicious third party.

  Flash boot:
  - Is validated by ROM Boot
  - Runs after ROM Boot and before the user application
  - Verifies the integrity of the user application
  - Enables system calls
  - Configures the Debug Access Port
  - Launches the user application in the CM0+ (CM4 for single-CPU devices).

  If the user application cannot be validated, then flash boot ensures that the device is transitioned into a safe state.

Memory Map

Both CPUs have a fixed address map, with shared access to memory and peripherals. The 32-bit (4 GB) address space is divided into the regions shown in Table 2. Note that code can be executed from the code and SRAM regions.

Table 2. Address Map for CM4 and CM0+

Address Range	Name	Use
0x0000 0000 – 0x1FFF FFFF	Code	Program code region. Data can also be placed here. It includes the exception vector table, which starts at address 0.
0x2000 0000 – 0x3FFF FFFF	SRAM	This region is not supported in PSoC 6.
0x4000 0000 – 0x5FFF FFFF	Peripheral	All peripheral registers. Code cannot be executed from this region. CM4 bit-band in this region is not supported in PSoC 6.
0x6000 0000 – 0x9FFF FFFF	External RAM	SMIF or Quad SPI, (see the Quad-SPI (QSPI)/Serial Memory Interface (SMIF) section). Code can be executed from this region.
0xA000 0000 – 0xDFFF FFFF	External Device	Not used.
0xE000 0000 – 0xE00F FFFF	Private Peripheral Bus	Provides access to peripheral registers within the CPU core.
0xE010 0A000 – 0xFFFF FFFF	Device	Device-specific system registers.

The device memory map shown in Table 3 applies to both CPUs. That is, the CPUs share access to all PSoC 6 MCU memory and peripheral registers. Note that code can be executed from the Code, SRAM, and External RAM regions.

Table 3. Internal Memory Address Map for CM4 and CM0+

Address Range	Memory Type	Size
0x0000 0000 – 0x0000 FFFF	SROM, initial ROM boot code	64 KB
0x0800 0000 – 0x0802 5FFF 0x0802 6000 - 0x0803 FFFF	Application SRAM System SRAM	Up to 152 KB 104 KB
0x1000 0000 – 0x1006 FFFF 0x1007 0000 - 0x1007 FFFF	Application flash Secure Code Flash Used for secure boot, secure bootloader, and system calls	Up to 448 KB 64 KB
0x1400 0000 – 0x1400 7FFF	Auxiliary Flash, can be used for EEPROM emulation	32 KB
0x1600 0000 – 0x1600 7FFF	Supervisory Flash, for secure access	32 KB

System Resources

Power System

The power system provides assurance that voltage levels are as required for each respective mode and will either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) when the power supply drops below specified levels. The design guarantees safe chip operation between power supply voltage dropping below specified levels (for example, below 1.7 V) and the reset occurring. There are no voltage sequencing requirements.

The V_{DD} supply (1.7 to 3.6 V) powers an on-chip buck regulator or an LDO, selectable by the user. In addition, both the buck and the LDO offer a selectable (0.9 or 1.1 V) core operating voltage (V_{CCD}). The selection lets users choose between two system power modes:

- System Low Power (LP) operates V_{CCD} at 1.1 V and offers high performance, with no restrictions on any of the device configurations.
- System Ultra Low Power (ULP) operates V_{CCD} at 0.9 V for exceptional low power results, but imposes limitations on maximum clock speeds.

An additional, backup domain adds an "always on" functionality using a separate power domain supplied by a backup supply (V_{BACKUP}) such as a battery or supercapacitor. It includes a real-time clock (RTC) with alarm feature, supported by a 32.768-kHz watch crystal oscillator (WCO), and power-management IC (PMIC) control.

Power Modes

PSoC 6 MCU can operate in four system and three CPU power modes. These modes are intended to minimize the average power consumption in an application. For more details on power modes and other power-saving configuration options, see the application note, AN219528: PSoC 6 MCU Low-Power Modes and Power Reduction Techniques and the Architecture TRM, Power Modes chapter (contact your local Cypress sales representative for the latest TRM).

Power modes supported by PSoC 6 MCUs, in the order of decreasing power consumption, are:

- System Low Power (LP) – All peripherals and CPU power modes are available at maximum speed
- System Ultra Low Power (ULP) – All peripherals and CPU power modes are available, but with limited speed
- CPU Active – CPU is executing code in system LP or ULP mode
- CPU Sleep – CPU code execution is halted in system LP or ULP mode
- CPU Deep Sleep – CPU code execution is halted and system Deep Sleep is requested in system LP or ULP mode
- System Deep Sleep – Only low-frequency peripherals are available after both CPUs enter CPU Deep Sleep mode
- System Hibernate – Device and I/O states are frozen and the device resets on wakeup

CPU Active, Sleep, and Deep Sleep are standard Arm-defined power modes supported by the Arm CPU instruction set architecture (ISA). LP, ULP, Deep Sleep and Hibernate modes are additional low-power modes supported by PSoC 6 MCU.

Hibernate mode is the lowest power mode in the PSoC 6 MCU and on wakeup, the CPU and all peripherals go through a reset.

Clock System

The clock system for PSoC 64 consists of the following:

- IMO
- ILO
- Watch crystal oscillator (WCO)
- External MHz crystal oscillator (ECO)
- External clock input
- One PLL
- One FLL

Clocks may be buffered and brought out to a pin on a smart I/O port.

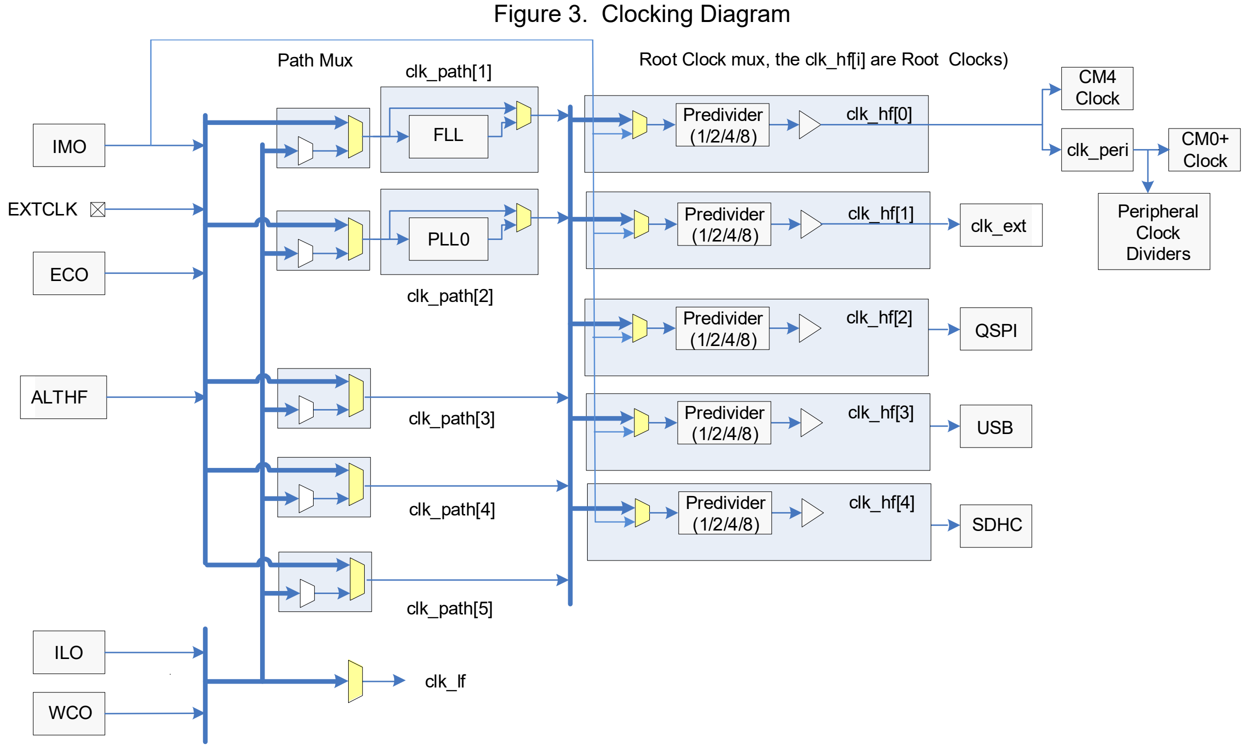
IMO Clock Source

The IMO is the primary source of internal clocking in PSoC 64. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 8 MHz and IMO tolerance is ± 2%. The IMO can be selected to operate in Deep Sleep mode to drive the LCD block for better contrast (and higher power) than is possible with the 32-kHz mode.

ILO Clock Source

The ILO is a very low power oscillator, nominally 32 kHz, which operates in all power modes including Hibernate. The ILO can be calibrated against a higher accuracy clock for better accuracy.

Figure 3. Clocking Diagram



Watchdog Timers (WDT, MCWDT)

PSoC 6 has one WDT and two multi-counter WDTs (MCWDT). The WDT has a 16-bit free-running counter. Each MCWDT has two 16-bit counters and one 32-bit counter, with multiple operating modes. All of the 16-bit counters can generate a watchdog device reset. All of the counters can generate an interrupt on a match event.

The WDT is clocked by the ILO. It can do interrupt/wakeup generation in LP/ULP, Deep Sleep, and Hibernate power modes. The MCWDTs are clocked by LFCLK (ILO or WCO). It can do periodic interrupt / wakeup generation in LP/ULP and Deep Sleep power modes.

Clock Dividers

Integer and fractional clock dividers are provided for peripheral use and timing purposes. There are:

- Four 8-bit clock dividers
- Eight 16-bit integer clock dividers
- Two 16.5-bit fractional clock dividers
- One 24.5-bit fractional clock divider

Trigger Routing

PSoC 6 MCU contains a trigger multiplexer block. This is a collection of digital multiplexers and switches that are used for routing trigger signals between peripheral blocks and between GPIOs and peripheral blocks.

PSoC 64 has two types of trigger routing. Trigger multiplexers have reconfigurability in the source and destination. There are also hardwired switches called “one-to-one triggers,” which connect a specific source to a destination. The user can enable or disable the route.

Reset

PSoC 6 MCU can be reset from a variety of sources:

- Power-on reset (POR) to hold the device in reset while the power supply ramps up to the level required for the device to function properly. POR activates automatically at power-up.
- Brown-out detect (BOD) reset to monitor the digital voltage supply V_{DDD} and generate a reset if V_{DDD} falls below the minimum required logic operating voltage.
- External reset (XRES) to reset the device using an external input. The XRES pin is active LOW – a logic ‘1’ on the pin has no effect and a logic ‘0’ causes reset. The pin is pulled to logic ‘1’ inside the device. XRES is available as a dedicated pin.
- Watchdog timer (WDT or MCWDT) to reset the device if firmware fails to service it within a specified timeout period.
- Software-initiated reset to reset the device on demand using firmware.
- Logic-protection fault can trigger an interrupt or reset the device if unauthorized operating conditions occur; for example, reaching a debug breakpoint while executing privileged code.
- Hibernate wakeup reset to bring the device out of the Hibernate low-power mode.

Reset events are asynchronous and guarantee reversion to a known state. Some of the reset sources are recorded in a register, which is retained through reset and allows software to determine the cause of the reset.

Programmable Analog Subsystems

12-bit SAR ADC

The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion. One of three internal reference voltages may be used for the ADC reference voltage. The references are, V_{DD}, $V_{DD}/2$, and V_{REF} (nominally 1.2 V and trimmed to ±1%). An external reference may also be used, by either driving the VREF pin or routing an external reference to GPIO pin P9.3. These reference options allow ratio-metric readings or absolute readings at the accuracy of the reference used. The input range of the ADC is the full supply voltage between V_{SS} and V_{DDA}/V_{DDIOA}. The SAR ADC may be configured with a mix of single ended and differential signals in the same configuration.

The SAR ADC’s sample-and-hold (S/H) aperture is programmable to allow sufficient time for signals with a high impedance to settle sufficiently, if required. System performance will be 65 dB for true 12-bit precision provided appropriate references are used and system noise levels permit it. To improve performance in noisy conditions, an external bypass capacitor for the internal reference amplifier (through the fixed “VREF” pin), may be added.

The SAR is connected to a fixed set of pins through an input multiplexer. The multiplexer cycles through the selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The result of each channel is buffered, so that an interrupt may be triggered only when a full scan of all channels is complete. Also, a pair of range registers can be set to detect and cause an interrupt if an input exceeds a minimum and/or maximum value. This allows fast detection of out-of-range values without having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software. The SAR can also be connected, under firmware control, to most other GPIO pins via the Analog Multiplexer Bus (AMUXBUS). The SAR is not available in Deep Sleep and Hibernate modes as it requires a high -speed clock (up to 18 MHz). The SAR operating range is 1.71 to 3.6 V.

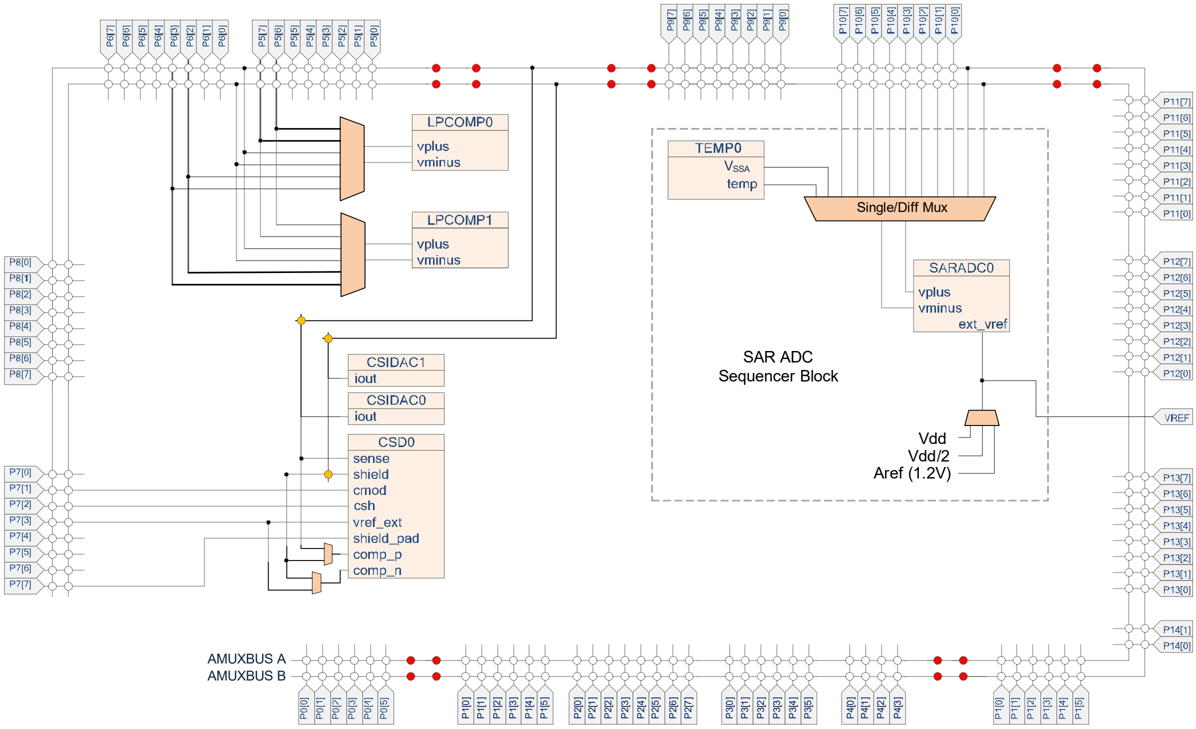
Temperature Sensor

An on-chip temperature sensor is part of the SAR and may be scanned by the SAR ADC. It consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor may be connected directly to the SAR ADC as one of the measurement channels. The ADC digitizes the temperature sensor’s output and a Cypress-supplied software function may be used to convert the reading to temperature which includes calibration and linearization.

Low-Power Comparators

Two low-power comparators are provided, which can operate in all power modes. This allows other analog system resources to be disabled while retaining the ability to monitor external voltage levels during Deep Sleep and Hibernate modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator-switch event.

Figure 4. PSoC 64 Analog Subsystem



Programmable Digital

Smart I/O

Smart I/O™ is a programmable logic fabric that enables Boolean operations on signals traveling from device internal resources to the GPIO pins or on signals traveling into the device from external sources. The Smart I/O block sits between the GPIO pins and the high-speed I/O matrix (HSIOM) and is dedicated to a single port.

On PSoC 64, there are two Smart I/O blocks: one on Port 8 and one on Port 9. When the Smart I/O is not enabled, all signals on Port 8 and Port 9 bypass the Smart I/O hardware.

Smart I/O supports:

- System Deep Sleep operation
- Boolean operations without CPU intervention
- Asynchronous or synchronous (clocked) operation

Each Smart I/O block contains a data unit (DU) and eight look up tables (LUTs).

The DU:

- Performs unique functions based on a selectable opcode.
- Can source input signals from internal resources, the GPIO port, or a value in the DU register.

Each LUT:

- Has three selectable input sources. The input signals may be sourced from another LUT, an internal resource, an external signal from a GPIO pin, or from the DU.
- Acts as a programmable Boolean logic table.
- Can be synchronous or asynchronous.

Fixed-Function Digital

Timer/Counter/Pulse-width Modulator (TCPWM)

- The TCPWM supports the following operational modes:
  - Timer-counter with compare
  - Timer-counter with capture
  - Quadrature decoding
  - Pulse width modulation (PWM)
  - Pseudo-random PWM
  - PWM with dead time
- Up, down, and up/down counting modes.
- Clock prescaling (division by 1, 2, 4, ... 64, 128)
- Double buffering of compare/capture and period values
- Underflow, overflow, and capture/compare output signals
- Supports interrupt on:
  - Terminal count – Depends on the mode; typically occurs on overflow or underflow
  - Capture/compare – The count is captured to the capture register or the counter value equals the value in the compare register
- Complementary output for PWMs
- Selectable start, reload, stop, count, and capture event signals for each TCPWM; with rising edge, falling edge, both edges, and level trigger options. The TCPWM has a Kill input to force outputs to a predetermined state.

In this device there are:

- Four 32-bit TCPWMs
- Eight 16-bit TCPWMs

Serial Communication Blocks (SCB)

PSoC 64 has seven SCBs:

- Six can implement either I^2C, UART, or SPI.
- One SCB (SCB #8) can operate in Deep Sleep with an external clock, this SCB can be either SPI slave or I^2C slave.

I^2C Mode: The SCB can implement a full multi-master and slave interface (it is capable of multimaster arbitration). This block can operate at speeds of up to 1 Mbps (Fast Mode Plus). The SCB supports a 256-byte FIFO for receive and transmit.

The I2C peripheral is compatible with I^2C standard-mode, Fast Mode, and Fast Mode Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open-drain modes.

UART Mode: This is a full-feature UART operating at up to 8 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows the addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. A 256-byte FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI Secure Simple Pairing (SSP) (essentially adds a start pulse that is used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block supports an EzSPI mode in which the data interchange is reduced to reading and writing an array in memory. The SPI interface will operate with a 25-MHz SPI Clock.

USB Full-Speed Device Interface

PSoC 64 incorporates a full-speed USB device interface. The device can have up to eight endpoints. A 512-byte SRAM buffer is provided and DMA is supported.

Quad-SPI/Serial Memory Interface (SMIF)

A serial memory interface is provided, running at up to 80 MHz. It supports single, dual, quad, dual-quad and octal SPI configurations, and supports up to four external memory devices.

It supports two modes of operation:

- Memory-mapped I/O (MMIO), a command mode interface that provides data access via the SMIF registers and FIFOs
- Execute in Place (XIP), in which AHB reads and writes are directly translated to SPI read and write transfers.

In XIP mode, the external memory is mapped into the PSoC 6 MCU internal address space, enabling code execution directly from the external memory. To improve performance, a 4-KB cache is included. XIP mode also supports AES-128 on-the-fly encryption and decryption, enabling secure storage and access of code and data in the external memory.

SDHC Controller

PSoC 64 contains one secure digital host controller (SDHC). The SDHC provides communication with IoT connectivity devices such as Bluetooth (BT), Bluetooth Low-Energy (BLE) and WiFi radios, as well as combination devices. The controller also supports embedded MultiMediaCards (eMMC) and Secure Digital (SD) cards.

Several bus speed modes under the SD specification are supported:

- DS (default speed)
- HS (high speed)
- SDR12 (single data rate)
- SDR25
- SDR50
- DDR50 (double data rate)

For eMMC, the supported modes are:

- BWC (backward compatibility)
- SDR
- DDR

Maximum clock restrictions and capacitive loads apply to some modes, and are also dependent on system power mode (LP/ULP). Consult the electrical characteristics for details. (See Table 39.)

SDHC is configured as a master. To be fully compatible with features provided in the driver software for speed and efficiency, the SDHC supports advanced DMA version 3 (ADMA3), defined by the SDIO standard, and has a 1 KB RX/TX FIFO allowing double buffering of 512-byte blocks.

CAN FD Block

There is one CAN FD block on the chip for industrial and automotive applications. The block includes Time-Stamp support and has a 4KB message RAM. FD Data rates of up to 5 Mbps will be supported. DMA transfers will be supported.

LCD Block

This block drives LCD commons and segments; routing is available to most of the GPIOs. The LCD block has two modes of operation: high speed (8 MHz) and low speed (32 kHz). Both modes operate in system LP, ULP, and Deep Sleep modes, however the low-speed mode operates with reduced contrast in system Deep Sleep mode. The 8-MHz IMO is available in system Deep Sleep mode, and can be used to generate a clock for the LCD block. Review the number of common and segment lines, viewing angle requirements, and prototype performance, and then select the appropriate LCD clock frequency before using system Deep Sleep mode.

GPIO

CYB06445LQI-S3D42 has up to 53 GPIOs. The GPIO block implements the following:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Hold mode for latching previous state (used for retaining the I/O state in system Hibernate mode)
- Selectable slew rates for dV/dt-related noise control to improve EMI

The pins are organized in logical entities called ports, which are up to 8 pins in width. Data output and pin state registers store, respectively, the values to be driven on the pins and the input states of the pins.

Every pin can generate an interrupt if enabled; each port has an interrupt request (IRQ) associated with it.

The port 1 pins are capable of overvoltage-tolerant (OVT) operation, where the input voltage may be higher than V_{DDD}. OVT pins are commonly used with I^2C, to allow powering the chip OFF while maintaining a physical connection to an operating I^2C bus without affecting its functionality.

GPIO pins can be ganged to source or sink higher values of current. GPIO pins, including OVT pins, may not be pulled up higher than the absolute maximum; see Electrical Specifications.

During power-on and reset, the pins are forced to the analog input drive mode, with input and output buffers disabled, so as not to crowbar any inputs and/or cause excess turn-on current.

A multiplexing network known as the high-speed I/O matrix (HSIOM) is used to multiplex between various peripheral and analog signals that may connect to an I/O pin.

Special-Function Peripherals

CapSense Subsystem

CapSense is supported in PSoC 6 MCU through a CapSense sigma-delta (CSD) hardware block. It is designed for high-sensitivity self-capacitance and mutual-capacitance measurements, and is specifically built for user interface solutions.

In addition to CapSense, the CSD hardware block supports three general-purpose functions. These are available when CapSense is not being used. Alternatively, two or more functions can be time-multiplexed in an application under firmware control. The four functions supported by the CSD hardware block are:

- CapSense
- 10-bit ADC
- Programmable current sources (IDAC)
- Comparator

CapSense

Capacitive touch sensors are designed for user interfaces that rely on human body capacitance to detect the presence of a finger on or near a sensor. Cypress CapSense solutions bring elegant, reliable, and simple capacitive touch sensing functions to applications including IoT, industrial, automotive, and home appliances.

The Cypress-proprietary CapSense technology offers the following features:

- Best-in-class signal-to-noise ratio (SNR) and robust sensing under harsh and noisy conditions
- Self-capacitance (CSD) and mutual-capacitance (CSX) sensing methods
- Support for various widgets, including buttons, matrix buttons, sliders, touchpads, and proximity sensors
- High-performance sensing across a variety of materials
- Best-in-class liquid tolerance
- SmartSense™ auto-tuning technology that helps avoid complex manual tuning processes
- Superior immunity against external noise
- Spread-spectrum clocks for low radiated emissions
- Gesture and built-in self-test libraries
- Ultra-low power consumption
- An integrated graphical CapSense tuner for real-time tuning, testing, and debugging

ADC

The CapSense subsystem slope ADC offers the following features:

- Selectable 8- or 10-bit resolution
- Selectable input range: GND to V_{REF} and GND to V_{DDA} on any GPIO input
- Measurement of V_{DDA} against an internal reference without the use of GPIO or external components

IDAC

The CSD block has two programmable current sources, which offer the following features:

- 7-bit resolution
- Sink and source current modes
- A current source programmable from 37.5 nA to 609 µA
- Two IDACs that can be used in parallel to form one 8-bit IDAC

Comparator

The CapSense subsystem comparator operates in the System Low Power and Ultra-Low Power modes. The inverting input is connected to an internal programmable reference voltage and the non-inverting input can be connected to any GPIO via the AMUXBUS.

CapSense Hardware Subsystem

Figure 5 shows the high-level hardware overview of the CapSense subsystem, which includes a delta sigma converter, internal clock dividers, a shield driver, and two programmable current sources.

The inputs are managed through analog multiplexed buses (AMUXBUS A/B). The input and output of all functions offered by the CSD block can be provided on any GPIO or on a group of GPIOs under software control, with the exception of the comparator output and external capacitors that use dedicated GPIOs.

Self-capacitance is supported by the CSD block using AMUXBUS A, an external modulator capacitor, and a GPIO for each sensor. There is a shield electrode (optional) for self-capacitance sensing. This is supported using AMUXBUS B and an optional external shield tank capacitor (to increase the drive capability of the shield driver) should this be required. Mutual-capacitance is supported by the CSD block using AMUXBUS A, two external integrated capacitors, and a GPIO for transmit and receive electrodes.

The ADC does not require an external component. Any GPIO that can be connected to AMUXBUS A can be an input to the ADC under software control. The ADC can accept V_{DDA} as an input without needing GPIOs (for applications such as battery voltage measurement).

The two programmable current sources (IDACs) in general-purpose mode can be connected to AMUXBUS A or B. They can therefore connect to any GPIO pin. The comparator resides in the delta-sigma converter. The comparator inverting input can be connected to the reference. Both comparator inputs can be connected to any GPIO using AMUXBUSB; see Figure 4. The reference has a direct connection to a dedicated GPIO; see Table 6.

The CSD block can operate in active and sleep CPU power modes, and seamlessly transition between LP and ULP system modes. It can be powered down in Deep Sleep and Hibernate modes. Upon wakeup from Hibernate mode, the CSD block requires re-initialization. However, operation can be resumed without re-initialization upon exit from Deep Sleep mode, under firmware control.

Figure 5. CapSense Hardware Subsystem

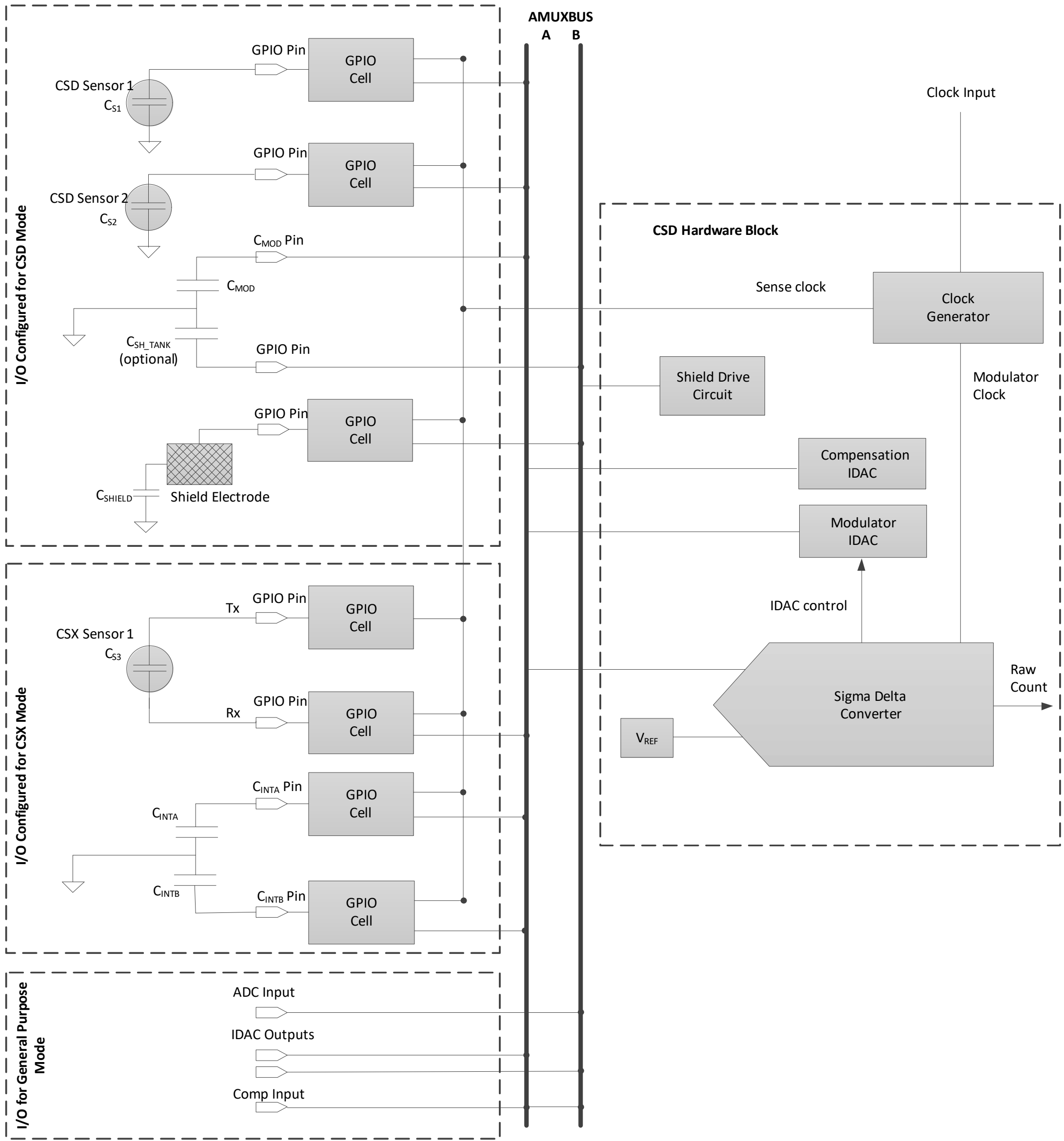


Figure 6 shows the high-level software overview. Cypress provides a middleware library for each function to enable quick integration. User applications interact only with middleware to implement functions of the CSD block. The middleware interacts with underlying drivers to access hardware as necessary. The CSD driver facilitates time-multiplexing of the CSD hardware if more than one piece of CSD-related middleware is present in a project. It prevents access conflicts in this case.

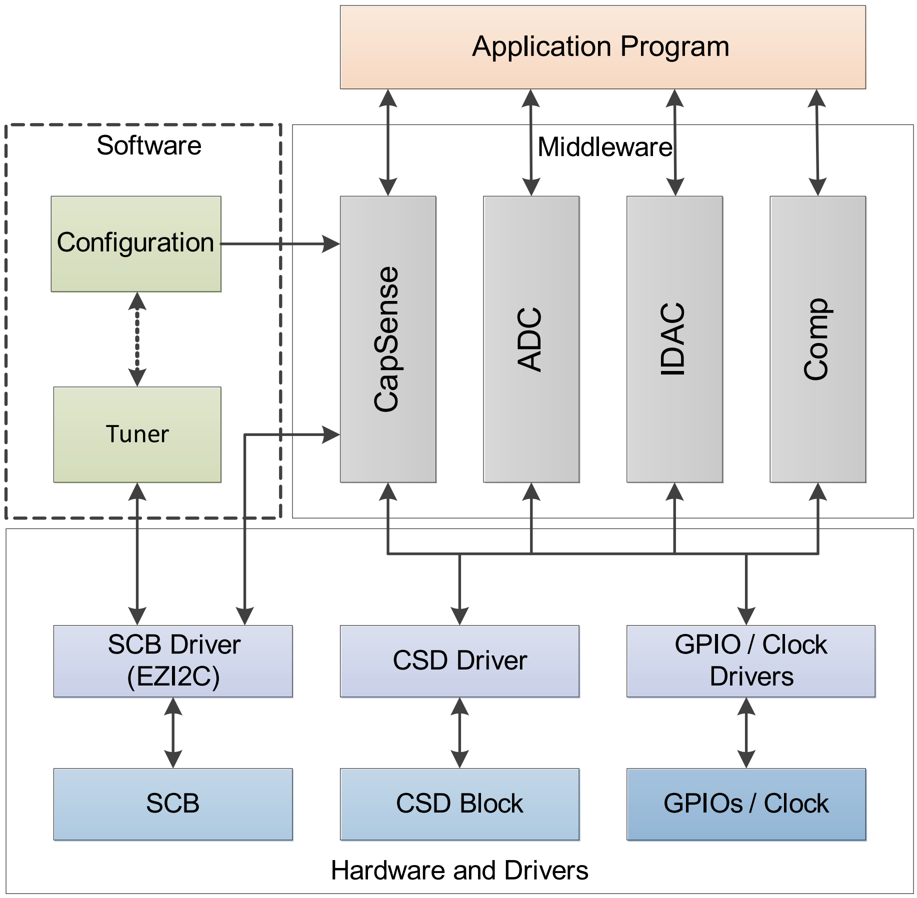
CapSense middleware has configurator software to enable fast configuration and incorporating it into middleware. It also has a tuner for performance evaluation and real-time tuning of the system. Both can be launched from the ModusToolbox IDE or in standalone mode. The tuner requires the EZ12C communication interface in the application to enable real-time tuning capability.

The tuner can update configuration parameters directly in the device as well as in the configurator.

CapSense and ADC middleware use the CSD interrupt to implement non-blocking sensing and A-to-D conversion. Therefore, interrupt service routines are a defined part of the middleware, which must be initialized by the application. Middleware and drivers can operate on either CPU. Cypress recommends using the middleware only in one CPU. If both CPUs must access the CSD driver, memory access should be managed in the application.

Refer to AN85951: PSoC 4 and PSoC 6 MCU CapSense Design Guide for more details on CSX sensing, CSD sensing, shield electrode usage and its benefits, and capacitive system design guidelines. Refer to the middleware API reference guide available in the PSoC 6 SDK for more detail on middleware.

Figure 6. CapSense Software/Firmware Subsystem



Secure Boot Functionality

The PSoC64 family of devices support both secure boot functionality and a way to securely provision user credentials. This is achieved by a chain of signed firmware launches, based on a hardware-based RoT. This RoT is initially owned by Cypress and will be handed off to the user/OEM during the provisioning process.

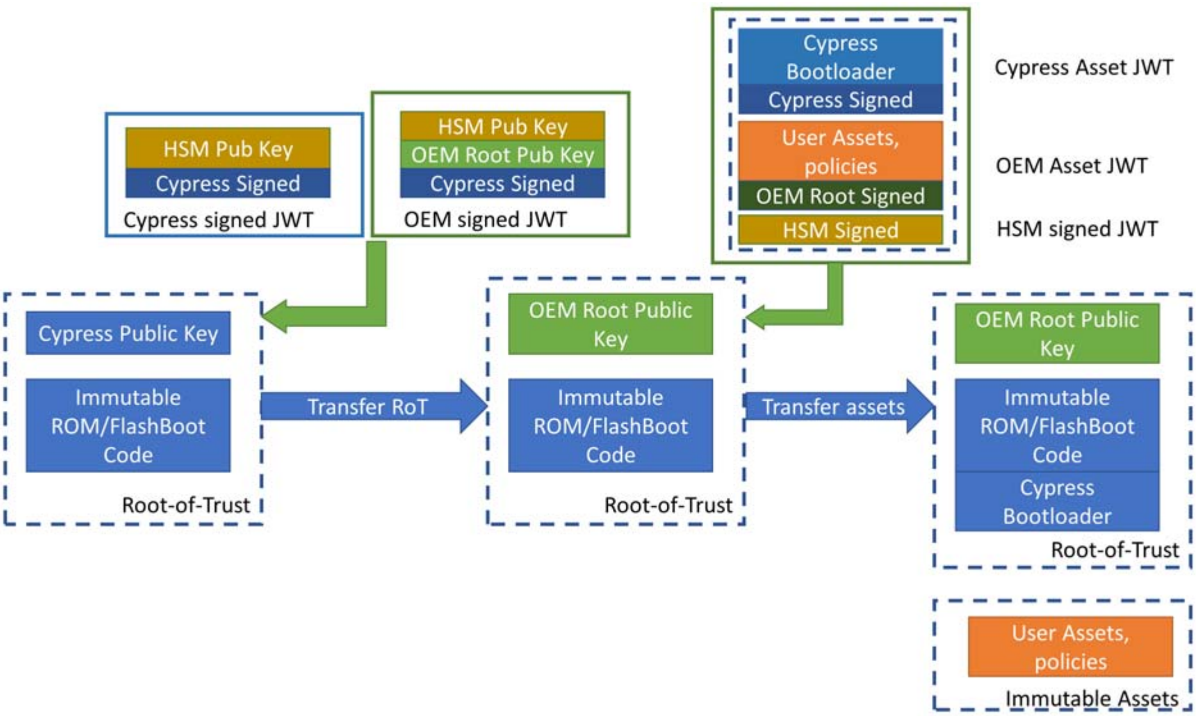
Provisioning Scheme

The provisioning process of the PSoC 64 secure parts achieves the following goals:

1. Transfer RoT from Cypress to the user/OEM
2. Transfer any secure assets such as keys, certificates, and secure bootloader into the device
3. Set up policies which govern the debug and boot-up behavior of the device

This is achieved by sending a series of signed Java Web Tokens (JWTs) to the part.

The high-level flow of provisioning is shown in the following diagram.



This provisioning scheme allows a chain of trust where assets and subsequent firmware can only be injected after the RoT is handed off to a Cypress-trusted distributor.

The transfer of the Root-of-Trust to the user/OEM key is done in a two step process where:

1. Cypress authorizes a Hardware Security Module (HSM) by signing the HSM public key
2. The User/OEM authorizes the HSM by signing the same public key as well as the public Root-of-Trust key, which needs to be put into the device

The PSoC 64 Secure MCU, which has the Cypress public key, will validate the signatures and contents of the presented tokens. Once verified, the Root-of-Trust is permanently moved to the OEM-public key and any OEM assets, such as keys and debug policies, will need to be signed by the OEM private key.

For development, the SecureBoot SDK will provide a pre-signed HSM public key along with an exposed HSM private key. These must not be used for production as they are inherently insecure as the private key is completely exposed in the SDK.

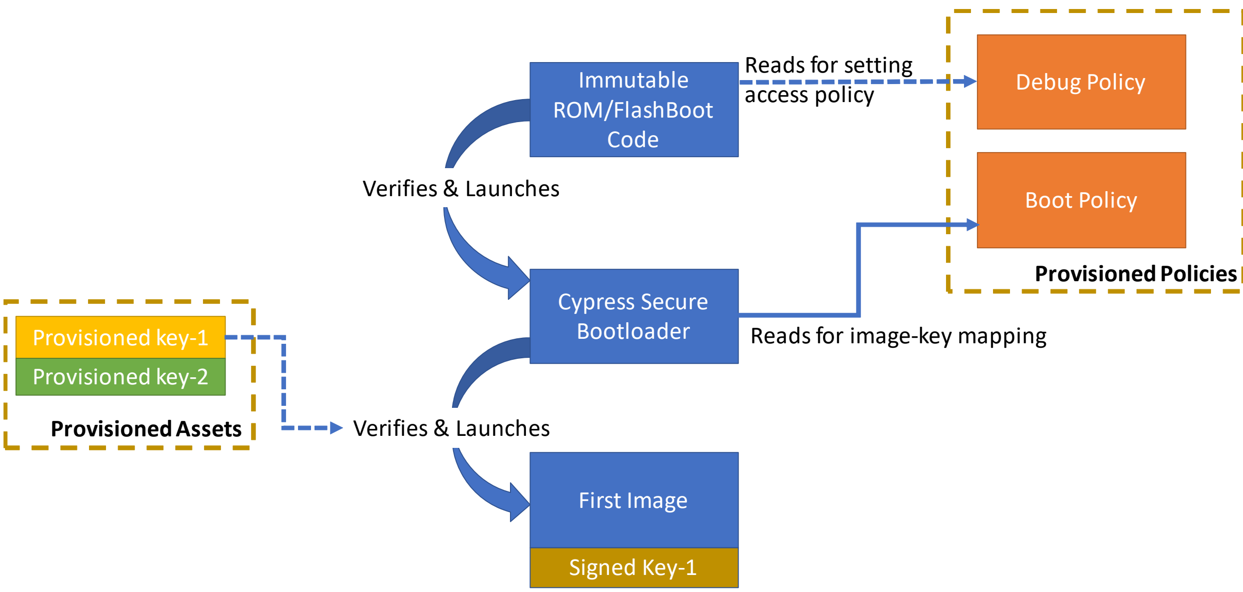
Secure Boot Scheme

Once the provisioning step is complete, the immutable boot code

1. Reads the debug policy for setting access restrictions to DAP ports
2. Reads the boot policy and verifies if the subsequent image is signed by the correct key before launch.

The PSoC 64 development libraries come with a Cypress-developed bootloader, which can be programmed into the part for the first image launch. The Cypress Secure Bootloader is a optimized version of the MCUBoot SecureBoot library with added features to use PSoC 6 protection contexts and the ability read provisioned policies to find the image-key mapping.

A high-level view of the image launches are shown in the following diagram.



Pinouts

GPIO ports are powered by V_{DDx} pins as follows:

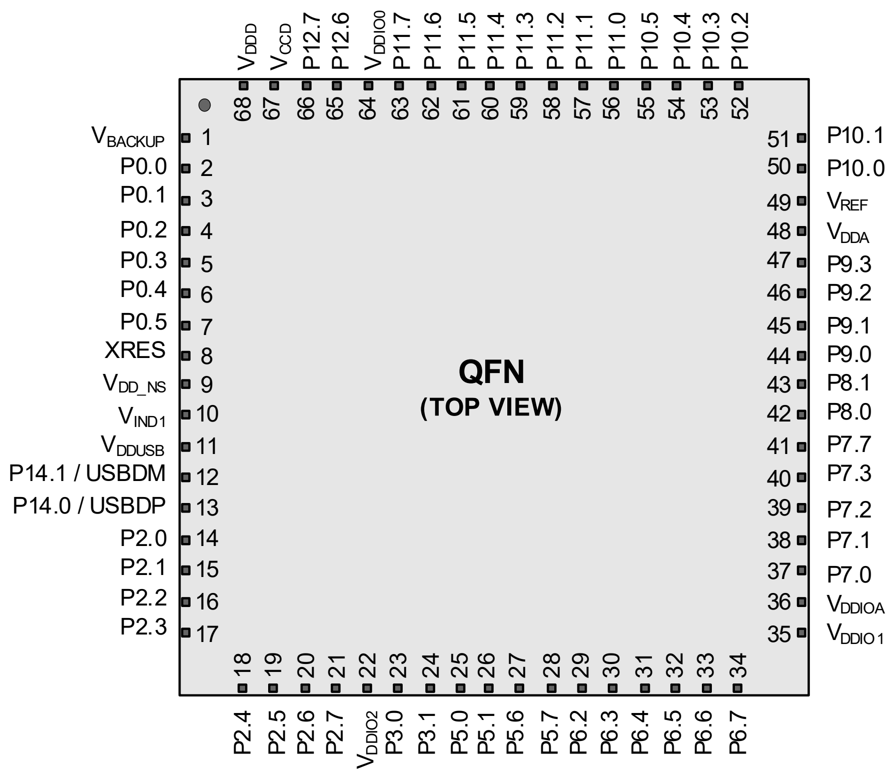
- P0: V_{BACKUP}
- P2, P3: V_{DDIO2}
- P5, P6, P7, P8: V_{DDIO1}
- P9, P10: V_{DDIOA}, V_{DDA} (V_{DDIOA}, when present, and V_{DDA} must be connected together on the PCB)
- P11, P12: V_{DDIO0}

Table 4. Packages and Pin Information

Pin	Package
	68-QFN
V_{DDD}	68
V_{CCD}	67
V_{DDA}	48
V_{DDIOA}	36
V_{DDIO0}	64
V_{DDIO1}	35
V_{DDIO2}	22
V_{BACKUP}	1
V_{DDUSB}	11
V_{SS}	GND PAD
V_{DD_NS}	9
V_{IND1}	10
XRES	8
V_{REF}	49
P0.0	2
P0.1	3
P0.2	4
P0.3	5
P0.4	6
P0.5	7
P2.0	14
P2.1	15
P2.2	16
P2.3	17
P2.4	18
P2.5	19
P2.6	20
P2.7	21
P3.0	23
P3.1	24
P5.0	25
P5.1	26
P5.6	27
P5.7	28
P6.2	29

Pin	Package
	68-QFN
P6.3	30
P6.4	31
P6.5	32
P6.6	33
P6.7	34
P7.0	37
P7.1	38
P7.2	39
P7.3	40
P7.7	41
P8.0	42
P8.1	43
P9.0	44
P9.1	45
P9.2	46
P9.3	47
P10.0	50
P10.1	51
P10.2	52
P10.3	53
P10.4	54
P10.5	55
P11.0	56
P11.1	57
P11.2	58
P11.3	59
P11.4	60
P11.5	61
P11.6	62
P11.7	63
P12.6	65
P12.7	66
P14.0 / USBDP	13
P14.1 / USBDM	12

Figure 7. Device Pinout for 68-QFN Package[2]



Note

2. The center pad on the QFN package should be connected to PCB ground relative to device VDDx for best mechanical, thermal, and electrical performance. For more information, see AN72845, Design Guidelines for QFN Devices.

Each port pin has multiple alternate functions. These are defined in Table 5. The columns ACT #x and DS #y denote active (System LP/ULP) and Deep Sleep mode signals respectively.

The notation for a signal is of the form IPName[x].signal_name[u]:y.

IPName = Name of the block (such as tcpwm), x = Unique instance of the IP, Signal_name = Name of the signal, u = Signal number where there is more than one signal for a particular signal name, y = Designates copies of the signal name.

For example, the name tcpwm[0].line_compl[3]:4 indicates that this is instance 0 of a tcpwm block, the signal is line_compl # 3 (complement of the line output) and this is the fourth occurrence (copy) of the signal. Signal copies are provided to allow flexibility in routing and to maximize use of on-chip resources.

Table 5. Multiple Alternate Functions

Port/Pin	ACT #0	ACT #1	ACT #2	ACT #3	DS #2	DS #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #5	DS #6	DS #7
P0.0	tcpwm[0].line[0]:0	tcpwm[1].line[0]:0	csd.csd_tx:0	csd.csd_tx_n:0			srss.ext_clk:0				scb[0].spi_select1:0			peri.tr_io_input[0]:0						
P0.1	tcpwm[0].line_compl[0]:0	tcpwm[1].line_compl[0]:0	csd.csd_tx:1	csd.csd_tx_n:1							scb[0].spi_select2:0			peri.tr_io_input[1]:0				cpuss.swj_trstn		
P0.2	tcpwm[0].line[1]:0	tcpwm[1].line[1]:0	csd.csd_tx:2	csd.csd_tx_n:2					scb[0].uart_rx:0	scb[0].i2c_scl:0	scb[0].spi_mosi:0									
P0.3	tcpwm[0].line_compl[1]:0	tcpwm[1].line_compl[1]:0	csd.csd_tx:3	csd.csd_tx_n:3					scb[0].uart_tx:0	scb[0].i2c_sda:0	scb[0].spi_miso:0									
P0.4	tcpwm[0].line[2]:0	tcpwm[1].line[2]:0	csd.csd_tx:4	csd.csd_tx_n:4					scb[0].uart_rts:0		scb[0].spi_clk:0			peri.tr_io_input[2]:0	peri.tr_io_output[0]:2					
P0.5	tcpwm[0].line_compl[2]:0	tcpwm[1].line_compl[2]:0	csd.csd_tx:5	csd.csd_tx_n:5			srss.ext_clk:1		scb[0].uart_cts:0		scb[0].spi_select0:0			peri.tr_io_input[3]:0	peri.tr_io_output[1]:2					
P2.0	tcpwm[0].line[3]:0	tcpwm[1].line[3]:0	csd.csd_tx:6	csd.csd_tx_n:6					scb[1].uart_rx:0	scb[1].i2c_scl:0	scb[1].spi_mosi:0			peri.tr_io_input[4]:0		sdhc[0].card_dat_3to0[0]				
P2.1	tcpwm[0].line_compl[3]:0	tcpwm[1].line_compl[3]:0	csd.csd_tx:7	csd.csd_tx_n:7					scb[1].uart_tx:0	scb[1].i2c_sda:0	scb[1].spi_miso:0			peri.tr_io_input[5]:0		sdhc[0].card_dat_3to0[1]				
P2.2	tcpwm[0].line[0]:1	tcpwm[1].line[4]:0	csd.csd_tx:8	csd.csd_tx_n:8					scb[1].uart_rts:0		scb[1].spi_clk:0					sdhc[0].card_dat_3to0[2]				
P2.3	tcpwm[0].line_compl[0]:1	tcpwm[1].line_compl[4]:0	csd.csd_tx:9	csd.csd_tx_n:9					scb[1].uart_cts:0		scb[1].spi_select0:0					sdhc[0].card_dat_3to0[3]				
P2.4	tcpwm[0].line[1]:1	tcpwm[1].line[5]:0	csd.csd_tx:10	csd.csd_tx_n:10							scb[1].spi_select1:0					sdhc[0].card_cmd				

Table 5. Multiple Alternate Functions *(continued)*

Port/Pin	ACT #0	ACT #1	ACT #2	ACT #3	DS #2	DS #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #5	DS #6	DS #7
P2.5	tcpwm[0].line_compl[1]:1	tcpwm[1].line_compl[5]:0	csd.csd_tx:11	csd.csd_tx_n:11							scb[1].spi_select2:0					sdhc[0].clk_card				
P2.6	tcpwm[0].line[2]:1	tcpwm[1].line[6]:0	csd.csd_tx:12	csd.csd_tx_n:12							scb[1].spi_select3:0			peri.tr_io_input[8]:0		sdhc[0].card_detect_n				
P2.7	tcpwm[0].line_compl[2]:1	tcpwm[1].line_compl[6]:0	csd.csd_tx:13	csd.csd_tx_n:13										peri.tr_io_input[9]:0		sdhc[0].card_mech_write_prot				
P3.0	tcpwm[0].line[3]:1	tcpwm[1].line[7]:0	csd.csd_tx:14	csd.csd_tx_n:14					scb[2].uart_rx:1	scb[2].i2c_scl:1	scb[2].spi_mosi:1			peri.tr_io_input[6]:0		sdhc[0].io_volt_sel				
P3.1	tcpwm[0].line_compl[3]:1	tcpwm[1].line_compl[7]:0	csd.csd_tx:15	csd.csd_tx_n:15					scb[2].uart_tx:1	scb[2].i2c_sda:1	scb[2].spi_miso:1			peri.tr_io_input[7]:0		sdhc[0].card_if_pwr_en				
P5.0	tcpwm[0].line[0]:2	tcpwm[1].line[0]:1	csd.csd_tx:16	csd.csd_tx_n:16					scb[5].uart_rx:1	scb[5].i2c_scl:1	scb[5].spi_mosi:1		canfd[0].ttcan_rx[0]	peri.tr_io_input[10]:0						
P5.1	tcpwm[0].line_compl[0]:2	tcpwm[1].line_compl[0]:1	csd.csd_tx:17	csd.csd_tx_n:17					scb[5].uart_tx:1	scb[5].i2c_sda:1	scb[5].spi_miso:1		canfd[0].ttcan_tx[0]	peri.tr_io_input[11]:0						
P5.6	tcpwm[0].line[1]:2	tcpwm[1].line[1]:1	csd.csd_tx:18	csd.csd_tx_n:18																
P5.7	tcpwm[0].line_compl[1]:2	tcpwm[1].line_compl[1]:1	csd.csd_tx:19	csd.csd_tx_n:19																
P6.0	tcpwm[0].line[2]:2	tcpwm[1].line[2]:1	csd.csd_tx:20	csd.csd_tx_n:20					scb[3].uart_rx:0	scb[3].i2c_scl:0	scb[3].spi_mosi:0				cpuss.fault_out[0]					
P6.1	tcpwm[0].line_compl[2]:2	tcpwm[1].line_compl[2]:1	csd.csd_tx:21	csd.csd_tx_n:21					scb[3].uart_tx:0	scb[3].i2c_sda:0	scb[3].spi_miso:0				cpuss.fault_out[1]					
P6.2	tcpwm[0].line[3]:2	tcpwm[1].line[3]:1	csd.csd_tx:22	csd.csd_tx_n:22					scb[3].uart_rts:0		scb[3].spi_clk:0									
P6.3	tcpwm[0].line_compl[3]:2	tcpwm[1].line_compl[3]:1	csd.csd_tx:23	csd.csd_tx_n:23					scb[3].uart_cts:0		scb[3].spi_select0:0									
P6.4	tcpwm[0].line[0]:3	tcpwm[1].line[4]:1	csd.csd_tx:24	csd.csd_tx_n:24	scb[6].i2c_scl:0									peri.tr_io_input[12]:0	peri.tr_io_output[0]:1			cpuss.swj_swo_tdo	scb[6].spi_mosi:0	srss.ddft_pin_in[0]:0
P6.5	tcpwm[0].line_compl[0]:3	tcpwm[1].line_compl[4]:1	csd.csd_tx:25	csd.csd_tx_n:25	scb[6].i2c_sda:0									peri.tr_io_input[13]:0	peri.tr_io_output[1]:1			cpuss.swj_swdoe_tdi	scb[6].spi_miso:0	srss.ddft_pin_in[1]:0

Table 5. Multiple Alternate Functions *(continued)*

Port/Pin	ACT #0	ACT #1	ACT #2	ACT #3	DS #2	DS #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #5	DS #6	DS #7
P6.6	tcpwm[0].line[1]:3	tcpwm[1].line[5]:1	csd.csd_tx:26	csd.csd_tx_n:26														cpuss.swj_swdio_tms	scb[6].spi_clk:0	
P6.7	tcpwm[0].line_compl[1]:3	tcpwm[1].line_compl[5]:1	csd.csd_tx:27	csd.csd_tx_n:27														cpuss.swj_swclk_tclk	scb[6].spi_select0:0	
P7.0	tcpwm[0].line[2]:3	tcpwm[1].line[6]:1	csd.csd_tx:28	csd.csd_tx_n:28					scb[4].uart_rx:1	scb[4].i2c_scl:1	scb[4].spi_mosi:1			peri.tr_io_input[14]:0		cpuss.trace_clock				
P7.1	tcpwm[0].line_compl[2]:3	tcpwm[1].line_compl[6]:1	csd.csd_tx:29	csd.csd_tx_n:29					scb[4].uart_tx:1	scb[4].i2c_sda:1	scb[4].spi_miso:1			peri.tr_io_input[15]:0						
P7.2	tcpwm[0].line[3]:3	tcpwm[1].line[7]:1	csd.csd_tx:30	csd.csd_tx_n:30					scb[4].uart_rts:1		scb[4].spi_clk:1									
P7.3	tcpwm[0].line_compl[3]:3	tcpwm[1].line_compl[7]:1	csd.csd_tx:31	csd.csd_tx_n:31					scb[4].uart_cts:1		scb[4].spi_select0:1									
P7.4	tcpwm[0].line[0]:4	tcpwm[1].line[0]:2	csd.csd_tx:32	csd.csd_tx_n:32							scb[4].spi_select1:1						cpuss.trace_data[3]:2			
P7.5	tcpwm[0].line_compl[0]:4	tcpwm[1].line_compl[0]:2	csd.csd_tx:33	csd.csd_tx_n:33							scb[4].spi_select2:1						cpuss.trace_data[2]:2			
P7.6	tcpwm[0].line[1]:4	tcpwm[1].line[1]:2	csd.csd_tx:34	csd.csd_tx_n:34							scb[4].spi_select3:1						cpuss.trace_data[1]:2			
P7.7	tcpwm[0].line_compl[1]:4	tcpwm[1].line_compl[1]:2	csd.csd_tx:35	csd.csd_tx_n:35								cpuss.clk_fm_pump					cpuss.trace_data[0]:2			
P8.0	tcpwm[0].line[2]:4	tcpwm[1].line[2]:2	csd.csd_tx:36	csd.csd_tx_n:36					scb[4].uart_rx:0	scb[4].i2c_scl:0	scb[4].spi_mosi:0			peri.tr_io_input[16]:0						
P8.1	tcpwm[0].line_compl[2]:4	tcpwm[1].line_compl[2]:2	csd.csd_tx:37	csd.csd_tx_n:37					scb[4].uart_tx:0	scb[4].i2c_sda:0	scb[4].spi_miso:0			peri.tr_io_input[17]:0						
P8.2	tcpwm[0].line[3]:4	tcpwm[1].line[3]:2	csd.csd_tx:38	csd.csd_tx_n:38		lpcomp.dsi_comp0:0			scb[4].uart_rts:0		scb[4].spi_clk:0									
P8.3	tcpwm[0].line_compl[3]:4	tcpwm[1].line_compl[3]:2	csd.csd_tx:39	csd.csd_tx_n:39		lpcomp.dsi_comp1:0			scb[4].uart_cts:0		scb[4].spi_select0:0									
P9.0	tcpwm[0].line[0]:5	tcpwm[1].line[4]:2	csd.csd_tx:40	csd.csd_tx_n:40					scb[2].uart_rx:0	scb[2].i2c_scl:0	scb[2].spi_mosi:0			peri.tr_io_input[18]:0			cpuss.trace_data[3]:0			

Table 5. Multiple Alternate Functions *(continued)*

Port/Pin	ACT #0	ACT #1	ACT #2	ACT #3	DS #2	DS #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #5	DS #6	DS #7
P9.1	tcpwm[0].line_compl[0]:5	tcpwm[1].line_compl[4]:2	csd.csd_tx:41	csd.csd_tx_n:41					scb[2].uart_tx:0	scb[2].i2c_sda:0	scb[2].spi_miso:0			peri.tr_io_input[19]:0			cpuss.trace_data[2]:0			srss.ddft_pin_in[0]:1
P9.2	tcpwm[0].line[1]:5	tcpwm[1].line[5]:2	csd.csd_tx:42	csd.csd_tx_n:42					scb[2].uart_rts:0		scb[2].spi_clk:0						cpuss.trace_data[1]:0			
P9.3	tcpwm[0].line_compl[1]:5	tcpwm[1].line_compl[5]:2	csd.csd_tx:43	csd.csd_tx_n:43					scb[2].uart_cts:0		scb[2].spi_select0:0						cpuss.trace_data[0]:0			srss.ddft_pin_in[1]:1
P10.0	tcpwm[0].line[2]:5	tcpwm[1].line[6]:2	csd.csd_tx:44	csd.csd_tx_n:44					scb[1].uart_rx:1	scb[1].i2c_scl:1	scb[1].spi_mosi:1			peri.tr_io_input[20]:0			cpuss.trace_data[3]:1			
P10.1	tcpwm[0].line_compl[2]:5	tcpwm[1].line_compl[6]:2	csd.csd_tx:45	csd.csd_tx_n:45					scb[1].uart_tx:1	scb[1].i2c_sda:1	scb[1].spi_miso:1			peri.tr_io_input[21]:0			cpuss.trace_data[2]:1			
P10.2	tcpwm[0].line[3]:5	tcpwm[1].line[7]:2	csd.csd_tx:46	csd.csd_tx_n:46					scb[1].uart_rts:1		scb[1].spi_clk:1						cpuss.trace_data[1]:1			
P10.3	tcpwm[0].line_compl[3]:5	tcpwm[1].line_compl[7]:2	csd.csd_tx:47	csd.csd_tx_n:47					scb[1].uart_cts:1		scb[1].spi_select0:1						cpuss.trace_data[0]:1			
P10.4	tcpwm[0].line[0]:6	tcpwm[1].line[0]:3	csd.csd_tx:48	csd.csd_tx_n:48							scb[1].spi_select1:1									
P10.5	tcpwm[0].line_compl[0]:6	tcpwm[1].line_compl[0]:3	csd.csd_tx:49	csd.csd_tx_n:49							scb[1].spi_select2:1									
P10.6	tcpwm[0].line[1]:6	tcpwm[1].line[1]:3	csd.csd_tx:50	csd.csd_tx_n:50							scb[1].spi_select3:1									
P10.7	tcpwm[0].line_compl[1]:6	tcpwm[1].line_compl[1]:3	csd.csd_tx:51	csd.csd_tx_n:51																
P11.0	tcpwm[0].line[2]:6	tcpwm[1].line[2]:3	csd.csd_tx:52	csd.csd_tx_n:52				smif.spi_select2	scb[5].uart_rx:0	scb[5].i2c_scl:0	scb[5].spi_mosi:0			peri.tr_io_input[22]:0						
P11.1	tcpwm[0].line_compl[2]:6	tcpwm[1].line_compl[2]:3	csd.csd_tx:53	csd.csd_tx_n:53				smif.spi_select1	scb[5].uart_tx:0	scb[5].i2c_sda:0	scb[5].spi_miso:0			peri.tr_io_input[23]:0						
P11.2	tcpwm[0].line[3]:6	tcpwm[1].line[3]:3	csd.csd_tx:54	csd.csd_tx_n:54				smif.spi_select0	scb[5].uart_rts:0		scb[5].spi_clk:0									

Table 5. Multiple Alternate Functions *(continued)*

Port/Pin	ACT #0	ACT #1	ACT #2	ACT #3	DS #2	DS #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #5	DS #6	DS #7
P11.3	tcpwm[0].line_compl[3]:6	tcpwm[1].line_compl[3]:3	csd.csd_tx:55	csd.csd_tx_n:55				smif.spi_data3	scb[5].uart_cts:0		scb[5].spi_select0:0				peri.tr_io_output[0]:0					
P11.4	tcpwm[0].line[0]:7	tcpwm[1].line[4]:3	csd.csd_tx:56	csd.csd_tx_n:56				smif.spi_data2			scb[5].spi_select1:0				peri.tr_io_output[1]:0					
P11.5	tcpwm[0].line_compl[0]:7	tcpwm[1].line_compl[4]:3	csd.csd_tx:57	csd.csd_tx_n:57				smif.spi_data1			scb[5].spi_select2:0									
P11.6	tcpwm[0].line[1]:7	tcpwm[1].line[5]:3	csd.csd_tx:58	csd.csd_tx_n:58				smif.spi_data0			scb[5].spi_select3:0									
P11.7	tcpwm[0].line_compl[1]:7	tcpwm[1].line_compl[5]:3	csd.csd_tx:59	csd.csd_tx_n:59				smif.spi_clk												
P12.0	tcpwm[0].line[2]:7	tcpwm[1].line[6]:3	csd.csd_tx:60	csd.csd_tx_n:60	scb[6].i2c_scl:1									peri.tr_io_input[24]:0						
P12.1	tcpwm[0].line_compl[2]:7	tcpwm[1].line_compl[6]:3	csd.csd_tx:61	csd.csd_tx_n:61	scb[6].i2c_sda:1									peri.tr_io_input[25]:0						
P12.6	tcpwm[0].line[3]:7	tcpwm[1].line[7]:3	csd.csd_tx:62	csd.csd_tx_n:62																
P12.7	tcpwm[0].line_compl[3]:7	tcpwm[1].line_compl[7]:3	csd.csd_tx:63	csd.csd_tx_n:63																

Analog and Smart I/O alternate port pin functionality is provided in Table 6.

Table 6. Port Pin Analog, and Smart I/O Functions

Name	Analog	Digital HV	AMUXA	AMUXB	SMARTIO
P0.0	wco_in				
P0.1	wco_out				
P0.2					
P0.3					
P0.4		pmic_wakeup_in hibernate_wakeup[1]			
P0.5		pmic_wakeup_out			
P5.6	lpcomp.inp_comp0				
P5.7	lpcomp.inn_comp0				
P6.2	lpcomp.inp_comp1				
P6.3	lpcomp.inn_comp1				
P6.6		swd_data			
P6.7		swd_clk			
P7.0			amuxbus_a_csd0	amuxbus_b_csd0	
P7.1	csd.cmodpadd csd.cmodpads		amuxbus_a_csd0	amuxbus_b_csd0	
P7.2	csd.csh_tankpadd csd.csh_tankpads		amuxbus_a_csd0	amuxbus_b_csd0	
P7.3	csd.vref_ext		amuxbus_a_csd0	amuxbus_b_csd0	
P7.4			amuxbus_a_csd0	amuxbus_b_csd0	
P7.5			amuxbus_a_csd0	amuxbus_b_csd0	
P7.6			amuxbus_a_csd0	amuxbus_b_csd0	
P7.7	csd.cshieldpads		amuxbus_a_csd0	amuxbus_b_csd0	
P8.0			amuxbus_a_csd0	amuxbus_b_csd0	smartio[8].io[0]
P8.1		hibernate_wakeup[0]	amuxbus_a_csd0	amuxbus_b_csd0	smartio[8].io[1]
P8.2			amuxbus_a_csd0	amuxbus_b_csd0	smartio[8].io[2]
P8.3			amuxbus_a_csd0	amuxbus_b_csd0	smartio[8].io[3]
P9.0			amuxbus_a_sar	amuxbus_b_sar	smartio[9].io[0]
P9.1			amuxbus_a_sar	amuxbus_b_sar	smartio[9].io[1]
P9.2			amuxbus_a_sar	amuxbus_b_sar	smartio[9].io[2]
P9.3	aref_ext_vref		amuxbus_a_sar	amuxbus_b_sar	smartio[9].io[3]
P10.0	sarmux_pads[0]				
P10.1	sarmux_pads[1]				
P10.2	sarmux_pads[2]				
P10.3	sarmux_pads[3]				
P10.4	sarmux_pads[4]				
P10.5	sarmux_pads[5]				
P10.6	sarmux_pads[6]				
P10.7	sarmux_pads[7]				
P12.6	eco_in				
P12.7	eco_out				

Power Supply Considerations

The following power system diagrams show typical connections for power pins, with and without usage of the buck regulator.

In these diagrams, the package pin is shown with the pin name, for example "V_{DDA}, 36". For V_{DDx} pins, the I/O port that is powered by that pin is also shown, for example "V_{BACKUP}, 1; I/O port P0".

In the QFN package, all internal grounds are routed to the metal pad (epad) in the package. This pad must be grounded on the PCB.

Figure 8. 68-QFN Power Connections Diagram

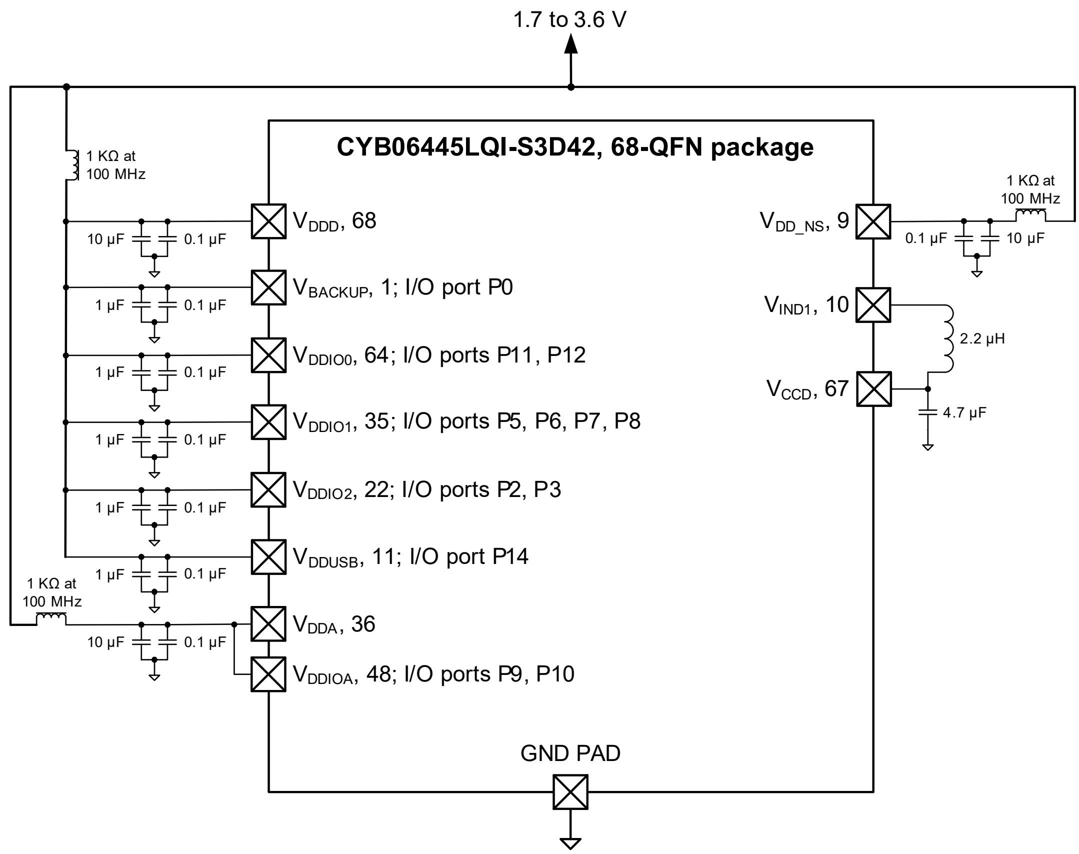
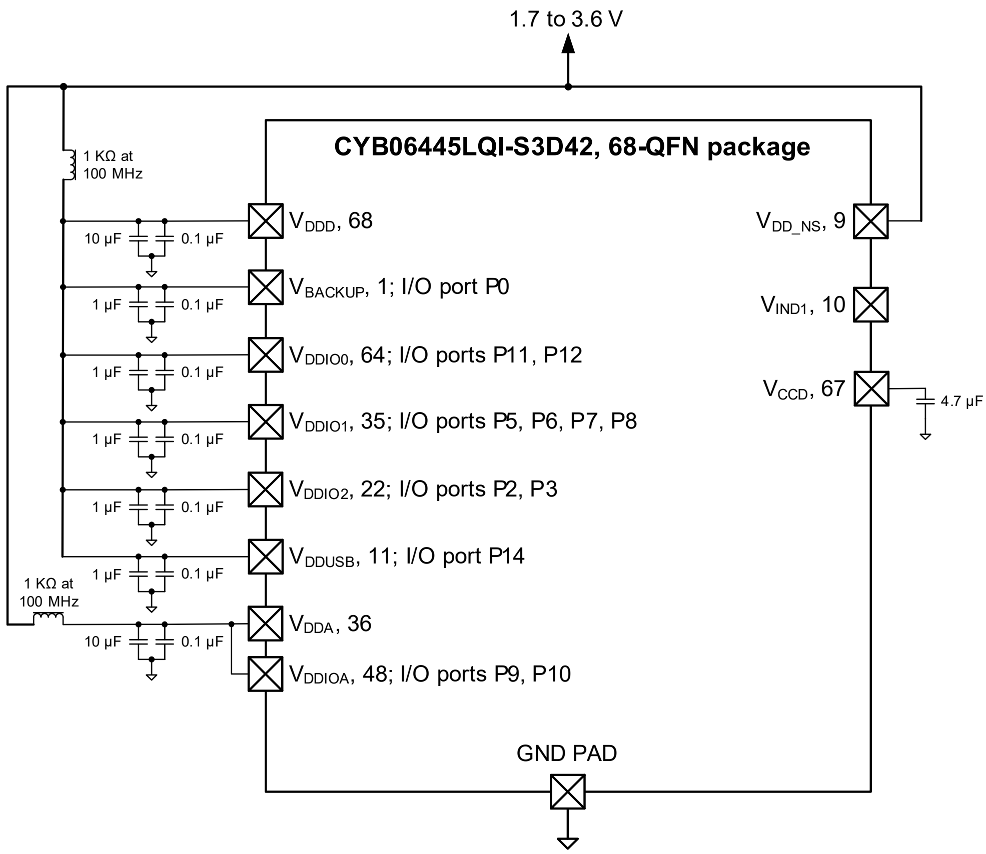


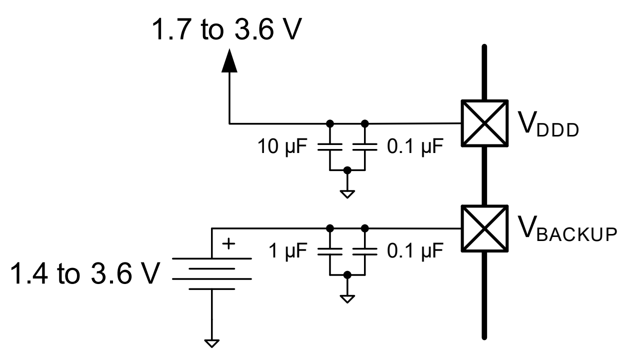
Figure 9. 68-QFN (No Buck) Power Connections Diagram



There are as many as eight V_{DDx} supply pins, depending on the package, and multiple V_{SS} ground pins. The power pins are:

- V_{DDD}: the main digital supply. It powers the low dropout (LDO) regulators.
- V_{CCD}: the main LDO output. It requires a 4.7-µF capacitor for regulation. The LDO can be turned off when V_{CCD} is driven from the switching regulator (see below). For more information, see the power system block diagram in the device technical reference manual (TRM).
- V_{DDA}: the supply for the analog peripherals.
- V_{DDIOA}: the supply for I/O ports 9 and 10. It must be connected to V_{DDA}.
- V_{DDIO0}: the supply for I/O ports 11 and 12.
- V_{DDIO1}: the supply for I/O ports 5, 6, 7, and 8.
- V_{DDIO2}: the supply for I/O ports 2 and 3.
- V_{BACKUP}: the supply for the backup domain, which includes the 32-kHz WCO and the RTC. It can be a separate supply as low as 1.4 V, for battery or supercapacitor backup, as Figure 10 shows. otherwise it is connected to V_{DDD}. It powers I/O port 0.

Figure 10. Separate Battery Connection to V_{BACKUP}



- V_{DDUSB}: the supply for the USB peripheral and the USBDP and USBDM pins. It must be 2.85 V to 3.6 V for USB operation. If USB is not used, it can be 1.7 V to 3.6 V, and the USB pins can be used as limited-capability GPIOs on I/O port 14.

Table 7 shows a summary of the I/O port supplies:

Table 7. I/O Power Supplies

Port	Supply	Alternate Supply
0	V_{BACKUP}	V_{DDD}
2, 3	V_{DDIO2}	-
5, 6, 7, 8	V_{DDIO1}	-
9, 10	V_{DDIOA}	V_{DDA}
11, 12	V_{DDIO0}	-
14	V_{DDUSB}	-

In addition to the LDO regulator, a switching regulator is included. The regulator pins are:

- V_{DD_NS}: the regulator supply.
- V_{IND1}: the regulator output. It is typically used to drive V_{CCD} through an inductor.

The V_{DD} power pins are not connected on chip. They can be connected off chip, in one or more separate nets. If separate power nets are used, they can be isolated from noise from the other nets using optional ferrite beads, as indicated in the diagrams.

No external load should be placed on V_{CCD}, or V_{IND1}, whether or not these pins are used.

There are no power pin sequencing requirements; power supplies may be brought up in any order. The power management system holds the device in reset until all power pins are at the voltage levels required for proper operation.

Note: If a battery is installed on the PCB first, V_{DDD} must be cycled for at least 50 µs. This prevents premature drain of the battery during product manufacture and storage.

Bypass capacitors must be connected to a common ground from the V_{DDx} and other pins, as indicated in the diagrams. Typical practice for systems in this frequency range is to use a 10-µF or 1-µF capacitor in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated for optimal bypassing.

All capacitors and inductors should be ±20% or better. The recommended inductor value is 2.2 µH ±20% (for example, TDK MLP2012H2R2MT0S1).

It is good practice to check the datasheets for your bypass capacitors, specifically the working voltage and the DC bias specifications. With some capacitors, the actual capacitance can decrease considerably when the applied voltage is a significant percentage of the rated working voltage.

For more information on pad layout, refer to PSoC 6 CAD libraries.

Electrical Specifications

Note: These are preliminary and subject to change.

Absolute Maximum Ratings

Table 8. Absolute Maximum Ratings[3]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID1	V_{DD_ABS}	Analog or digital supply relative to V_{SS} ($V_{SSD} = V_{SSA}$)	–0.5	–	4	V	
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to V_{SSD}	–0.5	–	1.2	V	
SID3	V_{GPIO_ABS}	GPIO voltage; V_{DDD} or V_{DDA}	–0.5	–	V_{DD} + 0.5	V	
SID4	I_{GPIO_ABS}	Current per GPIO	–25	–	25	mA	
SID5	$I_{GPIO\_injection}$	GPIO injection current per pin	–0.5	–	0.5	mA	
SID3A	ESD_HBM	Electrostatic discharge Human Body Model	2200	–	–	V	
SID4A	ESD_CDM	Electrostatic discharge Charged Device Model	500	–	–	V	
SID5A	LU	Pin current for latchup-free operation	–100	–	100	mA	

All specifications are valid for –40 °C ≤ TA ≤ 85 °C and for 1.71 V to 3.6 V except where noted. All AC specs are valid for 8-mA GPIO output drive setting except where noted.

Device-Level Specifications

All specifications are valid for –40 °C ≤ TA ≤ 85 °C and for 1.71 V to 3.6 V except where noted.

Power Supplies

Table 9. Power Supplies

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
DC Specifications							
SID6	V_{DDD}	Internal regulator	1.7	–	3.6	V	–
SID7	V_{DDA}	Analog power supply voltage. Shorted to V_{DDIOA} on PCB.	1.7	–	3.6	V	Internally unregulated supply
SID7A	V_{DDIO1}	GPIO supply for Ports 5 to 8 when present	1.7	–	3.6	V	
SID7B	V_{DDIO0}	GPIO supply for Ports 11 and 12	1.7	–	3.6	V	–
SID7E	V_{DDIO0}	Supply for eFuse programming	2.38	2.5	2.62	V	–
SID7C	V_{DDIO2}	GPIO supply for Ports 2 and 3	1.7	–	3.6	V	–
SID7D	V_{DDIOA}	GPIO supply for Ports 9 to 10. Must be connected to V_{DDA} on PCB.	1.7	–	3.6	V	–
SID7F	V_{DDUSB}	Supply for Port 14 (USB or GPIO) when present	1.7	–	3.6	V	Min supply is 2.85 V for USB
SID6B	V_{BACKUP}	Backup power and GPIO Port 0 supply when present	1.7	–	3.6	V	Min. is 1.4 V when V_{DDD} is removed.
SID8	V_{CCD1}	Output voltage (for core logic bypass)	–	1.1	–	V	High-speed mode
SID9	V_{CCD2}	Output voltage (for core logic bypass)	–	0.9	–		ULP mode. Valid for –20 to 85°C.

Note
3. Usage above the absolute maximum conditions listed in Table 8 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 9. Power Supplies *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID10	C_{EFC}	External regulator voltage (V_{CCD}) bypass	3.8	4.7	5.6	µF	X5R ceramic or better. Value for 0.8 to 1.2 V.
SID11	C_{EXC}	Power supply decoupling capacitor	–	10	–	µF	X5R ceramic or better

CPU Current and Transition Times

Table 10. CPU Current and Transition Times

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
LP RANGE POWER SPECIFICATIONS (for V_{CCD} = 1.1 V with Buck and LDO)							
Cortex-M4. Active Mode							
Execute with Cache Disabled (Flash)							
SIDF1	I_{DD1}	Execute from flash; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO and FLL. While(1).	–	2.3	3.2	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	3.1	3.6	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
			–	4.2	5.1	mA	V_{DDD} = 1.8 to 3.3 V, LDO, max at 60°C.
SIDF2	I_{DD2}	Execute from flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz.With IMO. While(1).	–	0.9	1.5	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	1.2	1.6	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
			–	1.6	2.4	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max at 60°C.
Execute with Cache Enabled							
SIDC1	I_{DD3}	Execute from cache;CM4 Active 150 MHz, CM0+ Sleep 75 MHz. IMO and FLL. Dhrystone.	–	6.3	7	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	9.7	11.2	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
			–	13.2	13.7	mA	V_{DDD} = 1.8 to 3.3 V, LDO, max at 60°C.
SIDC2	I_{DD4}	Execute from cache;CM4 Active 100 MHz, CM0+ Sleep 100MHz. IMO and FLL. Dhrystone.	–	4.8	5.8	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	7.4	8.4	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
			–	10.1	10.7	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max at 60°C.
SIDC3	I_{DD5}	Execute from cache;CM4 Active 50 MHz, CM0+ Sleep 25MHz. IMO and FLL. Dhrystone.	–	2.4	3.4	mA	V_{DDD}=3.3 V, Buck ON, Max at 60°C.
			–	3.7	4.1	mA	V_{DDD} = 1.8V, Buck ON, Max at 60°C.
			–	5.1	5.8	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max at 60°C.
SIDC4	I_{DD6}	Execute from cache;CM4 Active 8 MHz, CM0+ Sleep 8 MHz. IMO. Dhrystone.	–	0.90	1.5	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	1.27	1.75	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
			–	1.8	2.6	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max at 60°C.

Table 10. CPU Current and Transition Times *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
Cortex-M0+. Active Mode							
Execute with Cache Disabled (Flash)							
SIDF3	I_{DD7}	Execute from flash;CM4 OFF, CM0+ Active 50 MHz. With IMO and FLL. While (1).	–	2.4	3.3	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	3.2	3.7	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
			–	4.1	4.8	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max at 60°C.
SIDF4	I_{DD8}	Execute from flash;CM4 OFF, CM0+ Active 8 MHz. With IMO. While (1).	–	0.8	1.5	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	1.1	1.6	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
			–	1.45	1.9	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max at 60°C.
Execute with Cache Enabled							
SIDC5	I_{DD9}	Execute from cache;CM4 OFF, CM0+ Active 100 MHz. With IMO and FLL. Dhrystone.	–	3.8	4.5	mA	V_{DDD} = 3.3V, Buck ON, Max at 60°C.
			–	5.9	6.5	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
			–	7.7	8.2	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max at 60°C.
SIDC6	I_{DD10}	Execute from cache;CM4 OFF, CM0+ Active 8 MHz. With IMO. Dhrystone.	–	0.80	1.3	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	1.2	1.7	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
			–	1.41	2	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max at 60°C.
Cortex-M4. Sleep Mode							
SIDS1	I_{DD11}	CM4 Sleep 100 MHz, CM0+ Sleep 25 MHz. With IMO and FLL.	–	1.5	2.2	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	2.2	2.7	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
			–	2.9	3.5	mA	V_{DDD} = 1.8 to 3.3 V, LDO, max at 60°C.
SIDS2	I_{DD12}	CM4 Sleep 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL.	–	1.20	1.9	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	1.70	2.2	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
			–	2.20	2.8	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max at 60°C.
SIDS3	I_{DD13}	CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz. With IMO.	–	0.7	1.3	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	0.96	1.5	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
			–	1.22	2	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max at 60°C.

Table 10. CPU Current and Transition Times *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
Cortex-M0+. Sleep Mode							
SIDS4	I_{DD14}	CM4 Off, CM0+ Sleep 50 MHz. With IMO and FLL.	–	1.3	2	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	1.94	2.4	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
			–	2.57	3.2	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max at 60°C.
SIDS5	I_{DD15}	CM4 Off, CM0+ Sleep 8 MHz. With IMO.	–	0.7	1.3	mA	V_{DDD} = 3.3V, Buck ON, Max at 60°C.
			–	0.95	1.5	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
			–	1.25	2	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max at 60°C.
Cortex-M4. Minimum Regular Current Mode							
SIDLPA1	I_{DD16}	Execute from flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While (1).	–	0.85	1.5	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	1.18	1.65	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
			–	1.63	2.4	mA	V_{DDD} = 1.8 to 3.3 V, LDO, max at 60°C.
SIDLPA2	I_{DD17}	Execute from cache; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. Dhrystone.	–	0.90	1.5	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	1.27	1.75	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
			–	1.77	2.5	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max at 60°C.
Cortex-M0+. Minimum Regulator Current Mode							
SIDLPA3	I_{DD18}	Execute from flash; CM4 OFF, CM0+ Active 8 MHz. With IMO. While (1).	–	0.8	1.4	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	1.14	1.6	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
			–	1.6	2.4	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max at 60°C.
SIDLPA4	I_{DD19}	Execute from cache; CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone	–	0.8	1.4	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	1.15	1.65	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
			–	1.62	2.4	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max at 60°C.
Cortex-M4. Minimum Regulator Current Mode							
SIDLPS1	I_{DD20}	CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz. With IMO.	–	0.65	1.1	mA	V_{DDD}=3.3 V, Buck ON, Max at 60°C.
			–	0.95	1.5	mA	V_{DDD}=1.8 V, Buck ON, Max at 60°C.
			–	1.31	2.1	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max at 60°C.

Table 10. CPU Current and Transition Times *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
Cortex-M0+. Minimum Regulator Current Mode							
SIDLPS3	I_{DD22}	CM4 Off, CM0+ Sleep 8 MHz. With IMO.	–	0.64	1.1	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	0.93	1.45	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
			–	1.29	2	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max at 60°C.
ULP RANGE POWER SPECIFICATIONS (for V_{CCD} = 0.9 V using the Buck). ULP mode is valid from –20 to +85 °C.							
Cortex-M4. Active Mode							
Execute with Cache Disabled (Flash)							
SIDF5	I_{DD3}	Execute from flash; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO and FLL. While(1).	–	1.7	2.2	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	2.1	2.4	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
SIDF6	I_{DD4}	Execute from flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While (1).	–	0.56	0.8	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	0.75	1	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
Execute with Cache Enabled							
SIDC8	I_{DD10}	Execute from cache; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO and FLL. Dhrystone.	–	1.6	2.2	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	2.4	2.7	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
SIDC9	I_{DD11}	Execute from cache; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. Dhrystone.	–	0.65	0.8	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	0.8	1.1	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
Cortex-M0+. Active Mode							
Execute with Cache Disabled (Flash)							
SIDF7	I_{DD16}	Execute from flash; CM4 OFF, CM0+ Active 25 MHz. With IMO and FLL. Write(1).	–	1.00	1.4	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	1.34	1.6	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
SIDF8	I_{DD17}	Execute from flash; CM4 OFF, CM0+ Active 8 MHz. With IMO. While(1).	–	0.54	0.75	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	0.73	1	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
Execute with Cache Enabled							
SIDC10	I_{DD18}	Execute from cache; CM4 OFF, CM0+ Active 25 MHz. With IMO and FLL. Dhrystone.	–	0.91	1.25	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	1.34	1.6	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
SIDC11	I_{DD19}	Execute from cache; CM4 OFF, CM0+ Active 8 MHz. With IMO. Dhrystone.	–	0.51	0.72	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	0.73	0.95	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
Cortex-M4. Sleep Mode							
SIDS7	I_{DD21}	CM4 Sleep 50 MHz, CM0+ Sleep 25 MHz. With IMO and FLL.	–	0.76	1.1	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	1.1	1.4	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.

Table 10. CPU Current and Transition Times *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SIDS8	I_{DD22}	CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz. With IMO.	–	0.42	0.65	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	0.59	0.8	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
Cortex-M0+. Sleep Mode							
SIDS9	I_{DD23}	CM4 Off, CM0+ Sleep 25 MHz. With IMO and FLL.	–	0.62	0.9	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	0.88	1.1	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
SIDS10	I_{DD24}	CM4 Off, CM0+ Sleep 8 MHz. With IMO.	–	0.41	0.6	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	0.58	0.8	mA	V_{DDD} = 1.8°V, Buck ON, Max at 60°C.
Cortex-M4. Minimum Regulator Current Mode							
SIDLPA5	I_{DD25}	Execute from flash. CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While(1).	–	0.52	0.75	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	0.76	1	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
SIDLPA6	I_{DD26}	Execute from cache. CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. Dhrystone.	–	0.54	0.76	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	0.78	1	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
Cortex-M0+. Minimum Regulator Current Mode							
SIDLPA7	I_{DD27}	Execute from flash. CM4 OFF, CM0+ Active 8 Hz. With IMO. While (1).	–	0.51	0.75	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	0.75	1	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
SIDLPA8	I_{DD28}	Execute from cache. CM4 OFF, CM0+ Active 8 MHz. With IMO. Dhrystone.	–	0.48	0.7	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	0.7	0.95	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
Cortex-M4. Minimum Regulator Current Mode							
SIDLPS5	I_{DD29}	CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz. With IMO.	–	0.4	0.6	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	0.57	0.8	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
Cortex-M0+. Minimum Regulator Current Mode							
SIDLPS7	I_{DD31}	CM4 Off, CM0+ Sleep 8 MHz. With IMO.	–	0.39	0.6	mA	V_{DDD} = 3.3 V, Buck ON, Max at 60°C.
			–	0.56	0.8	mA	V_{DDD} = 1.8 V, Buck ON, Max at 60°C.
Deep Sleep Mode							
SIDDS1	I_{DD33A}	With internal Buck enabled and 64-KB SRAM retention	–	7	–	µA	Max value is at 85 °C
SIDDS1_B	I_{DD33A_B}	With internal Buck enabled and 64-KB SRAM retention	–	7	–	µA	Max value is at 60°C.
SIDDS2	I_{DD33B}	With internal Buck enabled and 256-KB SRAM retention	–	9	–	µA	Max value is at 85 °C
SIDDS2_B	I_{DD33B_B}	With internal Buck enabled and 256-KB SRAM retention	–	9	–	µA	Max value is at 60°C.

Table 10. CPU Current and Transition Times *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
Hibernate Mode							
SIDHIB1	I_{DD34}	V_{DDD} = 1.8 V	–	300	–	nA	No clocks running
SIDHIB2	I_{DD34A}	V_{DDD} = 3.3 V	–	800	–	nA	No clocks running
Power Mode Transition Times							
SID12	T_{LPACT_ACT}	Minimum Regulator Current to LP transition time	–	–	35	µs	Including PLL lock time
SID13	T_{DS_LPACT}	Deep Sleep to LP transition time	–	–	15	µs	Guaranteed by design
SID14	T_{HIB_ACT}	Hibernate to LP transition time	–	500	–	µs	Including PLL lock time

XRES

Table 11. XRES

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
XRES (Active Low) Specifications							
XRES AC Specifications							
SID15	T_{XRES_ACT}	POR or XRES release to Active transition time	–	750	–	µs	Normal mode, 50 MHz CM0+.
SID16	T_{XRES_PW}	XRES pulse width	5	–	–	µs	–
XRES DC Specifications							
SID17	T_{XRES_IDD}	I_{DD} when XRES asserted	–	300	–	nA	V_{DDD} = 1.8 V
SID17A	$T_{XRES\_IDD\_1}$	I_{DD} when XRES asserted	–	800	–	nA	V_{DDD} = 3.3 V
SID77	V_{IH}	Input voltage HIGH threshold	0.7 * V_{DD}	–	–	V	CMOS input
SID78	V_{IL}	Input voltage LOW threshold	–	–	0.3 * V_{DD}	V	CMOS input
SID80	C_{IN}	Input capacitance	–	3	–	pF	–
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	–
SID82	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–

GPIO

Table 12. GPIO Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
GPIO DC Specifications							
SID57	V_{IH}	Input voltage HIGH threshold	0.7 * V_{DD}	–	–	V	CMOS Input
SID57A	I_{IHS}	Input current when Pad > V_{DDIO} for OVT inputs	–	–	10	µA	Per I^{2}C Spec
SID58	V_{IL}	Input voltage LOW threshold	–	–	0.3 * V_{DD}	V	CMOS Input
SID241	V_{IH}	LVTTL input, V_{DD} < 2.7 V	0.7 * V_{DD}	–	–	V	–
SID242	V_{IL}	LVTTL input, V_{DD} < 2.7 V	–	–	0.3 * V_{DD}	V	–
SID243	V_{IH}	LVTTL input, V_{DD} ≥ 2.7 V	2.0	–	–	V	–
SID244	V_{IL}	LVTTL input, V_{DD} ≥ 2.7 V	–	–	0.8	V	–
SID59	V_{OH}	Output voltage HIGH level	V_{DD} – 0.5	–	–	V	I_{OH} = 8 mA
SID62A	V_{OL}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 8 mA
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	–
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DD} = 3.0 V
SID66	C_{IN}	Input capacitance	–	–	5	pF	–
SID67	V_{HYSTTL}	Input hysteresis LVTTL V_{DD} > 2.7 V	100	0	–	mV	–
SID68	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05*V_{DD}	–	–	mV	–
SID69	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–
SID69A	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	–
GPIO AC Specifications							
SID70	T_{RISEF}	Rise time in Fast Strong Mode. 10% to 90% of V_{DD}.	–	–	2.5	ns	Cload = 15 pF, 8mA drive strength
SID71	T_{FALLF}	Fall time in Fast Strong Mode. 10% to 90% of V_{DD}.	–	–	2.5	ns	Cload = 15 pF, 8 mA drive strength
SID72	T_{RISES_1}	Rise time in Slow Strong Mode. 10% to 90% of V_{DD}.	52	–	142	ns	Cload = 15 pF, 8 mA drive strength, V_{DD} ≤ 2.7 V
SID72A	T_{RISES_2}	Rise time in Slow Strong Mode. 10% to 90% of V_{DD}.	48	–	102	ns	Cload = 15 pF, 8 mA drive strength, 2.7 V < V_{DD} ≤ 3.6 V
SID73	T_{FALLS_1}	Fall time in Slow Strong Mode. 10% to 90% of V_{DD}.	44	–	211	ns	Cload = 15 pF, 8 mA drive strength, V_{DD} ≤ 2.7 V
SID73A	T_{FALLS_2}	Fall time in Slow Strong Mode. 10% to 90% of V_{DD}.	42	–	93	ns	Cload = 15 pF, 8 mA drive strength, 2.7 V < V_{DD} ≤ 3.6 V
SID73G	T_{FALL_I2C}	Fall time (30% to 70% of V_{DD}) in Slow Strong mode.	20 * V_{DDIO} / 5.5	–	250	ns	Cload = 10 pF to 400 pF, 8-mA drive strength
SID74	$F_{GPIOUT1}$	GPIO Fout. Fast Strong mode.	–	–	100	MHz	90/10%, 15-pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO Fout; Slow Strong mode.	–	–	1.5	MHz	90/10%, 15-pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO Fout; Fast Strong mode.	–	–	100	MHz	90/10%, 25-pF load, 60/40 duty cycle

Table 12. GPIO Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID245	$F_{GPIOUT4}$	GPIO Fout; Slow Strong mode.	–	–	1.3	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V_{DD} ≤ 3.6 V	–	–	100	MHz	90/10% V_{IO}

Analog Peripherals

Low-Power (LP) Comparator

Table 13. Low-Power (LP) Comparator Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
LP Comparator DC Specifications							
SID84	$V_{OFFSET1}$	Input offset voltage. Normal power mode.	–10	–	10	mV	–
SID85A	$V_{OFFSET2}$	Input offset voltage. Low-power mode.	–25	±12	25	mV	–
SID85B	$V_{OFFSET3}$	Input offset voltage. Ultra low-power mode.	–25	±12	25	mV	–
SID86	V_{HYST1}	Hysteresis when enabled in Normal mode	–	–	60	mV	–
SID86A	V_{HYST2}	Hysteresis when enabled in Low-power mode	–	–	80	mV	–
SID87	V_{ICM1}	Input common mode voltage in Normal mode	0	–	V_{DDIO1} – 0.1	V	–
SID247	V_{ICM2}	Input common mode voltage in Low power mode	0	–	V_{DDIO1} – 0.1	V	–
SID247A	V_{ICM3}	Input common mode voltage in Ultra low power mode	0	–	V_{DDIO1} – 0.1	V	–
SID88	CMRR	Common mode rejection ratio in Normal power mode	50	–	–	dB	–
SID89	I_{CMP1}	Block current, Normal mode	–	–	150	µA	–
SID248	I_{CMP2}	Block current, Low-power mode	–	–	10	µA	–
SID259	I_{CMP3}	Block current in Ultra low-power mode	–	0.3	0.85	µA	–
SID90	ZCMP	DC input impedance of comparator	35	–	–	MΩ	–
LP Comparator AC Specifications							
SID91	T_{RESP1}	Response time, Normal mode, 100 mV overdrive	–	–	100	ns	–
SID258	T_{RESP2}	Response time, Low power mode, 100 mV overdrive	–	–	1000	ns	–
SID92	T_{RESP3}	Response time, Ultra-low power mode, 100 mV overdrive	–	–	20	µs	–
SID92E	T_CMP_EN1	Time from Enabling to operation	–	–	10	µs	Normal and low-power modes
SID92F	T_CMP_EN2	Time from Enabling to operation	–	–	50	µs	Ultra-low-power mode

Temperature Sensor

Table 14. Temperature Sensor Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID93	$T_{SENSACC}$	Temperature sensor accuracy	–5	±1	5	°C	–40 to +85 °C

Internal Reference

Table 15. Internal Reference Specification

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID93R	V_{REFBG}	–	1.188	1.2	1.212	V	–

SAR ADC

Table 16. 12-bit SAR ADC DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID94	A_RES	SAR ADC Resolution	–	–	12	bits	–
SID95	A_CHNLS_S	Number of channels - single ended	–	–	16	–	8 full speed
SID96	A-CHNKS_D	Number of channels - differential	–	–	8	–	Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–	–	Yes
SID98	A_GAINERR	Gain error	–	–	±0.2	%	With external reference.
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V reference
SID100	A_ISAR_1	Current consumption at 1 Msps	–	–	1	mA	At 1 Msps. External bypass cap.
SID100A	A_ISAR_2	Current consumption at 1 Msps. Reference = V_{DD}	–	–	1.25	mA	At 1 Msps. External bypass cap.
SID101	A_VINS	Input voltage range - single-ended	Vss	–	V_{DDA}	V	–
SID102	A_VIND	Input voltage range - differential	Vss	–	V_{DDA}	V	–
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	–
SID104	A_INCAP	Input capacitance	–	–	10	pF	–

Table 17. 12-bit SAR ADC AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
12-bit SAR ADC AC Specifications							
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	–
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
One Megasample per second mode							
SID108	A_SAMP_1	Sample rate with external reference bypass cap.	–	–	1	Msps	–
SID108A	A_SAMP_2	Sample rate with no bypass cap; Reference = V_{DD}	–	–	250	ksps	–
SID108B	A_SAMP_3	Sample rate with no bypass cap. Internal reference.	–	–	100	ksps	–
SID109	A_SINAD	Signal-to-noise and Distortion ratio (SINAD). V_{DDA} = 2.7 to 3.6 V, 1 Msps.	64	–	–	dB	Fin = 10 kHz
SID111A	A_INL	Integral non linearity. V_{DDA} = 2.7 to 3.6 V, 1 Msps	–2	–	2	LSB	Measured with internal V_{REF} = 1.2 V and bypass cap.
SID111B	A_INL	Integral non-linearity. V_{DDA} = 2.7 to 3.6 V, 1 Msps	–4	–	4	LSB	Measured with external $V_{REF} \geq 1$ V and V_{IN} common mode < 2 * V_{REF}
SID112A	A_DNL	Differential non linearity. V_{DDA} = 2.7 to 3.6 V, 1 Msps	–1	–	1.4	LSB	Measured with internal V_{REF} = 1.2 V and bypass cap.
SID112B	A_DNL	Differential non linearity. V_{DDA} = 2.7 to 3.6 V, 1 Msps	–1	–	1.7	LSB	Measured with external $V_{REF} \geq 1$ V and V_{IN} common mode < 2 * V_{REF}
SID113	A_THD	Total harmonic distortion. V_{DDA} = 2.7 to 3.6 V, 1 Msps.	–	–	–65	dB	Fin = 10 kHz

CSD

Table 18. CapSense Sigma-Delta (CSD) Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
CSD V2 Specifications							
SYS.PER#3	V_{DD_RIPPLE}	Max allowed ripple on power supply, DC to 10 MHz	–	–	±50	mV	V_{DDA} > 2 V (with ripple), 25 °C T_A, Sensitivity = 0.1 pF
SYS.PER#16	$V_{DD\_RIPPLE\_1.8}$	Max allowed ripple on power supply, DC to 10 MHz	–	–	±25	mV	V_{DDA} > 1.75 V (with ripple), 25 ° C T_A, Parasitic Capacitance (C_P) < 20 pF, Sensitivity ≥ 0.4 pF
SID.CSD.BLK	I_{CSD}	Maximum block current			4500	µA	–
SID.CSD#15	V_{REF}	Voltage reference for CSD and Comparator	0.6	1.2	V_{DDA} – 0.6	V	$V_{DDA} – V_{REF}$ ≥ 0.6 V
SID.CSD#15A	V_{REF_EXT}	External Voltage reference for CSD and Comparator	0.6		V_{DDA} – 0.6	V	$V_{DDA} – V_{REF}$ ≥ 0.6 V
SID.CSD#16	$I_{DAC1IDD}$	IDAC1 (7-bits) block current	–	–	1900	µA	–
SID.CSD#17	$I_{DAC2IDD}$	IDAC2 (7-bits) block current	–	–	1900	µA	–
SID308	V_{CSD}	Voltage range of operation	1.7	–	3.6	V	1.71 to 3.6 V
SID308A	$V_{COMPIDAC}$	Voltage compliance range of IDAC	0.6	–	V_{DDA} – 0.6	V	$V_{DDA} – V_{REF}$ ≥ 0.6 V
SID309	$I_{DAC1DNL}$	DNL	–1	–	1	LSB	–
SID310	$I_{DAC1INL}$	INL	–3	–	3	LSB	If V_{DDA} < 2 V then for LSB of 2.4 µA or less
SID311	$I_{DAC2DNL}$	DNL	–1	–	1	LSB	–
SID312	$I_{DAC2INL}$	INL	–3	–	3	LSB	If V_{DDA} < 2 V then for LSB of 2.4 µA or less
SNRC of the following is Ratio of counts of finger to noise. Guaranteed by characterization.							
SID313_1A	SNRC_1	SRSS Reference. IMO + FLL Clock Source. 0.1-pF sensitivity.	5	–	–	Ratio	9.5 pF max. capacitance
SID313_1B	SNRC_2	SRSS Reference. IMO + FLL Clock Source. 0.3-pF sensitivity.	5	–	–	Ratio	31 pF max. capacitance
SID313_1C	SNRC_3	SRSS Reference. IMO + FLL Clock Source. 0.6-pF sensitivity.	5	–	–	Ratio	61 pF max. capacitance
SID313_2A	SNRC_4	PASS Reference. IMO + FLL Clock Source. 0.1-pF sensitivity.	5	–	–	Ratio	12 pF max. capacitance
SID313_2B	SNRC_5	PASS Reference. IMO + FLL Clock Source. 0.3-pF sensitivity.	5	–	–	Ratio	47 pF max. capacitance
SID313_2C	SNRC_6	PASS Reference. IMO + FLL Clock Source. 0.6-pF sensitivity.	5	–	–	Ratio	86 pF max. capacitance
SID313_3A	SNRC_7	PASS Reference. IMO + PLL Clock Source. 0.1-pF sensitivity.	5	–	–	Ratio	27 pF max. capacitance
SID313_3B	SNRC_8	PASS Reference. IMO + PLL Clock Source. 0.3-pF sensitivity.	5	–	–	Ratio	86 pF max. capacitance
SID313_3C	SNRC_9	PASS Reference. IMO + PLL Clock Source. 0.6-pF sensitivity.	5	–	–	Ratio	168 pF Max. capacitance

Table 18. CapSense Sigma-Delta (CSD) Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID314	$IDAC_{1CRT1}$	Output current of IDAC1 (7 bits) in low range	4.2		5.7	µA	LSB = 37.5-nA typ.
SID314A	$IDAC_{1CRT2}$	Output current of IDAC1 (7 bits) in medium range	33.7		45.6	µA	LSB = 300-nA typ.
SID314B	$IDAC_{1CRT3}$	Output current of IDAC1 (7 bits) in high range	270		365	µA	LSB = 2.4-µA typ.
SID314C	$IDAC_{1CRT12}$	Output current of IDAC1 (7 bits) in low range, 2X mode	8		11.4	µA	LSB = 37.5-nA typ. 2X output stage
SID314D	$IDAC_{1CRT22}$	Output current of IDAC1 (7 bits) in medium range, 2X mode	67		91	µA	LSB = 300-nA typ. 2X output stage
SID314E	$IDAC_{1CRT32}$	Output current of IDAC1 (7 bits) in high range, 2X mode. V_{DDA} > 2 V	540		730	µA	LSB = 2.4-µA typ. 2X output stage
SID315	$IDAC_{2CRT1}$	Output current of IDAC2 (7 bits) in low range	4.2		5.7	µA	LSB = 37.5-nA typ.
SID315A	$IDAC_{2CRT2}$	Output current of IDAC2 (7 bits) in medium range	33.7		45.6	µA	LSB = 300-nA typ.
SID315B	$IDAC_{2CRT3}$	Output current of IDAC2 (7 bits) in high range	270		365	µA	LSB = 2.4-µA typ.
SID315C	$IDAC_{2CRT12}$	Output current of IDAC2 (7 bits) in low range, 2X mode	8		11.4	µA	LSB = 37.5-nA typ. 2X output stage
SID315D	$IDAC_{2CRT22}$	Output current of IDAC2 (7 bits) in medium range, 2X mode	67		91	µA	LSB = 300-nA typ. 2X output stage
SID315E	$IDAC_{2CRT32}$	Output current of IDAC2 (7 bits) in high range, 2X mode. V_{DDA} > 2V	540		730	µA	LSB = 2.4-µA typ. 2X output stage
SID315F	$IDAC_{3CRT13}$	Output current of IDAC in 8-bit mode in low range	8		11.4	µA	LSB = 37.5-nA typ.
SID315G	$IDAC_{3CRT23}$	Output current of IDAC in 8-bit mode in medium range	67		91	µA	LSB = 300-nA typ.
SID315H	$IDAC_{3CRT33}$	Output current of IDAC in 8-bit mode in high range. V_{DDA} > 2V	540		730	µA	LSB = 2.4-µA typ.
SID320	$IDAC_{OFFSET}$	All zeroes input	–	–	1	LSB	Polarity set by Source or Sink
SID321	$IDAC_{GAIN}$	Full-scale error less offset	–	–	±15	%	LSB = 2.4-µA typ.
SID322	$IDAC_{MISMATCH1}$	Mismatch between IDAC1 and IDAC2 in Low mode	–	–	9.2	LSB	LSB = 37.5-nA typ.
SID322A	$IDAC_{MISMATCH2}$	Mismatch between IDAC1 and IDAC2 in Medium mode	–	–	6	LSB	LSB = 300-nA typ.
SID322B	$IDAC_{MISMATCH3}$	Mismatch between IDAC1 and IDAC2 in High mode	–	–	5.8	LSB	LSB = 2.4-µA typ.
SID323	$IDAC_{SET8}$	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID324	$IDAC_{SET7}$	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

Table 19. CSD ADC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
CSDv2 ADC Specifications							
SIDA94	A_RES	Resolution	–	–	10	bits	Auto-zeroing is required every millisecond
SID95	A_CHNLS_S	Number of channels - single ended	–	–	–	16	–
SIDA97	A-MONO	Monotonicity	–	–	Yes	–	V_{REF} mode
SIDA98	A_GAINERR_VREF	Gain error	–	0.6	–	%	Reference Source: SRSS (V_{REF} = 1.20 V, V_{DDA} < 2.2 V), (V_{REF} = 1.6 V, 2.2 V < V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)
SIDA98A	A_GAINERR_VDDA	Gain error	–	0.2	–	%	Reference Source: SRSS (V_{REF}=1.20 V, V_{DDA} < 2.2V), (V_{REF}=1.6 V, 2.2 V < V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)
SIDA99	A_OFFSET_VREF	Input offset voltage	–	0.5	–	LSb	After ADC calibration, Ref. Src = SRSS, (V_{REF} = 1.20 V, V_{DDA} < 2.2 V), (V_{REF} = 1.6 V, 2.2 V < V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)
SIDA99A	A_OFFSET_VDDA	Input offset voltage	–	0.5	–	LSb	After ADC calibration, Ref. Src = SRSS, (V_{REF} = 1.20 V, V_{DDA} < 2.2 V), (V_{REF} = 1.6 V, 2.2 V < V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)
SIDA100	A_ISAR_VREF	Current consumption	–	0.3	–	mA	CSD ADC Block current
SIDA100A	A_ISAR_VDDA	Current consumption	–	0.3	–	mA	CSD ADC Block current
SIDA101	A_VINS_VREF	Input voltage range - single ended	V_{SSA}	–	V_{REF}	V	(V_{REF} = 1.20 V, V_{DDA} < 2.2 V), (V_{REF} = 1.6 V, 2.2 V < V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)
SIDA101A	A_VINS_VDDA	Input voltage range - single ended	V_{SSA}	–	V_{DDA}	V	(V_{REF} = 1.20 V, V_{DDA} < 2.2 V), ($V_{RE F}$ = 1.6 V, 2.2 V < V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)
SIDA103	A_INRES	Input charging resistance	–	15	–	kΩ	–
SIDA104	A_INCAP	Input capacitance	–	41	–	pF	–
SIDA106	A_PSRR	Power supply rejection ratio (DC)	–	60	–	dB	–
SIDA107	A_TACQ	Sample acquisition time	–	10	–	µs	Measured with 50-Ω source impedance. 10 µs is default software driver acquisition time setting. Settling to within 0.05%.
SIDA108	A_CONV8	Conversion time for 8-bit resolution at conversion rate = Fhclk / (2"(N + 2)). Clock frequency = 50 MHz.	–	25	–	µs	Does not include acquisition time.
SIDA108A	A_CONV10	Conversion time for 10-bit resolution at conversion rate = Fhclk / (2"(N + 2)). Clock frequency = 50 MHz.	–	60	–	µs	Does not include acquisition time.

Table 19. CSD ADC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SIDA109	A_SND_VRE	Signal-to-noise and Distortion ratio (SINAD)	–	57	–	dB	Measured with 50-Ω source impedance
SIDA109A	A_SND_VDDA	Signal-to-noise and Distortion ratio (SINAD)	–	52	–	dB	Measured with 50-Ω source impedance
SIDA111	A_INL_VREF	Integral non-linearity. 11.6 ksps	–	–	2	LSB	Measured with 50-Ω source impedance
SIDA111A	A_INL_VDDA	Integral non-linearity. 11.6 ksps	–	–	2	LSB	Measured with 50-Ω source impedance
SIDA112	A_DNL_VREF	Differential non-linearity. 11.6 ksps	–	–	1	LSB	Measured with 50-Ω source impedance
SIDA112A	A_DNL_VDDA	Differential non-linearity. 11.6 ksps	–	–	1	LSB	Measured with 50-Ω source impedance

Digital Peripherals

Timer/Counter/PWM

Table 20. Timer/Counter/PWM (TCPWM) Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.1	I_{TCPWM1}	Block current consumption at 8 MHz	–	–	70	µA	All modes (TCPWM)
SID.TCPWM.2	I_{TCPWM2}	Block current consumption at 24 MHz	–	–	180	µA	All modes (TCPWM)
SID.TCPWM.2A	I_{TCPWM3}	Block current consumption at 50 MHz	–	–	270	µA	All modes (TCPWM)
SID.TCPWM.2B	I_{TCPWM4}	Block current consumption at 100 MHz	–	–	540	µA	All modes (TCPWM)
SID.TCPWM.3	$TCPWM_{FREQ}$	Operating frequency	–	–	100	MHz	Maximum = 100 MHz
SID.TCPWM.4	$TPWM_{ENEXT}$	Input trigger pulse width for all trigger events	2/Fc	–	–	ns	Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected. Fc is counter operating frequency.
SID.TCPWM.5	$TPWM_{EXT}$	Output trigger pulse widths	1.5/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs
SID.TCPWM.5A	TC_{RES}	Resolution of counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–	ns	Minimum pulse width of PWM output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	2/Fc	–	–	ns	Minimum pulse width between Quadrature phase inputs. Delays from pins should be similar.

Serial Communication Block (SCB)

Table 21. Serial Communication Block (SCB) Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
Fixed I^2C DC Specifications							
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	30	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	80	µA	–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	180	µA	–
SID152	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	–	1.7	µA	At 60°C.
Fixed I^2C AC Specifications							
SID153	F_{I2C1}	Bit Rate	–	–	1	Mbps	–
Fixed UART DC Specifications							
SID160	I_{UART1}	Block current consumption at 100 kbps	–	–	30	µA	–
SID161	I_{UART2}	Block current consumption at 1000 kbps	–	–	180	µA	–
Fixed UART AC Specifications							
SID162A	F_{UART1}	Bit Rate	–	–	3	Mbps	ULP Mode
SID162B	F_{UART2}		–	–	8		LP Mode
Fixed SPI DC Specifications							
SID163	I_{SPI1}	Block current consumption at 1 Mbps	–	–	220	µA	–

Table 21. Serial Communication Block (SCB) Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID164	I_{SPI2}	Block current consumption at 4 Mbps	–	–	340	µA	–
SID165	I_{SPI3}	Block current consumption at 8 Mbps	–	–	360	µA	–
SID165A	I_{SP14}	Block current consumption at 25 Mbps	–	–	800	µA	–
Fixed SPI AC Specifications for LP Mode (1.1 V) unless noted otherwise.							
SID166	F_{SPI}	SPI Operating frequency externally clocked slave	–	–	25	MHz	12-MHz max for ULP (0.9 V) mode
SID166B	F_{SPI_EXT}	SPI operating frequency master (F_{scb} is SPI clock).	–	–	F_{scb}/4	MHz	F_{scb} max is 100 MHz in LP (1.1 V) mode, 25 MHz in ULP mode.
SID166A	F_{SPI_IC}	SPI slave internally clocked	–	–	15	MHz	5 MHz max for ULP (0.9 V) mode
Fixed SPI Master mode AC Specifications for LP Mode (1.1 V) unless noted otherwise.							
SID167	T_{DMO}	MOSI valid after SClock driving edge	–	–	12	ns	20 ns max for ULP (0.9 V) mode
SID168	T_{DSI}	MISO valid before SClock capturing edge	5	–	–	ns	Full clock, late MISO sampling
SID169	T_{HMO}	MOSI data hold time	0	–	–	ns	Referred to Slave capturing edge
Fixed SPI Slave mode AC Specifications for LP Mode (1.1 V) unless noted otherwise.							
SID170	T_{DMI}	MOSI valid before Sclock capturing edge	5	–	–	ns	–
SID171A	T_{DSO_EXT}	MISO valid after Sclock driving edge in Ext. Clk. mode	–	–	20	ns	35 ns max. for ULP (0.9 V) mode
SID171	T_{DSO}	MISO valid after Sclock driving edge in Internally Clk. mode	–	–	TDSO_EXT + 3 * Tscb	ns	Tscb is Serial Comm. Block clock period.
SID171B	T_{DSO}	MISO Valid after Sclock driving edge in Internally Clk. Mode with median filter enabled.	–	–	TDSO_EXT + 4 * Tscb	ns	Tscb is Serial Comm. Block clock period.
SID172	T_{HSO}	Previous MISO data hold time	5	–	–	ns	–
SID172A	$TSSEL_{SCK1}$	SSEL Valid to first SCK valid edge	65	–	–	ns	–
SID172B	$TSSEL_{SCK2}$	SSEL Hold after Last SCK valid edge	65	–	–	ns	–

LCD Specifications

Table 22. LCD Direct Drive DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID154	$I_{LCDLOW1}$	Operating current with 100-kHz LCD block clock in ULP mode in Deep Sleep	–	90	–	µA	32×4 small display. 30-Hz. PWM mode. Slow slew rate. 460 kΩ series resistors
SID154A	$I_{LCDLOW2}$	Operating current with 32- kHz LCD block clock in ULP mode in Deep Sleep	–	50	–	µA	32×4 small display. 30-Hz. PWM mode. Slow slew rate. 460 kΩ series resistors
SID155	C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	–
SID156	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	–
SID157	I_{LCDOP1}	PWM Mode current. 3.3 V bias. 8 MHz IMO. 25°C.	–	0.6	–	mA	32 × 4 segments 50 Hz
SID158	I_{LCDOP2}	PWM Mode current. 3.3 V bias. 8 MHz IMO. 25°C.	–	0.5	–	mA	32 × 4 segments 50 Hz

Table 23. LCD Direct Drive AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID159	F_{LCD}	LCD frame rate	10	50	150	Hz	–

Memory

Table 24. Flash Specifications[4]

All specifications are valid for –40 °C ≤ T_A ≤ 85 °C and 1.71 V to 3.6 V, except where noted.

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Flash DC Specifications							
SID173A	IPE	Erase and Program current	–	–	6	mA	
Flash AC Specifications							
SID174	$T_{ROWWRITE}$	Row write time (erase and program)	–	–	16	ms	Row = 512 bytes
SID175	$T_{ROWERASE}$	Row erase time	–	–	11	ms	–
SID176	$T_{ROWPROGRAM}$	Row program time after erase	–	–	5	ms	–
SID178	$T_{BULKERASE}$	Bulk erase time (512 KB)	–	–	11	ms	–
SID179	$T_{SECTORERASE}$	Sector erase time (256 KB)	–	–	11	ms	512 rows per sector
SID178S	$T_{SSERIAE}$	Subsector erase time	–	–	11	ms	8 rows per subsector
SID179S	$T_{SSWRITE}$	Subsector write time; 1 erase plus 8 program times	–	–	51	ms	–
SID180S	T_{SWRITE}	Sector write time; 1 erase plus 512 program times	–	–	2.6	seconds	–
SID180	$T_{DEVPROG}$	Total device write time	–	–	7.5	seconds	–
SID181	F_{END}	Flash endurance	100K	–	–	cycles	–
SID182	F_{RET1}	Flash retention. T_A ≤ 25 °C, 100K P/E cycles	10	–	–	years	–
SID182A	F_{RET2}	Flash retention. T_A ≤ 85 °C, 10K P/E cycles	10	–	–	years	–
SID182B	F_{RET3}	Flash retention. T_A ≤ 55 °C, 20K P/E cycles	20	–	–	years	–
SID256	T_{WS100}	Number of Wait states at 100 MHz	3	–	–		–
SID257	T_{WS50}	Number of Wait states at 50 MHz	2	–	–		–

Note

4. It can take as much as 16 milliseconds to write to flash. During this time, the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

System Resources

Table 25. System Resources

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Power-On-Reset with Brown-out DC Specifications							
Precise POR (PPOR)							
SID190	$V_{FALLPPOR}$	BOD trip voltage in Active and Sleep modes. V_{DDD}.	1.54	–	–	V	BOD Reset guaranteed for levels below 1.54 V
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep. V_{DDD}.	1.54	–	–	V	–
SID192A	V_{DDRAMP}	Maximum power supply ramp rate (any supply)	–	–	100	mV/µs	Active mode
POR with Brown-out AC Specification							
SID194A	V_{DDRAMP_DS}	Maximum power supply ramp rate (any supply) in Deep Sleep	–	–	10	mV/µs	BOD operation guaranteed
Voltage Monitors DC Specifications							
SID195R	V_{HVD0}	–	1.18	1.23	1.27	V	–
SID195	V_{HVDI1}	–	1.38	1.43	1.47	V	–
SID196	V_{HVDI2}	–	1.57	1.63	1.68	V	–
SID197	V_{HVDI3}	–	1.76	1.83	1.89	V	–
SID198	V_{HVDI4}	–	1.95	2.03	2.1	V	–
SID199	V_{HVDI5}	–	2.05	2.13	2.2	V	–
SID200	V_{HVDI6}	–	2.15	2.23	2.3	V	–
SID201	V_{HVDI7}	–	2.24	2.33	2.41	V	–
SID202	V_{HVDI8}	–	2.34	2.43	2.51	V	–
SID203	V_{HVDI9}	–	2.44	2.53	2.61	V	–
SID204	V_{HVDI10}	–	2.53	2.63	2.72	V	–
SID205	V_{HVDI11}	–	2.63	2.73	2.82	V	–
SID206	V_{HVDI12}	–	2.73	2.83	2.92	V	–
SID207	V_{HVDI13}	–	2.82	2.93	3.03	V	–
SID208	V_{HVDI14}	–	2.92	3.03	3.13	V	–
SID209	V_{HVDI15}	–	3.02	3.13	3.23	V	–
SID211	LVI_IDD	Block current	–	5	15	µA	–
Voltage Monitors AC Specification							
SID212	$T_{MONTRIP}$	Voltage monitor trip time	–	–	170	ns	–

SWD Interface

Table 26. SWD and Trace Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SWD and Trace Interface							
SID214	F_SWDCLK2	1.7 V ≤ V_{DDD} ≤ 3.6 V	–	–	25	MHz	LP Mode. V_{CCD} = 1.1 V.
SID214L	F_SWDCLK2L	1.7 V≤ V_{DDD} ≤ 3.6 V	–	–	12	MHz	ULP Mode. V_{CCD} = 0.9 V.
SID215	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 * T	–	–	ns	–
SID216	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 * T	–	–	ns	–
SID217	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5 * T	ns	–
SID217A	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	–
SID214T	F_TRCLK_LP1	With Trace Data setup/hold times of 2/1 ns respectively	–	–	50	MHz	LP Mode. V_{DD} = 1.1 V.
SID215T	F_TRCLK_LP2	With Trace Data setup/hold times of 3/2 ns respectively	–	–	50	MHz	LP Mode. V_{DD} = 1.1 V.
SID216T	F_TRCLK_ULP	With Trace Data setup/hold times of 3/2 ns respectively	–	–	20	MHz	ULP Mode. V_{DD} = 0.9 V.

Internal Main Oscillator

Table 27. IMO DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 8 MHz	–	9	15	µA	–

Table 28. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	$F_{IMOTOL1}$	Frequency variation centered on 8 MHz	–	–	±2	%	–
SID227	T_{JITR}	Cycle-to-Cycle and Period jitter	–	250	–	ps	–

Internal Low-Speed Oscillator

Table 29. ILO DC Specification

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_{ILO2}	ILO operating current at 32 kHz	–	0.3	0.7	µA	–

Table 30. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	$T_{STARTILO1}$	ILO startup time	–	–	7	µs	Startup time to 95% of final frequency
SID236	TLIODUTY	ILO Duty cycle	45	50	55	%	–
SID237	$F_{ILOTRIM1}$	32 kHz trimmed frequency	28.8	32	35.2	kHz	±10% variation

Crystal Oscillator Specifications

Table 31. ECO Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
MHz ECO DC Specifications							
SID316	I_{DD_MHz}	Block operating current with Cload up to 18 pF	–	800	1600	µA	Max = 33 MHz, Type = 16 MHz
MHz ECO AC Specifications							
SID317	F_MHz	Crystal frequency range	4	–	35	MHz	–
kHz ECO DC Specification							
SID318	I_{DD_kHz}	Block operating current with 32-kHz crystal	–	0.38	1	µA	–
SID321E	ESR32K	Equivalent series resistance	–	80	–	kΩ	–
SID322E	PD32K	Drive level	–	–	1	µW	–
kHz ECO AC Specification							
SID319	F_kHz	32 kHz trimmed frequency	–	32.768	–	kHz	–
SID320	Ton_kHz	Startup time	–	–	500	ms	–
SID320E	F_{TOL32K}	Frequency tolerance	–	50	250	ppm	–

External Clock Specifications

Table 32. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305	$EXTCLK_{FREQ}$	External clock input frequency	0	–	100	MHz	–
SID306	$EXTCLK_{DUTY}$	Duty cycle; measured at $V_{DD}/2$	45	–	55	%	–

PLL Specifications

Table 33. PLL Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305P	PLL_LOCK	Time to achieve PLL lock	–	16	35	µs	–
SID306P	PLL_OUT	Output frequency from PLL block	–	–	150	MHz	–
SID307P	PLL_IDD	PLL current	–	0.55	1.1	mA	Typ. at 100 MHz out.
SID308P	PLL_JTR	Period jitter	–	–	150	ps	100 MHz output frequency

Table 34. Clock Source Switching Time

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID262	$TCLK_{SWITCH}$	Clock switching from clk1 to clk2 in clock periods; for example, from IMO (clk1) to FLL (clk2).	–	–	4 clk1 + 3 clk2	periods	–

FLL Specifications

Table 35. Frequency Locked Loop (FLL) Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
Frequency Locked Loop (FLL) Specifications							
SID450	FLL_RANGE	Input frequency range.	0.001	–	100	MHz	Lower limit allows lock to USB SOF signal (1 kHz). Upper limit is for External input.
SID451	FLL_OUT_DIV2	Output frequency range. V_{CCD} = 1.1 V	24.00	–	100.00	MHz	Output range of FLL divided-by-2 output
SID451A	FLL_OUT_DIV2	Output frequency range. V_{CCD} = 0.9 V	24.00	–	50.00	MHz	Output range of FLL divided-by-2 output
SID452	FLL_DUTY_DIV2	Divided-by-2 output; High or Low	47.00	–	53.00	%	–
SID454	FLL_WAKEUP	Time from stable input clock to 1% of final value on Deep Sleep wakeup	–	–	7.50	µs	With IMO input, less than 10 °C change in temperature while in Deep Sleep, and Fout ≥ 50 MHz.
SID455	FLL_JITTER	Period jitter (1 sigma) at 100 MHz	–	–	35.00	ps	50 ps at 48 MHz, 35 ps at 100 MHz
SID456	FLL_CURRENT	CCO + Logic current	–	–	5.50	µA/MHz	–

USB

Table 36. USB Specifications (USB requires LP Mode 1.1-V internal supply)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
USB Block Specifications							
SID322U	Vusb_3.3	Device supply for USB operation	3.15	–	3.6	V	USB Configured
SID323U	Vusb_3	Device supply for USB operation (functional operation only)	2.85	–	3.6	V	USB Configured
SID325U	Iusb_config	Device supply current in Active mode	–	8	–	mA	VDDD = 3.3 V
SID328	Isub_suspend	Device supply current in Sleep mode	–	0.5	–	mA	VDDD = 3.3 V, Device connected
SID329	Isub_suspend	Device supply current in Sleep mode	–	0.3	–	mA	VDDD = 3.3 V, Device disconnected
SID330U	USB_Drive_Res	USB driver impedance	28	–	44	Ω	Series resistors are on chip
SID332U	USB_Pullup_Idle	Idle mode range	900	–	1575	Ω	Bus idle
SID333U	USB_Pullup	Active mode	1425	–	3090	Ω	Upstream device transmitting

Table 37. QSPI Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SMIF QSPI Specifications. All specs with 15-pF load.							
SID390Q	Fsmifclock	SMIF QSPI output clock frequency	–	–	80	MHz	LP mode (1.1 V)
SID390QU	Fsmifclocku	SMIF QSPI output clock frequency	–	–	50	MHz	ULP mode (0.9 V). Guaranteed by Char.
SID399Q	Clk_dutycycle	Clock duty cycle (high or low time)	45	–	55	%	
SID397Q	Idd_qspi	Block current in LP mode (1.1 V)	–	–	1900	µA	LP mode (1.1 V)
SID398Q	Idd_qspi_u	Block current in ULP mode (0.9 V)	–	–	590	µA	ULP mode (0.9 V)
SID391Q	Tsetup	Input data set-up time with respect to clock capturing edge	4.5	–	–	ns	–
SID392Q	Tdatahold	Input data hold time with respect to clock capturing edge	0	–	–	ns	–
SID393Q	Tdataoutvalid	Output data valid time with respect to clock falling edge	–	–	3.7	ns	7.5-ns max for ULP mode (0.9 V)
SID394Q	Tholdtime	Output data hold time with respect to clock rising edge	3	–	–	ns	–
SID395Q	Tseloutvalid	Output Select valid time with respect to clock rising edge	–	–	7.5	ns	15-ns max for ULP mode (0.9 V)
SID396Q	Tselouthold	Output Select hold time with respect to clock rising edge	Tsclk	–	–	ns	Tsclk = Fsmifclk cycle time

Smart I/O

Table 38. Smart I/O Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID420	SMIO_BYP	Smart I/O bypass delay	–	–	2	ns	–
SID421	SMIO_LUT	Smart I/O LUT prop delay	–	8	–	ns	–

SDHC and eMMC

Table 39. SDHC and eMMC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SDHC and eMMC Specifications (Block Clock must be divided by 2 or more when used as source in DDR modes)							
SID_SD390	SD_DS	I/O drive select	–	–	4	mA	drive_sel = '01' for all modes
SID_SD391	SD_TR	Input transition time	0.7	–	3	ns	–
SD:DS Timing							
SID_SD392	SD_CLK	Interface clock period (LP mode)	–	–	25	MHz	(40 ns period)
SID_SD393	SD_CLK	Interface clock period (ULP mode)	–	–	8	MHz	(125 ns period)
SID_SD394	SD_DCMD_CL	I/O loading at DATA/CMD pins	30	–	30	pF	–
SID_SD395	SD_CLK_CL	I/O loading at CLK pins	30	–	30	pF	–
SID_SD396	SD_TS_OUT	Output: Setup time of CMD/DAT prior to CLK	5.1	–	–	ns	–
SID_SD397	SD_HLD_OUT	Output: Hold time of CMD/DAT after CLK	5.1	–	–	ns	–
SID_SD398	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (LP mode)	24	–	–	ns	–
SID_SD399	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (ULP mode)	109	–	–	ns	–

Table 39. SDHC and eMMC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID_SD400	SD_HLD_IN	Input: Hold time of CMD/DAT after CLK	2.1	–	–	ns	–
SD:HS Timing							
SID_SD401	SD_CLK	Interface clock period (LP mode)	–	–	45	MHz	(22.5 ns period)
SID_SD402	SD_CLK	Interface clock period (ULP mode)	–	–	16	MHz	(62.5 ns period)
SID_SD403	SD_DCMD_CL	I/O loading at DATA/CMD pins	30	-	30	pF	–
SID_SD404	SD_CLK_CL	I/O loading at CLK pins	30	–	30	pF	–
SID_SD405	SD_TS_OUT	Output: Setup time of CMD/DAT prior to CLK	6.1	–	–	ns	–
SID_SD406	SD_HLD_OUT	Output: Hold time of CMD/DAT after CLK	2.1	–	–	ns	–
SID_SD407	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (LP mode)	8	–	–	ns	–
SID_SD408	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (ULP mode)	48.3	–	–	ns	–
SID_SD409	SD_HLD_IN	Input: Hold time of CMD/DAT after CLK	2.5	–	–	ns	–
SD:SDR-12 Timing							
SID_SD410	SD_CLK	Interface clock period (LP mode)	–	–	25	MHz	(40 ns period)
SID_SD411	SD_CLK	Interface clock period (ULP mode)	–	–	8	MHz	(125 ns period)
SID_SD412	SD_CLK_DC	Duty cycle of output CLK	30	–	70	%	–
SID_SD413	SD_DCMD_CL	I/O loading at DATA/CMD pins	30	–	30	pF	–
SID_SD414	SD_CLK_CL	I/O loading at CLK pins	30	–	30	pF	–
SID_SD415	SD_TS_OUT	Output: Setup time of CMD/DAT prior to CLK	3.1	–	–	ns	–
SID_SD416	SD_HLD_OUT	Output: Hold time of CMD/DAT after CLK	0.9	–	–	ns	–
SID_SD417	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (LP mode)	24	–	–	ns	–
SID_SD418	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (ULP mode)	109	–	–	ns	–
SID_SD419	SD_HLD_IN	Input: Hold time of CMD/DAT after CLK	1.8	–	–	ns	–
SD:SDR-25 Timing							
SID_SD420	SD_CLK	Interface clock period (LP mode)	–	–	50	MHz	(20 ns period)
SID_SD421	SD_CLK	Interface clock period (ULP mode)	–	–	16	MHz	(62.5 ns period)
SID_SD422	SD_CLK_DC	Duty cycle of output CLK	30	–	70	%	–
SID_SD423	SD_DCMD_CL	I/O loading at DATA/CMD pins	30	–	30	pF	–
SID_SD424	SD_CLK_CL	I/O loading at CLK pins	30	–	30	pF	–
SID_SD425	SD_TS_OUT	Output: Setup time of CMD/DAT prior to CLK	3.1	–	–	ns	–
SID_SD426	SD_HLD_OUT	Output: Hold time of CMD/DAT after CLK	0.9	–	–	ns	–
SID_SD427	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (LP mode)	5.8	–	–	ns	–
SID_SD428	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (ULP mode)	48.3	–	–	ns	–
SID_SD429	SD_HLD_IN	Input: Hold time of CMD/DAT after CLK	1.8	–	–	ns	–
SD:SDR-50 Timing							
SID_SD430	SD_CLK	Interface clock period (LP mode)	–	–	80	MHz	(12.5 ns period)
SID_SD431	SD_CLK	Interface clock period (ULP mode)	–	–	32	MHz	(31.25 ns period)

Table 39. SDHC and eMMC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID_SD432	SD_CLK_DC	Duty cycle of output CLK	30	–	70	%	–
SID_SD433	SD_DCMD_CL	I/O loading at DATA/CMD pins	20	–	20	pF	–
SID_SD434	SD_CLK_CL	I/O loading at CLK pins	20	–	20	pF	–
SID_SD435	SD_TS_OUT	Output: Setup time of CMD/DAT prior to CLK	3.1	–	–	ns	–
SID_SD436	SD_HLD_OUT	Output: Hold time of CMD/DAT after CLK	0.9	–	–	ns	–
SID_SD437	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (LP mode)	5	–	–	ns	–
SID_SD438	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (ULP mode)	23.6	–	–	ns	–
SID_SD439	SD_HLD_IN	Input: Hold time of CMD/DAT after CLK	1.8	–	–	ns	–
SD:DDR-50 Timing							
SID_SD440	SD_CLK	Interface clock period (LP mode)	–	–	40	MHz	(25 ns period).
SID_SD441	SD_CLK	Interface clock period (ULP mode)	–	–	16	MHz	(62.5 ns period)
SID_SD442	SD_CLK_DC	Duty cycle of output CLK	45	–	55	%	–
SID_SD443	SD_DCMD_CL	I/O loading at DATA/CMD pins	30	–	30	pF	–
SID_SD444	SD_CLK_CL	I/O loading at CLK pins	30	–	30	pF	–
SID_SD445	SD_TS_OUT	Output: Setup time of CMD/DAT prior to CLK	3.1	–	–	ns	–
SID_SD446	SD_HLD_OUT	Output: Hold time of CMD/DAT after CLK	0.9	–	–	ns	–
SID_SD447	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (LP mode)	5.7	–	–	ns	–
SID_SD448	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (ULP mode)	24	–	–	ns	–
SID_SD449	SD_HLD_IN	Input: Hold time of CMD/DAT after CLK	1.8	–	–	ns	–
eMMC:BWC Timing							
SID_SD450	SD_CLK	Interface clock period (LP mode)	–	–	26	MHz	(38.4 ns period)
SID_SD451	SD_CLK	Interface clock period (ULP mode)	–	–	8	MHz	(125 ns period)
SID_SD452	SD_DCMD_CL	I/O loading at DATA/CMD pins	30	–	30	pF	–
SID_SD453	SD_CLK_CL	I/O loading at CLK pins	30	–	30	pF	–
SID_SD454	SD_TS_OUT	Output: Setup time of CMD/DAT prior to CLK	3.1	–	–	ns	–
SID_SD455	SD_HLD_OUT	Output: Hold time of CMD/DAT after CLK	3.1	–	–	ns	–
SID_SD456	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (LP mode)	9.7	–	–	ns	–
SID_SD457	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (ULP mode)	96.3	–	–	ns	–
SID_SD458	SD_HLD_IN	Input: Hold time of CMD/DAT after CLK	8.3	–	–	ns	–
eMMC:SDR Timing							
SID_SD459	SD_CLK	Interface clock period (LP mode)	–	–	52	MHz	(19.2 ns period)
SID_SD460	SD_CLK	Interface clock period (ULP mode)	–	–	16	MHz	(62.5 ns period)
SID_SD461	SD_DCMD_CL	I/O loading at DATA/CMD pins	30	–	30	pF	–
SID_SD462	SD_CLK_CL	I/O loading at CLK pins	30	–	30	pF	–
SID_SD463	SD_TS_OUT	Output: Setup time of CMD/DAT prior to CLK	3.1	–	–	ns	–
SID_SD464	SD_HLD_OUT	Output: Hold time of CMD/DAT after CLK	3.1	–	–	ns	–

Table 39. SDHC and eMMC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID_SD465	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (LP mode)	5.3	–	–	ns	–
SID_SD466	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (ULP mode)	48.6	–	–	ns	–
SID_SD467	SD_HLD_IN	Input: Hold time of CMD/DAT after CLK	2.5	–	–	ns	–
eMMC:DDR Timing							
SID_SD468	SD_CLK	Interface clock period (LP mode)	–	–	52	MHz	–
SID_SD469	SD_CLK	Interface clock period (ULP mode)	–	–	16	MHz	(62.5 ns period)
SID_SD470	SD_CLK_DC	Dutycycle requirement at output CLK	40	–	60	%	–
SID_SD471	SD_DCMD_CL	I/O loading at DATA/CMD pins	20	–	20	pF	–
SID_SD472	SD_CLK_CL	I/O loading at CLK pins	20	–	20	pF	–
SID_SD473	SD_TS_OUT	Output: Setup time of CMD/DAT prior to CLK	2.6	–	–	ns	–
SID_SD474	SD_HLD_OUT	Output: Hold time of CMD/DAT after CLK	2.6	–	–	ns	–
SID_SD475	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (LP mode)	9.6	–	–	ns	–
SID_SD476	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (ULP mode)	31.3	–	–	ns	–
SID_SD477	SD_HLD_IN	Input: Hold time of CMD/DAT after CLK	1.5	–	–	ns	–
SID400SD	IDD_SD_1	SDHC block current consumption at 100 MHz	TBD	–	–	ns	SDR-50
SID401SD	IDD_SD_2	SDHC block current consumption at 50 MHz	TBD	–	–	ns	SDR-25

JTAG Boundary Scan

Table 40. JTAG Boundary Scan

Spec ID#		Parameter	Description	Min	Typ	Max	Units
JTAG Boundary Scan Parameters							
JTAG Boundary Scan Parameters for 1.1 V (LP) Mode Operation:							
SID468	TCKLOW	TCK LOW	52	–	–	ns	–
SID469	TCKHIGH	TCK HIGH	10	–	–	ns	–
SID470	TCK_TDO	TCK falling edge to output valid		–	40	ns	–
SID471	TSU_TCK	Input valid to TCK rising edge	12	–	–	ns	–
SID472	TCk_THD	Input hold time to TCK rising edge	10	–	–	ns	–
SID473	TCK_TDOV	TCK falling edge to output valid (High-Z to Active).	40	–	–	ns	–
SID474	TCK_TDOZ	TCK falling edge to output valid (Active to High-Z).	40	–	–	ns	–
JTAG Boundary Scan Parameters for 0.9 V (ULP) Mode Operation:							
SID468A	TCKLOW	TCK low	102	–	–	ns	–
SID469A	TCKHIGH	TCK high	20	–	–	ns	–
SID470A	TCK_TDO	TCK falling edge to output valid		–	80	ns	–
SID471A	TSU_TCK	Input valid to TCK rising edge	22	–	–	ns	–
SID472A	TCk_THD	Input hold time to TCK rising edge	20	–	–	ns	–

Table 40. JTAG Boundary Scan *(continued)*

Spec ID#		Parameter	Description	Min	Typ	Max	Units
SID473A	TCK_TDOV	TCK falling edge to output valid (high-Z to active).	80	–	–	ns	–
SID474A	TCK_TDOZ	TCK falling edge to output valid (active to high-Z).	80	–	–	ns	–

Ordering Information

Table 41 lists the CYB06445LQI-S3D42 part numbers and features. See also the product selector guide.

Table 41. Ordering Information

Family	Base Features	Marketing Part Number	Flash (KB)	SRAM (KB)	CapSense	CAN FD	Crypto	GPIO	Package
64	Arm CM4 and CM0+, 12-bit SAR ADC, 2 LPCOMPs, 7 SCBs, 12 TCPWMs, SD Host Controller, USB-FS	CYB06445LQI-S3D42	512	256	Y	1	Y	53	68-QFN

PSoC 6 MPN Decoder

CY XX 6 A B C DD E - FF G H I JJ K L

Field	Description	Values	Meaning
CY	Cypress	CY	Cypress
XX	Firmware	8C	Standard
		B0	Secure Boot v1
		S0	Std. Secure - AWS
6	Architecture	6	PSoC 6
A	Line	0	Value
		1	Programmable
		2	Performance
		3	Connectivity
		4	Security
B	Speed	2	100 MHz
		3	150 MHz
		4	150/50 MHz
C	Memory Size (Flash/SRAM)	0-3	RFU
		4	256K/128K
		5	512K/256K
		6	512K/128K
		7	1024K/288K
		8	1024K/512K
		9	RFU
		A	2048K/1024K
DD	Package	AZ, AX	TQFP
		LQ	QFN
		BZ	BGA
		FM	M-CSP
		FN, FD, FT	WLCSP

Field	Description	Values	Meaning
E	Temperature Range	C	Consumer
		I	Industrial
		Q	Extended Industrial
FF	Feature Code		Cypress internal
		S2-S6	
		BL	Integrated BLE
G	CPU Core	F	Single Core
		D	Dual Core
H	Attributes Code	0–9	Feature set
I	GPIO count	1	31-50
		2	51-70
		3	71-90
		4	91-110
JJ	Engineering sample (optional)	ES	Engineering samples or not
K	Die Revision (optional)		Base
		A1-A9	Die revision
L	Tape/Reel Shipment (optional)	T	Tape and Reel shipment

Packaging

This product line is offered in a 68-QFN package.

Table 42. Package Dimensions

Spec ID#	Package	Description	Package Dwg #
PKG_1	68-QFN	68-QFN package	001-96836

Table 43. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	–	–40	25	85	°C
T_J	Operating junction temperature	–	–40	–	100	°C
T_{JA}	Package θ_{JA} (68-QFN)	–	–	15.4	–	°C/watt
T_{JC}	Package θ_{JC} (68-QFN)	–	–	2	–	°C/watt

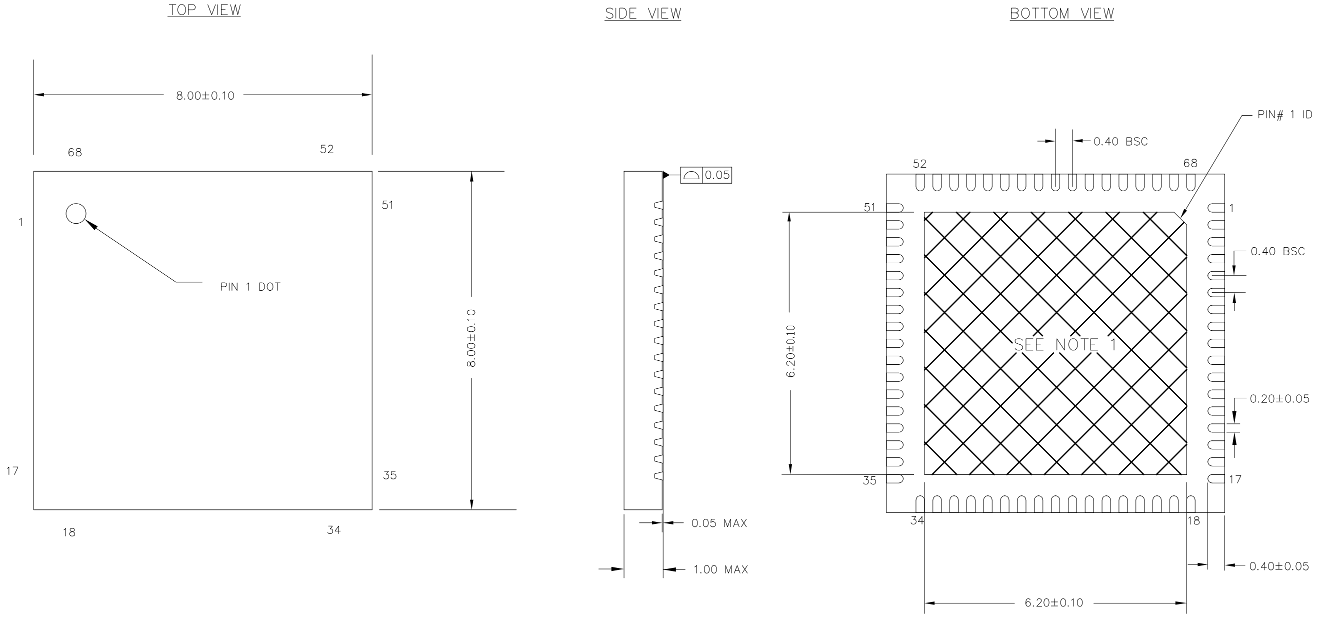
Table 44. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
68-QFN	260°C	30 seconds

Table 45. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
68 QFN	MSL 3

Figure 11. 68-QFN Package Diagram



NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. ALL DIMENSIONS ARE IN MILLIMETERS

001-96836 *A

Acronyms

Acronym	Description
3DES	triple DES (data encryption standard)
ADC	analog-to-digital converter
ADMA3	advanced DMA version 3, a Secure Digital data transfer mode
AES	advanced encryption standard
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm data transfer bus
AMUX	analog multiplexer
AMUXBUS	analog multiplexer bus
API	application programming interface
Arm®	advanced RISC machine, a CPU architecture
BGA	ball grid array
BOD	brown-out detect
BREG	backup registers
BWC	backward compatibility (eMMC data transfer mode)
CAD	computer aided design
CCO	current controlled oscillator
ChaCha	a stream cipher
CM0+	Cortex-M0+, an Arm CPU
CM4	Cortex-M4, an Arm CPU
CMAC	cypher-based message authentication code
CMOS	complementary metal-oxide-semiconductor, a process technology for IC fabrication
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CSD	CapSense Sigma-Delta
CSV	clock supervisor
CSX	Cypress mutual capacitance sensing method. See also CSD
CTI	cross trigger interface
DAC	digital-to-analog converter, see also IDAC, VDAC
DAP	debug access port
DDR	double data rate
DES	data encryption standard
DFT	design for test
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DSI	digital system interconnect
DU	data unit
DW	data wire, a DMA implementation
ECC	error correcting code

Acronym	Description
ECC	elliptic curve cryptography
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
eMMC	embedded MultiMediaCard
ESD	electrostatic discharge
ETM	embedded trace macrocell
FIFO	first-in, first-out
FLL	frequency locked loop
FPU	floating-point unit
FS	full-speed
GND	Ground
GPIO	general-purpose input/output, applies to a PSoC pin
HMAC	Hash-based message authentication code
HSIOM	high-speed I/O matrix
I/O	input/output, see also GPIO, DIO, SIO, USBIO
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
I^2S	inter-IC sound
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
IOSS	input output subsystem
IoT	internet of things
IPC	inter-processor communication
IRQ	interrupt request
ISR	interrupt service routine
ITM	instrumentation trace macrocell
JTAG	Joint Test Action Group
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol
LP	low power
LS	low-speed
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit

Acronym	Description
MCWDT	multi-counter watchdog timer
MISO	master-in slave-out
MMIO	memory-mapped input output
MOSI	master-out slave-in
MPU	memory protection unit
MSL	moisture sensitivity level
Msps	million samples per second
MTB	micro trace buffer
MUL	multiplier
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
OTP	one-time programmable
OVP	over voltage protection
OVT	overvoltage tolerant
PASS	programmable analog subsystem
PCB	printed circuit board
PCM	pulse code modulation
PDM	pulse density modulation
PHY	physical layer
PICU	port interrupt control unit
PLL	phase-locked loop
PMIC	power management integrated circuit
POR	power-on reset
PPU	peripheral protection unit
PRNG	pseudo random number generator
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
QD	quadrature decoder
QSPI	quad serial peripheral interface
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
ROM	read-only memory
RSA	Rivest–Shamir–Adleman, a public-key cryptography algorithm
RTC	real-time clock
RWW	read-while-write
RX	receive
S/H	sample and hold
SAR	successive approximation register

Acronym	Description
SARMUX	SAR ADC multiplexer bus
SC/CT	switched capacitor/continuous time
SCB	serial communication block
SCL	I^2C serial clock
SD	Secure Digital
SDA	I^2C serial data
SDHC	Secure Digital host controller
SDR	single data rate
Sflash	supervisory flash
SHA	secure hash algorithm
SINAD	signal to noise and distortion ratio
SMPU	shared memory protection unit
SNR	signal-to-noise ration
SOF	start of frame
SONOS	silicon-oxide-nitride-oxide-silicon, a flash memory technology
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SROM	supervisory read-only memory
SRSS	system resources subsystem
SWD	serial wire debug, a test protocol
SWJ	serial wire JTAG
SWO	single wire output
SWV	single-wire viewer
TCPWM	timer, counter, pulse-width modulator
TDM	time division multiplexed
THD	total harmonic distortion
TQFP	thin quad flat package
TRM	technical reference manual
TRNG	true random number generator
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
ULP	ultra-low power
USB	Universal Serial Bus
WCO	watch crystal oscillator
WDT	watchdog timer
WIC	wakeup interrupt controller
WLCSP	wafer level chip scale package
XIP	execute-in-place
XRES	external reset input pin

Document Conventions

Units of Measure

Table 46. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
W	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Errata

This section describes the errata for the PSoC 6 CYB06445LQI-S3D42 Product Family. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Compare this document to the device's datasheet for a complete functional description.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Device Characteristics
CYB06445LQI-S3D42	PSoC CYB06445LQI-S3D42 Product Family

PSoC 64 Qualification Status

Engineering Samples

PSoC 64 Errata Summary

This table defines the errata applicability to available PSoC 6 6A-512K family devices.

Items	CY8C6XX 6A-512K	Silicon Revision	Fix Status
[1] MHz ECO usage requires Ports 11, 12, and 13 be restricted to slow slew rate (2.5-MHz max frequency).	All	Production silicon	Investigation underway. Resolution planned by Q3 20.

1. MHz ECO usage requires Ports 11, 12, and 13 be restricted to slow slew rate (2.5-MHz max frequency).	
Problem Definition	MHz ECO usage requires Port0s 11 and 12 be restricted to slow slew rate (2.5-MHz ECO is sensitive to GPIO Switching noise on adjacent I/O Ports and requires edge rates be restricted when the MHz ECO is used.MHz max frequency).
Parameters Affected	Slew rate is restricted to slow switching and this affects switching frequency which is restricted to 2.5 MHz.
Trigger Condition(s)	Usage of fast slew rates on ECO Port and adjacent port (Ports 11 and 12).
Scope of Impact	Slew rates must be restricted to slow mode for reliable ECO operation. Note this includes the QSPI interface port (Port 11).
Workaround	None
Fix Status	Investigation underway. Resolution planned by Q3 20.

Revision History

Revision	ECN	Submission Date	Description of Change
Description Title: PSoC 6 MCU: CYB06445LQI-S3D42 Datasheet Document Number: 002-28785			
**	6711017	10/22/2019	New datasheet.
*A	6776273	01/16/2020	Updated Features. Updated Blocks and Functionality and Functional Description. Updated Pinouts and Power Supply Considerations. Updated Packaging.
*B	6851682	04/10/2020	Updated Features. Updated Functional Description. Updated Pinouts. Updated PSoC 6 MPN Decoder.

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