


# CYW9P62S1-43012CAR-01

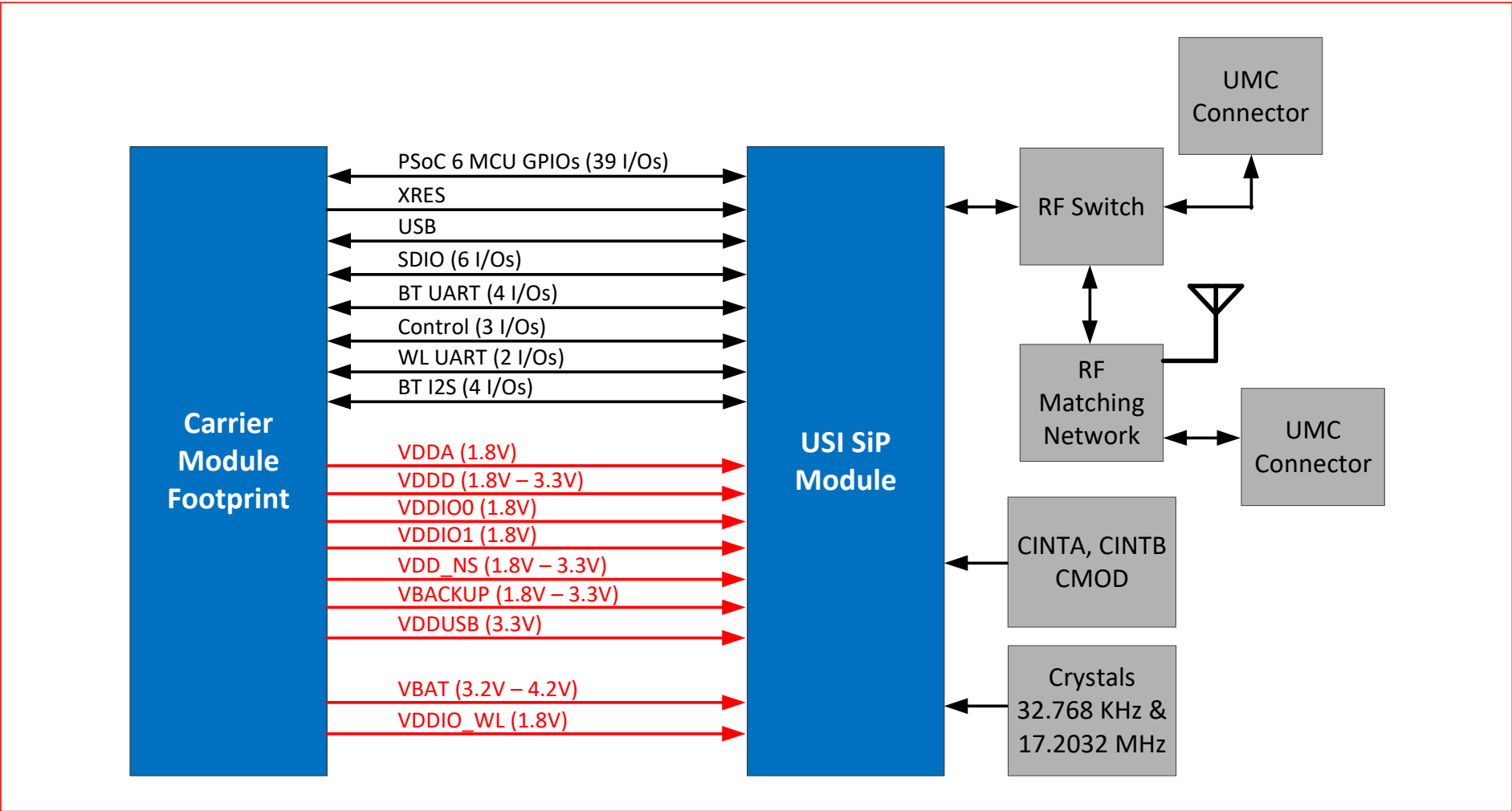
## PSoC 6 (1M) with CYW43012 USI SiP Carrier Module

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<b>Drawing Numbers</b>	
PCBA	121-60559-01
PCB	600-60559-01
FAB DRW	610-60559-01
ASSY DRW	620-60559-01
SCH DRW	630-60559-01

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<b>Page Title : Title Page</b>				
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# Block Diagram



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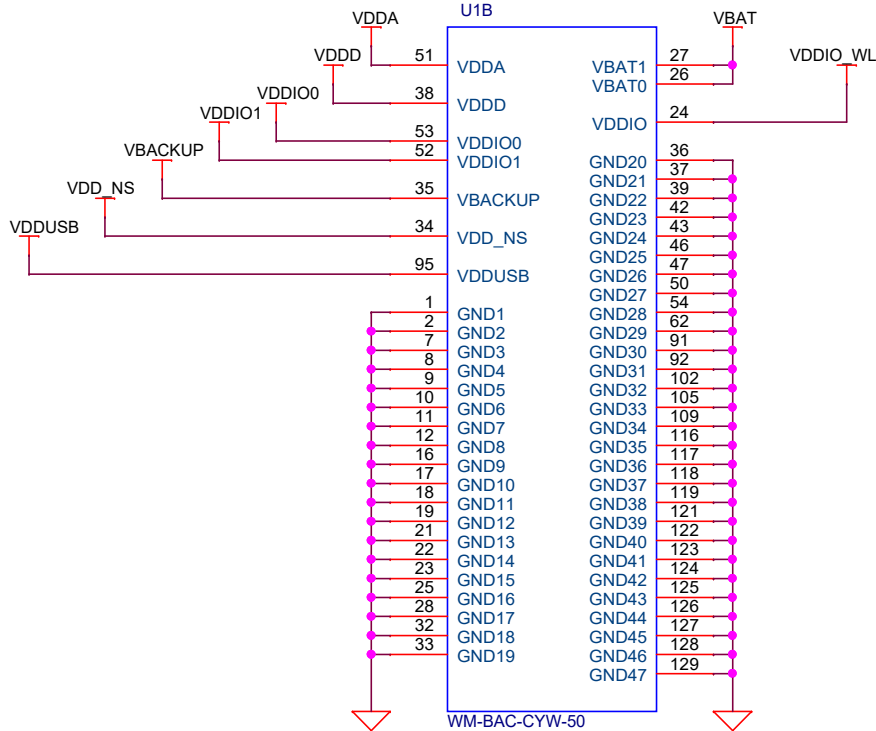
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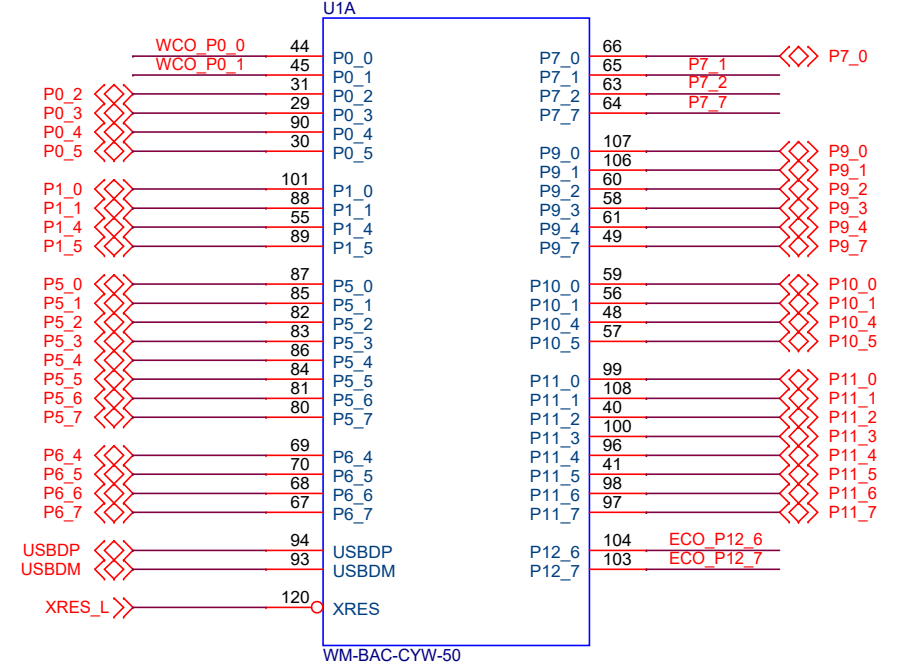
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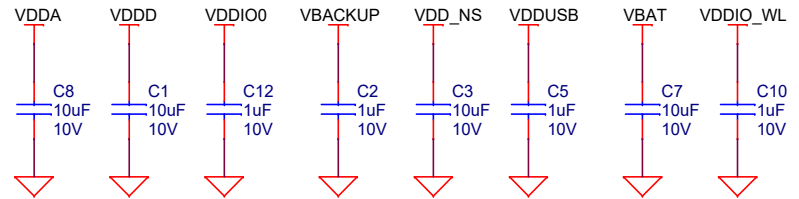
### USI SiP Module Power



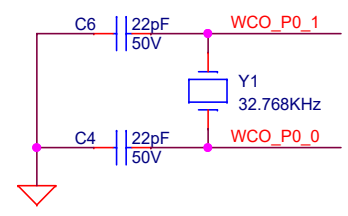
### USI SiP Module PSoC 6 MCU Signals



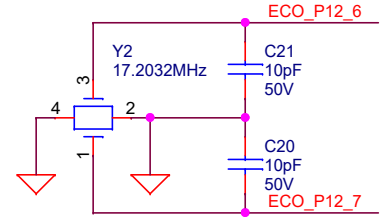
### Decoupling Capacitors



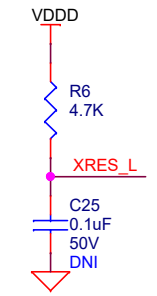
### WCO



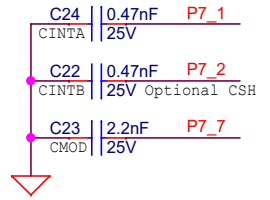
### ECO



### Pull-up for Reset



### CINT, CMOD & CSH

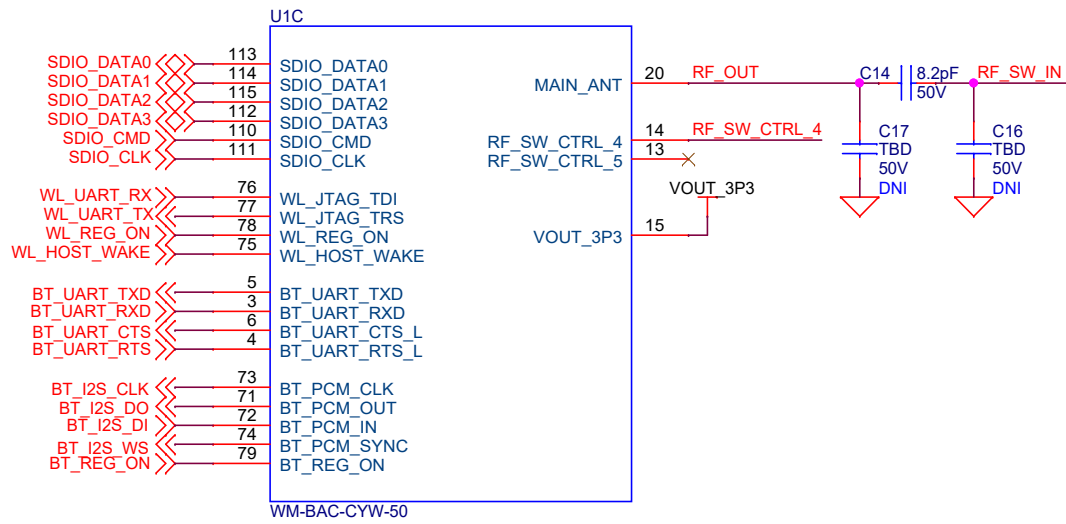


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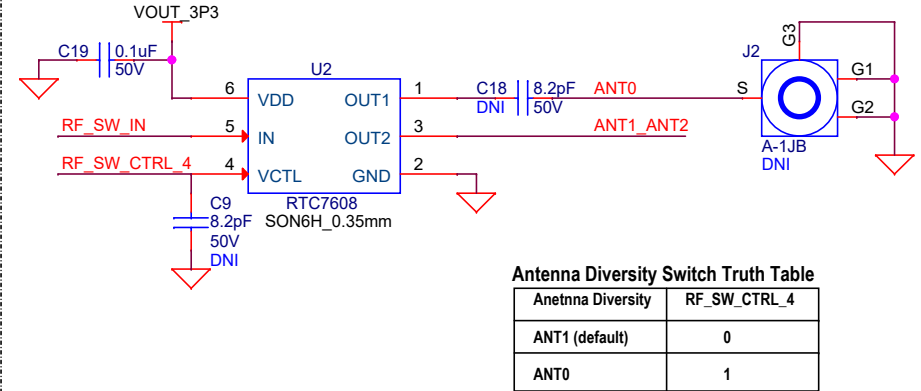
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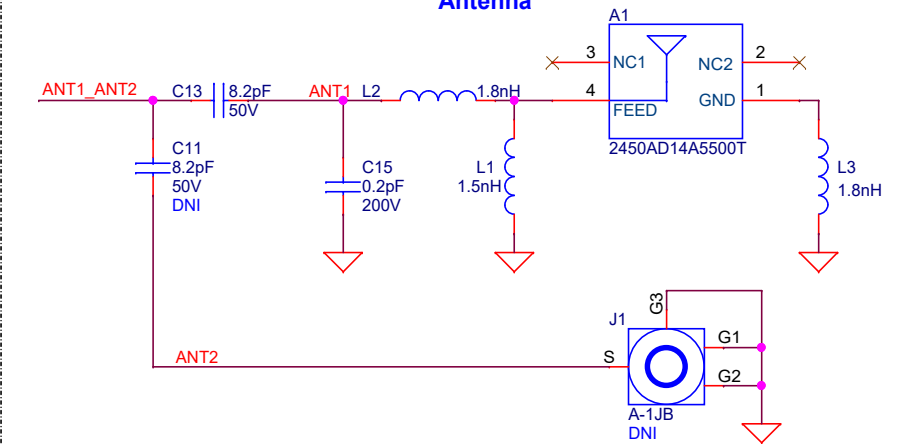
### USI SiP Module CYW43012 Signals



### Antenna Diversity Switch



### Antenna



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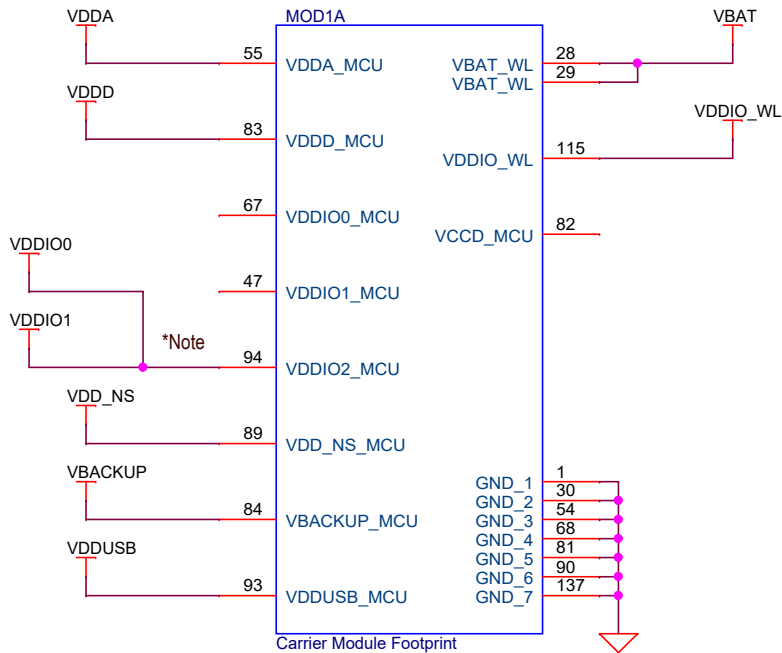
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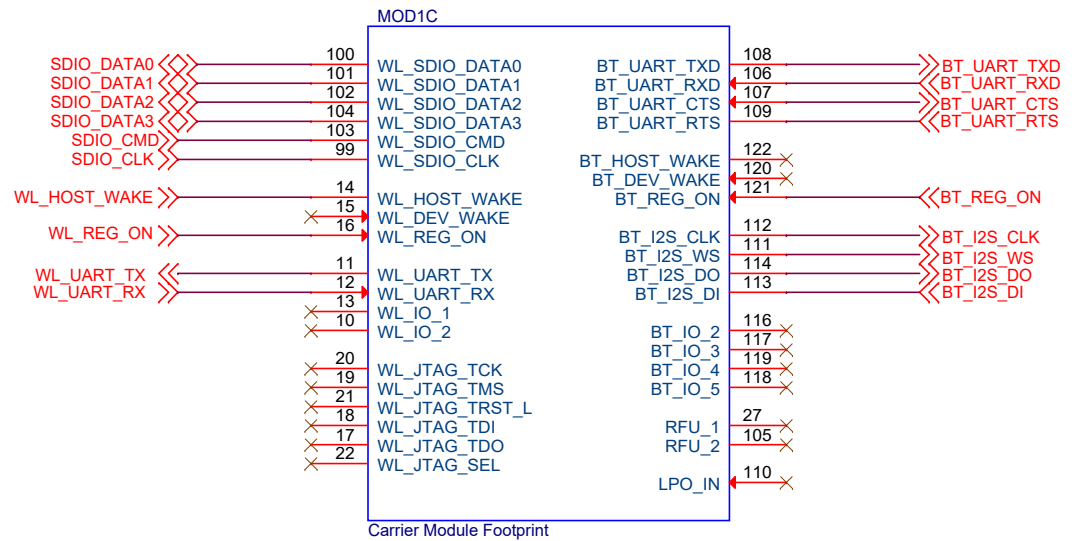
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### Carrier Module Footprint (Power)



Note: In WM-BAC-CYW-50, VDDIO0 & VDDIO1 need to be same voltage as VDDIO\_WL.  
 VDDIO2\_MCU will be same voltage as VDDIO\_WL as per baseboard design, the reason  
 VDDIO0 & VDDIO1 connected to VDDIO2\_MCU

### Carrier Module Footprint (Wi-Fi BT Signals)



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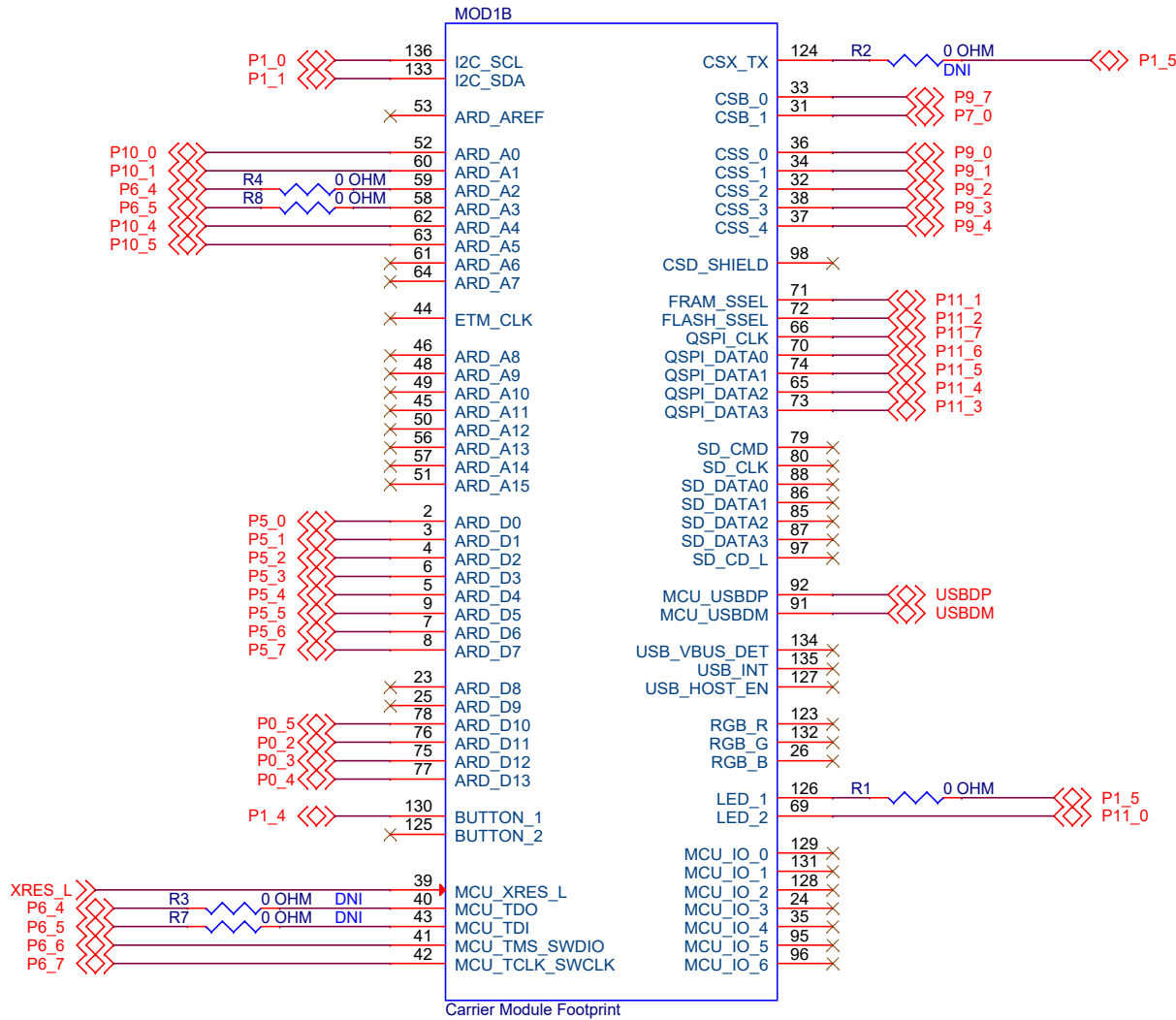
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### Carrier Module Footprint (PSoC 6 MCU Signals)



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**REVISION HISTORY**

<b>REV</b>	<b>DESCRIPTION OF CHANGE</b>	<b>Orig. of Change</b>	<b>DATE</b>
01	Internal Release	AARA	2019/07/10
02	Internal Release	AARA	2019/10/31
03	Initial Release	TARE	2020/01/16



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