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SEE/SEL Final Report for Cypress Semiconductor CYRS1643, 144-Mbit QDR SRAMs

L9729013

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1.0 Test Overview

Single Event Effects (SEE) and Single Event Latchup (SEL) testing was performed on Cypress Semiconductor 144-Mbit QDR SRAMs on 18-19 May, 2019 at the Texas A&M University Cyclotron facility. Memory on this device is accessed via an 18 bit wide data buss. Because of the QDR architecture there are 18 inputs (D0 – D17) and 18 separate outputs (Q0 – Q17). Write and READ operations are both done in bursts of 4 to successive internal memory locations.

Internally read and write operations are 72 bits wide as shown in figure 1. Control logic and latches convert the internal memory architecture to the "X18" architecture seen externally.

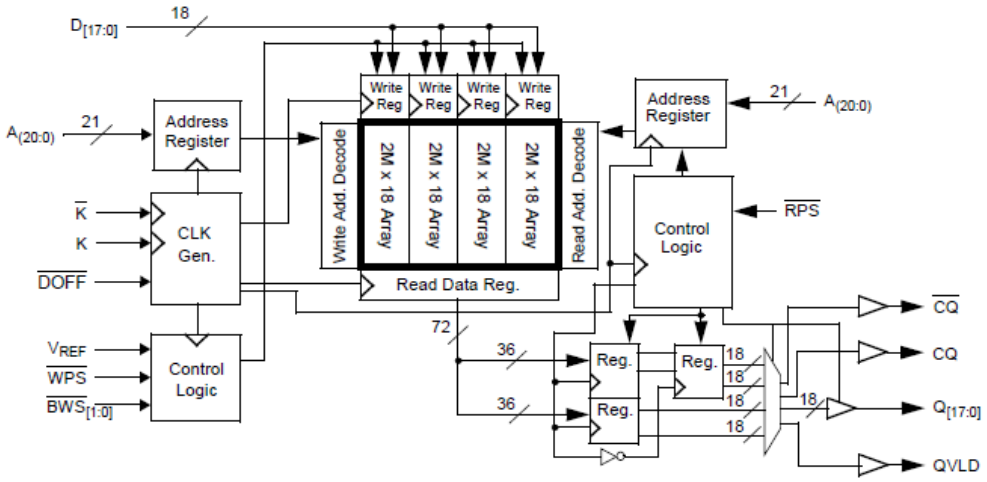

Figure 1. Functional Diagram for CYRS1643AV18

These devices were packaged in column grid array (CGA) packages which had their lids attached with tape. They were permanently mounted to small carrier cards to make handling them easier at the facility and to prevent damaging them when their tops were removed. An overview of the carrier card is shown in figure 2.

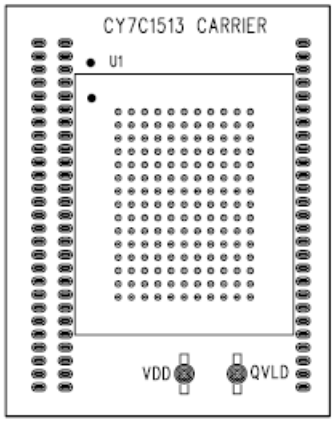

Figure 2. Carrier Card for CYRS1643AV18

Testing was performed using a JD Instruments Algorithmic Test Vector (ATV) system. The main chassis of the tester was located in the SEE irradiation room and connected to the test head mounted on the actuating arm of the chamber. A USB cable connected the tester to a controlling computer located in the experimenter area.

All testing was done with one device at a time inserted into a test card mounted on the ATV test head.

Testing was performed by Jake Tausch of JD Instruments and Helmut Puchner of Cypress Semiconductor.

Parts were irradiated in air at a distance of 30mm from the aramica window of the source. Testing was performed using four ion species in the 25 MeV SEE beam. Xenon (^{129}Xe) was used for LETs between 40 and 120 (MeV*cm^2)/mg, Krypton (^{84}Kr) for LETs of 20 and 30 (MeV*cm^2)/mg, Argon (^{40}Ar) for LETs of 5.6 and 12 (MeV*cm^2)/mg and Neon (^{22}Ne) for an LET of 1.8 (MeV*cm^2)/mg.

Figures 3 and 4 show the range vs. LET for various ions available with this set-up. Note that all ions used had a range >200u in silicon

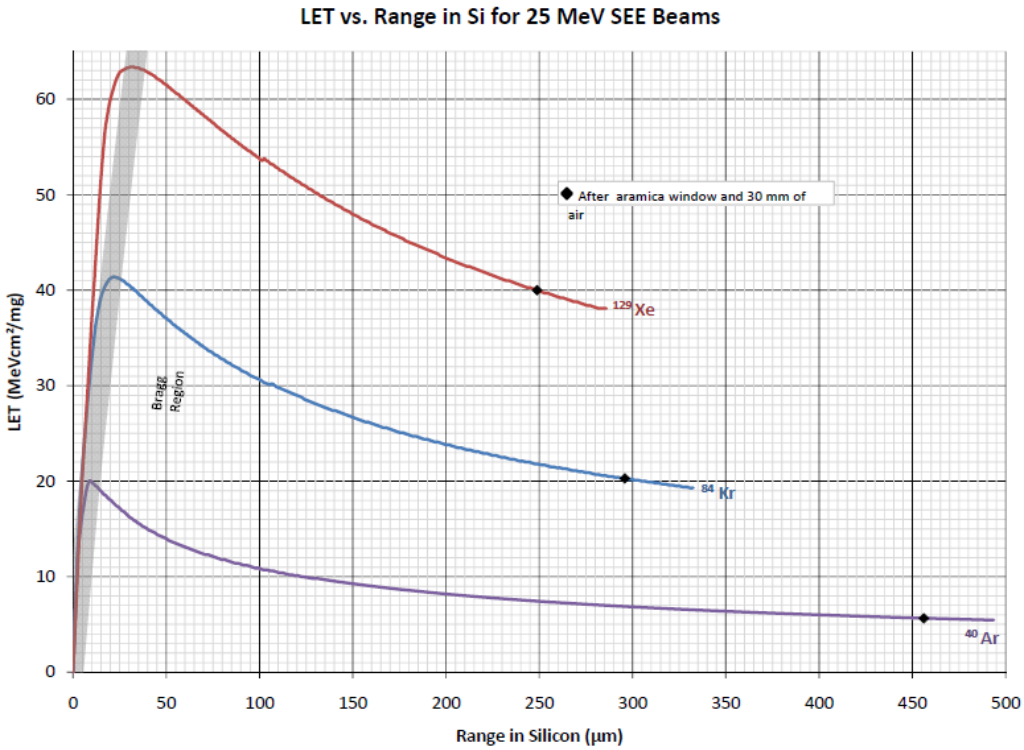

Figure 3. Ion Range vs. LET, Various Ions, 25 MeV beam, Texas A&M Cyclotron

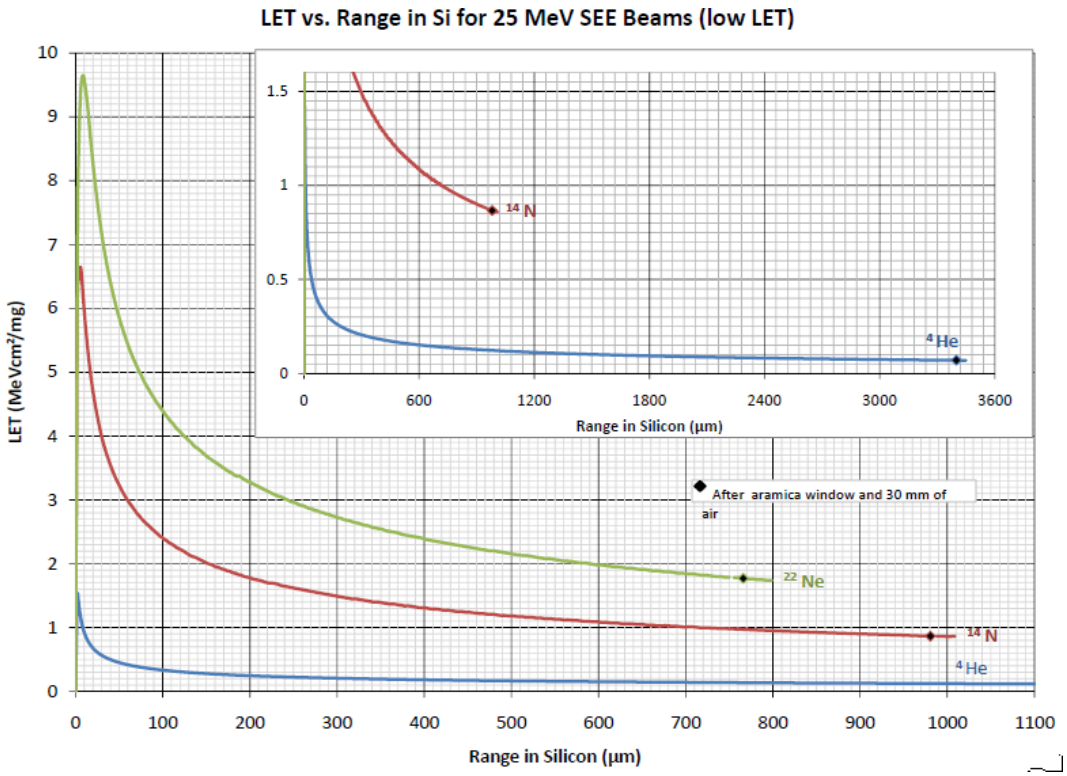

Figure 4. Ion Range vs. LET, low LET Ions, 25 MeV beam, Texas A&M Cyclotron

Testing was done in compliance with ASTM F1192, "Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices" and also in compliance with EIA/JESD57, "Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation".

Latch-up testing was performed to determine the upper limits of temperature and Linear Energy Transfer (LET) where these parts could be safely operated.

Static memory upsets were measured vs. LET to generate a capture cross-section curve for memory bits.

Dynamic upset tests were performed vs. LET to determine functional upset rates of internal logic paths and clock circuitry.

2.0 Dosimetry

Dosimetry was provided by TAMU personnel in electronic form. Records of this testing will be maintained along with test data as described in JD Instruments test procedures.

3.0 Test Results

TV1 QML-V production screened units (TV1-23/24/25/26/27) have been used for SEE qualification testing. The corresponding Cypress Fab Lot was L9729013.

3.1 Latch-Up

These parts were tested for single event latch-up (SEL) over a range of LETs from 40 to 120 (MeV*cm^2)/mg with device temperature always being held above 125^0C and devices biased Vdd = Vddq = 1.9V. Prior to radiation each device was loaded with a logical checkerboard pattern. Devices were clocked at 250MHz during radiation exposures but no logical read/write operations were performed. Proper device functionality was verified at the conclusion of each exposure.

All test points were measured with by exposing DUTs to 1E7 ions/cm^2.

LETs greater than 60 (MeV*cm^2)/mg were achieved by degrading the Xe ion to a normal incident LET of 60 (MeV*cm^2)/mg and irradiating the DUT at an angle.

Elevated DUT temperature was achieved by placing strip heaters underneath the carrier card of each DUT and heating the carrier card/DUT from the back side. An infrared thermometer was used to measure the actual die temperature. The infrared thermometer had a calibrated accuracy of +/- 1^0C (see figure 5). DUT temperatures greater than 125^0C were maintained for all DUTs at all LETs.

Figure 5. Infrared Thermometer

A total of 5 parts were tested for SEL. Over the course of testing no parts ever latched, even when exposed to the upper limit of 125^0C and an LET of 120 MeV/(mg/cm^2). A copy of the SEL portion of the run log is shown in Fig. 6 to illustrate these results.

								DOSE - rad(Si)		
Run#	DUT	deg-C	ION	Angle	LET	Flux	Fluence	This Run	Cumulative	Latch?
1	TV1-23	130	Xe	0	40	5300	1.00E+07	6430	6430	No
2		127	"	0	60	13000	1.00E+07	9620	16050	No
3		127	"	45	80	14500	1.00E+07	12820	28870	No
4		127	"	60	100	11600	1.00E+07	16020	44890	No
5		127	"	60	120	9980	1.00E+07	19200	64090	No
6		127	"	60	120	8500	1.00E+07	19320	83410	No
7	TV1-24	127	"	60	120	19110	1.00E+07	19220	19220	No
8	"	127	"	60	120	14260	1.00E+07	19220	38440	No
9	TV1-25	126	"	60	120	50600	1.00E+07	19210	19210	No
10	TV1-26	126	"	60	120	58600	1.00E+07	19200	19200	No
11	TV1-27	127	"	60	120	53500	1.00E+07	19230	19230	No

Figure 6. SEL RUN Log for CYRS1643 QDR Memories

3.2 Current Increase During SEL Exposures

During SEL testing it was noted that Idd would increase over the course of exposure. This increase followed a very consistent path vs. fluence regardless of LET. At the conclusion of each SEL exposure the devices were fully functional and would operate at the elevated current until Vdd was cycled. After power cycling Idd would drop back to its initial level and devices would be fully functional at that lower current level.

Figure 7 shows how Idd would increase vs. fluence for all parts and all LETs used for SEL testing. In the legend for this plot each curve is labeled to show the lot number, device number and LET used for the exposure. Thus, the topmost curve in the legend is "TV1-23-40" which indicates it is for device serial number 23 from lot TV1 and the ion had an LET of 40 MeV/(mg/cm^2).

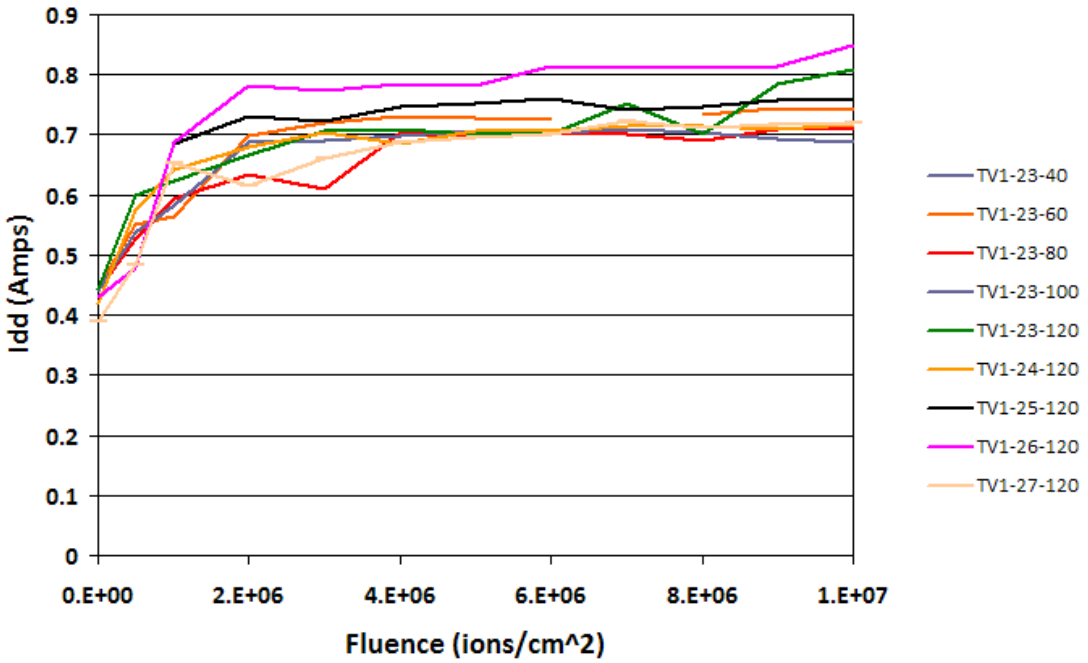

Figure 7. Idd vs Fluence during SEL Exposures

The reason for this increase is unknown, but it does not seem to adversely affect device performance.

3.3 Memory Upset Cross-Section

Memory upset testing on these parts tests was performed with Vdd = 1.7V and Vddq = 1.4V. Upset behavior was determined by loading them with a logical checkerboard pattern, irradiating to some fluence and then reading the pattern back. Even though this was a static test the parts were operated at a constant clock frequency of 250 MHz during irradiation.

Five DUTs were exposed to ions having LETs between 1.8 and 60 MeV/(mg/cm^2). Results of these measurements are shown in figure 8 along with a fitted Weibull curve.

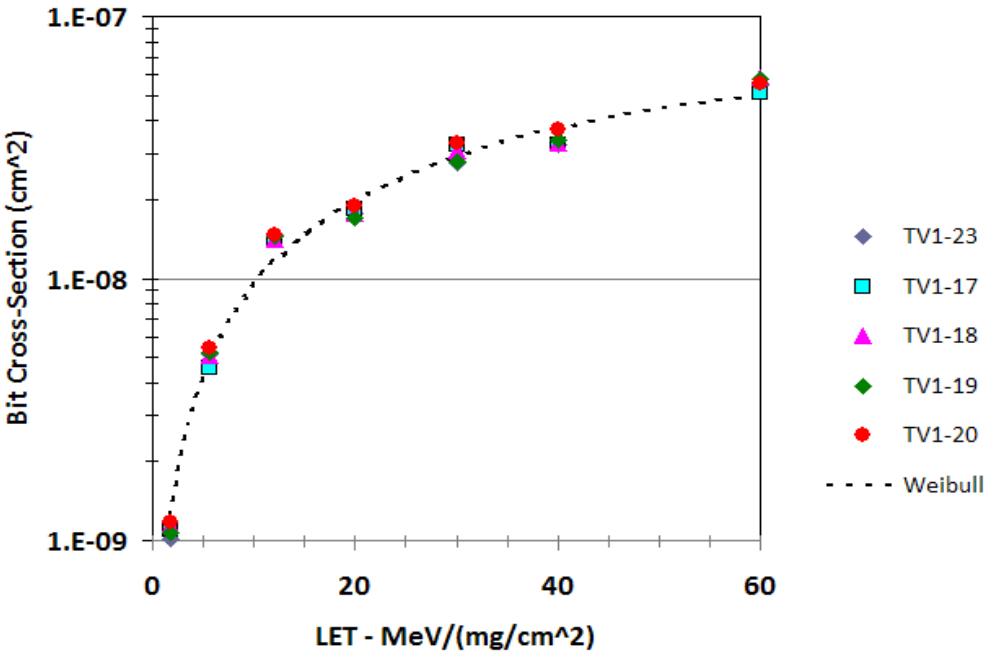

Figure 8. Static Memory Upset Cross-Section Curve

All DUTs in this test were from the same wafer (TV1) which resulted in all parts having very similar results. The run log for memory upset testing is presented in Attachment 1.

Weibull parameters for the curve in Figure 8 are as follows:

OnSet LET = 0.13 MeV/(mg/(cm^2))
Width = 50
Exponent = 1.2
Saturated X-Section = 7.2 u^2 = 7.2e-8 cm^2

Using these parameters the upset rates in various orbits and conditions can be calculated. Figure 9 shows the upset rates for these devices in a selection of conditions

	SEUs/Device/Day
Space Station, Solar Minimum	6.37
Space Station, Worst Day (Flare)	2.94E+03
Geosynchronous, Solar Minimum	5.05E+01
Geosynchronous, Worst Day (Flare)	4.00E+05

Figure 9. Upset Rates for Various Orbits and Conditions

3.4 Memory Upset Patterns

Detailed failure information was collected as part of this test. When the ATV system detects an error it automatically records the address of that error along with the expected data pattern and the location of failing bits. Figure 10 shows an excerpt of the data log from Run 76 where DUT TV1-17 was exposed to Neon ions having an LET of 1.8 MeV/(mg/(cm^2)).

ADDR	DATA		Dhi	
	EXP	ERR	EXP	ERR
0x26c0	0101010101010101	-------F--------	01	
0x9564	0101010101010101	---------F-----	01	
0xc7bd	1010101010101010	---F-----------	10	
0xec4d	1010101010101010		10	-F
0xecd0	0101010101010101	------------F-	01	
0x10e88	1010101010101010	----F----------	10	
0x128f7	0101010101010101	-----F---------	01	
0x1386a	0101010101010101	-------F--------	01	
0x13c83	0101010101010101	------------F--	01	
0x13cb0	0101010101010101	---------F-----	01	
0x15312	0101010101010101	-F------------	01	
0x1a0aa	1010101010101010	F-------------	10	
0x1b829	0101010101010101	----------F---	01	
0x1c727	0101010101010101	------------F-	01	
0x1faf9	0101010101010101	-------F------	01	
0x23fe7	0101010101010101	-F------------	01	
0x2c959	0101010101010101	------F--------	01	
0x2c95d	1010101010101010	------F--------	10	
0x3168f	1010101010101010	------F--------	10	
0x37476	1010101010101010		10	-F
0x37df3	0101010101010101	----------F---	01	
0x39cd8	0101010101010101	------F--------	01	
0x3cde7	0101010101010101	----F----------	01	
0x3d402	0101010101010101		01	-F
0x411b8	1010101010101010	--F------------	10	
0x450f0	1010101010101010	---F-----------	10	
0x4aa86	1010101010101010	-----F---------	10	
0x4cb4a	0101010101010101	-------F--------	01	
0x4daa8	1010101010101010	---F-----------	10	
0x4e0c7	1010101010101010		10	-F
0x4f2b8	1010101010101010	----F----------	10	
0x50f59	1010101010101010	------------F	10	
0x53563	0101010101010101	----------F----	01	
0x5ad1b	1010101010101010	----F----------	10	

Figure 10. Partial Error Log from Run 76, SN TV1-17, Neon ion, LET = 1.8 MeV/(mg/(cm^2))

The error log is arranged so that failing addresses are shown first followed by pairs of entries for each “Pin Group”. The entries for each pin group are the expected pattern followed by the pattern of failed bits. ATV test cards are limited to 16 bits of data each so the 18 bits of data from these parts were split into 2 pin groups. The first pin group is 16 bits long and called “DATA”. The second pin group is 2 bits long and called “Dhi”.

In this log the first failure was located at address 0x26C0 where there was a single bit failure at the bit D8 location of the “DATA” pin group and no failure in the “Dhi” pin group. At address 0xEC4D there was a single bit failure at bit D0 in the “Dhi” pin group.

Note that all failing addresses had single bit errors. Also note that there were 2 failures in the same bit location at addresses 0x2C959 and 0x2C95D which are very close in logical space.

These memories are layed out such that memory cells associated with any data bit are physically close. If an ion strike causes a multi-cell upset the errors will show up as occurring at some bit location across a series of closely related addresses. This phenomena is further illustrated in Figure 11 which shows partial error logs for cases where LETs were 12 and 60 MeV/(mg/(cm^2)) . Note that, as LET increases, there is an increase in the number of closely related addresses with the same failing bit pattern.

ADDR	DATA EXP	DATA ERR	Dhi EXP	Dhi ERR
0x113	0101010101010101	----------F--	01	
0x117	1010101010101010	----------F--	10	
0x572	0101010101010101	------F--------	01	
0x6a0	0101010101010101	----------F---	01	
0x6bc	1010101010101010	----------F---	10	
0x1560	1010101010101010	----------F-	10	
0x1574	0101010101010101	----------F-	01	
0x1578	1010101010101010	----------F-	10	
0x1630	1010101010101010	----F---------	10	
0x1634	0101010101010101	----F---------	01	
0x1638	1010101010101010	----F---------	10	
0x163c	0101010101010101	----F---------	01	
0x17c3	1010101010101010	----------F---	10	
0x17db	1010101010101010	----------F---	10	
0x17df	0101010101010101	----------F---	01	
0x2074	1010101010101010	--------F------	10	
0x2078	0101010101010101	--------F------	01	
0x2707	1010101010101010	----------F-	10	
0x270b	0101010101010101	----------F-	01	
0x270f	1010101010101010	----------F-	10	
0x27c3	0101010101010101	----------F---	01	
0x27c7	1010101010101010	----------F---	10	
0x2b27	1010101010101010	--------F------	10	
0x2b2b	0101010101010101	--------F------	01	
0x2c95	1010101010101010	----F----------	10	
0x2c99	0101010101010101	----F----------	01	
0x2c9d	1010101010101010	----F----------	10	
0x2f8e	1010101010101010	---F----------	10	
0x2f92	0101010101010101	---F----------	01	
0x2f96	1010101010101010	---F----------	10	
0x3240	1010101010101010	-F----------	10	
0x3258	1010101010101010	-F----------	10	
0x325c	0101010101010101	-F----------	01	
0x3d36	0101010101010101	---F----------	01	

LET = 12

ADDR	DATA EXP	DATA ERR	Dhi EXP	Dhi ERR
0x3c5	1010101010101010	----------F--	10	
0x3cd	1010101010101010	----------F--	10	
0x3d9	0101010101010101	----------F--	01	
0x3dd	1010101010101010	----------F--	10	
0x760	0101010101010101	------F--------	01	
0x764	1010101010101010	------F--------	10	
0x774	1010101010101010	------F--------	10	
0x778	0101010101010101	------F--------	01	
0x77c	1010101010101010	------F--------	10	
0x8ee	1010101010101010	-------F-------	10	
0x8f2	0101010101010101	-------F-------	01	
0x93a	0101010101010101	----------F---	01	
0x946	1010101010101010	----------F---	10	
0x94a	0101010101010101	----------F---	01	
0xab7	1010101010101010	--------F------	10	
0xabf	1010101010101010	--------F------	10	
0xac3	0101010101010101	--------F------	01	
0xac7	1010101010101010	--------F------	10	
0xacb	0101010101010101	--------F------	01	
0xacf	1010101010101010	--------F------	10	
0xce9	0101010101010101	----------F----	01	
0xced	1010101010101010	----------F----	10	
0xcf1	0101010101010101	----------F----	01	
0xcf9	0101010101010101	----------F----	01	
0xcfd	1010101010101010	----------F----	10	
0xdc9	0101010101010101	---------F-----	01	
0xdcd	1010101010101010	---------F-----	10	
0x12c7	0101010101010101	-----F----------	01	
0x12cb	1010101010101010	-----F----------	10	
0x12d3	1010101010101010	-----F----------	10	
0x12df	0101010101010101	-----F----------	01	
0x1764	0101010101010101	------F--------	01	
0x176c	0101010101010101	------F--------	01	
0x1778	1010101010101010	------F--------	10	

LET = 60

Figure 11. Partial Error Log from Runs 59 and 22, SN TV1-17, Argon (LET = 12) and Xenon (LET=60)

3.5 Logic Upsets

The primary upset mechanism for these devices is memory upsets. In fact, with normal testing, so many memory upsets occur at low fluences that other upset mechanisms will probably never be observed. With this in mind a special test algorithm was developed in which a pattern (Data = Address) would be written to a burst of 4 addresses and then immediately read back. The next 4 addresses would then be written/read, etc until the entire memory space had been tested. Since there was very little time between writing and reading any set of 4 memory patterns then there would be a correspondingly low probability of memory upsets. Consequently, any upsets that occurred would probably come from strikes in other circuitry.

A simplified timing diagram for this test is shown in Figure 12.

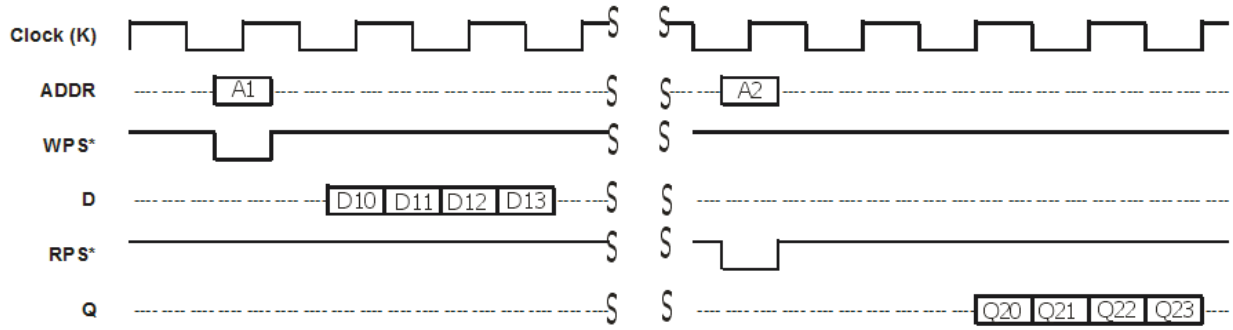

Figure 12. Simplified Timing Diagram for "Logic Upset" Test

Note that a burst of 4 write sequence is started by holding pin WPS* low during the rising edge of the clock. After a delay of 1 clock cycle data is then written to 4 sequential memory addresses on each of the following 4 clock edges. A burst of 4 read sequence is started by holding pin RPS* low on the rising edge of the clock. After a delay of 2 clock cycles data from 4 sequential addresses is then presented after each of the following clock edges.

In the actual test there was a constant time delay of 200nS between the WPS* and RPS* commands due to the speed of the ATV tester and the details of the algorithm it was performing. This translated into 48 DUT clock cycles at 240MHz where logic testing was performed. Thus, there were 44 clock cycles between the end of the last clock of the write sequence and beginning of the read sequence.

When this test was run the error generation rate, as expected, was much lower than that seen for memory upset testing and patterns in the data log files were markedly different from those shown earlier. Figure 13 shows a simplified data log from run #23 which was a test on DUT TV1-17 with an LET of 60 MeV/(mg/(cm^2)).

Test#	Time	ADDR	DATA EXP	ERR	Dhi EXP	Dhi ERR
5114	49:21.2	0x1f507c	0101000001111100	----------FFF	11	
		0x1f507d	0101000001111101	----------FF-	11	
		0x1f507e	0101000001111110	----------F-F	11	
		0x1f507f	0101000001111111	----------F--	11	
		0x1f5080	0101000010000000	--------FFFFF-FF	11	
		0x1f5081	0101000010000001	--------FFFFF-F-	11	
		0x1f5082	0101000010000010	--------FFFFF--F	11	
		0x1f5083	0101000010000011	--------FFFFF---	11	
5119	49:35.0	0x332bf8	0010101111111000	----------FF--	11	
		0x332bf9	0010101111111001	----------FF--	11	
		0x332bfa	0010101111111010	----------FF--	11	
		0x332bfb	0010101111111011	----------FF--	11	
5126	49:54.8	0x28d735	1101011100110100	----------F	00	
		0x28d736	1101011100110110	----------FF	00	
		0x28d737	1101011100110110	----------F	00	
5128	50:00.5	0x195f2a	0101111100101010	----------F-	01	
		0x195f2b	0101111100101011	----------F-	01	
5130	50:06.0	0x322da	0010001011011010	----------F-	11	
		0x322db	0010001011011011	----------F-	11	
5131	50:09.0	0x24296c	0010100101101100	----------FFF	00	
		0x24296d	0010100101101101	----------FF-	00	
		0x24296e	0010100101101110	----------F-F	00	
		0x24296f	0010100101101111	----------F--	00	
		0x242972	0010100101110010	----------FF	00	
		0x242973	0010100101110011	----------F-	00	
		0x242978	0010100101111000	----------FFFF	00	
		0x242979	0010100101111001	----------FFF-	00	
		0x24297a	0010100101111010	----------FF-F	00	
		0x24297b	0010100101111011	----------FF--	00	

Figure 13. Simplified Data Log for Run #23, Dynamic Test, SN TV1-17, LET = 60 MeV/(mg/(cm^2))

The error log shown in Figure 13 includes a test number and start time (minutes). The dynamic test algorithm would step through the entire memory space in ~3 seconds, logging any errors that occurred during that test. The test would be constantly re-run over the duration of radiation exposure. Quite often no errors would be detected for a run so nothing would be logged. In this log errors were detected during run #5114 and again during run #5119. No errors were detected during runs 5115, 5116, 5117 or 5118.

An examination of this error log shows bit upsets during runs 5128 and 5130 that were probably due to memory cell upsets. Other groups of errors have signatures that are totally different from random memory upsets. Errors in each of the other runs show up as multiple bit errors across a series of sequential (or almost sequential) addresses. Each of these is interpreted as an ion strike in some portion of the circuitry other than memory cells.

For analysis each of the failing groups of cells in Figure 13 would be considered a single upset at the device level. Thus, data in Figure 13 would represent 4 device upsets and 4 single bit errors.

Logic upset testing was performed on 5 DUTs over a range of LETs between 5.6 and 120 MeV/(mg/(cm^2)). Results for these tests are shown in Figure 14. The wide scatter across the data is due to the low number of occurrences for this type of upset. Even when irradiated to fluences above

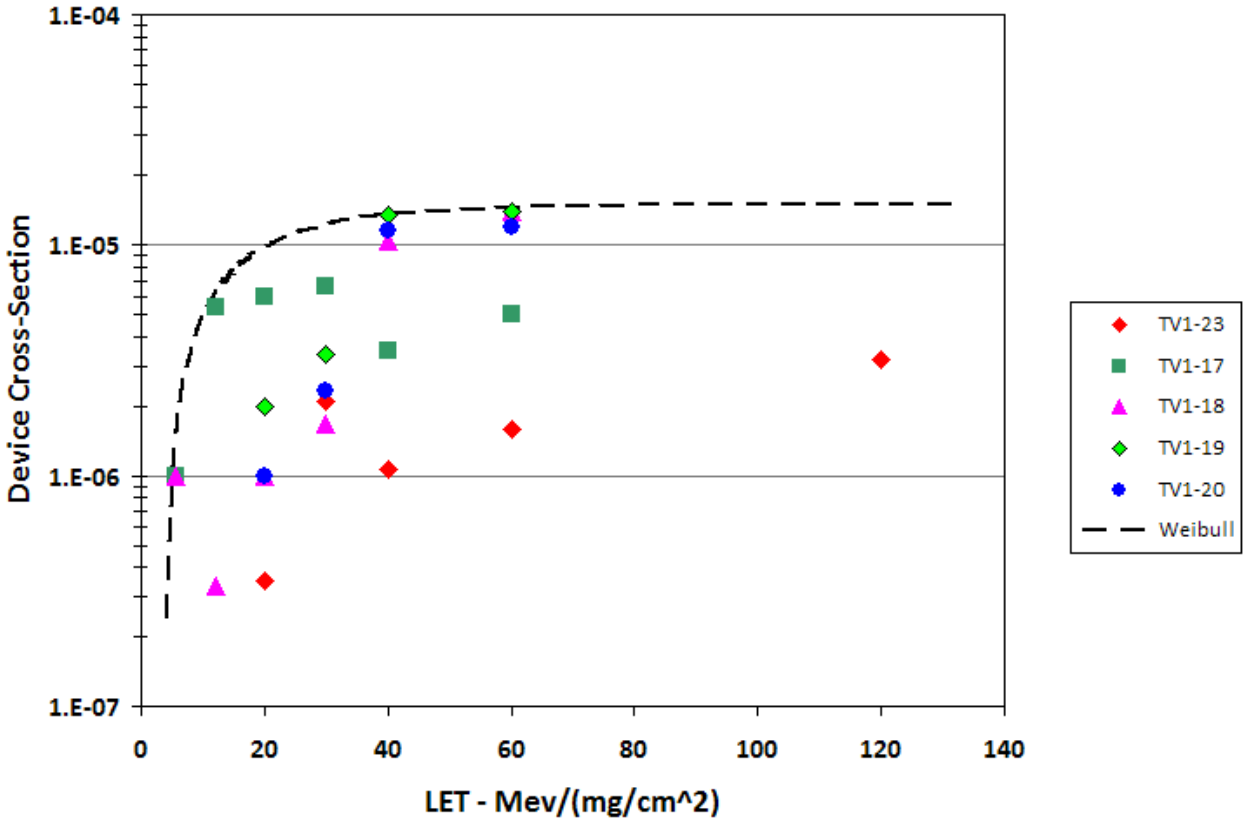

Figure 14. Device Cross-Section Curve for "Logic" Upsets

A Weibull curve was calculated for the data in figure 14 that would "bound" all errors. Parameters for this Weibull curve are as follows:

OnSet LET = 4.0 MeV/(mg/(cm^2))
Width = 15
Exponent = 1.0
Saturated X-Section = 1.5e-5 cm^2

4.0 Conclusions

All test goals were met. Specific things learned from this test are as follows

1) No latch-ups were observed in any of the 5 test devices up to:
   - 125^0C
   - Vdd = Vddq = 1.9V
   - 120MeV(mg/cm^2)
   - 1E7 ions/cm^2
2) A memory cell upset curve was developed using 5 devices. Upset cross-sections were very repeatable across all devices.
3) Device level upset cross-sections were measured for logic circuitry.
4) No SEFI's were ever observed … just bit upsets

Attachment 1. Memory Upset Run Log

Run#	DUT	ION	LET	Flux	Fluence	Upset						Cross-Section					
						TVI-23	TVI-27	TVI-17	TVI-18	TVI-19	TVI-20	TVI-23	TVI-27	TVI-17	TVI-18	TVI-19	TVI-20
12	TVI-27	Xe	40.0	179	1.06E+03		1833						1.5E-08				
13	"	"	40.0	248	5.00E+03		8105						1.4E-08				
14	"	"	60.0	208	4.90E+03		12264						2.2E-08				
17	TVI-23	"	40.0	235	2.00E+04	46351						3.3E-08					
18	"	"	60.0	181	1.11E+04	43946						5.6E-08					
21	TVI-17	"	40.0	210	1.00E+04			24293						3.2E-08			
22	"	"	60.0	160	1.00E+04			38438						5.1E-08			
25	TVI-18	"	40.0	208	2.00E+04				49409						3.3E-08		
26	"	"	60.0	178	1.00E+04				44050						5.8E-08		
29	TVI-19	"	40.0	247	1.00E+04					25370						3.4E-08	
30	"	"	60.0	178	5.14E+03					22498						5.7E-08	
33	"	"	40.0	151	4.90E+03						13743						3.7E-08
34	"	"	60.0	159	4.98E+03						20876						5.6E-08
38	TVI-23	Kr	20.0	165	9.86E+03	12442						1.8E-08					
39	"	"	30.0	144	5.68E+03	11110						2.7E-08					
42	TVI-20	"	20.0	226	5.20E+03						7456						1.9E-08
43	"	"	30.0	187	6.46E+03						16069						3.3E-08
46	TVI-19	"	20.0	234	5.12E+03					6550						1.7E-08	
47	"	"	30.0	182	5.00E+03					10612						2.8E-08	
50	TVI-18	"	20.0	196	5.08E+03				6759						1.8E-08		
51	"	"	30.0	148	5.00E+03				11627						3.1E-08		
54	TVI-17	"	20.0	193	5.00E+03			6941						1.8E-08			
55	"	"	30.0	220	7.33E+03			17921						3.2E-08			
58	"	Ar	5.6	177	5.08E+03			1754						4.6E-09			
59	"	"	12.0	114	4.91E+03			5130						1.4E-08			
62	TVI-18	"	5.6	232	4.99E+03				1915						5.1E-09		
63	"	"	12.0	138	5.07E+03				5389						1.4E-08		
66	TVI-19	"	5.6	262	7.58E+03					2974						5.2E-09	
67	"	"	12.0	212	5.09E+03					5560						1.4E-08	
68	TVI-20	"	12.0	149	3.32E+03						3658						1.5E-08
69	"	"	5.6	277	5.00E+03						2058						5.5E-09
70	TVI-23	"	5.6	438	4.95E+03	1828						5.2E-09					
71	"	"	12.0	267	4.88E+03	5124						1.5E-08					
72	"	Ne	1.8	259	5.09E+03	368						1.0E-09					
73	TVI-20	"	1.8	280	5.01E+03						444						1.2E-09
74	TVI-19	"	1.8	330	5.16E+03					416						1.1E-09	
75	TVI-18	"	1.8	300	5.05E+03				434						1.1E-09		
76	TVI-17	"	1.8	280	5.10E+03			422						1.1E-09			