CY15B104QN
CY15V104QN

Excelon™ Auto 4-Mbit (512K × 8) Automotive-A Serial (SPI) F-RAM

Features

- 4-Mbit ferroelectric random access memory (F-RAM) logically organized as 512K × 8
  - Virtually unlimited endurance of 100 trillion (10^{14}) read/write cycles
  - 151-year data retention (see Data Retention and Endurance on page 20)
  - NoDelay™ writes
  - Advanced high-reliability ferroelectric process
- Fast serial peripheral interface (SPI)
  - Up to 50 MHz frequency
  - Supports SPI mode 0 (0, 0) and mode 3 (1, 1)
- Sophisticated write protection scheme
  - Hardware protection using the Write Protect ($\overline{\text{WP}}$) pin
  - Software protection using Write Disable (WRDI) instruction
  - Software block protection for 1/4, 1/2, or entire array
- Device ID and Serial Number
  - Device ID includes manufacturer ID and product ID
  - Unique ID
  - Serial Number
- Dedicated 256-byte special sector F-RAM
  - Dedicated special sector write and read
  - Stored content can survive up to 3 standard reflow soldering cycles
- Low-power consumption
  - 400 µA (typ) active current at 1 MHz
  - 3.7 mA (typ) active current at 40 MHz
  - 2.7 µA (typ) standby current
  - 1.1 µA (typ) Deep Power Down mode current
  - 0.1 µA (typ) Hibernate mode current
- Low-voltage operation:
  - CY15V104QN: V_{DD} = 1.71 V to 1.89 V
  - CY15B104QN: V_{DD} = 1.8 V to 3.6 V
- Automotive-A operating temperature: –40 °C to +85 °C
- AEC-Q100 Grade 3 compliant
- 8-pin Small Outline Integrated Circuit (SOIC) package
- Restriction of hazardous substances (RoHS) compliant

Functional Description

The Excelon Auto CY15X104QN is an automotive grade, 4-Mbit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or F-RAM is nonvolatile and performs reads and writes similar to a RAM. It provides reliable data retention for 151 years while eliminating the complexities, overhead, and system-level reliability problems caused by serial flash, EEPROM, and other nonvolatile memories.

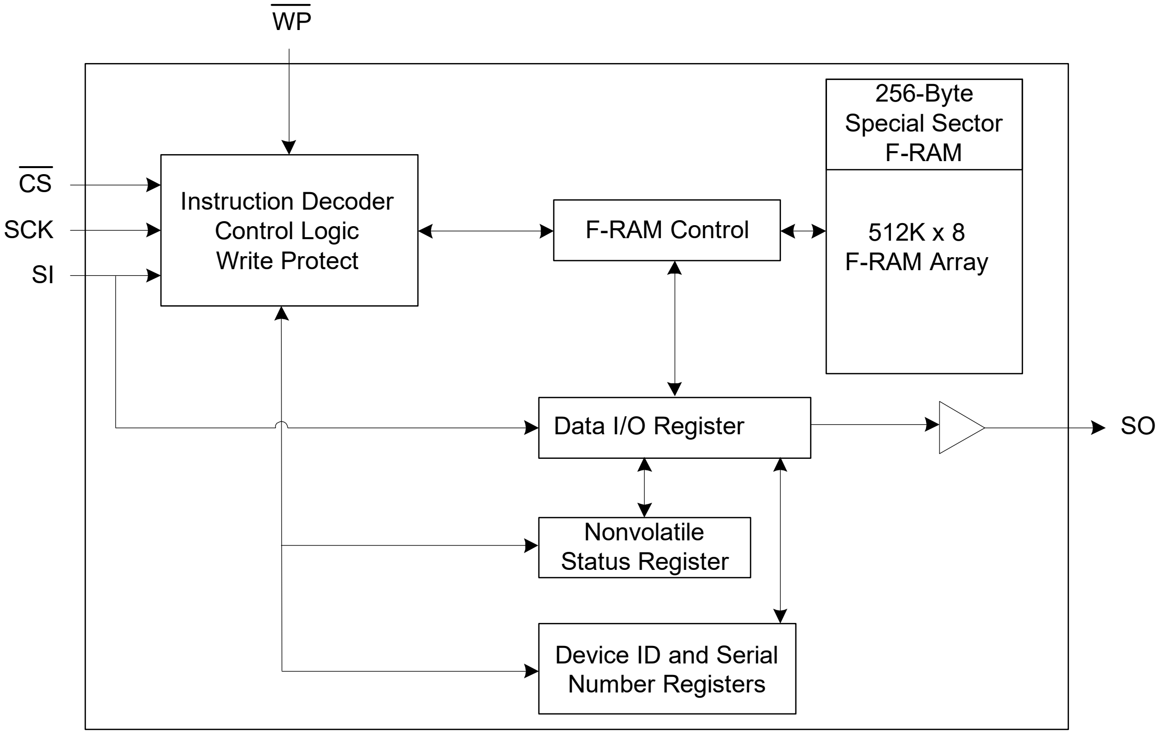
Unlike serial flash and EEPROM, the CY15X104QN performs write operations at bus speed. No write delays are incurred. Data is written to the memory array immediately after each byte is successfully transferred to the device. The next bus cycle can commence without the need for data polling. In addition, the product offers substantial write endurance compared to other nonvolatile memories. The CY15X104QN is capable of supporting 10^{14} read/write cycles, or 10 million times more write cycles than EEPROM.

These capabilities make the CY15X104QN ideal for nonvolatile memory applications, requiring frequent or rapid writes. Examples range from data collection, where the number of write cycles may be critical, to demanding industrial controls where the long write time of serial flash or EEPROM can cause data loss.

The CY15X104QN provides substantial benefits to users of serial EEPROM or flash as a hardware drop-in replacement. The CY15X104QN uses the high-speed SPI bus, which enhances the high-speed write capability of F-RAM technology. The device incorporates a read-only Device ID and Unique ID features, which allow the host to determine the manufacturer, product density, product revision, and unique ID for each part. The device also provides a writable, 8-byte serial number registers, which can be used to identify a specific board or a system.

For a complete list of related resources, click here.

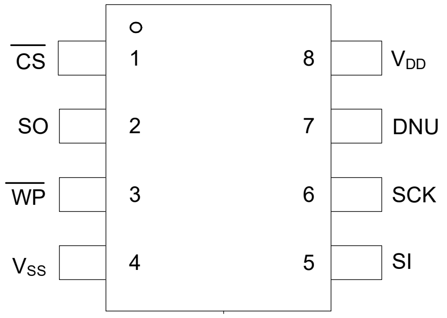
Logic Block Diagram



Contents

Pinouts

Figure 1. 8-pin SOIC Pinout



TOP View
(Not to Scale)

Pin Definitions

Pin Name	I/O Type	Description
$\overline{\text{CS}}$	Input	**Chip Select**. This active LOW input activates the device. When HIGH, the device enters low-power standby mode, ignores other inputs, and the output is tristated. When LOW, the device internally activates the SCK signal. A falling edge on $\overline{\text{CS}}$ must occur before every opcode.
SCK	Input	**Serial Clock**. All I/O activity is synchronized to the serial clock. Inputs are latched on the rising edge and outputs occur on the falling edge of the serial clock. The clock frequency can be any value between 0 and 50 MHz and may be interrupted at any time due to its synchronous behavior.
SI [1]	Input	**Serial Input**. All data is input to the device on this pin. The pin is sampled on the rising edge of SCK and is ignored at other times. It should always be driven to a valid logic level to meet the power (I_{DD}) specifications.
SO [1]	Output	**Serial Output.** This is the data output pin. It is driven during a read and remains tristated at all other times. Data transitions are driven on the falling edge of the serial clock SCK.
$\overline{\text{WP}}$	Input	**Write Protect.** This Active LOW pin prevents write operation to the Status Register when WPEN bit in the Status Register is set to '1'. This is critical because other write protection features are controlled through the Status Register. A complete explanation of write protection is provided in Table 2 and Table 5 on page 9. This pin has an internal weak pull-up resistor which keeps this pin HIGH if left floating (not connected on the board). This pin can also be tied to V_{DD} if not used.
DNU	Do not use	**Do Not Use.** Either leave this pin floating (not connected on the board) or tie to V_{DD}.
V_{SS}	Power supply	Ground for the device. Must be connected to the ground of the system.
V_{DD}	Power supply	Power supply input to the device.

Note

1. SI may be connected to SO for a single pin data interface.

Functional Overview

The CY15X104QN is a serial F-RAM memory. The memory array is logically organized as 524,288 × 8 bits and is accessed using an industry-standard serial peripheral interface (SPI) bus. The functional operation of the F-RAM is similar to serial flash and serial EEPROMs. The major difference between the CY15X104QN and a serial flash or EEPROM with the same pinout is the F-RAM's superior write performance, high endurance, and low power consumption.

Memory Architecture

When accessing the CY15X104QN, the user addresses 512K locations of eight data bits each. These eight data bits are shifted in or out serially. The addresses are accessed using the SPI protocol, which includes a chip select (to permit multiple devices on the bus), an opcode, and a three-byte address. The upper five bits of the address range are 'don't care' values. The complete address of 19 bits specifies each byte address uniquely.

Most functions of the CY15X104QN are either controlled by the SPI interface or handled by on-board circuitry. The access time for the memory operation is essentially zero, beyond the time needed for the serial protocol. That is, the memory is read or written at the speed of the SPI bus. Unlike a serial flash or EEPROM, it is not necessary to poll the device for a ready condition because writes occur at bus speed. By the time a new bus transaction can be shifted into the device, a write operation is complete. This is explained in more detail in the interface section.

Serial Peripheral Interface (SPI) Bus

The CY15X104QN is an SPI slave device and operates at speeds of up to 50 MHz. This high-speed serial bus provides high-performance serial communication to an SPI master. Many common microcontrollers have hardware SPI ports allowing a direct interface. It is simple to emulate the port using ordinary port pins for microcontrollers that do not have this feature. The CY15X104QN operates in SPI Modes 0 and 3.

SPI Overview

The SPI is a four-pin interface with Chip Select ($\overline{\text{CS}}$), Serial Input (SI), Serial Output (SO), and Serial Clock (SCK) pins.

The SPI is a synchronous serial interface, which uses clock and data pins for memory access and supports multiple devices on the data bus. A device on the SPI bus is activated using the $\overline{\text{CS}}$ pin.

The relationship between chip select, clock, and data is dictated by the SPI mode. This device supports SPI modes 0 and 3. In both of these modes, data is clocked into the F-RAM on the rising edge of SCK starting from the first rising edge after $\overline{\text{CS}}$ goes active.

The SPI protocol is controlled by opcodes. These opcodes specify the commands from the bus master to the slave device. After $\overline{\text{CS}}$ is activated, the first byte transferred from the bus master is the opcode. Following the opcode, any addresses and data are then transferred. The $\overline{\text{CS}}$ must go inactive after an operation is complete and before a new opcode can be issued.

Terms used in SPI Protocol

The commonly used terms in the SPI protocol are as follows:

SPI Master

The SPI master device controls the operations on the SPI bus. An SPI bus may have only one master with one or more slave devices. All the slaves share the same SPI bus lines and the master may select any of the slave devices using the $\overline{\text{CS}}$ pin. All of the operations must be initiated by the master activating a slave device by pulling the $\overline{\text{CS}}$ pin of the slave LOW. The master also generates the SCK and all the data transmission on SI and SO lines are synchronized with this clock.

SPI Slave

The SPI slave device is activated by the master through the Chip Select line. A slave device gets the SCK as an input from the SPI master and all the communication is synchronized with this clock. An SPI slave never initiates a communication on the SPI bus and acts only on the instruction from the master.

The CY15X104QN operates as an SPI slave and may share the SPI bus with other SPI slave devices.

Chip Select ($\overline{\text{CS}}$)

To select any slave device, the master needs to pull down the corresponding $\overline{\text{CS}}$ pin. Any instruction can be issued to a slave device only while the $\overline{\text{CS}}$ pin is LOW. When the device is not selected, data through the SI pin is ignored and the serial output pin (SO) remains in a high-impedance state.

Note: A new instruction must begin with the falling edge of $\overline{\text{CS}}$. Therefore, only one opcode can be issued for each active Chip Select cycle.

Serial Clock (SCK)

The serial clock is generated by the SPI master and the communication is synchronized with this clock after $\overline{\text{CS}}$ goes LOW.

The CY15X104QN enables SPI modes 0 and 3 for data communication. In both of these modes, the inputs are latched by the slave device on the rising edge of SCK and outputs are issued on the falling edge. Therefore, the first rising edge of SCK signifies the arrival of the first Most Significant Bit (MSb) of an SPI instruction on the SI pin. Further, all data inputs and outputs are synchronized with SCK.

Data Transmission (SI/SO)

The SPI data bus consists of two lines, SI and SO, for serial data communication. SI is also referred to as Master Out Slave In (MOSI) and SO is referred to as Master In Slave Out (MISO). The master issues instructions to the slave through the SI pin, while the slave responds through the SO pin. Multiple slave devices may share the SI and SO lines as described earlier.

The CY15X104QN has two separate pins for SI and SO, which can be connected with the master as shown in Figure 2. For a microcontroller that has no dedicated SPI bus, a general-purpose port may be used. To reduce hardware resources on the controller, it is possible to connect the two data pins (SI, SO) together and tie off (HIGH) the $\overline{WP}$ pin. Figure 3 shows such a configuration, which uses only three pins.

Figure 2. System Configuration with SPI Port

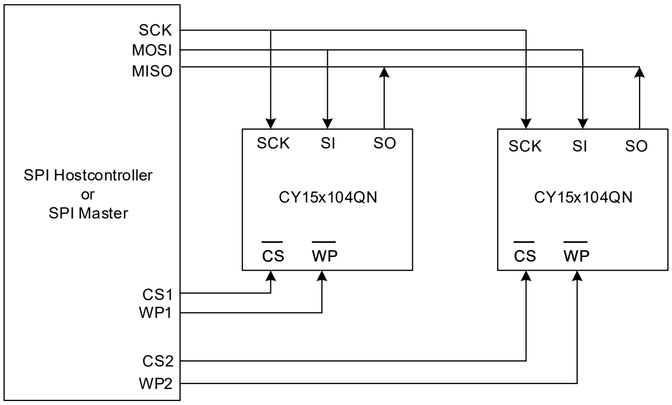
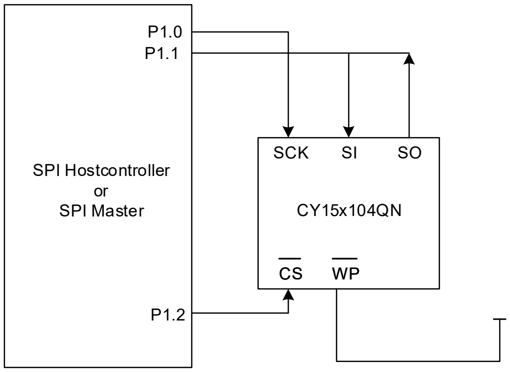


Figure 3. System Configuration without SPI Port



Most Significant Bit (MSb)

The SPI protocol requires that the first bit to be transmitted is the MSb. This is valid for both address and data transmission.

The 4-Mbit serial F-RAM requires a 3-byte address for any read or write operation. Because the address is only 19 bits, the first five bits, which are fed in are ignored by the device. Although these five bits are 'don't care', Cypress recommends that these bits be set to 0s to enable seamless transition to higher memory densities.

Serial Opcode

After the slave device is selected with $\overline{CS}$ going LOW, the first byte received is treated as the opcode for the intended operation. CY15X104QN uses the standard opcodes for memory accesses.

Invalid Opcode

If an invalid opcode is received, the opcode is ignored and the device ignores any additional serial data on the SI pin until the next falling edge of $\overline{CS}$, and the SO pin remains tristated.

Status Register

CY15X104QN has an 8-bit Status Register. The bits in the Status Register are used to configure the device. These bits are described in Table 3 on page 9.

SPI Modes

CY15X104QN may be driven by a microcontroller with its SPI peripheral running in either of the following two modes:

- SPI Mode 0 (CPOL = 0, CPHA = 0)
- SPI Mode 3 (CPOL = 1, CPHA = 1)

For both these modes, the input data is latched in on the rising edge of SCK starting from the first rising edge after $\overline{CS}$ goes active. If the clock starts from a HIGH state (in mode 3), the first rising edge after the clock toggles is considered. The output data is available on the falling edge of SCK. The two SPI modes are shown in Figure 4 and Figure 5. The status of the clock when the bus master is not transferring data is:

- SCK remains at 0 for Mode 0
- SCK remains at 1 for Mode 3

The device detects the SPI mode from the status of the SCK pin when the device is selected by bringing the $\overline{CS}$ pin LOW. If the SCK pin is LOW when the device is selected, SPI Mode 0 is assumed and if the SCK pin is HIGH, it works in SPI Mode 3.

Figure 4. SPI Mode 0

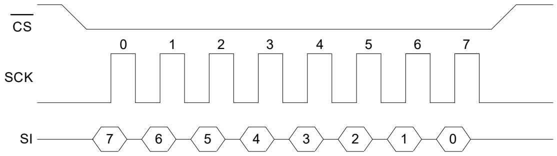
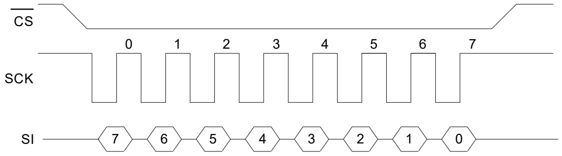


Figure 5. SPI Mode 3



Power-Up to First Access

The CY15X104QN is not accessible for a t_{PU} time after power-up. Users must comply with the timing parameter, t_{PU}, which is the minimum time from V_{DD} (min) to the first $\overline{CS}$ LOW. See Power Cycle Timing on page 23 for details.

Functional Description

Command Structure

There are 15 commands, called opcodes, that can be issued by the bus master to the CY15X104QN (see Table 1). These opcodes control the functions performed by the memory.

Table 1. Opcode Commands

Name	Description	Opcode		Max. Frequency (MHz)
		Hex	Binary	
Write Enable Control				
WREN	Set write enable latch	06h	0000 0110b	50
WRDI	Reset write enable latch	04h	0000 0100b	50
Register Access				
RDSR	Read Status Register	05h	0000 0101b	50
WRSR	Write Status Register	01h	0000 0001b	50
Memory Write				
WRITE	Write memory data	02h	0000 0010b	50
Memory Read				
READ	Read memory data	03h	0000 0011b	40
FSTRD	Fast read memory data	0Bh	0000 1011b	50
Special Sector Memory Access				
SSWR	Special Sector Write	42h	0100 0010b	50
SSRD	Special Sector Read	4Bh	0100 1011b	40
Identification and Serial Number				
RDID	Read device ID	9Fh	1001 1111b	50
RUID	Read Unique ID	4Ch	0100 1100b	50
WRSN	Write Serial Number	C2h	1100 0010b	50
RDSN	Read Serial Number	C3h	11000 011b	50
Low Power Modes				
DPD	Enter Deep Power-Down	BAh	1011 1010b	50
HBN	Enter Hibernate Mode	B9h	1011 1001b	50
Reserved				
Reserved	Reserved	Unused opcodes are reserved for future use.		–

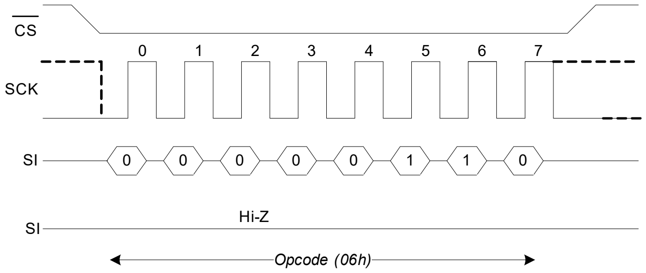
Write Enable Control Commands

Set Write Enable Latch (WREN, 06h)

The CY15X104QN will power up with writes disabled. The WREN command must be issued before any write operation. Sending the WREN opcode allows the user to issue subsequent opcodes for write operations. These include writing to the Status Register (WRSR), the memory (WRITE), Special Sector (SSWR), and Write Serial Number (WRSN).

Sending the WREN opcode causes the internal Write Enable Latch to be set. A flag bit in the Status Register, called WEL, indicates the state of the latch. WEL = ‘1’ indicates that writes are permitted. Attempting to write the WEL bit in the Status Register has no effect on the state of this bit - only the WREN opcode can set this bit. The WEL bit will be automatically cleared on the rising edge of $\overline{CS}$ following a WRDI, a WRSR, a WRITE, a SSWR, or a WRSN operation. This prevents further writes to the Status Register or the F-RAM array without another WREN command. Figure 6 illustrates the WREN command bus configuration.

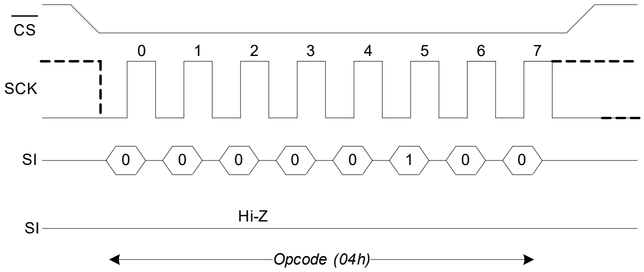
Figure 6. WREN Bus Configuration



Reset Write Enable Latch (WRDI, 04h)

The WRDI command disables all write activity by clearing the Write Enable Latch. Verify that the writes are disabled by reading the WEL bit in the Status Register and verify that WEL is equal to ‘0’. Figure 7 illustrates the WRDI command bus configuration.

Figure 7. WRDI Bus Configuration



Status Register and Write Protection

The write protection features of the CY15X104QN are multi-tiered and are enabled through the status register. The Status Register is organized as follows. (The default value shipped from the factory for WEL, BP0, BP1, bits 4–5, and WPEN is ‘0’, and for bit 6 is ‘1’.)

Table 2. Status Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN (0)	X (1)	X (0)	X (0)	BP1 (0)	BP0 (0)	WEL (0)	X (0)

Table 3. Status Register Bit Definition

Bit	Definition	Description
Bit 0	Don’t care	This bit is non-writable and always returns ‘0’ upon read.
Bit 1 (WEL)	Write Enable	WEL indicates if the device is write enabled. This bit defaults to ‘0’ (disabled) on power-up. WEL = ‘1’ --> Write enabled WEL = ‘0’ --> Write disabled
Bit 2 (BP0)	Block Protect bit ‘0’	Used for block protection. For details, see Table 4.
Bit 3 (BP1)	Block Protect bit ‘1’	
Bit 4–5	Don’t care	These bits are non-writable and always return ‘0’ upon read.
Bit 6	Don’t care	This bit is non-writable and always returns ‘1’ upon read.
Bit 7 (WPEN)	Write Protect Enable bit	Used to enable the function of Write Protect Pin ($\overline{\text{WP}}$). For details, see Table 5.

Bits 0 and 4–5 are fixed at ‘0’ and bit 6 is fixed at ‘1’; none of these bits can be modified. Note that bit 0 (“Ready or Write in progress” bit in serial flash and EEPROM) is unnecessary, as the F-RAM writes in real-time and is never busy, so it reads out as a ‘0’. An exception to this is when the device is waking up either from Deep Power-Down Mode (DPD, BAh) or Hibernate Mode (HBN, B9h). The BP1 and BP0 control the software write-protection features and are nonvolatile bits. The WEL flag indicates the state of the Write Enable Latch. Attempting to directly write the WEL bit in the Status Register has no effect on its state. This bit is internally set and cleared via the WREN and WRDI commands, respectively.

BP1 and BP0 are memory block write protection bits. They specify portions of memory that are write-protected as shown in Table 4.

Table 4. Block Memory Write Protection

BP1	BP0	Protected Address Range
0	0	None
0	1	60000h to 7FFFFh (upper 1/4)
1	0	40000h to 7FFFFh (upper 1/2)
1	1	00000h to 7FFFFh (all)

The BP1 and BP0 bits and the Write Enable Latch are the only mechanisms that protect the memory from writes. The remaining write protection features protect inadvertent changes to the block protect bits.

The write protect enable bit (WPEN) in the Status Register controls the effect of the hardware write protect ($\overline{\text{WP}}$) pin. Refer to Figure 23 on page 22 for the $\overline{\text{WP}}$ pin timing diagram. When the WPEN bit is set to ‘0’, the status of the $\overline{\text{WP}}$ pin is ignored. When the WPEN bit is set to ‘1’, a LOW on the $\overline{\text{WP}}$ pin inhibits a write to the Status Register. Thus the Status Register is write-protected only when WPEN = ‘1’ and $\overline{\text{WP}}$ = ‘0’. Table 5 summarizes the write protection conditions.

Table 5. Write Protection

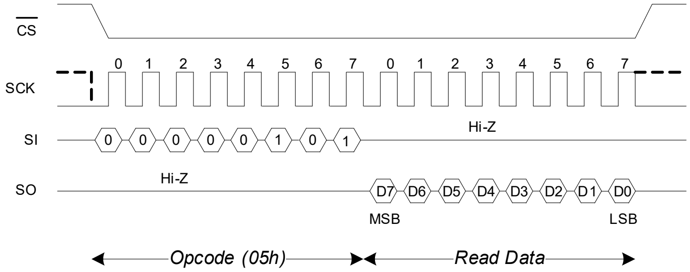
WEL	WPEN	$\overline{\text{WP}}$	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Unprotected	Unprotected
1	1	0	Protected	Unprotected	Protected
1	1	1	Protected	Unprotected	Unprotected

Register Access Commands

Read Status Register (RDSR, 05h)

The RDSR command allows the bus master to verify the contents of the Status Register. Reading the status register provides information about the current state of the write-protection features. Following the RDSR opcode, the CY15X104QN will return one byte with the contents of the Status Register.

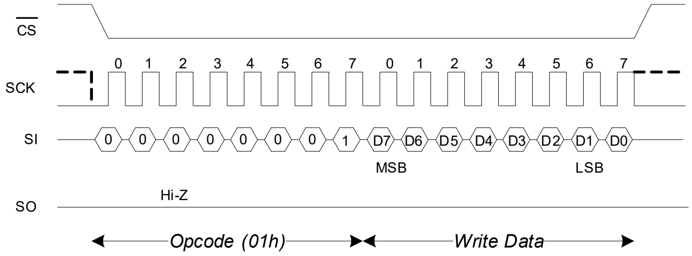
Figure 8. RDSR Bus Configuration



Write Status Register (WRSR, 01h)

The WRSR command allows the SPI bus master to write into the Status Register and change the write protect configuration by setting the WPEN, BP0, and BP1 bits as required. Before issuing a WRSR command, the WP pin must be HIGH or inactive. Note that on the CY15X104QN, WP only prevents writing to the Status Register, not the memory array. Before sending the WRSR command, the user must send a WREN command to enable writes. Executing a WRSR command is a write operation and therefore, clears the Write Enable Latch.

Figure 9. WRSR Bus Configuration (WREN not shown)



Memory Operation

The SPI interface, which is capable of a high clock frequency, highlights the fast write capability of the F-RAM technology. Unlike serial flash and EEPROMs, the CY15X104QN can perform sequential writes at bus speed. No page register is needed and any number of sequential writes may be performed.

Memory Write Operation Commands

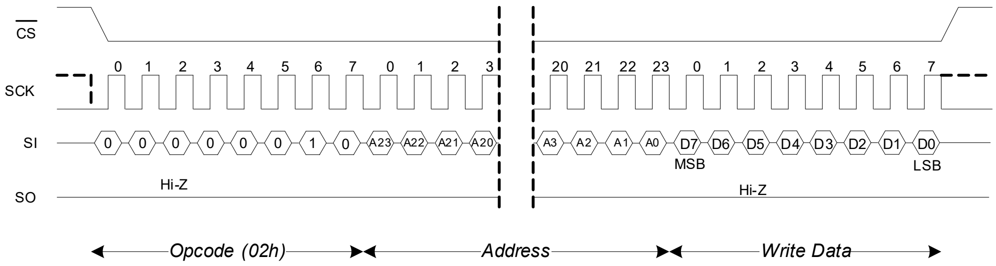
Write Operation (WRITE, 02h)

All writes to the memory begin with a WREN opcode with $\overline{\text{CS}}$ being asserted and deasserted. The next opcode is WRITE. The WRITE opcode is followed by a three-byte address containing the 19-bit address (A18–A0) of the first data byte to be written into the memory. The upper five bits of the three-byte address are ignored. Subsequent bytes are data bytes, which are written sequentially. Addresses are incremented internally as long as the bus master continues to issue clocks and keeps $\overline{\text{CS}}$ LOW. If the last address of 7FFFFh is reached, the internal address counter will roll over to 00000h. Data is written on MSb first. The rising edge of $\overline{\text{CS}}$ terminates a write operation. The CY15X104QN write operation is shown in Figure 10.

Notes

- When a burst write reaches a protected block address, the automatic address increment stops and all the subsequent data bytes received for write will be ignored by the device. EEPROMs use page buffers to increase their write throughput. This compensates for the technology's inherently slow write operations. F-RAM memories do not have page buffers because each byte is written to the F-RAM array immediately after it is clocked in (after the eighth clock). This allows any number of bytes to be written without page buffer delays.
- If power is lost in the middle of the write operation, only the last completed byte will be written.

Figure 10. Memory Write (WREN not shown) Operation

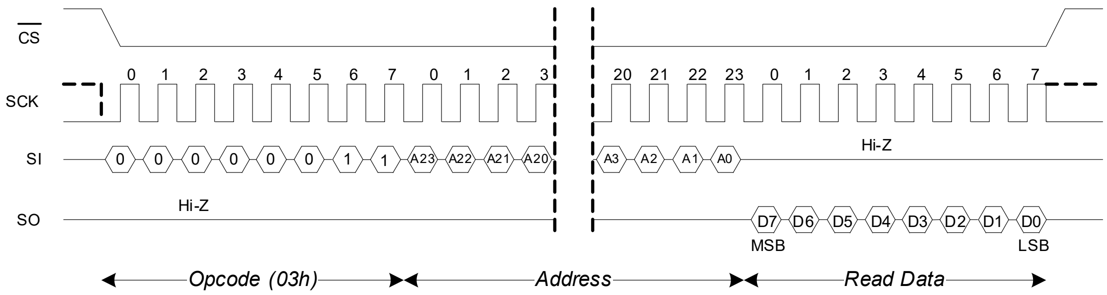


Memory Read Operation Commands

Read Operation (READ, 03h)

After the falling edge of CS, the bus master can issue a READ opcode. Following the READ command is a three-byte address containing the 19-bit address (A18–A0) of the first byte of the read operation. The upper five bits of the address are ignored. After the opcode and address are issued, the device drives out the read data on the next eight clocks. The SI input is ignored during read data bytes. Subsequent bytes are data bytes, which are read out sequentially. Addresses are incremented internally as long as the bus master continues to issue clocks and CS is LOW. If the last address of 7FFFFh is reached, the internal address counter will roll over to 00000h. Data is read on MSb first. The rising edge of CS terminates a read operation and tristates the SO pin. The CY15X104QN read operation is shown in Figure 11.

Figure 11. Memory Read Operation

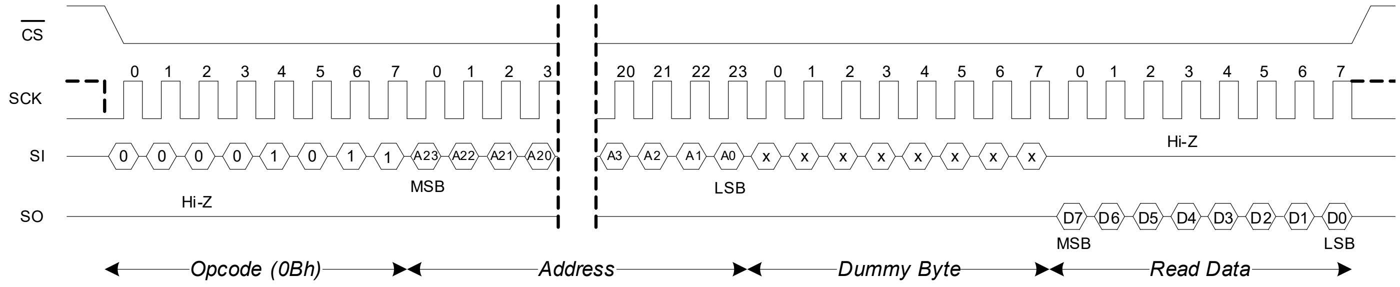


Fast Read Operation (FAST_READ, 0Bh)

The CY15X104QN supports a FAST READ opcode (0Bh) that is provided for opcode compatibility with serial flash devices. The FAST READ opcode is followed by a three-byte address containing the 19-bit address (A18–A0) of the first byte of the read operation and then a dummy byte. The dummy byte inserts a read latency of 8-clock cycle. The fast read operation is otherwise the same as an ordinary read operation except that it requires an additional dummy byte. After receiving the opcode, address, and a dummy byte, the CY15X104QN starts driving its SO line with data bytes, with MSB first, and continues transmitting as long as the device is selected and the clock is available. In case of bulk read, the internal address counter is incremented automatically, and after the last address 7FFFFh is reached, the counter rolls over to 00000h. When the device is driving data on its SO line, any transition on its SI line is ignored. The rising edge of CS terminates a fast read operation and tristates the SO pin. The CY15X104QN Fast Read operation is shown in Figure 12.

Note: The dummy byte can be any 8-bit value but Axh (8'b1010xxxx). The lower 4 bits of Axh are don't care bits. Hence, Axh essentially represents 16 different 8-bit values which shouldn't be transmitted as the dummy byte. 00h is typically used as the dummy byte in most use cases.

Figure 12. Fast Read Operation



Special Sector Memory Access Commands

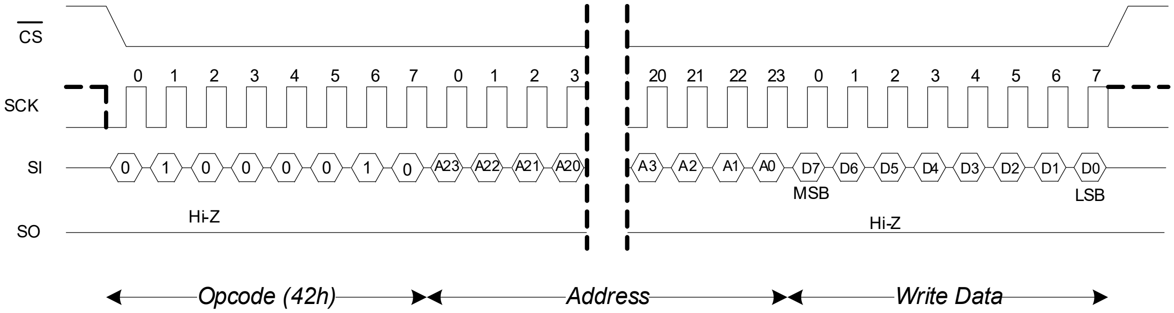
Special Sector Write (SSWR, 42h)

All writes to the 256-byte special begin with a WREN opcode with CS being asserted and deasserted. The next opcode is SSWR. The SSWR opcode is followed by a three-byte address containing the 8-bit sector address (A7–A0) of the first data byte to be written into the special sector memory. The upper 16 bits of the three-byte address are ignored. Subsequent bytes are data bytes, which are written sequentially. Addresses are incremented internally as long as the bus master continues to issue clocks and keeps CS LOW. Once the internal address counter auto increments to XXXFFh, CS should toggle HIGH to terminate the ongoing SSWR operation. Data is written on MSb first. The rising edge of CS terminates a write operation. The CY15X104QN special sector write operation is shown in Figure 13.

Notes

- If power is lost in the middle of the write operation, only the last completed byte will be written.
- The special sector F-RAM memory guarantees to retain data integrity up to three cycles of standard reflow soldering.

Figure 13. Special Sector Write (WREN not shown) Operation

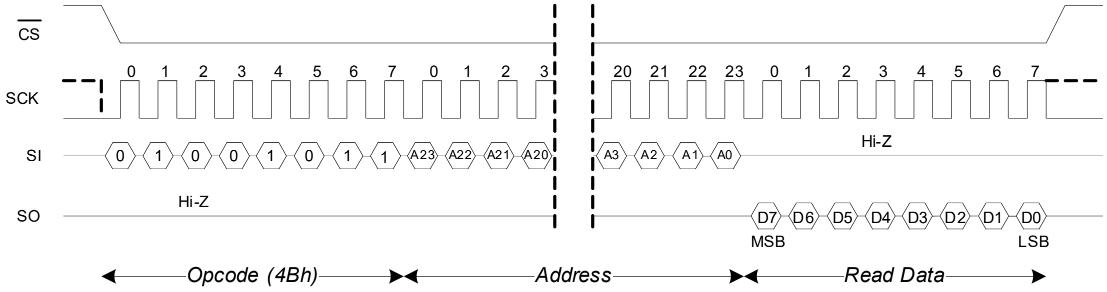


Special Sector Read (SSRD, 4Bh)

After the falling edge of CS, the bus master can issue an SSRD opcode. Following the SSRD command is a three-byte address containing the 8-bit address (A7–A0) of the first byte of the special sector read operation. The upper 16 bits of the address are ignored. After the opcode and address are issued, the device drives out the read data on the next eight clocks. The SI input is ignored during read data bytes. Subsequent bytes are data bytes, which are read out sequentially. Addresses are incremented internally as long as the bus master continues to issue clocks and CS is LOW. Address wrap is not supported in SSRD. Once the internal address counter auto increments to XXXFFh, CS should toggle HIGH to terminate the ongoing SSRD operation. Data is read on MSb first. The rising edge of CS terminates a special sector read operation and tristates the SO pin. The CY15X104QN special sector read operation is shown in Figure 14.

Note: The special sector F-RAM memory guarantees to retain data integrity up to three cycles of standard reflow soldering.

Figure 14. Special Sector Read Operation



Identification and Serial Number Commands

Read Device ID (RDID, 9Fh)

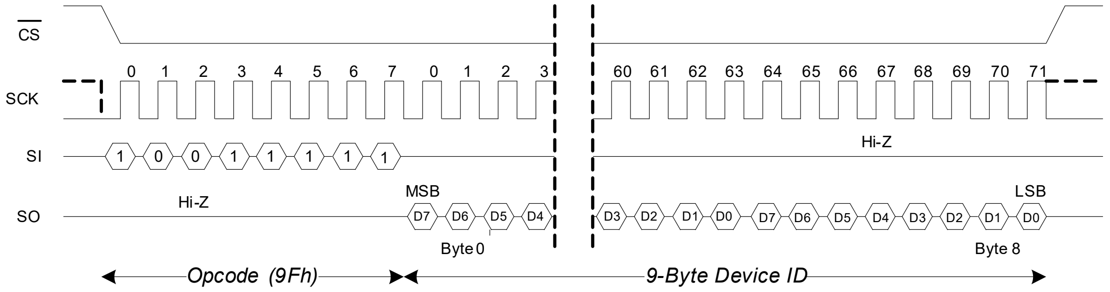
The CY15X104QN device can be interrogated for its manufacturer, product identification, and die revision. The RDID opcode 9Fh allows the user to read the 9-byte manufacturer ID and product ID, both of which are read-only bytes. The JEDEC-assigned manufacturer ID places the Cypress (Ramtron) identifier in bank 7; therefore, there are six bytes of the continuation code 7Fh followed by the single byte C2h. There are two bytes of product ID, which includes a family code, a density code, a sub code, and the product revision code. Table 6 shows 9-Byte Device ID field description. Refer to Ordering Information on page 24 for 9-Byte device ID of an individual part. The CY15X104QN read device ID operation is shown in Figure 15 on page 14.

Note: The least significant data byte (Byte 0) shifts out first and the most significant data byte (Byte 8) shifts out last.

Table 6. 9-Byte Device ID

Device ID Field Description							
Manufacturer ID [71:16]	**Family [15:13]**	**Density [12:9]**	**Inrush [8]**	**Sub Type [7:5]**	**Revision [4:3]**	**Voltage [2]**	**Frequency [1:0]**
56-bit	3-bit	4-bit	1-bit	3-bit	2-bit	1-bit	2-bit

Figure 15. Read Device ID



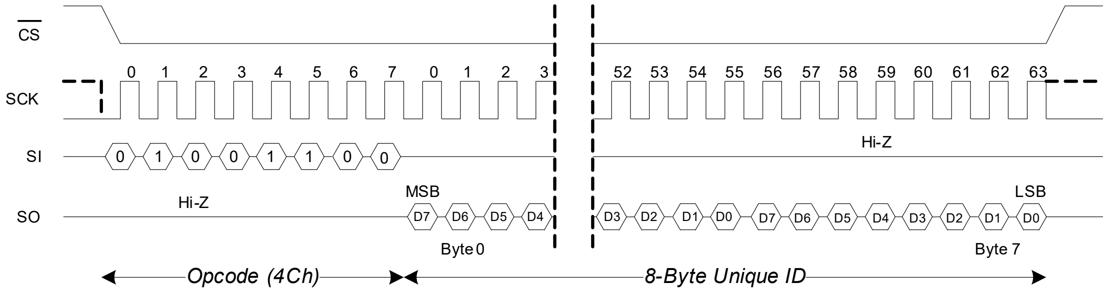
Read Unique ID (RUID, 4Ch)

The CY15X104QN device can be interrogated for unique ID which is a factory programmed, 64-bit number unique to each device. The RUID opcode, 4Ch allows to read the 8-byte, read only unique ID. The CY15X104QN read unique ID operation is shown in Figure 16.

Notes

- The least significant data byte (Byte 0) shifts out first and the most significant data byte (Byte 7) shifts out last.
- The unique ID registers are guaranteed to retain data integrity of up to three cycles of the standard reflow soldering.

Figure 16. Read Unique ID



Write Serial Number (WRSN, C2h)

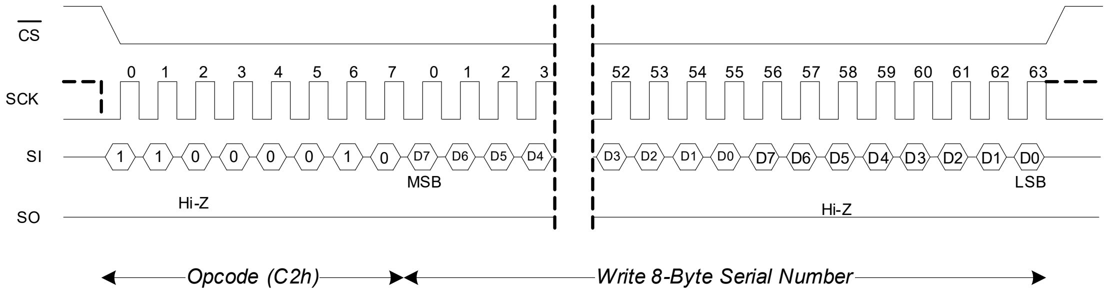
The serial number is an 8-byte one-time programmable memory space provided to the user to uniquely identify a PC board or a system. A serial number typically consists of a two-byte Customer ID, followed by five bytes of a unique serial number and one byte of CRC check. However, the end application can define its own format for the 8-byte serial number. All writes to the Serial Number Register begin with a WREN opcode with $\overline{CS}$ being asserted and deasserted. The next opcode is WRSN. The WRSN instruction can be used in burst mode to write all the 8 bytes of serial number. After the last byte of the serial number is shifted in, $\overline{CS}$ must be driven HIGH to complete the WRSN operation. The CY15X104QN write serial number operation is shown in Figure 17.

Note: The CRC checksum is not calculated by the device. The system firmware must calculate the CRC checksum on the 7-byte content and append the checksum to the 7-byte user-defined serial number before programming the 8-byte serial number into the serial number register. The factory default value for the 8-byte Serial Number is ‘0000000000000000h’.

Table 7. 8-Byte Serial Number

16-bit Customer Identifier		40-bit Unique Number					8-bit CRC
SN[63:56]	SN[55:48]	SN[47:40]	SN[39:32]	SN[31:24]	SN[23:16]	SN[15:8]	SN[7:0]

Figure 17. Write Serial Number (WREN not shown) Operation

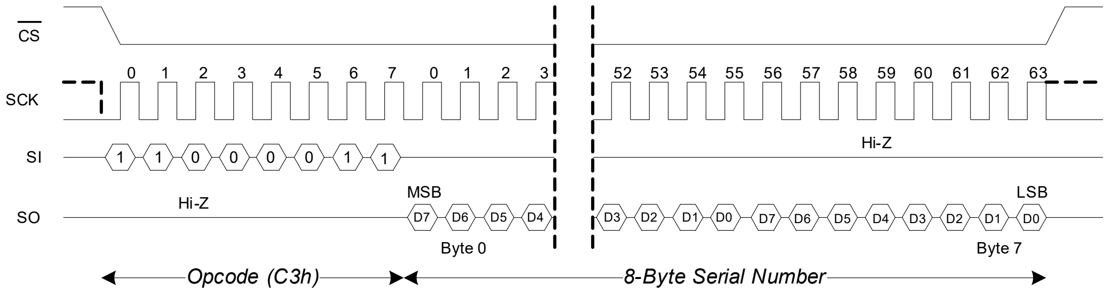


Read Serial Number (RDSN, C3h)

The CY15X104QN device incorporates an 8-byte serial space provided to the user to uniquely identify the device. The serial number is read using the RDSN instruction. A serial number read may be performed in burst mode to read all the eight bytes at once. After the last byte of the serial number is read, the device loops back to the first (MSB) byte of the serial number. An RDSN instruction can be issued by shifting the opcode for RDSN after $\overline{CS}$ goes LOW. The CY15X104QN read serial number operation is shown in Figure 18.

Note: The least significant data byte (Byte 0) shifts out first and the most significant data byte (Byte 7) shifts out last.

Figure 18. Read Serial Number Operation



Low Power Mode Commands

Deep Power-Down Mode (DPD, BAh)

A power-saving Deep Power-Down mode is implemented on the CY15X104QN device. The device enters the Deep Power-Down mode after t_{ENTDPD} time after the DPD opcode BAh is clocked in and a rising edge of $\overline{CS}$ is applied. When in Deep-Power-Down mode, the SCK and SI pins are ignored and SO will be Hi-Z, but the device continues to monitor the $\overline{CS}$ pin.

A $\overline{CS}$ pulse-width of t_{CSDPD} exits the DPD mode after t_{EXTDPD} time. The $\overline{CS}$ pulse-width can be generated either by sending a dummy command cycle or toggling $\overline{CS}$ alone while SCK and I/Os are don't care. The I/Os remain in hi-Z state during the wakeup from deep power-down. Refer to Figure 19 for DPD entry and Figure 20 for DPD exit timing.

Figure 19. DPD Entry Timing

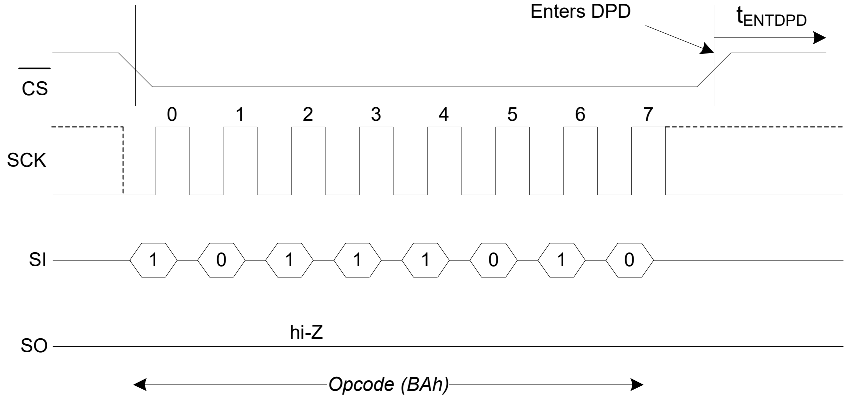
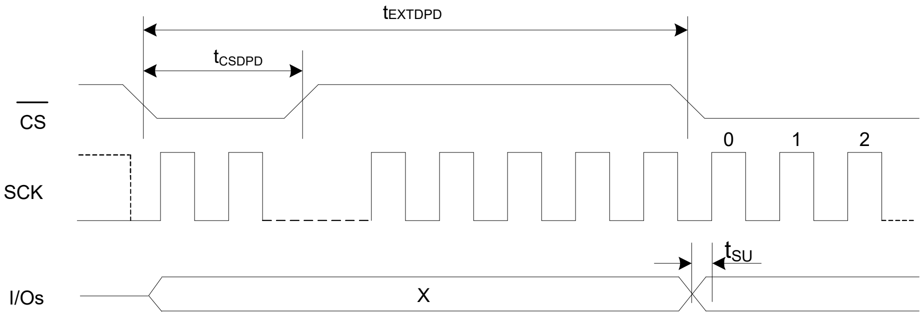


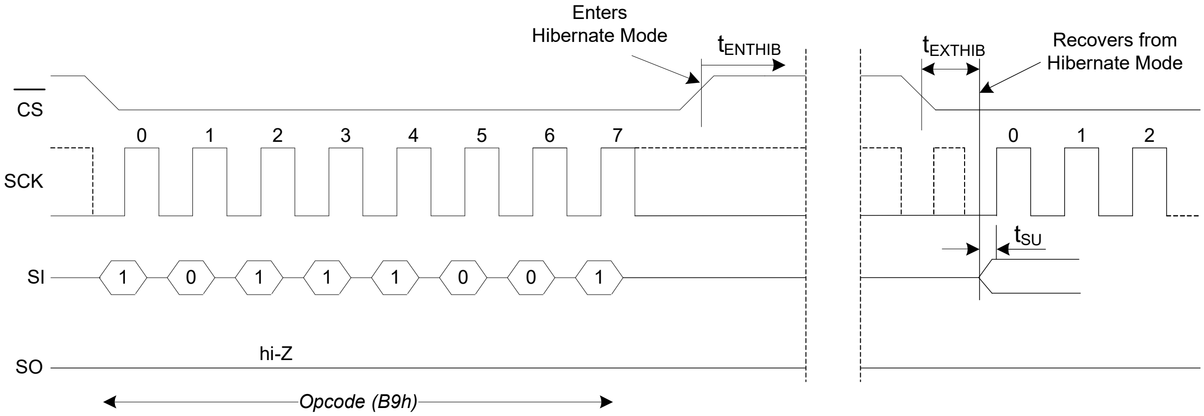
Figure 20. DPD Exit Timing



Hibernate Mode (HBN, B9h)

A lowest power Hibernate mode is implemented on the CY15X104QN device. The device enters Hibernate mode after t_{ENTHIB} time after the HBN opcode B9h is clocked in and a rising edge of $\overline{CS}$ is applied. When in Hibernate mode, the SCK and SI pins are ignored and SO will be Hi-Z, but the device continues to monitor the $\overline{CS}$ pin. On the next falling edge of $\overline{CS}$, the device will return to normal operation within t_{EXTHIB} time. The SO pin remains in a Hi-Z state during the wakeup from hibernate period. The device does not necessarily respond to an opcode within the wakeup period. To exit the Hibernate mode, the controller may send a “dummy” read, for example, and wait for the remaining t_{EXTHIB} time.

Figure 21. Hibernate Mode Operation



Endurance

The CY15X104QN devices are capable of being accessed at least 10^{14} times, reads or writes.

An F-RAM memory operates with a read and restore mechanism. Therefore, an endurance cycle is applied on a row basis for each access (read or write) to the memory array. The F-RAM architecture is based on an array of rows and columns of 64K rows of 64-bit each. The entire row is internally accessed once, whether a single byte or all eight bytes are read or written. Each byte in the row is counted only once in an endurance calculation. Table 8 shows endurance calculations for a 64-byte repeating loop, which includes an opcode, a starting address, and a sequential 64-byte data stream. This causes each byte to experience one endurance cycle through the loop.

Table 8. Time to Reach Endurance Limit for Repeating 64-byte Loop

SCK Freq (MHz)	Endurance Cycles/sec	Endurance Cycles/year	Years to Reach 10^{14} Limit
50	91,900	2.9×10^{12}	34.5
40	73,520	2.32×10^{12}	43.1
10	18,380	5.79×10^{11}	172.7
5	9,190	2.90×10^{11}	345.4

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage temperature	–65 °C to + 125 °C
Maximum accumulated storage time	
At 125 °C ambient temperature	1000 h
At 85 °C ambient temperature	10 Years
Maximum junction temperature	125 °C
Supply voltage on V_{DD} relative to V_{SS}:	
CY15V104QN:	–0.5 V to +2.4 V
CY15B104QN:	–0.5 V to +4.1 V
Input voltage	$V_{IN} \leq V_{DD}$ + 0.5 V
DC voltage applied to outputs in High-Z state	–0.5 V to V_{DD} + 0.5 V
Transient voltage (< 20 ns) on any pin to ground potential	–2.0 V to V_{DD} + 2.0 V
Package power dissipation capability (T_A = 25 °C)	1.0 W
Surface mount lead soldering temperature (3 seconds)	+260 °C
DC output current (1 output at a time, 1s duration)	15 mA
Electrostatic discharge voltage	
Human Body Model (JEDEC Std JESD22-A114-B)	2 kV
Charged Device Model (JEDEC Std JESD22-C101-A)	500 V
Latch-up current	>140 mA

Operating Range

Device	Range	Ambient Temperature	V_{DD}
CY15V104QN	Automotive-A	–40 °C to +85 °C	1.71 V to 1.89 V
CY15B104QN			1.8 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ [2, 3]	Max	Unit
V_{DD}	Power supply	CY15V104QN		1.71	1.8	1.89	V
		CY15B104QN		1.8	3.3	3.6	
I_{DD}	V_{DD} supply current	V_{DD} = 1.71 V to 1.89 V; SCK toggling between V_{DD} – 0.2 V and V_{SS}, other inputs V_{SS} or V_{DD} – 0.2 V. SO = Open	f_{SCK} = 1 MHz	–	0.4	0.6	mA
			f_{SCK} = 40 MHz	–	3.7	4.8	
			f_{SCK} = 50 MHz	–	5.0	5.2	
		V_{DD} = 1.8 V to 3.6 V; SCK toggling between V_{DD} – 0.2 V and V_{SS}, other inputs V_{SS} or V_{DD} – 0.2 V. SO = Open	f_{SCK} = 1 MHz	–	0.5	0.8	
			f_{SCK} = 40 MHz	–	4.3	5.5	
			f_{SCK} = 50 MHz	–	6.0	6.6	
I_{SB}	V_{DD} standby current	V_{DD} = 1.71 V to 1.89 V; $\overline{CS}$ = V_{DD}. All other inputs V_{SS} or V_{DD}.	T_A = 25 °C	–	2.7	–	µA
			T_A = 85 °C	–	–	75	
		V_{DD} = 1.8 V to 3.6 V; $\overline{CS}$ = V_{DD}. All other inputs V_{SS} or V_{DD}.	T_A = 25 °C	–	3.2	–	
			T_A = 85 °C	–	–	75	
I_{DPD}	Deep power-down current	V_{DD} = 1.71 V to 1.89 V; $\overline{CS}$ = V_{DD}. All other inputs V_{SS} or V_{DD}.	T_A = 25 °C	–	1.1	–	
			T_A = 85 °C	–	–	15	
		V_{DD} = 1.8 V to 3.6 V; $\overline{CS}$ = V_{DD}. All other inputs V_{SS} or V_{DD}.	T_A = 25 °C	–	1.3	–	
			T_A = 85 °C	–	–	17	

Notes

[2] Typical values are at 25 °C, V_{DD} = V_{DD} (Typ).

[3] This parameter is guaranteed by characterization; not tested in production.

DC Electrical Characteristics (continued)

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ [2, 3]	Max	Unit
I_{HBN}	Hibernate mode current	V_{DD} = 1.71 V to 1.89 V; $\overline{CS}$ = V_{DD}. All other inputs V_{SS} or V_{DD}.	T_A = 25 °C	–	0.1	–	µA
			T_A = 85 °C	–	–	0.9	
		V_{DD} = 1.8 V to 3.6 V; $\overline{CS}$ = V_{DD}. All other inputs V_{SS} or V_{DD}.	T_A = 25 °C	–	0.1	–	
			T_A = 85 °C	–	–	1.6	
I_{LI}	Input leakage current on I/O pins except $\overline{WP}$ pin	$V_{SS} < V_{IN} < V_{DD}$		–1	–	1	
	Input leakage current on $\overline{WP}$ pin			–100	–	1	
I_{LO}	Output leakage current	$V_{SS} < V_{OUT} < V_{DD}$		–1	–	1	
V_{IH}	Input HIGH voltage			0.7 × V_{DD}	–	V_{DD} + 0.3	V
V_{IL}	Input LOW voltage			–0.3	–	0.3 × V_{DD}	
V_{OH1}	Output HIGH voltage	I_{OH} = –1 mA, V_{DD} = 2.7 V		2.4	–	–	
V_{OH2}		I_{OH} = –100 µA		V_{DD} – 0.2	–	–	
V_{OL1}	Output LOW voltage	I_{OL} = 2 mA, V_{DD} = 2.7 V		–	–	0.4	
V_{OL2}		I_{OL} = 150 µA		–	–	0.2	

Data Retention and Endurance

Parameter	Description	Test condition	Min	Max	Unit
T_{DR}	Data retention	T_A = 85 °C	10	–	Years
		T_A = 70 °C	141	–	
		T_A = 60 °C	151	–	
		T_A = 50 °C	160	–	
NV_C	Endurance	Over operating temperature	10^{14}	–	Cycles

Capacitance

For all packages.

Parameter[4]	Description	Test Conditions	Max	Unit
C_O	Output pin capacitance (SO)	T_A = 25 °C, f = 1 MHz, V_{DD} = V_{DD} (Typ)	8	pF
C_I	Input pin capacitance		6	

Thermal Resistance

Parameter[4]	Description	Test Conditions	8-pin SOIC Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	88.6	°C/W
Θ_{JC}	Thermal resistance (junction to case)		56	

AC Test Conditions

Input pulse levels .... 10% and 90% of V_{DD}
Input rise and fall times .... 3 ns
Input and output timing reference levels .... 0.5 × V_{DD}
Output load capacitance .... 30 pF

Note

[4] This parameter is guaranteed by characterization; not tested in production.

AC Switching Characteristics

Over the Operating Range

Parameters[5]		Description	40 MHz		50 MHz		Unit
Cypress Parameter	Alt. Parameter		Min	Max	Min	Max	
f_{SCK}	–	SCK clock frequency	0	40	0	50	MHz
t_{CH}	–	Clock HIGH time	11	–	9	–	ns
t_{CL}	–	Clock LOW time	11	–	9	–	
t_{CLZ}[6]	–	Clock LOW to Output low-Z	0	–	0	–	
t_{CSS}	t_{CSU}	Chip select setup	5	–	5	–	
t_{CSH}	t_{CSH}	Chip select hold - SPI mode 0	5	–	5	–	
t_{CSH1}	–	Chip select hold - SPI mode 3	10	–	10	–	
t_{HZCS}[7, 8]	t_{OD}	Output disable time	–	12	–	10	
t_{CO}	t_{ODV}	Output data valid time	–	9	–	8	
t_{OH}	–	Output hold time	1	–	1	–	
t_{CS}	t_{D}	Deselect time	40	–	40	–	
t_{SD}	t_{SU}	Data setup time	5	–	5	–	
t_{HD}	t_{H}	Data hold time	5	–	5	–	
t_{WPS}	t_{WHSL}	$\overline{WP}$ setup time (w.r.t $\overline{CS}$)	20	–	20	–	
t_{WPH}	t_{SHWL}	$\overline{WP}$ hold time (w.r.t $\overline{CS}$)	20	–	20	–	

Notes

5. Test conditions assume a signal transition time of 3 ns or less, timing reference levels of 0.5 × V_{DD}, input pulse levels of 10% to 90% of V_{DD}, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance shown in AC Test Conditions on page 20.
6. Guaranteed by design.
7. t_{HZCS} is specified with a load capacitance of 5 pF. Transition is measured when the output enters a high-impedance state.
8. This parameter is guaranteed by characterization; not tested in production.

Figure 22. Synchronous Data Timing (Mode 0 and Mode 3)

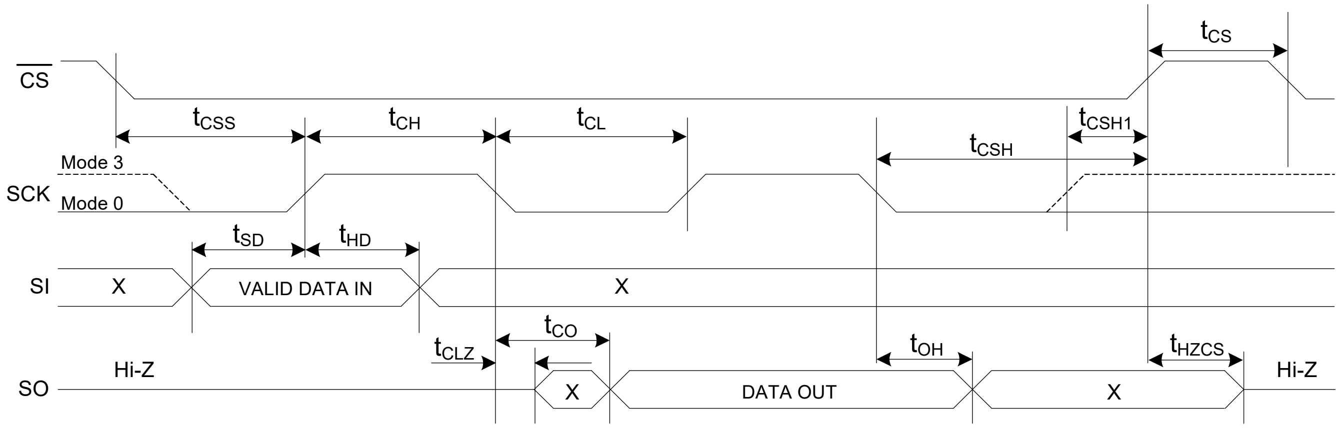
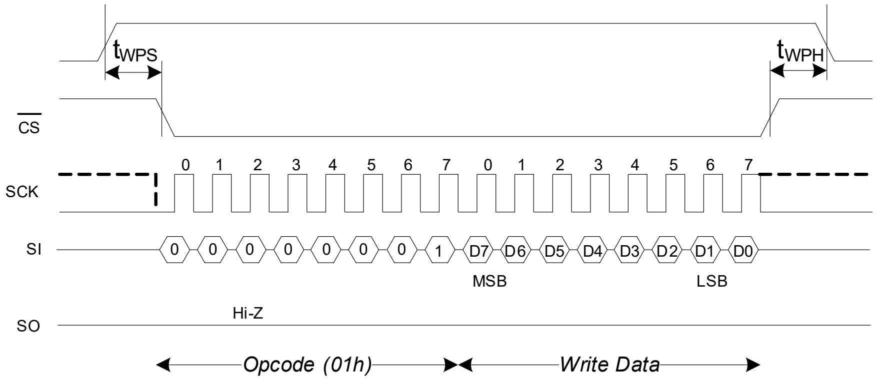


Figure 23. Write Protect Timing During Write Status Register (WRSR) Operation

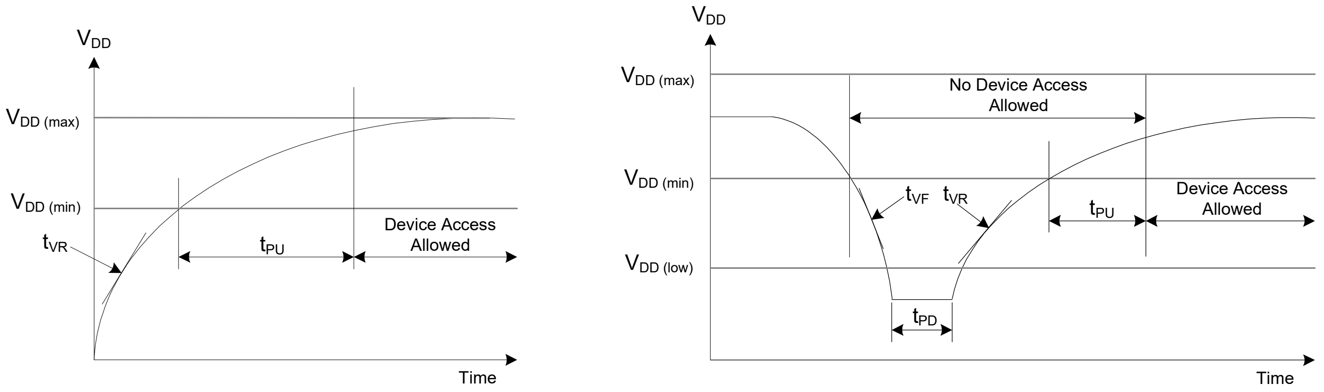


Power Cycle Timing

Over the Operating Range

Parameter[9]		Description	Min	Max	Unit
Cypress Parameter	Alt. Parameter				
t_{PU}		Power-up $V_{DD(min)}$ to first access ($\overline{CS}$ LOW)	450	–	μs
t_{VR}[10]		V_{DD} power-up ramp rate	30	–	μs/V
t_{VF}[10, 11]		V_{DD} power-down ramp rate	20	–	
t_{ENTDPD}[12]	t_{DP}	$\overline{CS}$ HIGH to enter deep power-down ($\overline{CS}$ HIGH to hibernate mode current)	–	3	μs
t_{CSDPD}		$\overline{CS}$ pulse width to wake up from deep power-down mode	0.015	4 × $1/f_{SCK}$	
t_{EXTDPD}	t_{RDP}	Recovery time from deep power-down mode ($\overline{CS}$ LOW to ready for access)	–	10	
t_{ENTHIB}[13]		Time to enter hibernate ($\overline{CS}$ HIGH to enter hibernate)	–	3	
t_{EXTHIB}	t_{REC}	Recovery time from hibernate mode ($\overline{CS}$ LOW to ready for access)	–	450	
$V_{DD}(low)$[11]		Low V_{DD} where initialization must occur	0.6	–	V
t_{PD}[11]		$V_{DD}(low)$ time when $V_{DD}(low)$ at 0.6 V	130	–	μs
		$V_{DD}(low)$ time when $V_{DD}(low)$ at V_{SS}	70	–	

Figure 24. Power Cycle Timing



Notes

9. Test conditions assume a signal transition time of 3 ns or less, timing reference levels of 0.5 × V_{DD}, input pulse levels of 10% to 90% of V_{DD}, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance shown in AC Test Conditions on page 20.
10. Slope measured at any point on the V_{DD} waveform.
11. This parameter is guaranteed by characterization; not tested in production.
12. Guaranteed by design. Refer to Figure 19 on page 16 for Deep Sleep mode timing.
13. Guaranteed by design. Refer to Figure 21 on page 17 for Hibernate mode timing.

Ordering Information

Ordering Code	Device ID	Package Diagram	Package Type	Operating Range
CY15B104QN-50SXA	7F7F7F7F7F7F7FC22C40	001-85261	8-pin SOIC (EIAJ)	Automotive-A
CY15B104QN-50SXAT				

All these parts are Pb-free. Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions

CY 15 B 104 Q N - 50 S X A T

Options:
Blank = Standard; T = Tape and Reel

Temperature Range:
A = Automotive-A (-40 °C to +85 °C)

X = Pb-free

Package Type:
S = 8-pin SOIC (EIAJ)

Frequency:
50 = 50 MHz

N = No Inrush Current Control

Interface:
Q = SPI F-RAM

Density:
104 = 4-Mbit

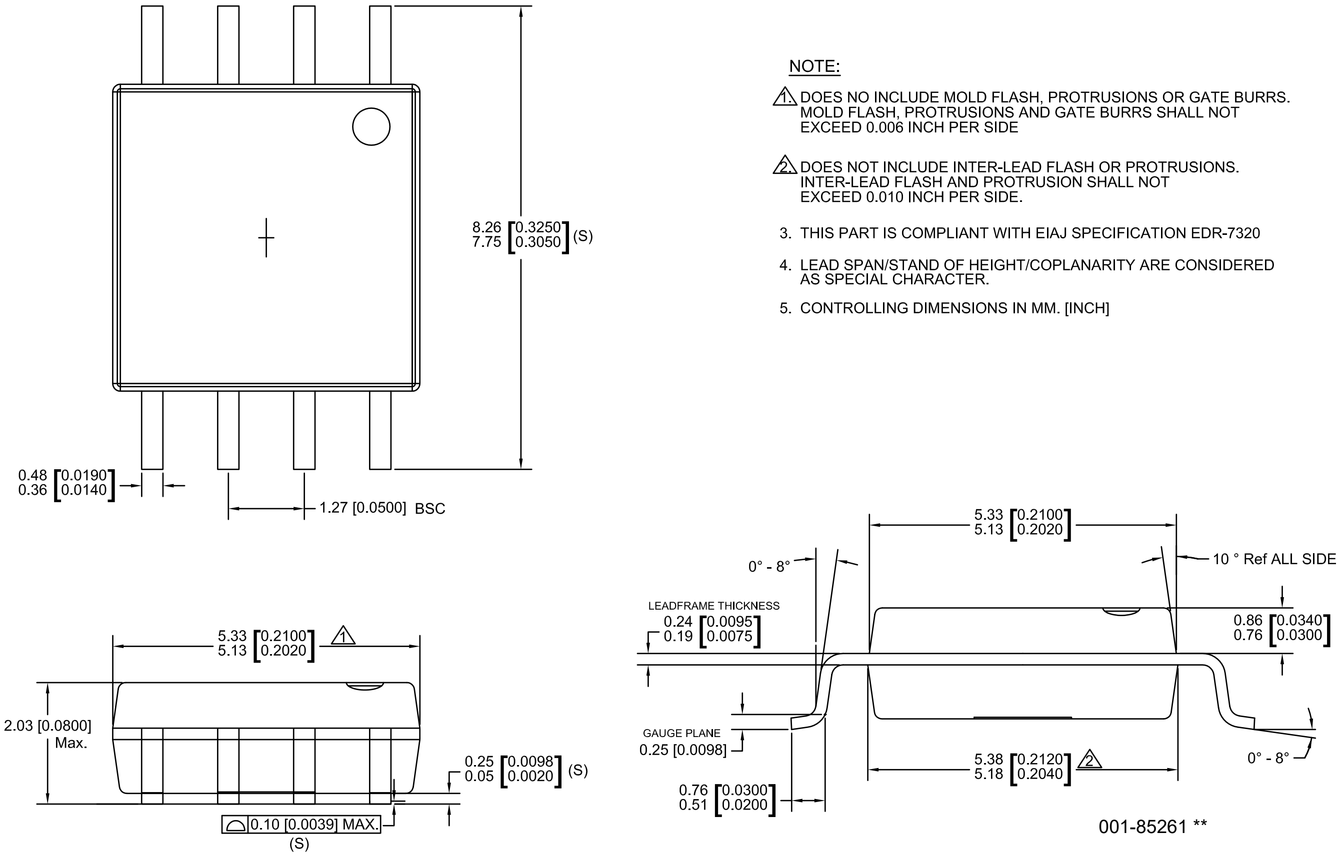
Voltage:
V = 1.71 V to 1.89 V (1.8 V typical)
B = 1.8 V to 3.6 V (3.3 V typical)

15 = F-RAM

CY = Cypress

Package Diagram

Figure 25. 8-pin SOIC (208 Mils) Package Outline, 001-85261



NOTE:

⚠1 DOES NO INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 INCH PER SIDE

⚠2 DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.010 INCH PER SIDE.

3. THIS PART IS COMPLIANT WITH EIAJ SPECIFICATION EDR-7320
4. LEAD SPAN/STAND OF HEIGHT/COPLANARITY ARE CONSIDERED AS SPECIAL CHARACTER.
5. CONTROLLING DIMENSIONS IN MM. [INCH]

Acronyms

Table 9. Acronyms used in this Document

Acronym	Description
CPHA	Clock Phase
CPOL	Clock Polarity
EEPROM	Electrically Erasable Programmable Read-Only Memory
EIA	Electronic Industries Alliance
F-RAM	Ferroelectric Random Access Memory
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
JESD	JEDEC standards
LSB	Least Significant Bit
MSB	Most Significant Bit
RoHS	Restriction of Hazardous Substances
SPI	Serial Peripheral Interface
SOIC	Small Outline Integrated Circuit
GQFN	Grid Array Flat No-lead

Document Conventions

Units of Measure

Table 10. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Hz	hertz
kHz	kilohertz
kΩ	kilohm
Mbit	megabit
MHz	megahertz
µA	microampere
µF	microfarad
µs	microsecond
mA	milliampere
ms	millisecond
ns	nanosecond
W	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY15B104QN/CY15V104QN, Excelon™ Auto 4-Mbit (512K × 8) Automotive-A Serial (SPI) F-RAM Document Number: 002-24681			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
**	6287260	08/22/2018	New data sheet.
*A	6393450	11/26/2018	Updated Maximum Ratings: Replaced "–55 °C to +125 °C" with "–65 °C to +125 °C" in ratings corresponding to "Storage temperature".
*B	6541959	04/17/2019	Updated Functional Description: Updated Command Structure: Updated Special Sector Memory Access Commands (Updated description). Updated Maximum Ratings: Updated details corresponding to "Supply voltage on V_{DD} relative to V_{SS}", "Input voltage", and "DC voltage applied to outputs in High-Z state". Updated AC Switching Characteristics: Added t_{CLZ}, t_{CSH1} parameters and their corresponding details. Added Note 6 and referred the same note in t_{CLZ} parameter. Updated details in "Description" column corresponding to t_{CSH} parameter. Updated Figure 22. Updated Power Cycle Timing: Added Note 11 and referred the same note in t_{VF} parameter. Removed Note 12 reference in t_{EXTDPD} parameter. Removed Note 13 reference in t_{EXTHIB} parameter. Updated Note 12. Updated Note 13. Updated Ordering Information: Updated part numbers.
*C	6664249	08/30/2019	Changed status from Preliminary to Final. Updated Maximum Ratings: Replaced "150 °C" with "125 °C" under "Maximum accumulated storage time". Updated to new template. Completing Sunset Review.

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