AN87352

F-RAM™ for Smart E-Meters

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Software Version: None
Related Application Notes: None

AN87352 discusses the advantages of F-RAM™ over EEPROM and describes how to leverage F-RAM in smart e-meter applications.

Contents

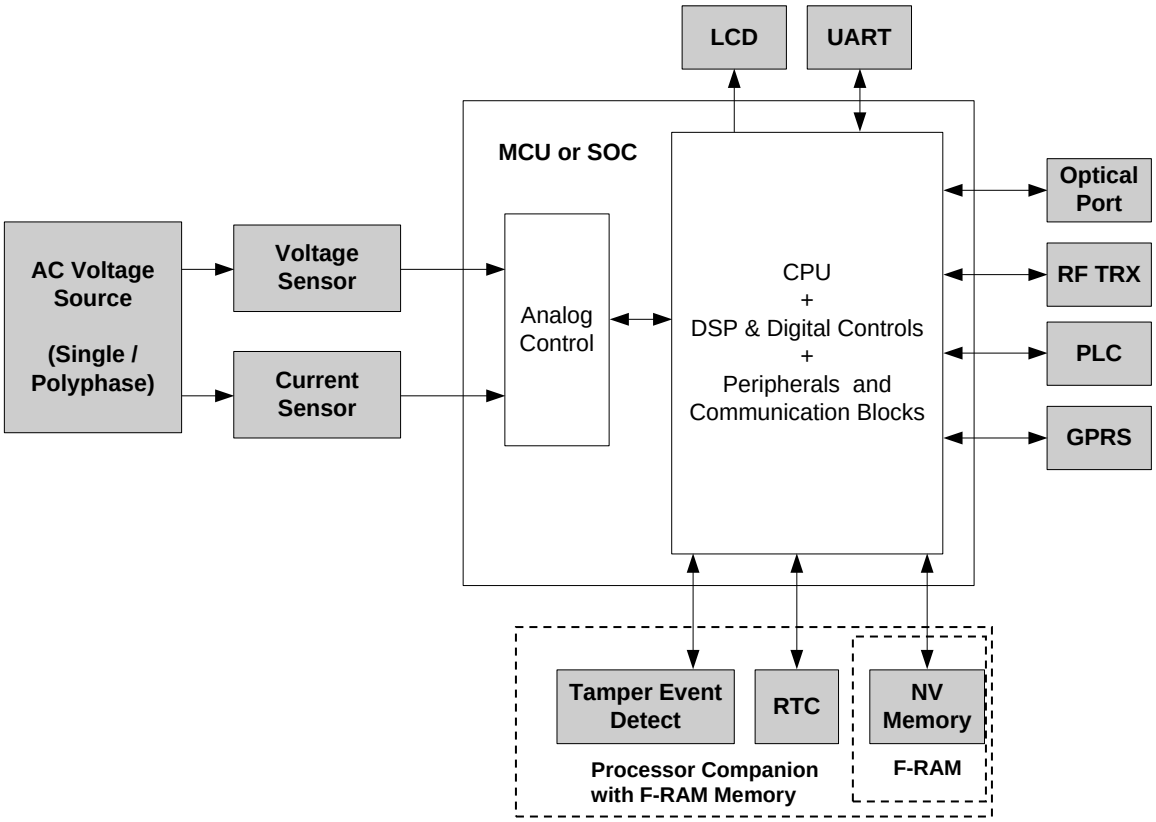
1 Introduction

This application note provides an overview of a smart electricity meter, or smart e-meter, and explains the benefits of using nonvolatile serial F-RAM over EEPROM in smart e-meter design. Figure 1 shows a simplified block diagram of a smart e-meter.

Nonvolatile memory is a critical component of a smart e-meter. The meter periodically captures electric power consumption and environmental data and stores it in nonvolatile memory in an allocated time slot for computation and data logging. At the end of a time slot in every data capture period, it uploads information over a network that is linked to the supply infrastructure. The data capture period can vary from once every few milliseconds to once every few seconds.

Included in this uploaded information are periodic electric power readings and suspicious physical changes, which might indicate an attempt to tamper with the meter. Smart e-meters help to control electrical leakage and to improve the distribution of electric power by managing with fine granularity power consumption metrics (active power, reactive power, apparent power–sometimes both imported and exported) that are recorded in a nonvolatile memory. Ensuring the reliability and integrity of electric power consumption data is critical. As a result, the density requirements for the nonvolatile memory have grown rapidly.

Figure 1. Smart E-Meter Block Diagram



2 Electricity Meters

Electricity meters measure and convey the amount of electric power consumed by a business, residence, or electrically powered equipment. These meters show the electric power consumption in units of energy used (kWh). The electric power consumption data is recorded periodically, and electricity bills are generated accordingly.

In addition, electricity meters provide configuration settings to measure the demand for electricity. Data is used to determine electricity usage patterns and time-of-day billing. This can lead to an intentional reduction in power consumption during certain periods. Also, in some areas, meters have relays for demand/response shedding to manage electricity loads during periods of peak electric power consumption.

Traditional electricity meters are not designed for two-way communication between a meter and either the power grid or a central processing system. In comparison, smart e-meters are capable of such communication.

3 Smart E-Meters

Smart e-meters record the consumption of electricity in intervals of every hour, minute, second, or millisecond. They communicate that information to the grid for monitoring and billing purposes. Although traditional electricity meters also measure total electric power consumption, they do not provide detailed information on when the electric power was consumed.

Smart e-meters provide a way to measure site-specific information, allowing price-setting regulatory agencies to introduce different prices for consumption based on time of day and season. Smart e-meters also measure and record surge voltages and harmonic distortion, allowing the diagnosis of power quality problems. Since the inception of electricity deregulation and market-driven pricing, utilities have been seeking ways to match consumption with generation.

Smart e-meters usually include real-time or near-real-time sensors, power outage notification, and power quality monitoring. These features represent more than simple automatic meter reading (AMR). Smart e-meters are similar in many respects to advanced metering infrastructure (AMI) meters. In addition, they make it easier to sell micro-generated electricity (such as from a solar panel or home wind turbine) to the national grid. Eventually, smart e-meters will entirely replace electricity meters.

4 Benefits of F-RAM

Almost all conventional e-meters have used serial EEPROM as the preferred nonvolatile memory because of its low cost, low power, and standard package options. These advantages have allowed EEPROM to dominate until recently, when metering supply companies started to develop and promote AMI for efficient electrical power generation, transmission, and distribution. AMI has been a key driver in the development of sophisticated smart e-meters.

Smart e-meters log electric power parameters, such as power consumption, active power, reactive power, load conditions, voltage, and frequency distortion, at regular intervals, varying from once every few seconds to once every few milliseconds. Recorded data is stored locally in the meter's nonvolatile memory and is periodically transmitted to the central processing system or the power grid.

The use of EEPROM in an AMI architecture limits the performance of the meter because of its slow nonvolatile write speed and limited endurance cycles. As a result, alternative nonvolatile memory solutions, such as F-RAM, nvSRAM, and battery-backed SRAM, are gaining favor over EEPROM.

The following sections discuss the benefits of using F-RAM for smart e-meters.

4.1 Zero Clock Cycle Write Latency

A typical EEPROM requires a 5-ms write cycle to transfer its page data to nonvolatile EEPROM. This results in a very long write time when several kilobytes of data need to be written. In contrast, with F-RAM, all writes occur at the bus speed, with no memory-based latency. Example 1 and Example 2 demonstrate that the zero clock cycle write latency in F-RAM improves nonvolatile write performance over the EEPROM. Figure 2 illustrates the impact of write latency.

4.1.1 Example 1

It takes 2 ms to transfer 256 bytes of page data from the controller to an EEPROM page over a 1-MHz I^2C bus, followed by 5 ms to write the data to EEPROM (see Table 1). A 1-MHz I^2C EEPROM with a 1-Mb density and a 256-byte page size takes 28 ms to back up 1 KB of data (4 x 2 ms + 4 x 5 ms).

Table 1. Typical 1-Mb EEPROM Configuration

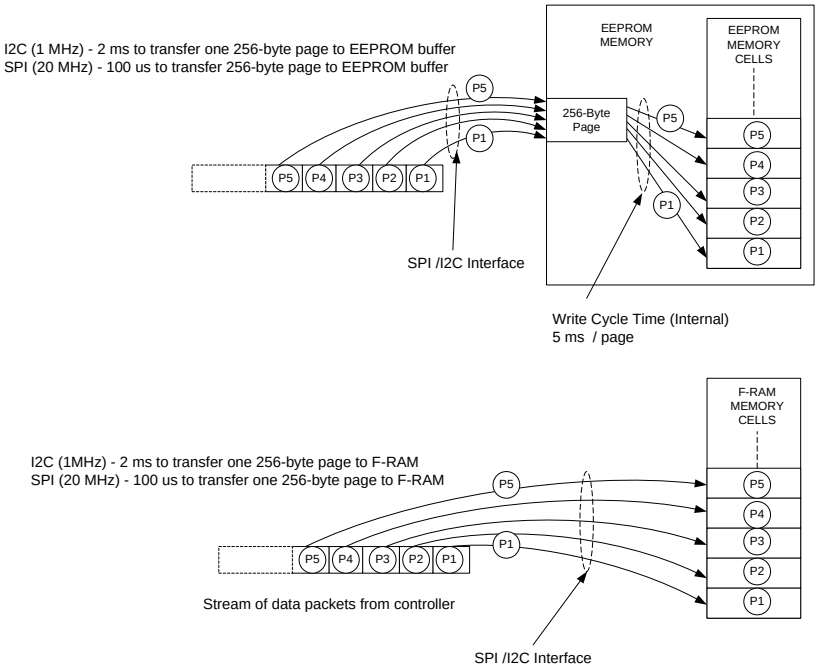
Features	Value	Unit
Page size	256	bytes
Write cycle time	5	ms
Speed (SPI)	20	MHz

However, it takes only 8 ms (4 x 2 ms) to 1 KB of data to F-RAM. (This time represents the total data transfer time from the controller to the EEPROM buffer.) To transfer the entire 1 Mb of data takes 3.584 seconds (512 x 2 ms + 512 x 5 ms) with EEPROM, compared with about 1.024 seconds (512 x 2 ms) with F-RAM.

4.1.2 Example 2

It takes 100 µs to transfer 256 bytes of page data from the controller to an EEPROM page over a 20-MHz SPI bus, followed by 5 ms to transfer one page of data to the EEPROM. A 20-MHz SPI EEPROM with a 1-Mb density and a 256-byte page size takes 20.4 ms to back up 1 KB of data (4 x 100 µs + 4 x 5 ms). In contrast, it takes only 400 µs (4 x 100 µs) to write 1 KB of data to F-RAM. (This time is equal to the total data transfer time from the SPI controller to the EEPROM buffer.) To transfer the entire 1 Mb of data takes 2.611 seconds (512 x 100 µs + 512 x 5 ms) with EEPROM, compared with about 51.1 ms (512 x 100 µs) with F-RAM.

Figure 2. Process to Write to EEPROM and F-RAM



In addition, EEPROM supports varying page sizes; in this example, the lower page size in EEPROM requires more page write operations and more write cycle time. The result is additional write delays. Because F-RAM is not paged memory, the time to write a given set of data to it remains the same across all memory density options.

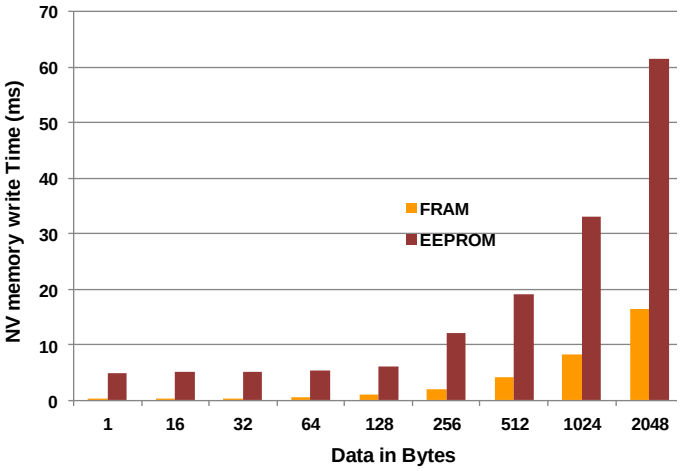
Table 2 and Figure 3 illustrate the time to write to nonvolatile memory in F-RAM and EEPROM.

Table 2. Time to Write to EEPROM and F-RAM Using 1-MHz SPI Interface

Data Bytes	Time to Write (ms) to Nonvolatile Memory	
	F-RAM	EEPROM
1	0.008	5.008
16	0.128	5.128
32	0.256	5.256
64	0.512	5.512
128	1.024	6.024
256	2.048	12.048
512	4.096	19.096
1024	8.192	33.192
2048	16.384	61.384

Note: The calculation in Table 2 does not include the SPI command overhead for sending the WRITE opcode and address bytes before sending the data bytes to be written. A multipage write operation in the SPI EEPROM requires the SPI command to be sent for every page write.

Figure 3. Write Performance in EEPROM versus F-RAM



4.2 Low-Power Design

F-RAM devices consume about one-third of the active current of EEPROM, while the standby/sleep current specifications of F-RAM are almost equal to the standby/sleep current specifications of EEPROM. This difference in active current has a huge impact on power consumption, especially when applications such as smart e-meters are write intensive due to frequent data logging. In addition to active current deficiency, EEPROM incurs an additional page write delay that causes the device to remain in active mode for an extended period, increasing power consumption.

The amount of energy required to write to F-RAM and EEPROM is calculated using the Energy Calculation Example. Table 3 compares the energy consumption of F-RAM and EEPROM, as shown in Figure 4. This comparison demonstrates relative energy consumption. The energy consumption in EEPROM is significantly higher than F-RAM mainly because the EEPROM device needs to be active for an extended duration to complete its nonvolatile write to EEPROM cells. Plus, it consumes at least three times more active current than F-RAM.

4.2.1 Energy Calculation Example

Equation 1 determines the energy consumed by F-RAM during a write cycle:

Equation 1 $E1 = V \; x \; I \; x \; t1$

Where:

V – Operating voltage

I – Active current

t1 – Total time to write data to F-RAM

Equation 2 determines the energy consumed by EEPROM during a write cycle:

Equation 2 $E2 = V \; x \; 3I \; x \; t2$

Where:

V – Operating voltage

I – Active current (three times that of F-RAM)

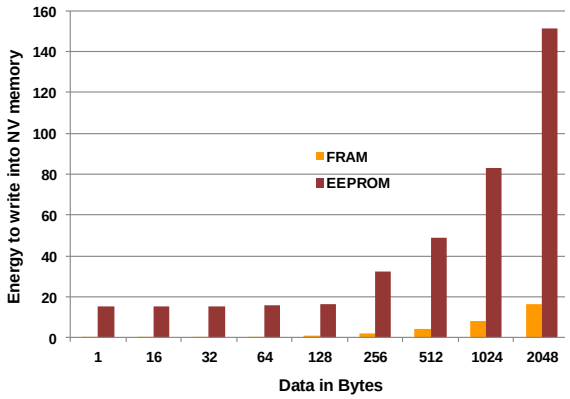
t2 – Total time to write data to EEPROM

Table 3. Energy to Write to EEPROM and F-RAM

Data in Bytes	Energy to Write to Nonvolatile Memory (relative unit)	
	F-RAM	EEPROM
1	0.008	15.008
16	0.128	15.128
32	0.256	15.256
64	0.512	15.512
128	1.024	16.024
256	2.048	32.048
512	4.096	49.096
1024	8.192	83.192
2048	16.384	151.384

Note: A typical 3-V, 256-Kb SPI EEPROM consumes 3 mA of active current during the write and read operations. Therefore, the amount of energy an SPI EEPROM will require to write 128 bytes of data is 144 µJ (3 V x 3 mA x 16.024 ms).

Figure 4. Energy Consumption During Data Write to EEPROM Versus F-RAM



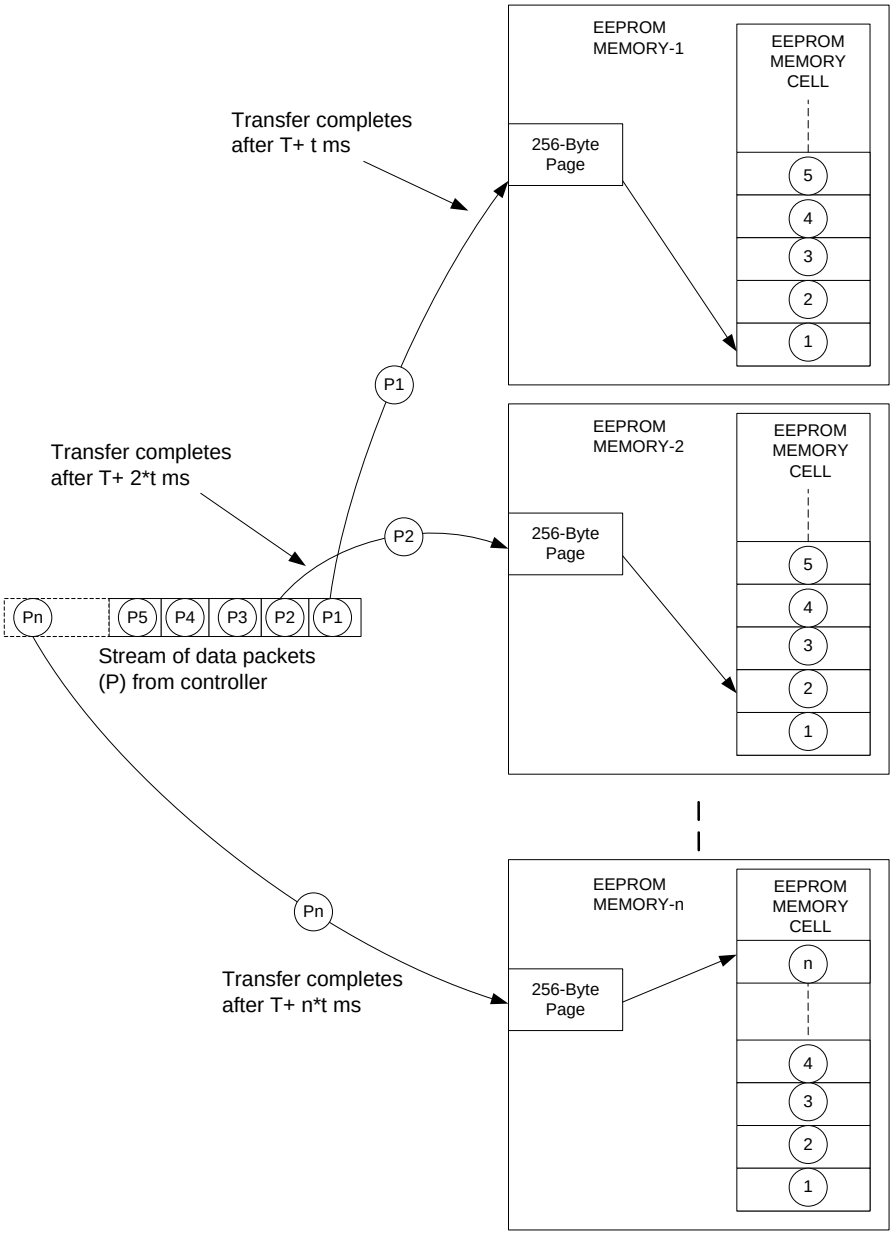
4.3 No Multi-Device Design Required

EEPROM writes incorporate two stages of data transfer. Data is written to the page buffer, and then a nonvolatile memory write cycle occurs. During the write cycle, EEPROM access is disabled; therefore, the next access cannot start until the ongoing write cycle is complete.

A few application examples have used two or more EEPROM devices in parallel to improve the data write throughput in EEPROMs, as illustrated in Figure 5. In this case, when one EEPROM device is busy executing the nonvolatile write cycle, the controller can initiate a write operation in the other EEPROM device and can follow this sequence for the remaining EEPROMs connected on the same bus in parallel. By the time the controller completes the data transfer in the page buffer of the last EEPROM device, the first EEPROM device gets ready for the access. The I^2C/SPI bus speed determines the number of pipeline stages (that is, the number of EEPROM devices sharing a system bus in parallel).

An I^2C interface EEPROM with a 400-kHz access speed takes 5 ms to transfer 256 bytes, or 1 page of data. It takes another 5 ms to complete a nonvolatile write cycle for the page. Therefore, a two-stage pipeline implementation is sufficient to achieve the write to EEPROM at the bus speed.

Figure 5. Write at Bus Speed to EEPROM Using a Pipelined Architecture



An I^2C EEPROM interface with a 1-MHz access speed takes 2 ms to transfer 256 bytes (1 page) of data and 5 ms to complete the nonvolatile write cycle for each page. Therefore, a three-stage pipeline implementation is required to achieve the write to EEPROM at the bus speed.

An SPI interface EEPROM with a 20-MHz access speed takes 100 µs to transfer 256 bytes (1 page) of data and 5 ms to complete the nonvolatile write cycle for each page. Therefore, a 50-stage pipeline implementation is required to achieve the write to EEPROM at the bus speed.

The serial F-RAM, on the other hand, writes data at the bus speed irrespective of interface and access speed. Therefore, the serial F-RAM doesn't require pipeline implementation, simplifies the system firmware architecture and reduces the development cycle time and associated test overheads.

4.4 No Page Size Restriction

The EEPROM page size can vary by density. So, the routines to interface to an EEPROM must be written flexibly and tested over a range of density options. F-RAM imposes no page size restriction, enabling you to write arbitrarily sized blocks of data, independent of the total size of memory in use.

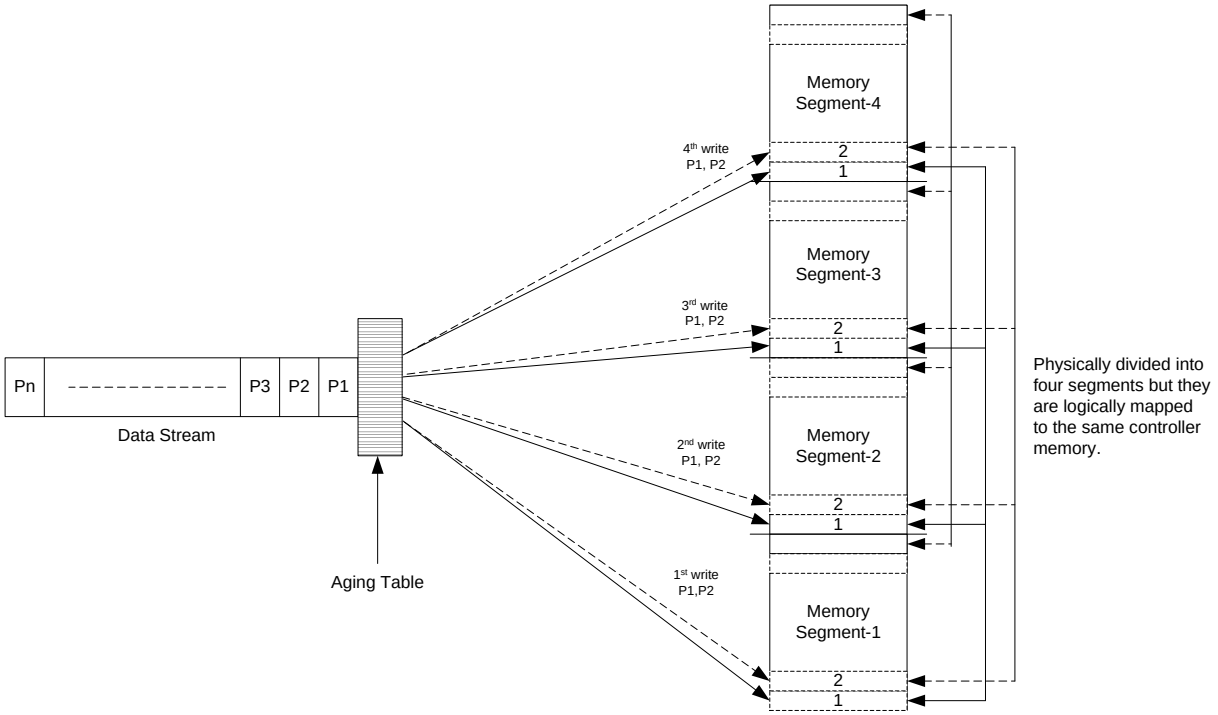
4.5 No Wear Leveling or Aging Tracking Required

Every write of a page or partial page (for example, a byte) to an EEPROM counts toward the finite endurance limit of nonvolatile technology. This is critical in a smart e-meter, in which data may have to be recorded once every few seconds or even every few milliseconds.

All EEPROM-based systems that write regularly to EEPROM use careful address management. This method, called “wear leveling,” aims to equalize the number of times each page is written.

Wear leveling is used in EEPROM to increase the effective endurance limit. In a wear leveling implementation, the entire memory array is divided into multiple segments that are mapped to identical addresses of a microcontroller or processor. For example, if a write happens to some address location(s) in the current memory segment, the subsequent write to the same address location(s) will be executed in a different segment. The wear leveling implementation is illustrated in Figure 6.

Figure 6. Wear Leveling Mechanism in EEPROM



Wear leveling requires a fairly sophisticated driver routine in the controller, through which all nonvolatile accesses are managed. This routine translates the internal addressing of data structures into a physical addressing scheme for the memory. Usually, an “aging table” on the memory array tracks how the device is being used. This consumes a significant amount of code space in a miniature filing system.

Because of the fundamental importance of data integrity in a smart e-meter application (which is legally prescribed in many territories), there is a substantial testing burden on such routines. During an architectural change, this increases the design cycle time when migrating to a new processor family.

The fundamental nonvolatile storage physical layer in F-RAM is similar to that of EEPROM. However, ferroelectric material wears out very slowly in comparison to EEPROM. For example, a typical EEPROM device specifies an endurance cycle of 1E+6, whereas the endurance count for F-RAM devices is 1E+14, which is 100 million times more than a typical EEPROM endurance cycle. Cypress's F-RAM does not require wear leveling or aging tracking. As a result, F-RAM more easily conforms to the requirements in smart e-meters relating to the security, location, format, and accessibility of stored information used for billing.

4.6 No Action Required After Power Failure

Data immediately becomes nonvolatile after it is written to F-RAM. This is one of the key benefits of using an F-RAM device: it increases confidence in system data integrity under extreme fault conditions. All writes happen directly to the nonvolatile memory. Therefore, no power backup or extended power supply is needed to save the data after power failure.

In contrast, to save valuable data in an EEPROM-based system, the controller must initiate and execute a complete write cycle to the desired data block size when a power fault is detected. The main power supply must store sufficient energy to reliably power the controller and its peripherals throughout this process. The controller must be protected against crashes caused by a rapid transition on the power supply during power failure. The system firmware must be thoroughly tested over a range of error conditions to ensure that the correct action is carried out at whatever system state existed before the power failure.

4.7 Dedicated Serial Number Registers

Every smart e-meter is identified with a unique serial number, which is stored in either a dedicated small-density EEPROM or a portion of the nonvolatile data logging memory that is write protected. A few F-RAM devices, such as FM24VN10, FM25VN10, and processor companion devices, provide a dedicated 8-byte (64-bit) storage for serial number read and write.

The serial number locations are dedicated F-RAM registers that can be read from or written to only with a unique command, preventing unintended access to the serial number. F-RAM provides a unique one-time-programmable serial number lock bit, which, once set, cannot be removed. This prevents any unintended writes to the serial number registers throughout a product's life. Until the serial number lock bit is set to one, the serial number can be written as many times as required. This setting is nonvolatile but alterable.

5 F-RAM with Processor Companion Features

Cypress's F-RAM memories integrate highly versatile processor companion features that are used to design most advanced systems, including smart e-meters. The following sections summarize the processor companion features, advantages, and use cases. See the respective product datasheets for further details. Refer to the product datasheet before designing with processor companion features.

5.1 Real-Time Clock

The real-time clock (RTC) feature provides the time and calendar update for a system. In addition to the standard RTC, the processor companion offers an on-chip software calibration feature, which can correct the ppm drift in the RTC clock and improve the RTC clock error from ±512 ppm (parts per million) to ±2.17 ppm. In other words, a timing error of ±22.11 minutes per month is corrected to ±2.592 seconds per month. The software calibration feature helps when designing a very precise system clock that operates in a controlled environment.

The software calibration feature is used to correct only the constant ppm error (within ±512 ppm) in an RTC clock. Many factors can cause the ppm error:

- Improper RTC crystal selection with high ppm errors
- Mismatch in crystal load from the datasheet's recommended load (C_L)
- An inherent temperature characteristic of the RTC crystal at a given temperature
- Improper RTC signal layout
- Component placement

5.2 Low-Voltage Detect

The low-voltage detect feature is designed to track and determine the status of a system's power supply before it is applied to other critical circuits. A user-programmable low-voltage detect threshold gives you the flexibility to determine and set the threshold according to the system's operating conditions.

Smart e-meters can use this feature to monitor the transmission line power supply status. By setting the appropriate threshold, you can detect an unexpected power outage or unintended fluctuations in the power supply in advance. Therefore, you can take the appropriate action by sending an early warning to the grid system or by implementing a safe shutdown of metering systems.

5.3 Watchdog Timer

The processor companion chip provides a watchdog timer with a programmable timeout duration from 100 ms to 3 seconds. It generates a nonmaskable interrupt (NMI) on one of its dedicated output pins upon timeout. You can design the watchdog timer feature of the processor companion to monitor the system's health externally.

5.4 Early Power Failure Warning

This is a simple but effective feature that you can use to trigger an early power failure warning well before the power supply drops out of its minimum spec. The power supply input is compared with an internal threshold voltage (typically 1.2 V), and it generates an NMI when the power supply drops below the threshold level.

5.5 Event Counter on Backup Power

The processor companion offers two battery-backed event counter pins, CNT1 and CNT2, on the chip. The input pins CNT1 and CNT2 are programmable edge detectors, and each clocks a 16-bit counter. When an edge occurs, the counters increment their respective registers. The two 16-bit counters can be cascaded to create a single 32-bit counter. In cascade mode, CNT1 is active and CNT2 is internally disabled, making it unavailable for use.

You can use the event counter feature to detect tampering in smart e-meters. A tamper attempt (in the form of either the decasing of meter enclosures or unauthorized access to meter circuits, the system, or connections) can be indicated using a signal transition from its known state (HIGH or LOW) to the opposite state. In processor companion parts, this signal transition can be detected easily on either of the event counter pins, both in active mode and power-down mode. Every transition detected on the CNT pin increments the nonvolatile counter value by one. The host controller can read out the counter value at any time when the device is active after power up.

6 Summary

The EEPROM has been the de facto choice of nonvolatile data logging memory in electricity meter applications. Its advantages have included low cost, an easy interface, and availability in industry-standard packages. Until a few years ago, the features offered by an EEPROM were sufficient to meet the critical requirements of a majority of electricity meter designs. However, the arrival of the AMI and smart grids, with their rapid adoption in many areas of the world, has revolutionized electricity meter architecture and design. This new class of meters is called smart e-meters.

Smart e-meters require a large amount of data to be stored periodically in a very short time interval. An EEPROM cannot meet this requirement because of its slow write speed and limited endurance cycles. This application note discusses the key challenges faced by EEPROM-based smart e-meters and describes how F-RAM can address these deficiencies without any hardware or architectural modifications.

Document History

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Document Number: 001-87352

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4102602	ZSK	08/26/2013	New Specification
*A	4307935	ZSK	03/17/2014	No update to the technical content of the application note Improved the resolution of Figure 3 and Figure 4. Modified energy consumption unit in Note below Figure 3 to µJoul.
*B	4316427	ZSK	03/21/2014	Modified “peak power tariff” to “time-of-day billing” to make it consistent with the commonly used terminology. Added low power as a benefit of F-RAM in Benefits of F-RAM. Modified “fixed internal threshold” to “an internal threshold” with 1.2-V threshold voltage in Early Power Failure Warning.
*C	4860028	ZSK	07/28/2015	Sunset ECN. Updated template. Fixed typos in Low-Power Design section.
*D	5807391	AESATMP8	07/13/2017	Updated logo and Copyright.

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