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Spec No: 001-87072

Spec Title: AN302 - F-RAM (TM) SPI READ AND WRITE INTERNAL OPERATION AND DATA PROTECTION

Replaced by: None

F-RAM™ SPI Read and Write Internal Operation and Data Protection

Author: Harsha Medu
Associated Code Examples: CE204087
Related Application Notes: AN304

AN302 discusses the importance of keeping $\overline{CS}$ HIGH during power transitions and suggests a circuit to accomplish this. It also describes the internal operation of Cypress's high-speed SPI F-RAM devices during memory read & write operations.

1 Overview

Ferroelectric random access memory (F-RAM) is a nonvolatile memory that uses a ferroelectric technology for storing data. The SPI F-RAM scores over other nonvolatile serial memory options due to its fast write speed and endurance (the number of writes that can be done before damaging the F-RAM's nonvolatile cells). Hundreds of bytes can be written in tens of microseconds. EEPROM and flash memories require tens of milliseconds to do the same. Writing data quickly before losing power is particularly useful in systems that require preserving machine state information, parameter settings, or other vital data in a power-down event. To preserve data make certain to control signals at both power up and power down.

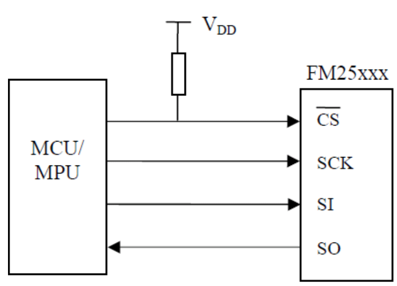
F-RAM SPI devices have no power management circuits other than a simple internal power-on reset circuit. The system designer must ensure that V_{DD}, V_{DD} power-up ramp rate, and V_{DD} power-down ramp rate are within datasheet tolerances to prevent any incorrect operation. The system designer should be aware of chip-enable and V_{DD} states during power cycles, especially considering the strange waveforms delivered by switching power supplies, manually controlled power switches, multi-stage turn-on supplies, and so on. As mentioned later in this document, the control pin ($\overline{CS}$) must be held inactive (HIGH) during any power transition.

This application note offers system design suggestions for keeping the $\overline{CS}$ pin HIGH during power transitions to avoid data corruption. It also describes the internal read and write operations of Cypress's high-speed F-RAM SPI devices. For more details on SPI F-RAM, refer to AN304 - SPI Guide for F-RAM.

2 Keep $\overline{CS}$ HIGH on Any Power Transition

To protect the F-RAM from corrupting data during power cycles, it is recommended to hold the control pin, $\overline{CS}$ inactive as V_{DD} powers up and powers down. In many cases, this may be as simple as a pull-up resistor on the MCU's output pin that drives $\overline{CS}$ as shown in Figure 1. A value in the 5 kΩ to 10 kΩ range is recommended. As the system microcontroller powers up, its outputs will tri-state before the power supply reaches sufficient voltage to turn various internal circuits on, thereby allowing the pull-up resistor to keep the signal at V_{DD}. Similarly, at power down there is a V_{DD} voltage level that causes the outputs to "let go", again allowing the pull-up resistor to do its job.

Figure 1. Pull-up Resistor Tied to Microcontroller's Tri-stateable Buffer



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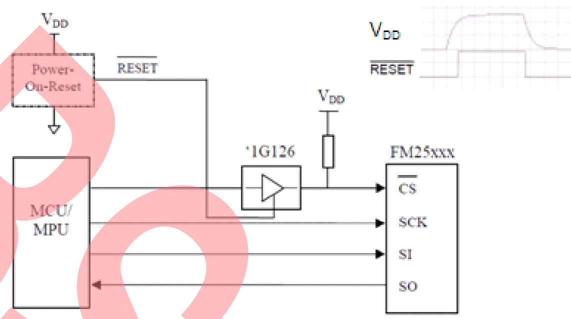
However not all microcontrollers will be HI-Z at voltages below their normal operating range. The use of a system reset chip and tri-stateable buffer between the system microcontroller and F-RAM may be required to keep $\overline{CS}$ pulled up to V_{DD} during power up or power down as shown in Figure 2. A tri-stateable buffer, which has an active HIGH enable input, places the output in a HI-Z state whenever the enable pin is low. For example, during system reset, the active LOW POR output ($\overline{RESET}$ in Figure 2) keeps the buffer in tristate and therefore, the $\overline{CS}$ pin is HIGH due to the pull-up resistor. The $\overline{RESET}$ is released when V_{DD} reaches its trip voltage and the $\overline{CS}$ pin is driven by the MCU. Figure 2 shows a 1G126 single-gate buffer. These are packaged in a very small SOT-23 package that requires very little board space.

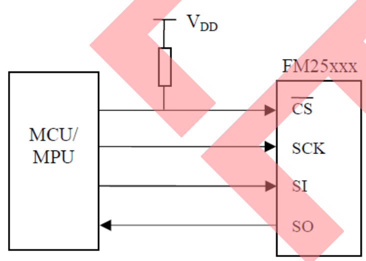
Figure 2. Tri-stateable Buffer Used on the $\overline{CS}$ pin of the F-RAM Device



3 F-RAM SPI Read/Write Cycles

A typical F-RAM SPI interface to a microcontroller is shown in Figure 3. F-RAM SPI transactions involve op-code, address bytes, and data bytes. All operations are initiated on the falling edge of $\overline{CS}$, which is an edge-triggered input. A read or a write opcode is then clocked-in, followed by address and data bytes. All SPI transactions are treated as 8-bit data; therefore, all internal operations including memory accesses are byte-wide in nature. The serial data is internally buffered by an 8-bit shift register. For reads, the data is internally pre-fetched into the 8-bit shift register and subsequently clocked out. Writes to the memory occur after each data byte is clocked-in to the shift register.

Figure 3. Basic F-RAM SPI Interface



3.1 Read Operations

For read cycles, the memory array access begins on the fifth rising clock edge of the last address byte (LSB Address) and the fifth clock of each subsequent data byte. The user has no control over the duration of the internal memory access. Figure 4 shows that the first access loads Data Byte 'n' at marker #3 and the data is shifted out, the second access loads Data Byte 'n+1' at marker #4 and the data is shifted out, and the third access loads Data Byte 'n+2'. However, because $\overline{CS}$ goes HIGH, the data is never shifted out. Note that because $\overline{CS}$ transitions are asynchronous, de-asserting $\overline{CS}$ at anytime immediately terminates the operation.

The Read Cycle is shown in Figure 4 and Figure 5. It is labeled with numbers that correspond to certain events.

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Figure 4. Example of a Read Cycle (F-RAM 256 Kbit Part)

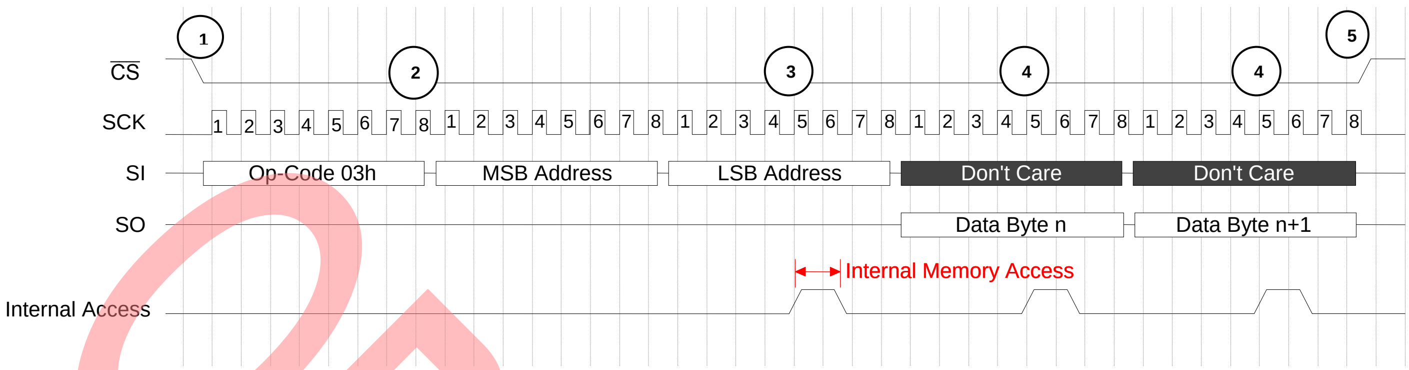
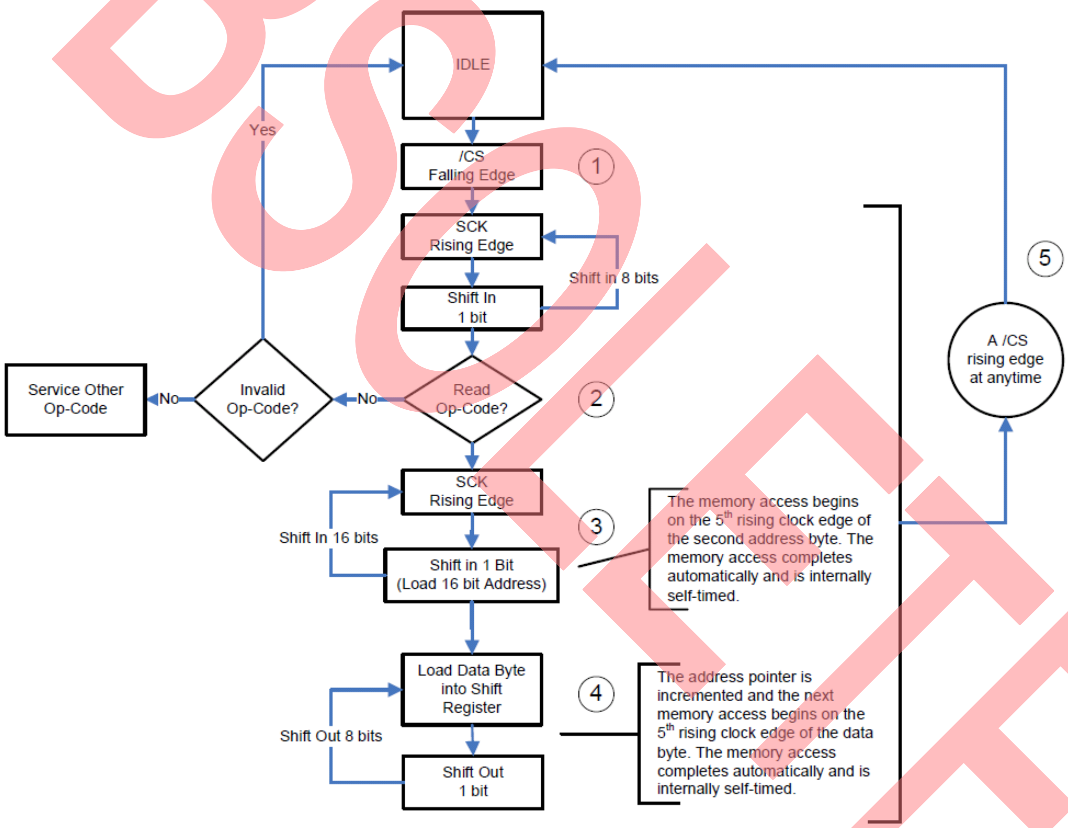


Figure 5. Detailed Flow Diagram of a Read Cycle



4 Write Operations

A write cycle will begin only if the Write Enable Latch (WEL) bit is set. The WEL bit is set by issuing the Write Enable (WREN) opcode. This enable bit is internally reset after the write cycle terminates. The WRITE op-code and two-byte address (for 256 Kbit part) is then clocked-in, and the memory array is accessed on the 5th clock of the data byte and remains open until the 8th rising clock edge. If the clock is suspended or $\overline{\text{HOLD}}$ is asserted, the memory access does not complete. It is therefore important that V_{DD} remains within its specified range while the memory access (write) is pending. The write operation is very fast (<200 ns). Since V_{DD} does not fall significantly in 200 ns, the write cycle is not compromised. After V_{DD} drops below the minimum specified voltage, the $\overline{\text{CS}}$ pin must be pulled up to V_{DD} to cleanly terminate any ongoing accesses.

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If $\overline{CS}$ is de-asserted before the eighth clock of the data byte, the write operation is aborted and the internal memory cycle is completed without the successful write of the data byte. If $\overline{CS}$ is de-asserted after the eighth clock, the write operation will complete automatically.

The Write Cycle is shown in Figure 6 and Figure 7. It is labeled with numbers that correspond to certain events.

Figure 6. Example of a Write Cycle (F-RAM 256 Kbit Part)

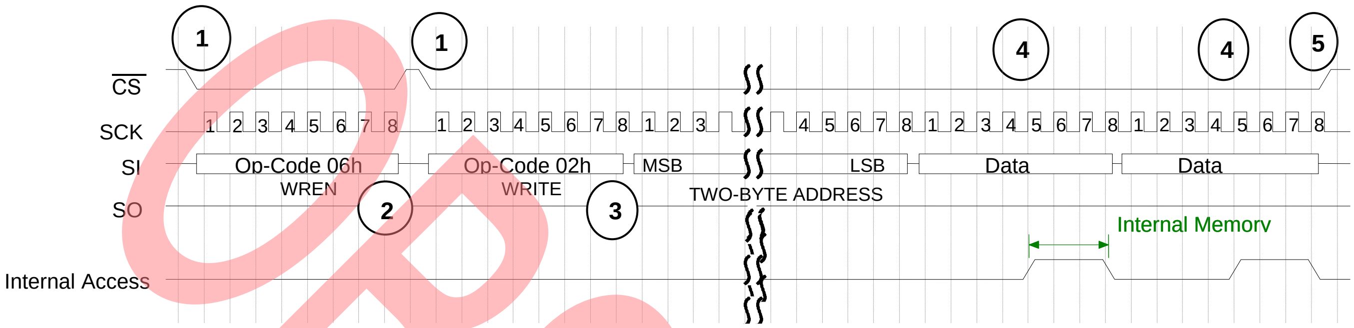

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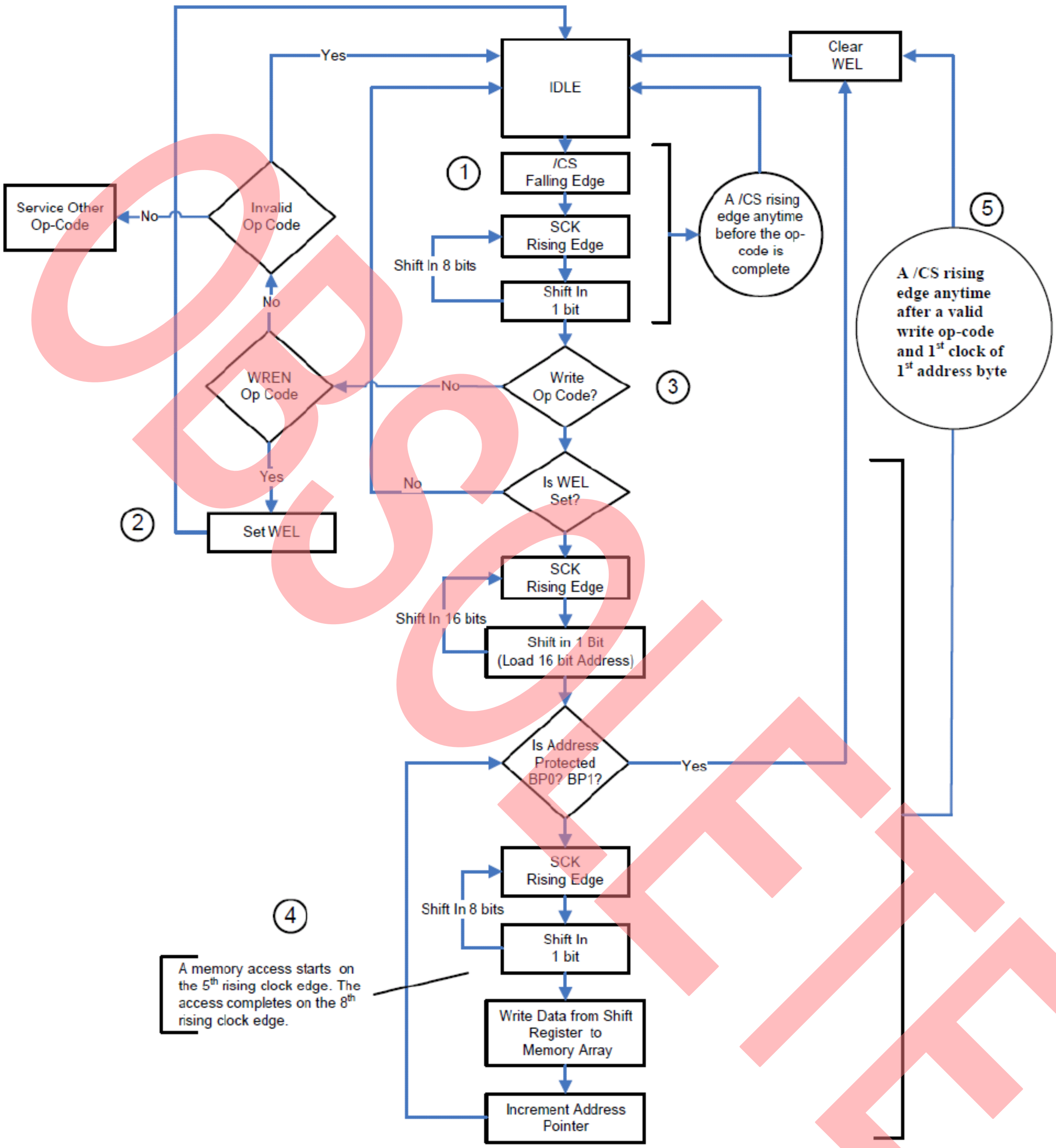
Figure 7. Detailed Flow Diagram of a Write Cycle



5 Summary

This application note recommends certain design considerations for the chip-select $\overline{CS}$ pin to prevent data corruption during power cycles and clearly describes the internal Read/Write operations in SPI F-RAMs.

Document History

Document Title: AN302 -F-RAM™ SPI Read and Write Internal Operation and Data Protection

Document Number: 001-87072

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4018188	MEDU	06/11/2013	New Spec.
*A	4564067	MEDU	11/10/2014	Changed the title from “AN302 - F-RAM SPI Read & Write and Data Protection during Power Cycles” to “F-RAM SPI Read & Write Internal Operation and Data Protection” Added a reference to AN304 – SPI Guide for F-RAM Updated Figure 8. Detailed Flow Diagram of a Write Cycle
*B	4573028	MEDU	11/18/2014	Attached the associated project.
*C	4609958	MEDU	12/29/2014	Updated to indicate that a project is attached with the application note
*D	5285474	MEDU	05/26/2016	Added a reference to code example CE204087
*E	5711154	AESATP12	04/27/2017	Updated logo and copyright. This product is no longer available and this Spec to be Obsolete.

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