PRELIMINARY

PSoC 6 MCU: CY8C62X8, CY8C62XA Datasheet

PSoC 62 MCU

General Description

PSoC® 6 MCU is a high-performance, ultra-low-power and secure MCU platform, purpose-built for IoT applications. The PSoC 62 product family, based on the PSoC 6 MCU platform, is a combination of a dual CPU microcontroller with low-power flash technology, digital programmable logic, high-performance analog-to-digital and standard communication and timing peripherals.

Features

32-bit Dual-CPU Subsystem

- 150-MHz Arm® Cortex®-M4F CPU with single-cycle multiply (Floating Point and Memory Protection Unit)
- 100-MHz Cortex-M0+ CPU with single-cycle multiply and MPU
- User-selectable core logic operation at either 1.1 V or 0.9 V
- 8-KB Instruction Caches for both CPU cores
- Active CPU current slope with 1.1-V core operation
  - Cortex-M4: 40 µA/MHz
  - Cortex-M0+: 28 µA/MHz
- Active CPU current slope with 0.9-V core operation
  - Cortex-M4: 27 µA/MHz
  - Cortex-M0+: 20 µA/MHz
- Three DMA controllers

Flexible Memory Subsystem

- 2048-KB Application Flash, 32-KB emulated EEPROM area, and 32-KB Supervisory Flash; Read-While-Write (RWW) support
- 1024-KB SRAM with three independent blocks for power and data retention control
- One-Time-Programmable (OTP) 1-Kb eFuse memory for validation and security

Low-Power 1.7-V to 3.6-V Operation

- Six power modes for fine-grained power management
- Deep Sleep mode current of 7 µA with 64-KB SRAM retention
- On-chip DC-DC Buck converter, <1 µA quiescent current
- Backup domain with 64 bytes of memory and Real-Time Clock

Flexible Clocking Options

- On-chip crystal oscillators (4 to 35 MHz, and 32 kHz)
- Two Phase-locked Loops (PLLs) for multiplying clock frequencies
- 8 MHz Internal Main Oscillator (IMO) with ±2% accuracy
- Ultra-low-power 32-kHz Internal Low-speed Oscillator (ILO)
- Frequency Locked Loop (FLL) for multiplying IMO frequency

Quad-SPI (QSPI)/Serial Memory Interface (SMIF)

- Execute-In-Place (XIP) from external Quad SPI Flash
- On-the-fly encryption and decryption
- 4-KB cache for greater XIP performance with lower power
- Supports single, dual, quad, dual-quad, and octal interfaces w/ throughput up to 640 Mbps

Serial Communication

- 13 run-time configurable serial communication blocks (SCBs)
  - Eight SCBs: configurable as SPI, I^2C, or UARTs
  - Four SCBs: configurable as I^2C or UART
  - One Deep Sleep SCB: configurable as SPI or I^2C
- USB Full-Speed Dual-role Host and Device interface
- Two independent SDHC/eMMC/SD controllers

Audio Subsystem

- Two PDM channels and two I^2S channels with TDM mode

Timing and Pulse-Width Modulation

- Thirty-two Timer/Counter Pulse-Width Modulator (TCPWM)
- Center-aligned, Edge, and Pseudo-random modes
- Comparator-based triggering of Kill signals

Programmable Analog

- 12-bit 1-Msps SAR ADC with differential and single-ended modes and 16-channel sequencer with result averaging
- Two low-power comparators available in Deep Sleep and Hibernate modes
- Built-in temp sensor connected to ADC

Up to 102 Programmable GPIOs

- Two Smart I/O ports (16 I/Os) enable Boolean operations on GPIO pins; available during Deep Sleep
- Programmable drive modes, strengths, and slew rates
- Six overvoltage-tolerant (OVT) pins

Capacitive Sensing

- Cypress CapSense Sigma-Delta (CSD) provides best-in-class SNR, liquid tolerance, and proximity sensing
- Enables dynamic usage of both self and mutual sensing
- Automatic hardware tuning (SmartSense™)

Security Built into Platform Architecture

- ROM-based root of trust via uninterruptible Secure Boot
- Step-wise authentication of execution images
- Secure execution of code in execute-only mode for protected routines
- All Debug and Test ingress paths can be disabled
- Up to eight Protection Contexts

Cryptography Accelerators

- Hardware acceleration for symmetric and asymmetric cryptographic methods and hash functions
- True Random Number Generator (TRNG) function

Packages: 124-BGA, 128-TQFP, 100-WLCSP

Development Ecosystem

PSoC 6 MCU Resources

Cypress provides a wealth of data at www.cypress.com to help you select the right PSoC device and quickly and effectively integrate it into your design. The following is an abbreviated, hyperlinked list of resources for PSoC 6 MCU:

- **Overview**: PSoC Portfolio, PSoC Roadmap
- **Product Selectors**: PSoC 6 MCU
- **Application Notes** cover a broad range of topics, from basic to advanced level, and include the following:
  - AN221774: Getting Started with PSoC 6 MCU
  - AN218241: PSoC 6 MCU Hardware Design Guide
  - AN213924: PSoC 6 MCU Device Firmware Update Guide
  - AN215656: PSoC 6 MCU Dual-CPU System Design
  - AN219528: PSoC 6 MCU Power Reduction Techniques
  - AN221111: PSoC 6 MCU Creating a Secure System
  - AN85951: PSoC 4, PSoC 6 MCU CapSense Design Guide
- **Code Examples** demonstrate product features and usage, and are also available on Cypress GitHub repositories.
- **Technical Reference Manuals (TRMs)** provide detailed descriptions of PSoC 6 MCU architecture and registers.
- PSoC 6 MCU Programming Specification provides the information necessary to program PSoC 6 MCU nonvolatile memory
- Development Tools
  - ModusToolbox™ enables cross platform code development with a robust suite of tools and software libraries
  - CY8CPROTO-062-4343W prototyping kit provides PSoC 6 MCU hardware support with WiFi and Bluetooth connectivity. Additional kits enable development for other PSoC 6 MCU devices with a variety of connectivity options.
  - PSoC 6 CAD libraries provide footprint and schematic support for common tools
- **Training Videos** are available on a wide range of topics including the PSoC 6 MCU 101 series
- **Cypress Developer Community** enables connection with fellow PSoC developers around the world, 24 hours a day, 7 days a week, and hosts a dedicated PSoC 6 MCU Community

ModusToolbox™ IDE and the PSoC 6 SDK

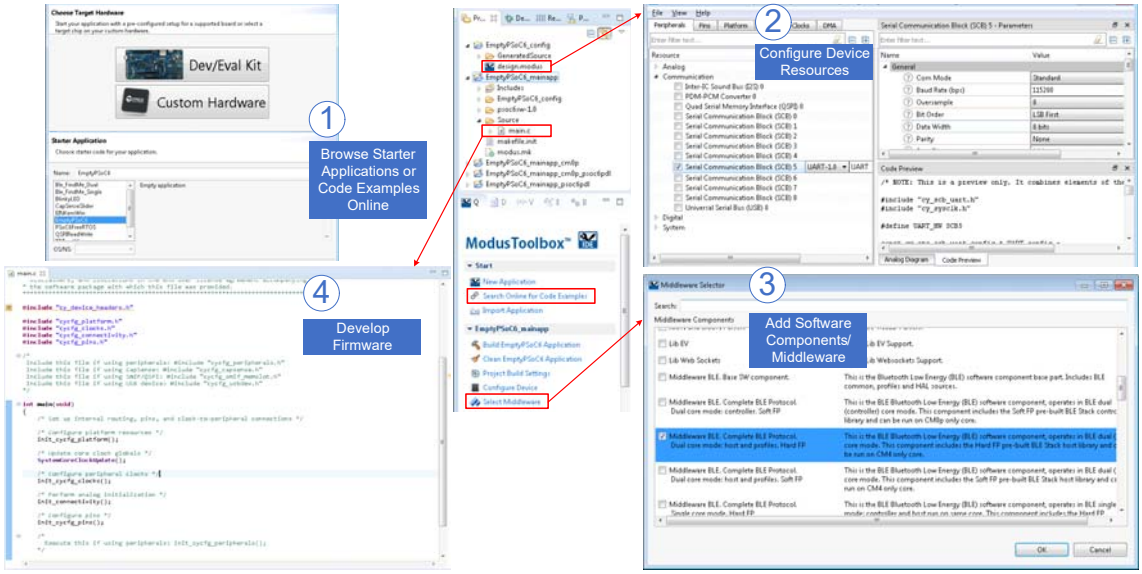
ModusToolbox is an Eclipse-based development environment on Windows, macOS, and Linux platforms that includes the ModusToolbox IDE and the PSoC 6 SDK. The ModusToolbox IDE brings together several device resources, middleware, and firmware to build an application. Using ModusToolbox, you can enable and configure device resources and middleware libraries, write `C/assembly` source code, and program and debug the device.

The PSoC 6 SDK is the software development kit for the PSoC 6 MCU. The SDK makes it easier to develop firmware for supported devices without the need to understand the intricacies of the device resources.

For additional detail on using the Cypress tools, refer to AN221774: Getting Started with PSoC 6 MCU and the documentation and help integrated into ModusToolbox. As Figure 1 shows, with the ModusToolbox IDE, you can:

1. Create a new application based on a list of starter applications, filtered by kit or device, or browse the collection of code examples online.
2. Configure device resources in *design.modus* to build your hardware system design in the workspace.
3. Add software components or middleware.
4. Develop your application firmware.

Figure 1. ModusToolbox IDE Resources and Middleware



Blocks and Functionality

The PSoC 62 block diagram is shown in Figure 2. There are four major subsystems: CPU subsystem, system resources, peripheral blocks, and I/O subsystem. For a description of the acronyms used in the diagram, refer to Acronyms.

Figure 2. Block Diagram

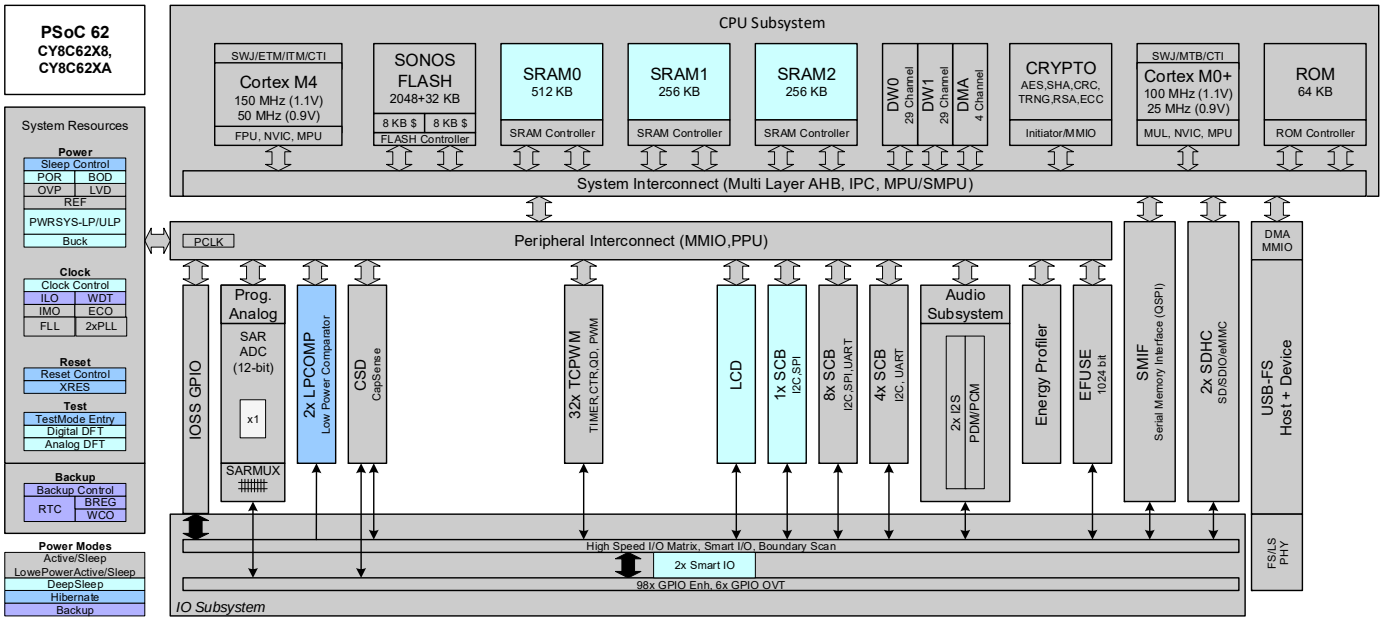


Figure 2 shows the subsystems of the chip and gives a very simplified view of their inter-connections (Multi-layer AHB is used in practice). The color-coding shows the lowest-power mode where the particular block is still functional (for example, LP Comparator is functional in System LP/ULP, Deep Sleep, and Hibernate modes).

PSoC 62 includes extensive support for programming, testing, debugging, and tracing both hardware and firmware.

Complete debug-on-chip functionality enables full device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The ModusToolbox Integrated Development Environment (IDE) provides fully integrated programming and debug support for PSoC 62 devices. The SWJ (SWD and JTAG) interface is fully compatible with industry-standard third party probes. With the ability to disable debug features, with very robust flash protection, and by allowing customer-proprietary functionality to be implemented in on-chip programmable blocks, PSoC 62 provides a very high level of security.

There are three debug access ports, one each for CM4 and CM0+, and a system port. They are enabled by default. Each can be disabled and enabled independently.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. The security level is a trade-off the customer can make.

Functional Description

The following sections provide an overview of the features, capabilities and operation of each functional block identified in the block diagram in Figure 2. For more detailed information, refer to the following three references.

- Peripheral Driver Library (PDL) Application Programming Interface (API) Reference Manual.

  PDL provides low-level drivers for each resource in the device, and supports the entire PSoC 6 MCU portfolio. PDL is an element of the PSoC 6 SDK, which is installed as part of ModusToolbox. With ModusToolbox installed, you can access the PDL API reference manual either from the Documentation tab of the Quick Panel, or you can navigate directly to it at `<install_directory>\ModusToolbox_<version>\libraries\psoc6sw-<version>\docs`. Using PDL should be the primary means of interacting with the PSoC 6 MCU hardware.

- Architecture Technical Reference Manual (TRM)

  The architecture TRM provides the detailed description of each resource in the device. This is the next reference to use if it is necessary to understand the operation of the hardware below the software provided by PDL. It describes the architecture and functionality of each resource and explains the operation of each resource in all modes. It provides specific guidance regarding the use of associated registers.

- Register Technical Reference Manual

  The register TRM provides the complete list of all registers in the device. It includes the breakdown of all register fields, their possible settings, read/write accessibility, and default states. All registers that have a reasonable use in typical applications have functions to access them from within PDL. Note that ModusToolbox and PDL may provide software default conditions for some registers that are different from and override the hardware defaults.

CPU and Memory Subsystem

PSoC 62 has multiple bus masters, as Figure 2 shows. They are: two CPUs, three DMA controllers, two SDHC controllers, and a Crypto block. Generally, in PSoC 62, all memory and peripherals can be accessed and shared by all bus masters through multi-layer Arm AMBA high-performance bus (AHB) arbitration. Accesses between CPUs can be synchronized using an inter-processor communication (IPC) block.

CPUs

There are two Arm Cortex CPUs:

The Cortex-M4 (CM4) CPU has single-cycle multiply, a floating-point unit (FPU), and a memory protection unit (MPU). It can run at up to 150 MHz. This is the main CPU, designed for a short interrupt response time, high code density, and high throughput.

CM4 implements a version of the Thumb instruction set based on Thumb-2 technology (defined in the *Armv7-M Architecture Reference Manual*).

The Cortex-M0+ (CM0+) CPU has single-cycle multiply, and an MPU. It can run at up to 100 MHz; however, for CM4 speeds above 100 MHz, CM0+ and bus peripherals are limited to half the speed of CM4. Thus, for CM4 running at 150 MHz, CM0+ and peripherals are limited to 75 MHz.

CM0+ is the secondary CPU; it is used to implement system calls and device-level security, safety, and protection features. CM0+ provides a secure, uninterruptible boot function. This guarantees that post boot, system integrity is checked and memory and peripheral access privileges are enforced.

CM0+ implements the Armv6-M Thumb instruction set (defined in the *Armv6-M Architecture Reference Manual*).

These CPUs have the following power draw, at V_{DD} = 3.3 V and using the internal buck regulator:

Table 1. Active Current Slope at V_{DD} = 3.3 V Using the Internal Buck Regulator

		System Power Mode	
		ULP	LP
CPU	Cortex-M0+	15 µA/MHz	20 µA/MHz
	Cortex-M4	22 µA/MHz	40 µA/MHz

These CPUs can be selectively placed in their Sleep and Deep Sleep power modes as defined by Arm.

Each CPU has an 8-KB instruction cache with 4-way set associativity. Both CPUs have nested vectored interrupt controllers (NVIC) for rapid and deterministic interrupt response, and wakeup interrupt controllers (WIC) for CPU wakeup from Deep Sleep power mode.

These CPUs have extensive debug support. PSoC 6 MCU has a debug access port (DAP) that acts as the interface for device programming and debug. An external programmer or debugger (the “host”) communicates with the DAP through the device serial wire debug (SWD) or Joint Test Action Group (JTAG) interface pins. Through the DAP (and subject to device security restrictions), the host can access the device memory and peripherals as well as the registers in both CPUs.

Each CPU offers debug and trace features as follows:

- CM4 supports six hardware breakpoints and four watchpoints, 4-bit embedded trace macrocell (ETM), serial wire viewer (SWV), and printf()-style debugging through the single wire output (SWO) pin.
- CM0+ supports four hardware breakpoints and two watchpoints, and a micro trace buffer (MTB) with 4 KB dedicated RAM.

PSoC 62 also has an Embedded Cross Trigger for synchronized debugging and tracing of both CPUs.

Interrupts

PSoC 62 has 168 system and peripheral interrupt sources and supports interrupts and system exception on both CPUs. CM4 has 168 interrupt request lines (IRQ), with the interrupt source ‘n’ directly connected to IRQn. CM0+ has eight interrupts IRQ[7:0] with configurable mapping of one or more interrupt sources to any of the IRQ[7:0]. CM0+ also supports eight internal (software only) interrupts.

Each interrupt supports configurable priority levels (eight levels for CM4 and four levels for CM0+). Up to four system interrupts can be mapped to each of the CPU's non-maskable interrupt (NMI). Up to 39 interrupt sources are capable of waking the device from Deep Sleep power mode using the WIC. Refer to the technical reference manual for details.

Direct Memory Access (DMA) Controllers

PSoC 62 has three DMA controllers, which support CPU-independent accesses to memory and peripherals. Two of them have 29 channels each and the third has 4 channels. The descriptors for DMA channels can be in SRAM or flash. Therefore, the number of descriptors are limited only by the size of the memory. Each descriptor can transfer data in two nested loops with configurable address increments to the source and destination. The size of data transfer per descriptor varies based on the type of DMA channel. Refer to the technical reference manual for detail.

Cryptography Accelerator (Crypto)

This subsystem consists of hardware implementation and acceleration of cryptographic functions and random number generators.

The Crypto subsystem supports the following:

- Encryption/Decryption Functions
  - Data Encryption Standard (DES)
  - Triple DES (3DES)
  - Advanced Encryption Standard (AES) (128-, 192-, 256-bit)
  - Elliptic Curve Cryptography (ECC)
  - RSA cryptography functions
- Hashing functions
  - Secure Hash Algorithm (SHA)
  - SHA1
  - SHA224/256/384/512
- Message authentication functions (MAC)
  - Hashed message authentication code (HMAC)
  - Cipher-based message authentication code (CMAC)
- 32-bit cyclic redundancy code (CRC) generator
- Random number generators
  - Pseudo random number generator (PRNG)
  - True random number generator (TRNG)

Protection Units

PSoC 62 has multiple types of protection units to control erroneous or unauthorized access to memory and peripheral registers. CM4 and CM0+ have Arm MPUs for protection at the bus master level. Other bus masters use additional MPUs. Shared memory protection units (SMPUs) help implement memory protection for memory/ resources that are shared among multiple bus masters. Peripheral protection units (PPU) are similar to SMPUs but are designed for protecting the peripheral register space.

Protection units support memory and peripheral access attributes including address range, read/write, code/data, privilege level, secure/non-secure, and protection context.

Protection units are configured at secure boot to control access privileges and rights for bus masters and peripherals.

Up to eight protection contexts (secure boot is in protection context 0) allow access privileges for memory and system resources to be set by the secure boot process per protection context by bus master and code privilege level. Multiple protection contexts are supported on a single CPU.

Memory

PSoC 62 contains flash, SRAM, ROM, and eFuse memory blocks.

- Flash

  Up to 2 MB of application flash is provided, with two additional 32-KB flash sectors. The application flash is organized into 256-KB sectors. The first 32-KB flash sector is typically used for EEPROM emulation, or equivalent data storage. The second 32-KB region is the supervisory flash (SFlash). Data stored in SFlash includes device trim values, Flash Boot executable code, and encryption keys. After the device transitions into secure mode, SFlash can no longer be changed.

  The flash has 128-bit-wide accesses to reduce power. It also supports read-while-write (RWW) operations; data can be written in one sector while read operations occur in any of the other sectors. This enables flash updates during code execution. Write operations can be performed at the row level. A row, also referred to as a page, is 512 bytes. Read operations are supported in both System Low Power and Ultra-Low Power modes, however write operations may not be performed in System Ultra-Low Power mode.

- SRAM

  Up to 1 MB of SRAM is provided in three banks of 512 KB, 256 KB, and 256 KB. Each SRAM bank provides control over power modes to manage power consumption. For Bank 0 (512 KB), power control and retention granularity are configurable in sixteen 32-KB regions. For banks 1 and 2 (256 KB each) power control is on a per bank basis. For normal operation, the banks can be enabled, or disabled to save power. For System Deep Sleep mode, the banks can also be configured to retain data.

- ROM

  The 64-KB ROM, also referred to as the supervisory ROM (SROM), provides code (ROM Boot) for several system functions. The PSoC 6 MCU ROM contains device initialization, flash write, security, eFuse programming, and other system-level routines. ROM code is executed only by the CM0+ CPU, in protection context 0. A system function can be initiated by either CPU, or through the DAP. This causes an NMI interrupt in CM0+, which causes CM0+ to execute the system function.

- eFuse

  One-time-programmable eFuse consists of 1024 bits, of which 512 are reserved for system use. The remaining bits are available for storing security key information, hash values, unique IDs or other similar user-defined content. Each fuse is individually programmed; once programmed (or "blown"), its state cannot be changed. Blowing a fuse transitions it from the default state of 0 to 1. To program an eFuse, V_{DDIO0} must be at 2.5 V ±5%, with a current draw of 14 mA (max).

Boot Code

Two blocks of code, ROM Boot and Flash Boot, are pre-programmed into the device and work together to provide device startup and configuration, basic security features, life-cycle stage management and other system functions.

■ ROM Boot

On a device reset, the boot code in ROM is the first code to execute. This code performs the following:

- ❒ Integrity checks of flash boot code
- ❒ Device trim setting (calibration)
- ❒ Setting the device protection units
- ❒ Setting device access restrictions for secure life-cycle states

ROM cannot be changed and acts as the Root of Trust in a secure system. ROM code will guarantee secure boot if authentication of application flash is required.

■ Flash Boot

Flash boot is firmware stored in SFlash that ensures that only a validated application may run on the device. It also ensures that the firmware image has not been modified, such as by a malicious third party.

Flash boot:

- ❒ Is validated by ROM Boot
- ❒ Runs after ROM Boot and before the user application
- ❒ Verifies the integrity of the user application
- ❒ Enables system calls
- ❒ Configures the Debug Access Port
- ❒ Launches the user application in the CM4

If the user application cannot be validated, then flash boot ensures that the device is transitioned into a safe state.

Memory Map

Both CPUs have a fixed address map, with shared access to memory and peripherals. The 32-bit (4 GB) address space is divided into the regions shown in Table 2. Note that code can be executed from the code and SRAM regions.

Table 2. Address Map for CM4 and CM0+

Address Range	Name	Use
0x0000 0000 – 0x1FFF FFFF	Code	Program code region. Data can also be placed here. It includes the exception vector table, which starts at address 0.
0x2000 0000 – 0x3FFF FFFF	SRAM	Data region. Code can also be executed from this region. Note that CM4 bit-band in this region is not supported.
0x4000 0000 – 0x5FFF FFFF	Peripheral	All peripheral registers. Code cannot be executed from this region. Note that CM4 bit-band in this region is not supported.
0x6000 0000 – 0x9FFF FFFF	External RAM	SMIF or Quad SPI, (see the Quad-SPI/Serial Memory Interface (SMIF) section). Code can be executed from this region.
0xA000 0000 – 0xDFFF FFFF	External device	Not used.
0xE000 0000 – 0xE00F FFFF	Private peripheral Bus	Provides access to peripheral registers within the CPU core.
0xE010 0A000 – 0xFFFF FFFF	Device	Device-specific system registers.

The device memory map shown in Table 3 applies to both CPUs. That is, the CPUs share access to all PSoC 6 MCU memory and peripheral registers. Note that code can be executed from the code and SRAM regions.

Table 3. Internal Memory Address Map for CM4 and CM0+

Address Range	Memory Type	Size
0x0000 0000 – 0x0001 0000	ROM	64 KB
0x0800 0000 – 0x0810 0000	SRAM	Up to 1 MB
0x1000 0000 – 0x1020 0000	Application flash	Up to 2 MB
0x1400 0000 – 0x1400 8000	EEPROM emulation flash	32 KB
0x1600 0000 – 0x1600 8000	Supervisory flash	32 KB

Note that the SRAM is located in the Code region for both CPUs (see Table 2). There is no physical memory located in the CPUs' SRAM region.

System Resources

Power System

The power system provides assurance that voltage levels are as required for each respective mode and will either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) when the power supply drops below specified levels. The design guarantees safe chip operation between power supply voltage dropping below specified levels (for example, below 1.7 V) and the reset occurring. There are no voltage sequencing requirements.

The V_{DD} supply (1.7 to 3.6 V) powers an on-chip buck regulator or an LDO, selectable by the user. In addition, both the buck and the LDO offer a selectable (0.9 or 1.1 V) core operating voltage (V_{CCD}). The selection lets users choose between two system power modes:

■ System Low Power (LP) operates V_{CCD} at 1.1 V and offers high performance, with no restrictions on any of the device configurations.

■ System Ultra Low Power (ULP) operates V_{CCD} at 0.9 V for exceptional low power results, but imposes limitations on maximum clock speeds.

An additional, backup domain adds an "always on" functionality using a separate power domain supplied by a backup supply (V_{BACKUP}) such as a battery or supercapacitor. It includes a real-time clock (RTC) with alarm feature, supported by a 32.768-kHz watch crystal oscillator (WCO), and power-management IC (PMIC) control. Pin 5 of Port 0 (P0.5) can be assigned as an enable signal for an external PMIC. RTC alarms can be used as a trigger for the PMIC enable signal.

Power Modes

PSoC 6 MCU can operate in four system and three CPU power modes. These modes are intended to minimize the average power consumption in an application. For more details on power modes and other power-saving configuration options, see the application note, AN219528: PSoC 6 MCU Low-Power Modes and Power Reduction Techniques and the Architecture TRM, Power Modes chapter.

Power modes supported by PSoC 6 MCUs, in the order of decreasing power consumption, are:

- System Low Power (LP) – All peripherals and CPU power modes are available at maximum speed
- System Ultra Low Power (ULP) – All peripherals and CPU power modes are available, but with limited speed
- CPU Active – CPU is executing code in system LP or ULP mode
- CPU Sleep – CPU code execution is halted in system LP or ULP mode
- CPU Deep Sleep – CPU code execution is halted and system Deep Sleep is requested in system LP or ULP mode
- System Deep Sleep – Only low-frequency peripherals are available after both CPUs enter CPU Deep Sleep mode
- System Hibernate – Device and I/O states are frozen and the device resets on wakeup

CPU Active, Sleep, and Deep Sleep are standard Arm-defined power modes supported by the Arm CPU instruction set architecture (ISA). LP, ULP, Deep Sleep and Hibernate modes are additional low-power modes supported by PSoC 6 MCU. Hibernate mode is the lowest power mode in the PSoC 6 MCU and on wakeup, the CPU and all peripherals go through a reset.

Clock System

The clock system for PSoC 62 consists of the following (see Figure 3):

- IMO
- ILO
- Watch crystal oscillator (WCO)
- External MHz crystal oscillator (ECO)
- External clock input
- Two PLLs
- One FLL

Clocks may be buffered and brought out to a pin on a smart I/O port.

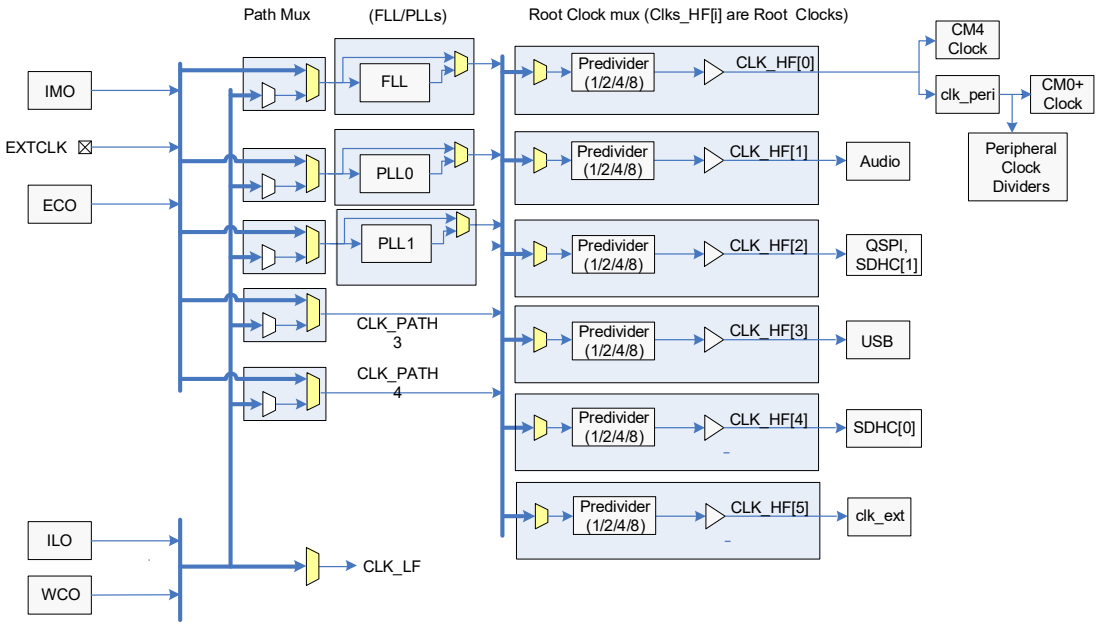
IMO Clock Source

The IMO is the primary source of internal clocking in PSoC 62 . It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 8 MHz. IMO tolerance is ± 2%.

ILO Clock Source

The ILO is a very low power oscillator, nominally 32 kHz, which operates in all power modes. The ILO can be calibrated against a higher accuracy clock for better accuracy.

Figure 3. Clocking Diagram



Watchdog Timer (WDT)

A WDT can be clocked from the ILO or from the WCO. This allows watchdog operation during Deep Sleep and Hibernate modes. The WDT generates a watchdog reset if not serviced before a timeout occurs. The watchdog reset is recorded in the Reset Cause register.

Clock Dividers

Integer and fractional clock dividers are provided for peripheral use and timing purposes. There are:

- Eight 8-bit clock dividers
- Sixteen 16-bit integer clock dividers
- Four 16.5-bit fractional clock dividers
- One 24.5-bit fractional clock divider

Trigger Routing

PSoC 6 MCU contains a trigger multiplexer block. This is a collection of digital multiplexers and switches that are used for routing trigger signals between peripheral blocks and between GPIOs and peripheral blocks.

PSoC 62 have two types of trigger routing. Trigger multiplexers have reconfigurability in the source and destination. There are also hardwired switches called “one-to-one triggers,” which connect a specific source to a destination. The user can enable or disable the route.

Reset

PSoC 6 MCU can be reset from a variety of sources:

- Power-on reset (POR) to hold the device in reset while the power supply ramps up to the level required for the device to function properly. POR activates automatically at power-up.
- Brown-out detect (BOD) reset to monitor the digital voltage supply V_{DDD} and generate a reset if V_{DDD} falls below the minimum required logic operating voltage.
- External reset (XRES) to reset the device using an external input. The XRES pin is active LOW – a logic ‘1’ on the pin has no effect and a logic ‘0’ causes reset. The pin is pulled to logic ‘1’ inside the device. XRES is available as a dedicated pin.
- Watchdog timer (WDT) reset to reset the device if the firmware execution fails to service the watchdog timer within a specified timeout period.
- Software-initiated reset to reset the device on demand using firmware.
- Logic-protection fault can trigger an interrupt to a fault handler or reset the device if unauthorized operating conditions occur; for example, reaching a debug breakpoint while executing privileged code.
- Hibernate wakeup reset to bring the device out of the Hibernate low-power mode.

Reset events are asynchronous and guarantee reversion to a known state. Some of the reset sources are recorded in a register, which is retained through reset and allows software to determine the cause of the reset.

Programmable Analog Subsystems

12-bit SAR ADC

The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion. One of three internal reference voltages may be used for the ADC reference voltage. The references are, V_{DD}, $V_{DD}/2$, and V_{REF} (nominally 1.2 V and trimmed to ±1%). An external reference may also be used, by either driving the VREF pin or routing an external reference to GPIO pin P9.7. These reference options allow ratio-metric readings or absolute readings at the accuracy of the reference used. The input range of the ADC is the full supply voltage between V_{SS} and V_{DDA}/V_{DDIOA}. The SAR ADC may be configured with a mix of single ended and differential signals in the same configuration.

The SAR ADC’s sample-and-hold (S/H) aperture is programmable to allow sufficient time for signals with a high impedance to settle sufficiently, if required. System performance will be 65 dB for true 12-bit precision provided appropriate references are used and system noise levels permit it. To improve performance in noisy conditions, an external bypass capacitor for the internal reference amplifier (through the fixed “VREF” pin), may be added.

The SAR is connected to a fixed set of pins through an input sequencer. The sequencer cycles through the selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The result of each channel is buffered, so that an interrupt may be triggered only when a full scan of all channels is complete. Also, a pair of range registers can be set to detect and cause an interrupt if an input exceeds a minimum and/or maximum value. This allows fast detection of out-of-range values without having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software. The SAR can also be connected, under firmware control, to most other GPIO pins via the Analog Multiplexer Bus (AMUXBUS). The SAR is not available in Deep Sleep and Hibernate modes as it requires a high -speed clock (up to 18 MHz). The SAR operating range is 1.71 to 3.6 V.

Temperature Sensor

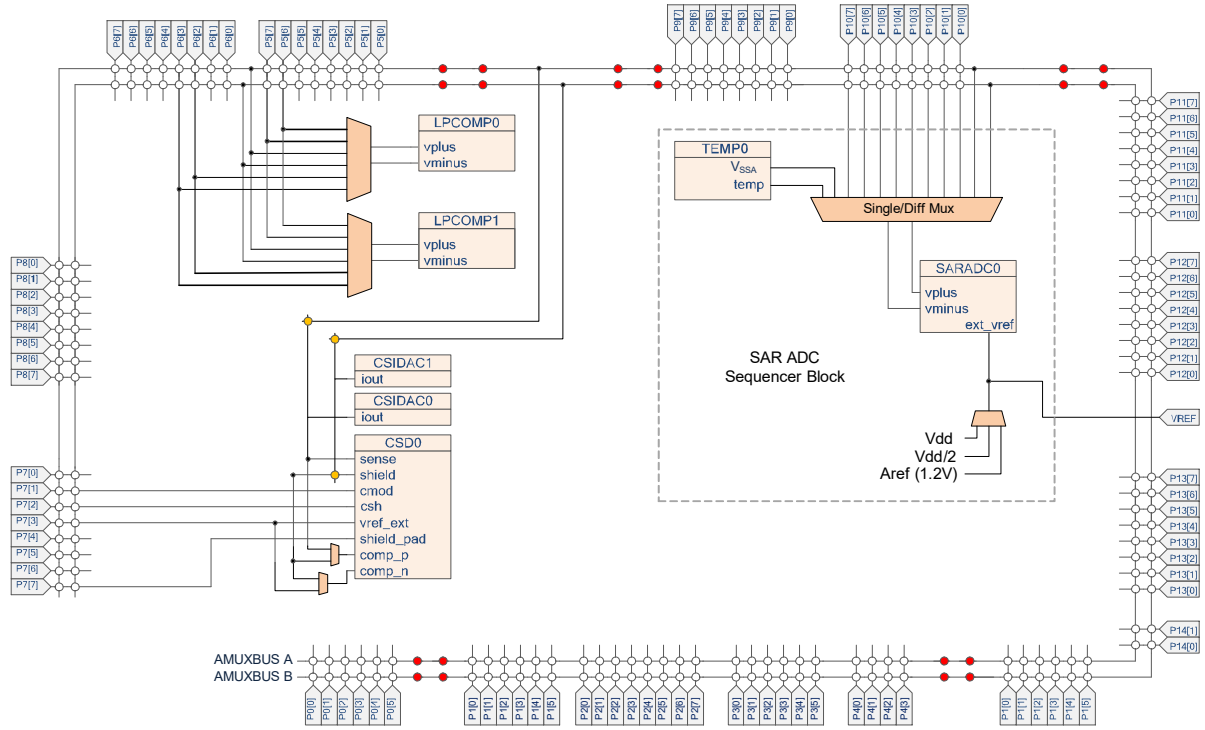
An on-chip temperature sensor is part of the SAR sequencer block and may be scanned by the SAR ADC. It consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor may be connected directly to the SAR ADC as one of the measurement channels. The ADC digitizes the temperature sensor’s output and a Cypress-supplied software function may be used to convert the reading to temperature which includes calibration and linearization.

Low-Power Comparators

Two low-power comparators are provided, which can operate in all power modes. This allows other analog system resources to be disabled while retaining the ability to monitor external voltage levels during Deep Sleep and Hibernate modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator-switch event.

Figure 4 provides an overview of the analog subsystem in PSoC 62.

Figure 4. PSoC 62 Analog Subsystem



Programmable Digital

Smart I/O

Smart I/O™ is a programmable logic fabric that enables Boolean operations on signals traveling from device internal resources to the GPIO pins or on signals traveling into the device from external sources. The Smart I/O block sits between the GPIO pins and the high-speed I/O matrix (HSIOM) and is dedicated to a single port.

On PSoC 62, there are two Smart I/O blocks: one on Port 8 and one on Port 9. When the Smart I/O is not enabled, all signals on Port 8 and Port 9 bypass the Smart I/O hardware.

Smart I/O supports:

- Deep Sleep operation
- Boolean operations without CPU intervention
- Asynchronous or synchronous (clocked) operation

Each Smart I/O block contains a data unit (DU) and eight look up tables (LUTs).

The DU:

- Performs unique functions based on a selectable opcode.
- Can source input signals from internal resources, the GPIO port, or a value in the DU register.

Each LUT:

- Has three selectable input sources. The input signals may be sourced from another LUT, an internal resource, an external signal from a GPIO pin, or from the DU.
- Acts as a programmable Boolean logic table.
- Can be synchronous or asynchronous.

Fixed-Function Digital

Timer/Counter/Pulse-width Modulator (TCPWM)

- The TCPWM supports the following operational modes:
  - Timer-counter with compare
  - Timer-counter with capture
  - Quadrature decoding
  - Pulse width modulation (PWM)
  - Pseudo-random PWM
  - PWM with dead time
- Up, down, and up/down counting modes.
- Clock prescaling (division by 1, 2, 4, ... 64, 128)
- Double buffering of compare/capture and period values
- Underflow, overflow, and capture/compare output signals
- Supports interrupt on:
  - Terminal count – Depends on the mode; typically occurs on overflow or underflow
  - Capture/compare – The count is captured to the capture register or the counter value equals the value in the compare register
- Complementary output for PWMs
- Selectable start, reload, stop, count, and capture event signals for each TCPWM; with rising edge, falling edge, both edges,

and level trigger options. The TCPWM has a Kill input to force outputs to a predetermined state.

In this device there are:

- Eight 32-bit TCPWMs
- Twenty-four 16-bit TCPWMs

Serial Communication Blocks (SCB)

PSoC 62 has 13 SCBs:

- Eight can implement either I^2C, UART, or SPI.
- Four can be either UARTs or I^2C.
- One SCB can operate in Deep Sleep with an external clock, this SCB can be either SPI slave or I^2C slave.

I^2C Mode: The SCB can implement a full multi-master and slave interface (it is capable of multimaster arbitration). This block can operate at speeds of up to 1 Mbps (Fast Mode Plus). It also supports EzI2C that creates a mailbox address range in the memory of PSoC 63 and effectively reduces the I2C communication to reading from and writing to an array in the memory.The SCB supports a 256-byte FIFO for receive and transmit.

The I^2C peripheral is compatible with I^2C standard-mode, Fast Mode, and Fast Mode Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open-drain modes.

UART Mode: This is a full-feature UART operating at up to 8 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows the addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. A 256-byte FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI Secure Simple Pairing (SSP) (essentially adds a start pulse that is used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block supports an EzSPI mode in which the data interchange is reduced to reading and writing an array in memory. The SPI interface will operate with a 25-MHz SPI Clock.

USB Full-Speed Device Interface

PSoC 62 incorporates a full-speed USB device interface. The device can have up to eight endpoints. A 512-byte SRAM buffer is provided and DMA is supported.

Quad-SPI/Serial Memory Interface (SMIF)

A serial memory interface is provided, running at up to 80 MHz. It supports single, dual, quad, dual-quad and octal SPI configurations, and supports up to four external memory devices. It supports two modes of operation:

- Memory-mapped I/O (MMIO), a command mode interface that provides data access via the SMIF registers and FIFOs
- Execute in Place (XIP), in which AHB reads and writes are directly translated to SPI read and write transfers.

In XIP mode, the external memory is mapped into the PSoC 6 MCU internal address space, enabling code execution directly from the external memory. To improve performance, a 4-KB cache is included. XIP mode also supports AES-128 on-the-fly encryption and decryption, enabling secure storage and access of code and data in the external memory.

SDHC Controllers

PSoC 62 contains two secure digital host controllers (SDHC). The SDHC provides communication with IoT connectivity devices such as Bluetooth (BT), Bluetooth Low-Energy (BLE) and WiFi radios, as well as combination devices. The controller also supports embedded MultiMediaCards (eMMC) and Secure Digital (SD) cards.

Several bus speed modes under the SD specification are supported:

- DS (default speed)
- HS (high speed)
- SDR12 (single data rate)
- SDR25
- SDR50
- DDR50 (double data rate)

For eMMC, the supported modes are:

- BWC (backward compatibility)
- SDR
- DDR

Maximum clock restrictions and capacitive loads apply to some modes, and are also dependent on system power mode (LP/ULP). Consult the Electrical Specifications for details.

SDHC is configured as a master. To be fully compatible with features provided in the driver software for speed and efficiency, the SDHC supports advanced DMA version 3 (ADMA3), defined by the SDIO standard, and has a 1 KB RX/TX FIFO allowing double buffering of 512-byte blocks.

GPIO

PSoC 62 has up to 102 GPIOs. The GPIO block implements the following:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Hold mode for latching previous state (used for retaining the I/O state in system Hibernate mode)
- Selectable slew rates for dV/dt-related noise control to improve EMI

The pins are organized in logical entities called ports, which are up to 8-pin in width. During power-on and reset, the pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as the high-speed I/O matrix (HSIOM) is used to multiplex between various peripheral and analog signals that may connect to an I/O pin. Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled; each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it. Six GPIO pins are capable of overvoltage-tolerant (OVT) operation where the input voltage may be higher than V_{DD}. (These OVT pins are commonly used for the I^2C functionality to allow powering the chip OFF while maintaining a physical connection to an operating I^2C bus without affecting its functionality.)

GPIO pins can be ganged to source or sink higher values of current. GPIO pins, including OVT pins, may not be pulled up higher than 3.6 V.

Special-Function Peripherals

Audio Subsystem

This subsystem consists of the following hardware blocks:

- Two Inter-IC Sound (I^2S) interfaces
- Two pulse-density modulation to pulse-code modulation decoder channels

Each of the I^2S interfaces implements two independent hardware FIFO buffers – TX and RX, which can operate in master or slave mode. The following features are supported:

- Multiple data formats – I^2S, left-justified, Time Division Multiplexed (TDM) mode A, and TDM mode B
- Programmable channel/word lengths – 8/16/18/20/24/32 bits
- Internal/external clock operation. Up to 192 ksps
- Interrupt mask events – trigger, not empty, full, overflow, underflow, watchdog
- Configurable FIFO trigger level with DMA support

The I^2S interface is commonly used to connect with audio codecs, simple DACs, and digital microphones.

The PDM-to-PCM decoder implements a single hardware RX FIFO that decodes a stereo or mono 1-bit PDM input stream to PCM data output. The following features are supported:

- Programmable data output word length – 16/18/20/24 bits
- Programmable gain amplifier (PGA) for volume control – from –12 dB to +10.5 dB in 1.5 dB steps
- Configurable PDM clock generation. Range from 384 kHz to 3.072 MHz
- Droop correction and configurable decimation rate for sampling; up to 48 ksps
- Programmable high-pass filter gain
- Interrupt mask events – not empty, overflow, trigger, underflow
- Configurable FIFO trigger level with DMA support

The PDM-to-PCM decoder is commonly used to connect to digital PDM microphones. Up to two microphones can be connected to the same PDM Data line.

CapSense Subsystem

CapSense is supported in PSoC 6 MCU through a CapSense sigma-delta (CSD) hardware block. It is designed for high-sensitivity self-capacitance and mutual-capacitance measurements, and is specifically built for user interface solutions.

In addition to CapSense, the CSD hardware block supports three general-purpose functions. These are available when CapSense is not being used. Alternatively, two or more functions can be time-multiplexed in an application under firmware control. The four functions supported by the CSD hardware block are:

- CapSense
- 10-bit ADC
- Programmable current sources (IDAC)
- Comparator

CapSense

Capacitive touch sensors are designed for user interfaces that rely on human body capacitance to detect the presence of a finger on or near a sensor. Cypress CapSense solutions bring elegant, reliable, and simple capacitive touch sensing functions to applications including IoT, industrial, automotive, and home appliances.

The Cypress-proprietary CapSense technology offers the following features:

- Best-in-class signal-to-noise ratio (SNR) and robust sensing under harsh and noisy conditions
- Self-capacitance (CSD) and mutual-capacitance (CSX) sensing methods
- Support for various widgets, including buttons, matrix buttons, sliders, touchpads, and proximity sensors
- High-performance sensing across a variety of materials
- Best-in-class liquid tolerance
- SmartSense™ auto-tuning technology that helps avoid complex manual tuning processes
- Superior immunity against external noise
- Spread-spectrum clocks for low radiated emissions
- Gesture and built-in self-test libraries
- Ultra-low power consumption
- An integrated graphical CapSense tuner for real-time tuning, testing, and debugging

ADC

The CapSense subsystem slope ADC offers the following features:

- Selectable 8- or 10-bit resolution
- Selectable input range: GND to V_{REF} and GND to V_{DDA} on any GPIO input
- Measurement of V_{DDA} against an internal reference without the use of GPIO or external components

IDAC

The CSD block has two programmable current sources, which offer the following features:

- 7-bit resolution
- Sink and source current modes
- A current source programmable from 37.5 nA to 609 µA
- Two IDACs that can be used in parallel to form one 8-bit IDAC

Comparator

The CapSense subsystem comparator operates in the System Low Power and Ultra-Low Power modes. The inverting input is connected to an internal programmable reference voltage and the non-inverting input can be connected to any GPIO via the AMUXBUS.

CapSense Hardware Subsystem

Figure 5 shows the high-level hardware overview of the CapSense subsystem, which includes a delta sigma converter, internal clock dividers, a shield driver, and two programmable current sources.

The inputs are managed through analog multiplexed buses (AMUXBUS A/B). The input and output of all functions offered by the CSD block can be provided on any GPIO or on a group of GPIOs under software control, with the exception of the comparator output and external capacitors that use dedicated GPIOs.

Self-capacitance is supported by the CSD block using AMUXBUS A, an external modulator capacitor, and a GPIO for each sensor. There is a shield electrode (optional) for self-capacitance sensing. This is supported using AMUXBUS B and an optional external shield tank capacitor (to increase the drive capability of the shield driver) should this be required. Mutual-capacitance is supported by the CSD block using AMUXBUS A, two external integrated capacitors, and a GPIO for transmit and receive electrodes.

The ADC does not require an external component. Any GPIO that can be connected to AMUXBUS A can be an input to the ADC under software control. The ADC can accept V_{DDA} as an input without needing GPIOs (for applications such as battery voltage measurement).

The two programmable current sources (IDACs) in general-purpose mode can be connected to AMUXBUS A or B. They can therefore connect to any GPIO pin. The comparator resides in the delta-sigma converter. The inverting input is connected to VREF, with output on dedicated GPIO. The non-inverting input and output is accessible on any GPIO using AMUXBUS.

The CSD block can operate in active and sleep CPU power modes, and seamlessly transition between LP and ULP system modes. It can be powered down in Deep Sleep and Hibernate modes. Upon wakeup from Hibernate mode, the CSD block requires re-initialization. However, operation can be resumed without re-initialization upon exit from Deep Sleep mode, under firmware control.

Figure 5. CapSense Hardware Subsystem

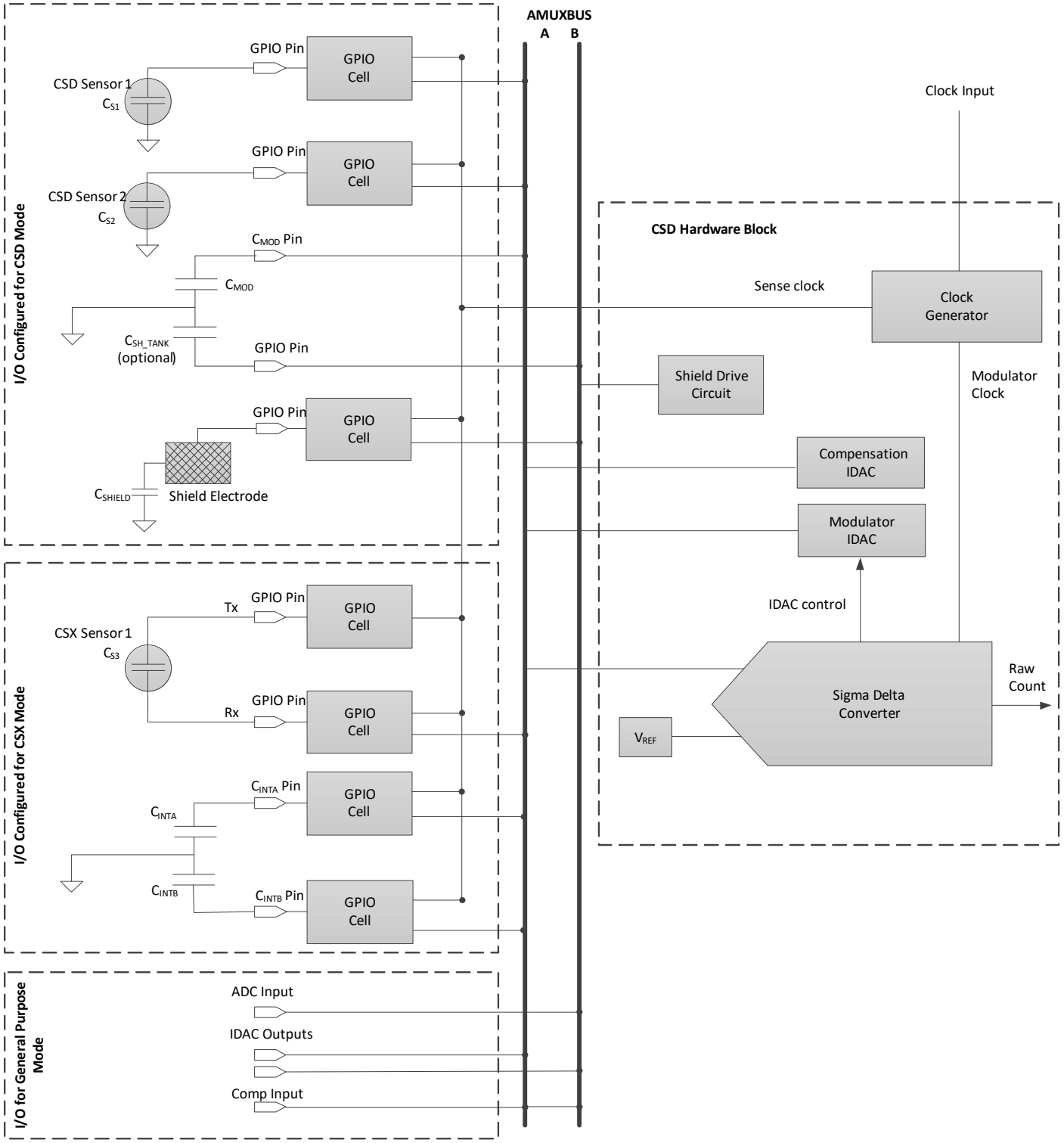


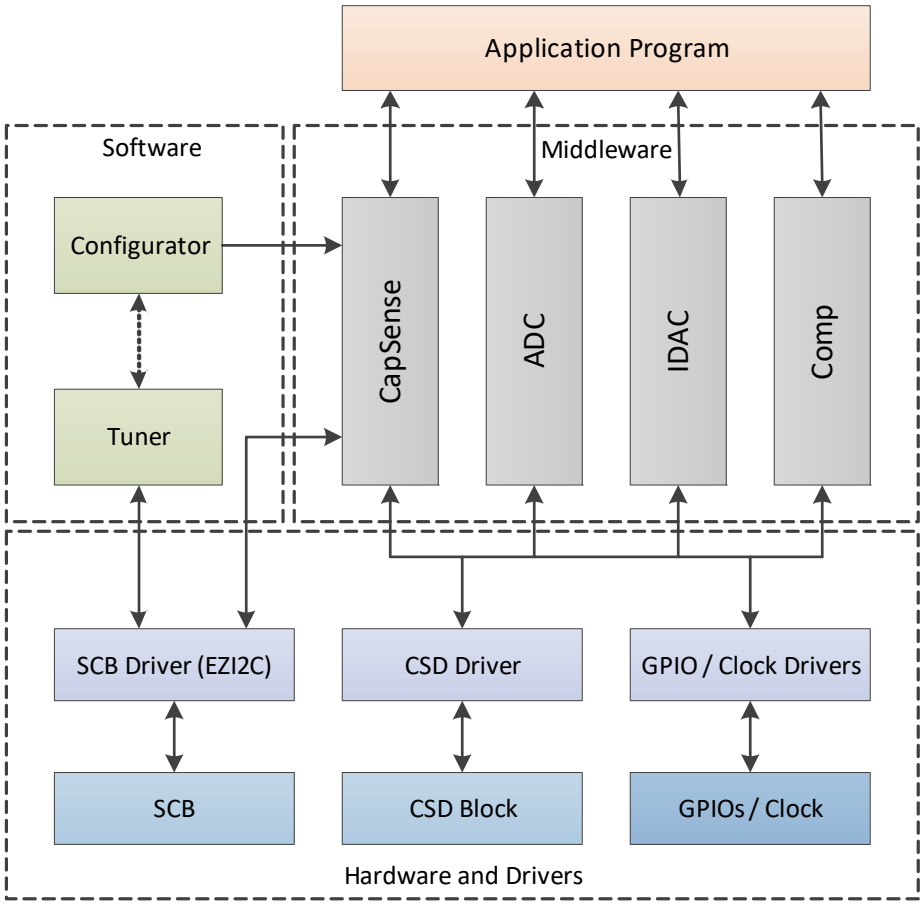
Figure 6 shows the high-level software overview. Cypress provides a middleware library for each function to enable quick integration. User applications interact only with middleware to implement functions of the CSD block. The middleware interacts with underlying drivers to access hardware as necessary. The CSD driver facilitates time-multiplexing of the CSD hardware if more than one piece of CSD-related middleware is present in a project. It prevents access conflicts in this case.

CapSense middleware has configurator software to enable fast configuration and incorporating it into middleware. It also has a tuner for performance evaluation and real-time tuning of the system. Both can be launched from the ModusToolbox IDE or in standalone mode. The tuner requires the EZ12C communication interface in the application to enable real-time tuning capability. The tuner can update configuration parameters directly in the device as well as in the configurator.

CapSense and ADC middleware use the CSD interrupt to implement non-blocking sensing and A-to-D conversion. Therefore, interrupt service routines are a defined part of the middleware, which must be initialized by the application. For dual-CPU devices, middleware and drivers can operate on either CPU. Cypress recommends using the middleware only in one CPU. If both CPUs must access the CSD driver, memory access should be managed in the application.

Refer to AN85951: PSoC 4 and PSoC 6 MCU CapSense Design Guide for more details on CSX sensing, CSD sensing, shield electrode usage and its benefits, and capacitive system design guidelines. Refer to the middleware API reference guide available in the PSoC 6 SDK for more detail on middleware.

Figure 6. CapSense Software/Firmware Subsystem



Pinouts

Note: Balls K2 and K3 are connected together internally in the package.

For ease of use, the CY8C62x8 and CY8C62xA datasheet web page contains a spreadsheet with the consolidated list of pin functions.

Table 4. PSoC 62 Pinouts

128-TQFP		124-BGA		100-WLCSP	
Pin	Name	Pin	Name	Pin	Name
4	VCCD	A2	VCCD	C15	VCCD
5	VCCD	A2	VCCD	C15	VCCD
6	VDDD	A1	VDDD	D14	VDDD
7	VSSQ	B12,C3,D4,D10,K4,K10	VSS	E13	VSS
8	VSSD0	B12,C3,D4,D10,K4,K10	VSS	E13	VSS
9	VBACKUP	D1	VBACKUP	C17	VBACKUP
10	P0.0	E3	P0.0	F14	P0.0
11	P0.1	E2	P0.1	G13	P0.1
12	P0.2	E1	P0.2	D16	P0.2
13	P0.3	F3	P0.3	E15	P0.3
14	P0.4	F2	P0.4	G11	P0.4
15	P0.5	G3	P0.5	F16	P0.5
16	XRES	F1	XRES	E17	XRES
17	P1.0	G2	P1.0	H12	P1.0
18	P1.1	G1	P1.1	G15	P1.1
19	P1.2	H3	P1.2		
20	P1.3	H2	P1.3		
21	P1.4	H1	P1.4	H14	P1.4
22	P1.5	J3	P1.5	G17	P1.5
23	VDD_NS	J1	VDD_NS	J15	VDD_NS
24	VIND1	J2	VIND1	H16	VIND1
25	VSS_NS	B12,C3,D4,D10,K4,K10	VSS	J13	VSS
26	VSSD1	B12,C3,D4,D10,K4,K10	VSS	J13	VSS
27	VDDUSB	M1	VDDUSB	J17	VDDUSB
28	USBDM	L1	USBDM	K16	USBDM
29	USBDP	L2	USBDP	K14	USBDP
30	P2.0	M2	P2.0	L17	P2.0
31	P2.1	N2	P2.1	K12	P2.1
32	P2.2	L3	P2.2	L15	P2.2
33	P2.3	M3	P2.3	L13	P2.3
34	P2.4	N3	P2.4	L11	P2.4
35	P2.5	N1	P2.5	M16	P2.5
37	P2.6	M4	P2.6	M14	P2.6
38	P2.7	N4	P2.7	M12	P2.7
39	VDDIO2	L4	VDDIO2	M10	VDDIO2

Table 4. PSoC 62 Pinouts *(continued)*

128-TQFP		124-BGA		100-WLCSP	
Pin	Name	Pin	Name	Pin	Name
40	VSSIO2	B12,C3,D4,D10,K4,K10	VSS	J13	VSS
41	P3.0	L5	P3.0		
42	P3.1	M5	P3.1		
43	P3.2	N5	P3.2		
44	P3.3	L6	P3.3		
45	P3.4	M6	P3.4		
46	P3.5	N6	P3.5		
47	P4.0	L7	P4.0		
48	P4.1	M7	P4.1		
49	P4.2				
50	P4.3				
51	P5.0	N7	P5.0	M8	P5.0
52	P5.1	L8	P5.1	K10	P5.1
53	P5.2	M8	P5.2	J11	P5.2
54	P5.3	N8	P5.3	H10	P5.3
55	P5.4	L9	P5.4	L9	P5.4
56	P5.5	M9	P5.5	M6	P5.5
57	P5.6	N9	P5.6	G9	P5.6
58	P5.7	N10	P5.7	G7	P5.7
59	P6.0	M10	P6.0	M4	P6.0
60	P6.1	L10	P6.1	L7	P6.1
61	P6.2	L11	P6.2	L5	P6.2
62	P6.3	M11	P6.3	K8	P6.3
63	P6.4	N11	P6.4	J9	P6.4
64	P6.5	M12	P6.5	L3	P6.5
65	P6.6	N12	P6.6	M2	P6.6
66	P6.7	M13	P6.7	K4	P6.7
67	VSSIO1	B12,C3,D4,D10,K4,K10	VSS	L1	VSS
68	VDDIO1	K12	VDDIO1	K2	VDDIO1
69	VDDA_CSD	A12	VDDA	J1	VDDA
70	VSSA_CSD	B12,C3,D4,D10,K4,K10	VSS	D2	VSS
71	P7.0	L13	P7.0	K6	P7.0
72	P7.1	L12	P7.1	J7	P7.1
73	P7.2	K13	P7.2	J3	P7.2
74	P7.3	N13	P7.3	H8	P7.3
75	P7.4	K11	P7.4		
76	P7.5	J13	P7.5		
77	P7.6	J12	P7.6		
78	P7.7	J11	P7.7	G1	P7.7

Table 4. PSoC 62 Pinouts *(continued)*

128-TQFP		124-BGA		100-WLCSP	
Pin	Name	Pin	Name	Pin	Name
79	P8.0	H13	P8.0	H2	P8.0
80	P8.1	H12	P8.1	J5	P8.1
81	P8.2	H11	P8.2	H6	P8.2
82	P8.3	G13	P8.3	H4	P8.3
83	P8.4	G12	P8.4	F2	P8.4
84	P8.5	G11	P8.5		
85	P8.6	F13	P8.6		
86	P8.7	F12	P8.7		
87	P9.0	E11	P9.0	E1	P9.0
88	P9.1	E12	P9.1	G3	P9.1
89	P9.2	E13	P9.2	G5	P9.2
90	P9.3	F11	P9.3	F4	P9.3
91	P9.4	D13	P9.4	E3	P9.4
92	P9.5	D12	P9.5		
93	P9.6	D11	P9.6		
94	P9.7	C13	P9.7	C1	P9.7
95	VSSA	B12,C3,D4,D10,K4,K10	VSS	D2	VSS
96	VDDA	A13	VDDIOA	J1	VDDA
97	VREF	B13	VREF	C3	VREF
98	P10.0	C12	P10.0	F6	P10.0
99	P10.1	A11	P10.1	E5	P10.1
100	P10.2	B11	P10.2	B2	P10.2
101	P10.3	C11	P10.3	D4	P10.3
102	P10.4	A10	P10.4	C5	P10.4
103	P10.5	B10	P10.5	B4	P10.5
104	P10.6	C10	P10.6	A3	P10.6
105	P10.7	A9	P10.7	F8	P10.7
106	P11.0	B9	P11.0	E9	P11.0
107	P11.1	C9	P11.1	D6	P11.1
108	P11.2	A8	P11.2	E7	P11.2
109	P11.3	B8	P11.3	A7	P11.3
110	P11.4	C8	P11.4	B6	P11.4
111	P11.5	A7	P11.5	A5	P11.5
112	P11.6	B7	P11.6	C7	P11.6
113	P11.7	C7	P11.7	B8	P11.7
114	VDDIO0	C4	VDDIO0	A11	VDDIO0
114	VDDIO0	C4	VDDIO0	A11	VDDIO0
115	VSSIO0	B12,C3,D4,D10,K4,K10	VSS	E13	VSS
116	P12.0	A6	P12.0	A9	P12.0

Table 4. PSoC 62 Pinouts *(continued)*

128-TQFP		124-BGA		100-WLCSP	
Pin	**Name**	**Pin**	**Name**	**Pin**	**Name**
117	P12.1	B6	P12.1	D8	P12.1
118	P12.2	C6	P12.2	A13	P12.2
119	P12.3	A5	P12.3	B10	P12.3
120	P12.4	B5	P12.4	C9	P12.4
121	P12.5	C5	P12.5	B12	P12.5
122	P12.6	A4	P12.6	C11	P12.6
123	P12.7	B4	P12.7	D10	P12.7
124	P13.0	B1	P13.0	B14	P13.0
125	P13.1	A3	P13.1	A15	P13.1
126	P13.2	B3	P13.2	C13	P13.2
127	P13.3	B2	P13.3	D12	P13.3
128	P13.4	C2	P13.4	E11	P13.4
1	P13.5	C1	P13.5	F10	P13.5
2	P13.6	D3	P13.6	F12	P13.6
3	P13.7	D2	P13.7	B16	P13.7
36	VSS	K1	DNC[1]		
		K2	DNC[1]		
		K3	DNC[1]		

Note
1. DNC means Do Not Connect. Do Not Connect anything to these pins.

Power supplies and ports correspond as follows:

- P0: VBACKUP
- P1: VDDD. Port 1 GPIO pins are overvoltage-tolerant (OVT).
- P2, P3, P4: VDDIO2
- P5, P6, P7, P8: VDDIO1
- P9, P10: VDDIO, VDDA (VDDIOA, when present, and VDDA must be connected together on the PCB)
- P11, P12, P13: VDDIO0

Each port pin has multiple alternate functions. These are defined in Table 5. The columns ACT #x and DS #y denote active (System LP/ULP) and Deep Sleep mode signals respectively.

The notation for a signal is of the form IPName[x].signal_name[u]:y.

IPName = Name of the block (such as tcpwm), x = Unique instance of the IP, Signal_name = Name of the signal, u = Signal number where there is more than one signal for a particular signal name, y = Designates copies of the signal name.

For example, the name tcpwm[0].line_compl[3]:4 indicates that this is instance 0 of a tcpwm block, the signal is line_compl # 3 (complement of the line output) and this is the fourth occurrence (copy) of the signal. Signal copies are provided to allow flexibility in routing and to maximize use of on-chip resources.

For ease of use, the CY8C62x8 and CY8C62xA datasheet web page contains a spreadsheet with the consolidated list of pin functions.

Table 5. Multiple Alternate Functions

Port/ Pin	ACT #0	ACT #1	ACT #2	ACT #3	DS #2	DS #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #5	DS #6
P0.0	tcpwm[0].line[0]:0	tcpwm[1].line[0]:0	csd.csd_tx:0	csd.csd_tx_n:0			srss.ext_clk:0				scb[0].spi_select1:0			peri.tr_io_input[0]:0					
P0.1	tcpwm[0].line_compl[0]:0	tcpwm[1].line_compl[0]:0	csd.csd_tx:1	csd.csd_tx_n:1							scb[0].spi_select2:0			peri.tr_io_input[1]:0				cpuss.swj_trstn	
P0.2	tcpwm[0].line[1]:0	tcpwm[1].line[1]:0	csd.csd_tx:2	csd.csd_tx_n:2					scb[0].uart_rx:0	scb[0].i2c_scl:0	scb[0].spi_mosi:0								
P0.3	tcpwm[0].line_compl[1]:0	tcpwm[1].line_compl[1]:0	csd.csd_tx:3	csd.csd_tx_n:3					scb[0].uart_tx:0	scb[0].i2c_sda:0	scb[0].spi_miso:0								
P0.4	tcpwm[0].line[2]:0	tcpwm[1].line[2]:0	csd.csd_tx:4	csd.csd_tx_n:4					scb[0].uart_rts:0		scb[0].spi_clk:0				peri.tr_io_output[0]:2				
P0.5	tcpwm[0].line_compl[2]:0	tcpwm[1].line_compl[2]:0	csd.csd_tx:5	csd.csd_tx_n:5			srss.ext_clk:1		scb[0].uart_cts:0		scb[0].spi_select0:0				peri.tr_io_output[1]:2				

Table 5. Multiple Alternate Functions *(continued)*

Port/ Pin	ACT #0	ACT #1	ACT #2	ACT #3	DS #2	DS #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #5	DS #6
P1.0	tcpwm[0].line[3]:0	tcpwm[1].line[3]:0	csd.csd_tx:6	csd.csd_tx_n:6					scb[7].uart_rx:0	scb[7].i2c_scl:0	scb[7].spi_mosi:0			peri.tr_io_input[2]:0					
P1.1	tcpwm[0].line_compl[3]:0	tcpwm[1].line_compl[3]:0	csd.csd_tx:7	csd.csd_tx_n:7					scb[7].uart_tx:0	scb[7].i2c_sda:0	scb[7].spi_miso:0			peri.tr_io_input[3]:0					
P1.2	tcpwm[0].line[4]:4	tcpwm[1].line[12]:1	csd.csd_tx:8	csd.csd_tx_n:8					scb[7].uart_rts:0		scb[7].spi_clk:0								
P1.3	tcpwm[0].line_compl[4]:4	tcpwm[1].line_compl[12]:1	csd.csd_tx:9	csd.csd_tx_n:9					scb[7].uart_cts:0		scb[7].spi_select0:0								
P1.4	tcpwm[0].line[5]:4	tcpwm[1].line[13]:1	csd.csd_tx:10	csd.csd_tx_n:10							scb[7].spi_select1:0								
P1.5	tcpwm[0].line_compl[5]:4	tcpwm[1].line_compl[14]:1	csd.csd_tx:11	csd.csd_tx_n:11							scb[7].spi_select2:0								
P2.0	tcpwm[0].line[6]:4	tcpwm[1].line[15]:1	csd.csd_tx:12	csd.csd_tx_n:12					scb[1].uart_rx:0	scb[1].i2c_scl:0	scb[1].spi_mosi:0			peri.tr_io_input[4]:0		sdhc[0].card_dat_3to0[0]			
P2.1	tcpwm[0].line_compl[6]:4	tcpwm[1].line_compl[15]:1	csd.csd_tx:13	csd.csd_tx_n:13					scb[1].uart_tx:0	scb[1].i2c_sda:0	scb[1].spi_miso:0			peri.tr_io_input[5]:0		sdhc[0].card_dat_3to0[1]			
P2.2	tcpwm[0].line[7]:4	tcpwm[1].line[16]:1	csd.csd_tx:14	csd.csd_tx_n:14					scb[1].uart_rts:0		scb[1].spi_clk:0					sdhc[0].card_dat_3to0[2]			
P2.3	tcpwm[0].line_compl[7]:4	tcpwm[1].line_compl[16]:1	csd.csd_tx:15	csd.csd_tx_n:15					scb[1].uart_cts:0		scb[1].spi_select0:0					sdhc[0].card_dat_3to0[3]			
P2.4	tcpwm[0].line[0]:5	tcpwm[1].line[17]:1	csd.csd_tx:16	csd.csd_tx_n:16					scb[9].uart_rx:0	scb[9].i2c_scl:0	scb[1].spi_select1:0					sdhc[0].card_cmd			
P2.5	tcpwm[0].line_compl[0]:5	tcpwm[1].line_compl[17]:1	csd.csd_tx:17	csd.csd_tx_n:17					scb[9].uart_tx:0	scb[9].i2c_sda:0	scb[1].spi_select2:0					sdhc[0].clk_card			
P2.6	tcpwm[0].line[1]:5	tcpwm[1].line[18]:1	csd.csd_tx:18	csd.csd_tx_n:18					scb[9].uart_rts:0		scb[1].spi_select3:0					sdhc[0].card_detect_n			

Table 5. Multiple Alternate Functions *(continued)*

Port/ Pin	ACT #0	ACT #1	ACT #2	ACT #3	DS #2	DS #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #5	DS #6
P2.7	tcpwm[0].line_compl[1]:5	tcpwm[1].line_compl[18]:1	csd.csd_tx:19	csd.csd_tx_n:19					scb[9].uart_cts:0							sdhc[0].card_mech_write_prot			
P3.0	tcpwm[0].line[2]:5	tcpwm[1].line[19]:1	csd.csd_tx:20	csd.csd_tx_n:20					scb[2].uart_rx:1	scb[2].i2c_scl:1	scb[2].spi_mosi:1			peri.tr_io_input[6]:0		sdhc[0].io_volt_sel			
P3.1	tcpwm[0].line_compl[2]:5	tcpwm[1].line_compl[19]:1	csd.csd_tx:21	csd.csd_tx_n:21					scb[2].uart_tx:1	scb[2].i2c_sda:1	scb[2].spi_miso:1			peri.tr_io_input[7]:0		sdhc[0].card_if_pwr_en			
P3.2	tcpwm[0].line[3]:5	tcpwm[1].line[20]:1	csd.csd_tx:22	csd.csd_tx_n:22					scb[2].uart_rts:1		scb[2].spi_clk:1								
P3.3	tcpwm[0].line_compl[3]:5	tcpwm[1].line_compl[20]:1	csd.csd_tx:23	csd.csd_tx_n:23					scb[2].uart_cts:1		scb[2].spi_select0:1								
P3.4	tcpwm[0].line[4]:5	tcpwm[1].line[21]:1	csd.csd_tx:24	csd.csd_tx_n:24							scb[2].spi_select1:1								
P3.5	tcpwm[0].line_compl[4]:5	tcpwm[1].line_compl[21]:1	csd.csd_tx:25	csd.csd_tx_n:25							scb[2].spi_select2:1								
P4.0	tcpwm[0].line[5]:5	tcpwm[1].line[22]:1	csd.csd_tx:26	csd.csd_tx_n:26					scb[7].uart_rx:1	scb[7].i2c_scl:1	scb[7].spi_mosi:1			peri.tr_io_input[8]:0					
P4.1	tcpwm[0].line_compl[5]:5	tcpwm[1].line_compl[22]:1	csd.csd_tx:27	csd.csd_tx_n:27					scb[7].uart_tx:1	scb[7].i2c_sda:1	scb[7].spi_miso:1			peri.tr_io_input[9]:0					
P4.2	tcpwm[0].line[6]:5	tcpwm[1].line[23]:1	csd.csd_tx:28	csd.csd_tx_n:28					scb[7].uart_rts:1		scb[7].spi_clk:1								
P4.3	tcpwm[0].line_compl[6]:5	tcpwm[1].line_compl[23]:1	csd.csd_tx:29	csd.csd_tx_n:29					scb[7].uart_cts:1		scb[7].spi_select0:1								
P5.0	tcpwm[0].line[4]:0	tcpwm[1].line[4]:0	csd.csd_tx:30	csd.csd_tx_n:30					scb[5].uart_rx:0	scb[5].i2c_scl:0	scb[5].spi_mosi:0		audioss[0].clk_i2s_if:0	peri.tr_io_input[10]:0					

Table 5. Multiple Alternate Functions *(continued)*

Port/ Pin	ACT #0	ACT #1	ACT #2	ACT #3	DS #2	DS #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #5	DS #6
P5.1	tcpwm[0].line_compl[4]:0	tcpwm[1].line_compl[4]:0	csd.csd_tx:31	csd.csd_tx_n:31					scb[5].uart_tx:0	scb[5].i2c_sda:0	scb[5].spi_miso:0		audioss[0].tx_sck:0	peri.tr_io_input[11]:0					
P5.2	tcpwm[0].line[5]:0	tcpwm[1].line[5]:0	csd.csd_tx:32	csd.csd_tx_n:32					scb[5].uart_rts:0		scb[5].spi_clk:0		audioss[0].tx_ws:0						
P5.3	tcpwm[0].line_compl[5]:0	tcpwm[1].line_compl[5]:0	csd.csd_tx:33	csd.csd_tx_n:33					scb[5].uart_cts:0		scb[5].spi_select0:0		audioss[0].tx_sdo:0						
P5.4	tcpwm[0].line[6]:0	tcpwm[1].line[6]:0	csd.csd_tx:34	csd.csd_tx_n:34					scb[10].uart_rx:0	scb[10].i2c_scl:0	scb[5].spi_select1:0		audioss[0].rx_sck:0						
P5.5	tcpwm[0].line_compl[6]:0	tcpwm[1].line_compl[6]:0	csd.csd_tx:35	csd.csd_tx_n:35					scb[10].uart_tx:0	scb[10].i2c_sda:0	scb[5].spi_select2:0		audioss[0].rx_ws:0						
P5.6	tcpwm[0].line[7]:0	tcpwm[1].line[7]:0	csd.csd_tx:36	csd.csd_tx_n:36					scb[10].uart_rts:0		scb[5].spi_select3:0		audioss[0].rx_sdi:0						
P5.7	tcpwm[0].line_compl[7]:0	tcpwm[1].line_compl[7]:0	csd.csd_tx:37	csd.csd_tx_n:37					scb[10].uart_cts:0		scb[3].spi_select3:0								
P6.0	tcpwm[0].line[0]:1	tcpwm[1].line[8]:0	csd.csd_tx:38	csd.csd_tx_n:38	scb[8].i2c_scl:0				scb[3].uart_rx:0	scb[3].i2c_scl:0	scb[3].spi_mosi:0				cpuss.fault_out[0]				scb[8].spi_mosi:0
P6.1	tcpwm[0].line_compl[0]:1	tcpwm[1].line_compl[8]:0	csd.csd_tx:39	csd.csd_tx_n:39	scb[8].i2c_sda:0				scb[3].uart_tx:0	scb[3].i2c_sda:0	scb[3].spi_miso:0				cpuss.fault_out[1]				scb[8].spi_miso:0
P6.2	tcpwm[0].line[1]:1	tcpwm[1].line[9]:0	csd.csd_tx:40	csd.csd_tx_n:40					scb[3].uart_rts:0		scb[3].spi_clk:0								scb[8].spi_clk:0
P6.3	tcpwm[0].line_compl[1]:1	tcpwm[1].line_compl[9]:0	csd.csd_tx:41	csd.csd_tx_n:41					scb[3].uart_cts:0		scb[3].spi_select0:0								scb[8].spi_select0:0
P6.4	tcpwm[0].line[2]:1	tcpwm[1].line[10]:0	csd.csd_tx:42	csd.csd_tx_n:42	scb[8].i2c_scl:1				scb[6].uart_rx:2	scb[6].i2c_scl:2	scb[6].spi_mosi:2			peri.tr_io_input[12]:0	peri.tr_io_output[0]:1			cpuss.swj_swo_tdo	scb[8].spi_mosi:1

Table 5. Multiple Alternate Functions *(continued)*

Port/ Pin	ACT #0	ACT #1	ACT #2	ACT #3	DS #2	DS #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #5	DS #6
P6.5	tcpwm[0].line_compl[2]:1	tcpwm[1].line_compl[10]:0	csd.csd_tx:43	csd.csd_tx_n:43	scb[8].i2c_sda:1				scb[6].uart_tx:2	scb[6].i2c_sda:2	scb[6].spi_miso:2			peri.tr_io_input[13]:0	peri.tr_io_output[1]:1			cpuss.swj_swdoe_tdi	scb[8].spi_miso:1
P6.6	tcpwm[0].line[3]:1	tcpwm[1].line[11]:0	csd.csd_tx:44	csd.csd_tx_n:44					scb[6].uart_rts:2		scb[6].spi_clk:2							cpuss.swj_swdio_tms	scb[8].spi_clk:1
P6.7	tcpwm[0].line_compl[3]:1	tcpwm[1].line_compl[11]:0	csd.csd_tx:45	csd.csd_tx_n:45					scb[6].uart_cts:2		scb[6].spi_select0:2							cpuss.swj_swclk_tclk	scb[8].spi_select0:1
P7.0	tcpwm[0].line[4]:1	tcpwm[1].line[12]:0	csd.csd_tx:46	csd.csd_tx_n:46					scb[4].uart_rx:1	scb[4].i2c_scl:1	scb[4].spi_mosi:1			peri.tr_io_input[14]:0		cpuss.trace_clock			
P7.1	tcpwm[0].line_compl[4]:1	tcpwm[1].line_compl[12]:0	csd.csd_tx:47	csd.csd_tx_n:47					scb[4].uart_tx:1	scb[4].i2c_sda:1	scb[4].spi_miso:1			peri.tr_io_input[15]:0					
P7.2	tcpwm[0].line[5]:1	tcpwm[1].line[13]:0	csd.csd_tx:48	csd.csd_tx_n:48					scb[4].uart_rts:1		scb[4].spi_clk:1								
P7.3	tcpwm[0].line_compl[5]:1	tcpwm[1].line_compl[13]:0	csd.csd_tx:49	csd.csd_tx_n:49					scb[4].uart_cts:1		scb[4].spi_select0:1								
P7.4	tcpwm[0].line[6]:1	tcpwm[1].line[14]:0	csd.csd_tx:50	csd.csd_tx_n:50							scb[4].spi_select1:1						cpuss.trace_data[3]:2		
P7.5	tcpwm[0].line_compl[6]:1	tcpwm[1].line_compl[14]:0	csd.csd_tx:51	csd.csd_tx_n:51							scb[4].spi_select2:1						cpuss.trace_data[2]:2		
P7.6	tcpwm[0].line[7]:1	tcpwm[1].line[15]:0	csd.csd_tx:52	csd.csd_tx_n:52							scb[4].spi_select3:1						cpuss.trace_data[1]:2		
P7.7	tcpwm[0].line_compl[7]:1	tcpwm[1].line_compl[15]:0	csd.csd_tx:53	csd.csd_tx_n:53							scb[3].spi_select1:0	cpuss.clk_fm_pump					cpuss.trace_data[0]:2		
P8.0	tcpwm[0].line[0]:2	tcpwm[1].line[16]:0	csd.csd_tx:54	csd.csd_tx_n:54					scb[4].uart_rx:0	scb[4].i2c_scl:0	scb[4].spi_mosi:0			peri.tr_io_input[16]:0					

Table 5. Multiple Alternate Functions *(continued)*

Port/ Pin	ACT #0	ACT #1	ACT #2	ACT #3	DS #2	DS #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #5	DS #6
P8.1	tcpwm[0].line_compl[0]:2	tcpwm[1].line_compl[16]:0	csd.csd_tx:55	csd.csd_tx_n:55					scb[4].uart_tx:0	scb[4].i2c_sda:0	scb[4].spi_miso:0			peri.tr_io_input[17]:0					
P8.2	tcpwm[0].line[1]:2	tcpwm[1].line[17]:0	csd.csd_tx:56	csd.csd_tx_n:56		lpcomp.dsi_comp0:0			scb[4].uart_rts:0		scb[4].spi_clk:0								
P8.3	tcpwm[0].line_compl[1]:2	tcpwm[1].line_compl[17]:0	csd.csd_tx:57	csd.csd_tx_n:57		lpcomp.dsi_comp1:0			scb[4].uart_cts:0		scb[4].spi_select0:0								
P8.4	tcpwm[0].line[2]:2	tcpwm[1].line[18]:0	csd.csd_tx:58	csd.csd_tx_n:58					scb[11].uart_rx:0	scb[11].i2c_scl:0	scb[4].spi_select1:0								
P8.5	tcpwm[0].line_compl[2]:2	tcpwm[1].line_compl[18]:0	csd.csd_tx:59	csd.csd_tx_n:59					scb[11].uart_tx:0	scb[11].i2c_sda:0	scb[4].spi_select2:0								
P8.6	tcpwm[0].line[3]:2	tcpwm[1].line[19]:0	csd.csd_tx:60	csd.csd_tx_n:60					scb[11].uart_rts:0		scb[4].spi_select3:0								
P8.7	tcpwm[0].line_compl[3]:2	tcpwm[1].line_compl[19]:0	csd.csd_tx:61	csd.csd_tx_n:61					scb[11].uart_cts:0		scb[3].spi_select2:0								
P9.0	tcpwm[0].line[4]:2	tcpwm[1].line[20]:0	csd.csd_tx:62	csd.csd_tx_n:62					scb[2].uart_rx:0	scb[2].i2c_scl:0	scb[2].spi_mosi:0		audioss[0].clk_i2s_if:1	peri.tr_io_input[18]:0			cpuss.trace_data[3]:0		
P9.1	tcpwm[0].line_compl[4]:2	tcpwm[1].line_compl[20]:0	csd.csd_tx:63	csd.csd_tx_n:63					scb[2].uart_tx:0	scb[2].i2c_sda:0	scb[2].spi_miso:0		audioss[0].tx_sck:1	peri.tr_io_input[19]:0			cpuss.trace_data[2]:0		
P9.2	tcpwm[0].line[5]:2	tcpwm[1].line[21]:0	csd.csd_tx:64	csd.csd_tx_n:64					scb[2].uart_rts:0		scb[2].spi_clk:0		audioss[0].tx_ws:1				cpuss.trace_data[1]:0		
P9.3	tcpwm[0].line_compl[5]:2	tcpwm[1].line_compl[21]:0	csd.csd_tx:65	csd.csd_tx_n:65					scb[2].uart_cts:0		scb[2].spi_select0:0		audioss[0].tx_sdo:1				cpuss.trace_data[0]:0		
P9.4	tcpwm[0].line[7]:5	tcpwm[1].line[0]:2	csd.csd_tx:66	csd.csd_tx_n:66							scb[2].spi_select1:0		audioss[0].rx_sck:1						

Table 5. Multiple Alternate Functions *(continued)*

Port/ Pin	ACT #0	ACT #1	ACT #2	ACT #3	DS #2	DS #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #5	DS #6
P9.5	tcpwm[0].line_compl[7]:5	tcpwm[1].line_compl[0]:2	csd.csd_tx:67	csd.csd_tx_n:67							scb[2].spi_select2:0		audioss[0].rx_ws:1						
P9.6	tcpwm[0].line[0]:6	tcpwm[1].line[1]:2	csd.csd_tx:68	csd.csd_tx_n:68							scb[2].spi_select3:0		audioss[0].rx_sdi:1						
P9.7	tcpwm[0].line_compl[0]:6	tcpwm[1].line_compl[1]:2	csd.csd_tx:69	csd.csd_tx_n:69															
P10.0	tcpwm[0].line[6]:2	tcpwm[1].line[22]:0	csd.csd_tx:70	csd.csd_tx_n:70					scb[1].uart_rx:1	scb[1].i2c_scl:1	scb[1].spi_mosi:1			peri.tr_io_input[20]:0			cpuss.trace_data[3]:1		
P10.1	tcpwm[0].line_compl[6]:2	tcpwm[1].line_compl[22]:0	csd.csd_tx:71	csd.csd_tx_n:71					scb[1].uart_tx:1	scb[1].i2c_sda:1	scb[1].spi_miso:1			peri.tr_io_input[21]:0			cpuss.trace_data[2]:1		
P10.2	tcpwm[0].line[7]:2	tcpwm[1].line[23]:0	csd.csd_tx:72	csd.csd_tx_n:72					scb[1].uart_rts:1		scb[1].spi_clk:1						cpuss.trace_data[1]:1		
P10.3	tcpwm[0].line_compl[7]:2	tcpwm[1].line_compl[23]:0	csd.csd_tx:73	csd.csd_tx_n:73					scb[1].uart_cts:1		scb[1].spi_select0:1						cpuss.trace_data[0]:1		
P10.4	tcpwm[0].line[0]:3	tcpwm[1].line[0]:1	csd.csd_tx:74	csd.csd_tx_n:74							scb[1].spi_select1:1	audioss[0].pdm_clk:0							
P10.5	tcpwm[0].line_compl[0]:3	tcpwm[1].line_compl[0]:1	csd.csd_tx:75	csd.csd_tx_n:75							scb[1].spi_select2:1	audioss[0].pdm_data:0							
P10.6	tcpwm[0].line[1]:6	tcpwm[1].line[2]:2	csd.csd_tx:76	csd.csd_tx_n:76							scb[1].spi_select3:1								
P10.7	tcpwm[0].line_compl[1]:6	tcpwm[1].line_compl[2]:2	csd.csd_tx:77	csd.csd_tx_n:77															
P11.0	tcpwm[0].line[1]:3	tcpwm[1].line[1]:1	csd.csd_tx:78	csd.csd_tx_n:78				smif.spi_select2	scb[5].uart_rx:1	scb[5].i2c_scl:1	scb[5].spi_mosi:1		audioss[1].clk_i2s_if:1	peri.tr_io_input[22]:0					
P11.1	tcpwm[0].line_compl[1]:3	tcpwm[1].line_compl[1]:1	csd.csd_tx:79	csd.csd_tx_n:79				smif.spi_select1	scb[5].uart_tx:1	scb[5].i2c_sda:1	scb[5].spi_miso:1		audioss[1].tx_sck:1	peri.tr_io_input[23]:0					

Table 5. Multiple Alternate Functions *(continued)*

Port/ Pin	ACT #0	ACT #1	ACT #2	ACT #3	DS #2	DS #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #5	DS #6
P11.2	tcpwm[0].line[2]:3	tcpwm[1].line[2]:1	csd.csd_tx:80	csd.csd_tx_n:80				smif.spi_select0	scb[5].uart_rts:1		scb[5].spi_clk:1		audioss[1].tx_ws:1						
P11.3	tcpwm[0].line_compl[2]:3	tcpwm[1].line_compl[2]:1	csd.csd_tx:81	csd.csd_tx_n:81				smif.spi_data3	scb[5].uart_cts:1		scb[5].spi_select0:1		audioss[1].tx_sdo:1		peri.tr_io_output[0]:0				
P11.4	tcpwm[0].line[3]:3	tcpwm[1].line[3]:1	csd.csd_tx:82	csd.csd_tx_n:82				smif.spi_data2			scb[5].spi_select1:1		audioss[1].rx_sck:1		peri.tr_io_output[1]:0				
P11.5	tcpwm[0].line_compl[3]:3	tcpwm[1].line_compl[3]:1	csd.csd_tx:83	csd.csd_tx_n:83				smif.spi_data1			scb[5].spi_select2:1		audioss[1].rx_ws:1						
P11.6			csd.csd_tx:84	csd.csd_tx_n:84				smif.spi_data0			scb[5].spi_select3:1		audioss[1].rx_sdi:1						
P11.7								smif.spi_clk											
P12.0	tcpwm[0].line[4]:3	tcpwm[1].line[4]:1	csd.csd_tx:85	csd.csd_tx_n:85				smif.spi_data4	scb[6].uart_rx:0	scb[6].i2c_scl:0	scb[6].spi_mosi:0			peri.tr_io_input[24]:0		sdhc[1].card_emmc_reset_n			
P12.1	tcpwm[0].line_compl[4]:3	tcpwm[1].line_compl[4]:1	csd.csd_tx:86	csd.csd_tx_n:86				smif.spi_data5	scb[6].uart_tx:0	scb[6].i2c_sda:0	scb[6].spi_miso:0			peri.tr_io_input[25]:0		sdhc[1].card_detect_n			
P12.2	tcpwm[0].line[5]:3	tcpwm[1].line[5]:1	csd.csd_tx:87	csd.csd_tx_n:87				smif.spi_data6	scb[6].uart_rts:0		scb[6].spi_clk:0					sdhc[1].card_mech_write_prot			
P12.3	tcpwm[0].line_compl[5]:3	tcpwm[1].line_compl[5]:1	csd.csd_tx:88	csd.csd_tx_n:88				smif.spi_data7	scb[6].uart_cts:0		scb[6].spi_select0:0					sdhc[1].led_ctrl			
P12.4	tcpwm[0].line[6]:3	tcpwm[1].line[6]:1	csd.csd_tx:89	csd.csd_tx_n:89				smif.spi_select3			scb[6].spi_select1:0	audioss[0].pdm_clk:1				sdhc[1].card_cmd			

Table 5. Multiple Alternate Functions *(continued)*

Port/ Pin	ACT #0	ACT #1	ACT #2	ACT #3	DS #2	DS #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #5	DS #6
P12.5	tcpwm[0].line_compl[6]:3	tcpwm[1].line_compl[6]:1	csd.csd_tx:90	csd.csd_tx_n:90							scb[6].spi_select2:0	audioss[0].pdm_data:1				sdhc[1].clk_card			
P12.6	tcpwm[0].line[7]:3	tcpwm[1].line[7]:1	csd.csd_tx:91	csd.csd_tx_n:91							scb[6].spi_select3:0					sdhc[1].card_if_pwr_en			
P12.7	tcpwm[0].line_compl[7]:3	tcpwm[1].line_compl[7]:1	csd.csd_tx:92	csd.csd_tx_n:92												sdhc[1].io_volt_sel			
P13.0	tcpwm[0].line[0]:4	tcpwm[1].line[8]:1	csd.csd_tx:93	csd.csd_tx_n:93					scb[6].uart_rx:1	scb[6].i2c_scl:1	scb[6].spi_mosi:1		audioss[1].clk_i2s_if:0	peri.tr_io_input[26]:0		sdhc[1].card_dat_3to0[0]			
P13.1	tcpwm[0].line_compl[0]:4	tcpwm[1].line_compl[8]:1	csd.csd_tx:94	csd.csd_tx_n:94					scb[6].uart_tx:1	scb[6].i2c_sda:1	scb[6].spi_miso:1		audioss[1].tx_sck:0	peri.tr_io_input[27]:0		sdhc[1].card_dat_3to0[1]			
P13.2	tcpwm[0].line[1]:4	tcpwm[1].line[9]:1	csd.csd_tx:95	csd.csd_tx_n:95					scb[6].uart_rts:1		scb[6].spi_clk:1		audioss[1].tx_ws:0			sdhc[1].card_dat_3to0[2]			
P13.3	tcpwm[0].line_compl[1]:4	tcpwm[1].line_compl[9]:1	csd.csd_tx:96	csd.csd_tx_n:96					scb[6].uart_cts:1		scb[6].spi_select0:1		audioss[1].tx_sdo:0			sdhc[1].card_dat_3to0[3]			
P13.4	tcpwm[0].line[2]:4	tcpwm[1].line[10]:1	csd.csd_tx:97	csd.csd_tx_n:97					scb[12].uart_rx:0	scb[12].i2c_scl:0	scb[6].spi_select1:1		audioss[1].rx_sck:0			sdhc[1].card_dat_7to4[0]			
P13.5	tcpwm[0].line_compl[2]:4	tcpwm[1].line_compl[10]:1	csd.csd_tx:98	csd.csd_tx_n:98					scb[12].uart_tx:0	scb[12].i2c_sda:0	scb[6].spi_select2:1		audioss[1].rx_ws:0			sdhc[1].card_dat_7to4[1]			
P13.6	tcpwm[0].line[3]:4	tcpwm[1].line[11]:1	csd.csd_tx:99	csd.csd_tx_n:99					scb[12].uart_rts:0		scb[6].spi_select3:1		audioss[1].rx_sdi:0			sdhc[1].card_dat_7to4[2]			
P13.7	tcpwm[0].line_compl[3]:4	tcpwm[1].line_compl[11]:1	csd.csd_tx:100	csd.csd_tx_n:100					scb[12].uart_cts:0							sdhc[1].card_dat_7to4[3]			

Analog and Smart I/O alternate port pin functionality is provided in Table 6.

For ease of use, the CY8C62x8 and CY8C62xA datasheet web page contains a spreadsheet with the consolidated list of pin functions.

Table 6. Port Pin Analog, Digital, and Smart I/O Functions

Port/Pin	Analog
P0.0	wco_in
P0.1	wco_out
P5.6	lpcomp.inp_comp0
P5.7	lpcomp.inn_comp0
P6.2	lpcomp.inp_comp1
P6.3	lpcomp.inn_comp1
P6.6	swd_data
P6.7	swd_clk
P7.2	csd.csh_tank
P7.3	csd.vref_ext
P7.7	csd.shield
P9.7	aref_ext_vref
P10.0	sarmux_pads[0]
P10.1	sarmux_pads[1]
P10.2	sarmux_pads[2]
P10.3	sarmux_pads[3]
P10.4	sarmux_pads[4]
P10.5	sarmux_pads[5]
P10.6	sarmux_pads[6]
P10.7	sarmux_pads[7]
P12.6	eco_in
P12.7	eco_out

Table 6. Port Pin Analog, Digital, and Smart I/O Functions

Port/Pin	Digital
P0.4	pmic_wakeup_in hibernate_wakeup[1]
P1.4	hibernate_wakeup[0]
P0.5	pmic_wakeup_out
Port/Pin	**SMARTIO**
P8.0	smartio[8].io[0]
P8.1	smartio[8].io[1]
P8.2	smartio[8].io[2]
P8.3	smartio[8].io[3]
P8.4	smartio[8].io[4]
P8.5	smartio[8].io[5]
P8.6	smartio[8].io[6]
P8.7	smartio[8].io[7]
P9.0	smartio[9].io[0]
P9.1	smartio[9].io[1]
P9.2	smartio[9].io[2]
P9.3	smartio[9].io[3]
P9.4	smartio[9].io[4]
P9.5	smartio[9].io[5]
P9.6	smartio[9].io[6]
P9.7	smartio[9].io[7]

Power Supply Considerations

The power system diagram (see Figure 7) shows the general requirements for power pins on PSoC 62. The power scheme allows different V_{DDIO} and V_{DDA} connections. Because no sequencing requirements need to be analyzed and specified, power supplies may be brought up in any order; the power system is responsible for ensuring power is good in all domains before allowing operation. V_{DDD}, V_{DDA}, and V_{DDIO} may be separate nets, which are not ohmically connected on chip. Depending on different package requirements, these may be required to be connected off chip.

The power system has a core buck regulator in addition to an LDO.

Figure 7. PSoC 62 Power Connections

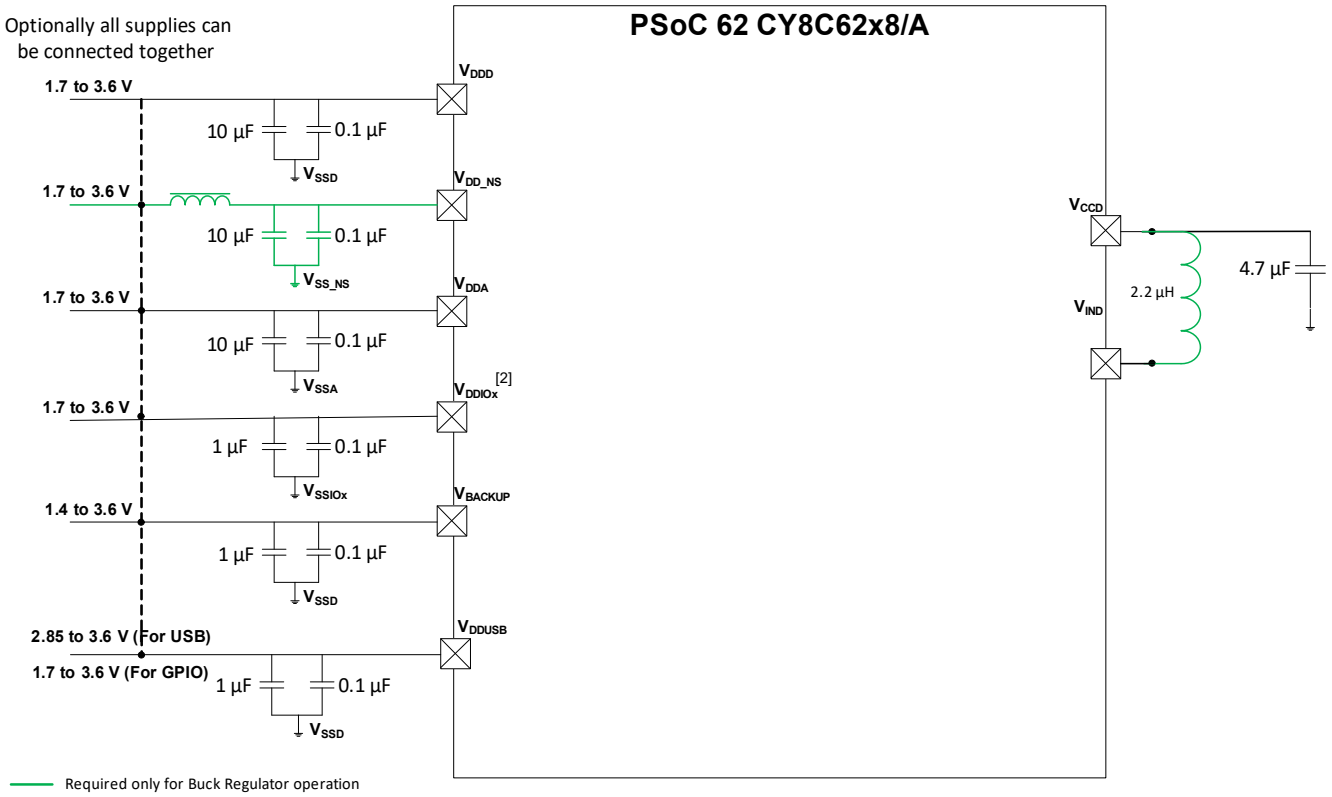


Figure 7 shows the power supply pins to PSoC 62. It also shows which pins need bypass capacitors. Refer to AN218241 - PSoC 6 MCU Hardware Design Considerations for details on the required connections for any given design.

Description of power pins is as follows:

- VBACKUP is the supply to the backup domain. The backup domain includes the 32-kHz WCO, RTC, and backup registers. It can generate a wake-up interrupt to the chip via RTC timers or an external input. It can also generate an output to wake up external circuitry. It is connected to V_{DDD} when not used as a separate battery backup domain. VBACKUP provides the supply for Port 0.
- V_{DDD} is the main digital supply input (1.7 to 3.6 V). It provides the inputs for the internal Regulators and for Port 1.
- V_{DDA} is the supply for analog peripherals (1.7 to 3.6 V). It must be connected to V_{DDIOA} on the PCB.
- V_{DDIOA} is the supply to for Ports 9 and 10. It must be connected to V_{DDA} on the PCB when present. Ports 9 and 10 are supplied by V_{DDA} when V_{DDIOA} is not present.
- V_{DD_NS} is the supply input to the Buck and should be at the same potential as V_{DDD}. The bypass capacitor between V_{DD_NS} and ground should be 10 µF. A ferrite bead may be used to reduce noise.
- V_{DDIO0} is the supply for Ports 11 to 13. When not present, these ports are supplied by V_{DDD}.
- V_{DDIO1} is the supply for Ports 5 to 8. When not present, these ports are supplied by VDDD.
- V_{DDIO2} is the supply for Ports 2 to 4. When not present, these ports are supplied by V_{DDD}.
- V_{DDUSB} is the USB supply and is required to be 2.85 V to 3.6 V for USB operation. In addition, the pin powers Port 14. When USB is not used, this pin can be 1.7 V to 3.6 V for using Port 14 pins as GPIOs.

Note
2. V_{DDIO} pins can be kept as independent supplies or connected together.

All the pins above may be shorted to V_{DDD} as shown in Figure 7.

- V_{IND1} is the buck output to the internal core logic and is to be connected to V_{CCD}.
- V_{CCD} is the internal core logic and needs to be connected to V_{IND1} and decoupled.
- When available, VDDx pins should be decoupled using the corresponding VSSx pins as shown in Figure 7. If the package contains only a VSS pin, then VDDx pins can be decoupled using any VSS pin in the package as all are shorted together inside the package.

The supply voltage range is 1.71 to 3.6 V with all functions and circuits operating over that range. All grounds must be shorted together on the PCB. Bypass capacitors must be used from VDDD and VDDA to ground and wherever indicated in the diagram. Typical practice for systems in this frequency range is to use a capacitor in the 10 µF range in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing. The recommended Buck output capacitor value is 4.7 µF for V_{IND1}. All capacitors should be ±20% or better; the recommended inductor value is 2.2 µH ±20% (for example, TDK MLP2012H2R2MT0S1).

Electrical Specifications

Note: These are preliminary and subject to change.

Absolute Maximum Ratings

Table 7. Absolute Maximum Ratings[3]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID1	V_{DD_ABS}	Analog or digital supply relative to V_{SS} (V_{SSD} = V_{SSA})	–0.5	–	4	V	
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to V_{SSD}	–0.5	–	1.2	V	
SID3	V_{GPIO_ABS}	GPIO voltage; V_{DDD} or V_{DDA}	–0.5	–	V_{DD} + 0.5	V	
SID4	I_{GPIO_ABS}	Current per GPIO	–25	–	25	mA	
SID5	$I_{GPIO\_injection}$	GPIO injection current per pin	–0.5	–	0.5	mA	
SID3A	ESD_HBM	Electrostatic discharge Human Body Model	2200	–	–	V	
SID4A	ESD_CDM	Electrostatic discharge Charged Device Model	500	–	–	V	
SID5A	LU	Pin current for latchup-free operation	–100	–	100	mA	

All specifications are valid for –40 °C ≤ TA ≤ 85 °C and for 1.71 V to 3.6 V except where noted. All AC specs are valid for 8-mA GPIO output drive setting except where noted.

Device-Level Specifications

All specifications are valid for –40 °C ≤ TA ≤ 85 °C and for 1.71 V to 3.6 V except where noted.

Power Supplies

Table 8. Power Supplies

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
DC Specifications							
SID6	V_{DDD}	Internal regulator and Port 1 GPIO supply	1.7	–	3.6	V	–
SID7	V_{DDA}	Analog power supply voltage. Shorted to V_{DDIOA} on PCB.	1.7	–	3.6	V	Internally unregulated supply
SID7A	V_{DDIO1}	GPIO supply for Ports 5 to 8 when present	1.7	–	3.6	V	V_{DDIO_1} must be ≥ to V_{DDA}.
SID7B	V_{DDIO0}	GPIO supply for Ports 11 to 13 when present	1.7	–	3.6	V	–
SID7E	V_{DDIO0}	Supply for eFuse Programming	2.38	2.5	2.62	V	eFuse programming voltage
SID7C	V_{DDIO2}	GPIO supply for Ports 2 to 4 on BGA 124 only	1.7	–	3.6	V	–
SID7D	V_{DDIOA}	GPIO supply for Ports 9 to 10. Shorted to V_{DDA} on PCB.	1.7	–	3.6	V	–
SID7F	V_{DDUSB}	Supply for Port 14 (USB or GPIO) when present	1.7	–	3.6	V	Min supply is 2.85 V for USB
SID6B	V_{BACKUP}	Backup power and GPIO Port 0 supply when present	1.7	–	3.6	V	Min. is 1.4 V in Backup mode
SID8	V_{CCD1}	Output voltage (for core logic bypass)	–	1.1	–	V	LP mode
SID9	V_{CCD2}	Output voltage (for core logic bypass)	–	0.9	–		ULP mode. Valid for –20 to 85°C.

Note
3. Usage above the absolute maximum conditions listed in Table 7 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 8. Power Supplies *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID10	C_{EFC}	External regulator voltage (V_{CCD}) bypass	3.8	4.7	5.6	µF	X5R ceramic or better. Value for 0.8 to 1.2 V.
SID11	C_{EXC}	Power supply decoupling capacitor	–	10	–	µF	X5R ceramic or better

CPU Current and Transition Times

Table 9. CPU Current and Transition Times

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
LP RANGE POWER SPECIFICATIONS (for V_{CCD} = 1.1 V with Buck and LDO)							
Cortex-M4. Active Mode							
Execute with Cache Disabled (Flash)							
SIDF1	IDD1	Execute from Flash; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. While(1).	-	2.85	4.5	mA	VDDD=3.3V, Buck ON, Max at 60 C
				4.1	5.1		VDDD=1.8V, Buck ON, Max at 60 C
				6.8	10		VDDD = 1.8 to 3.3 V, LDO, max at 60 C
SIDF2	IDD2	Execute from Flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz.With IMO. While(1)	-	0.9	2.1	mA	VDDD=3.3V, Buck ON, Max at 60 C
				1.2	2.2		VDDD=1.8V, Buck ON, Max at 60 C
				2.4	5.5		VDDD = 1.8 to 3.3 V, LDO, max at 60 C
Execute with Cache Enabled							
SIDC1	IDD3	Execute from Cache;CM4 Active150 MHz, CM0+ Sleep 75 MHz. IMO & FLL. Dhrystone.	-	7.35	9.5	mA	VDDD=3.3V, Buck ON, Max at 60 C
				12	14.5		VDDD=1.8V, Buck ON, Max at 60 C
				18	21		VDDD = 1.8 to 3.3 V, LDO, max at 60 C
SIDC2	IDD4	Execute from Cache;CM4 Active100 MHz, CM0+ Sleep 100MHz. IMO & FLL. Dhrystone.	-	5.4	6.8	mA	VDDD=3.3V, Buck ON, Max at 60 C
				8.95	10		VDDD=1.8V, Buck ON, Max at 60 C
				13.8	17		VDDD = 1.8 to 3.3 V, LDO, max at 60 C
SIDC3	IDD5	Execute from Cache;CM4 Active 50 MHz, CM0+ Sleep 25MHz. IMO & FLL. Dhrystone	-	2.65	3.8	mA	VDDD=3.3V, Buck ON, Max at 60 C
				4.25	5.3		VDDD=1.8V, Buck ON, Max at 60 C
				6.8	10		VDDD = 1.8 to 3.3 V, LDO, max at 60 C
SIDC4	IDD6	Execute from Cache;CM4 Active 8 MHz, CM0+ Sleep 8 MHz. IMO. Dhrystone	-	0.9	2	mA	VDDD=3.3V, Buck ON, Max at 60 C
				1.27	2.1		VDDD=1.8V, Buck ON, Max at 60 C
				2.3	5.5		VDDD = 1.8 to 3.3 V, LDO, max at 60 C
Cortex M0+. Active Mode							

Table 9. CPU Current and Transition Times *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
Execute with Cache Disabled (Flash)							
SIDF3	IDD7	Execute from Flash;CM4 Off, CM0+ Active 50 MHz. With IMO & FLL. While (1).	-	2.6	4	mA	VDDD=3.3V, Buck ON, Max at 60 C
				3.9	5		VDDD=1.8V, Buck ON, Max at 60 C
				6.5	10		VDDD = 1.8 to 3.3 V, LDO, max at 60 C
SIDF4	IDD8	Execute from Flash;CM4 Off, CM0+ Active 8 MHz. With IMO. While (1)	-	0.8	1.5	mA	VDDD=3.3V, Buck ON, Max at 60 C
				1.1	2		VDDD=1.8V, Buck ON, Max at 60 C
				2.2	5.5		VDDD = 1.8 to 3.3 V, LDO, max at 60 C
Execute with Cache Enabled							
SIDC5	IDD9	Execute from Cache;CM4 Off, CM0+ Active 100 MHz. With IMO & FLL. Dhrystone.	-	4.40	5.8	mA	VDDD=3.3V, Buck ON, Max at 60 C
				7.35	8.5		VDDD=1.8V, Buck ON, Max at 60 C
				11.5	14.5		VDDD = 1.8 to 3.3 V, LDO, max at 60 C
SIDC6	IDD10	Execute from Cache;CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone	-	0.8	2	mA	VDDD=3.3V, Buck ON, Max at 60 C
				1.2	2		VDDD=1.8V, Buck ON, Max at 60 C
				2.2	5.5		VDDD = 1.8 to 3.3 V, LDO, max at 60 C
Cortex M4. Sleep Mode							
SIDS1	IDD11	CM4 Sleep 100 MHz, CM0+ Sleep 25 MHz. With IMO & FLL.		1.55	2.2	mA	VDDD=3.3V, Buck ON, Max at 60 C
				2.4	3.5		VDDD=1.8V, Buck ON, Max at 60 C
				4.2	7.2		VDDD = 1.8 to 3.3 V, LDO, max at 60 C
SIDS2	IDD12	CM4 Sleep 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL		1.2	2	mA	VDDD=3.3V, Buck ON, Max at 60 C
				1.75	2.7		VDDD=1.8V, Buck ON, Max at 60 C
				3.2	6.3		VDDD = 1.8 to 3.3 V, LDO, max at 60 C
SIDS3	IDD13	CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz. With IMO.		0.7	1.3	mA	VDDD=3.3V, Buck ON, Max at 60 C
				0.96	1.8		VDDD=1.8V, Buck ON, Max at 60 C
				1.7	5		VDDD = 1.8 to 3.3 V, LDO, max at 60 C
Cortex M0+. Sleep Mode							

Table 9. CPU Current and Transition Times *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SIDS4	IDD14	CM4 Off, CM0+ Sleep 50 MHz. With IMO & FLL.		1.3	2	mA	VDDD=3.3V, Buck ON, Max at 60 C
				2.05	3		VDDD=1.8V, Buck ON, Max at 60 C
				3.6	6.8		VDDD = 1.8 to 3.3 V, LDO, max at 60 C
SIDS5	IDD15	CM4 Off, CM0+ Sleep 8 MHz. With IMO.		0.7	1.3	mA	VDDD=3.3V, Buck ON, Max at 60 C
				0.95	1.5		VDDD=1.8V, Buck ON, Max at 60 C
				1.7	5		VDDD = 1.8 to 3.3 V, LDO, max at 60 C
Cortex M4. Minimum Regulator Current Mode							
SIDLPA1	IDD16	Execute from Flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While (1).	-	0.85	1.8	mA	VDDD=3.3V, Buck ON, Max at 60 C
				1.18	2		VDDD=1.8V, Buck ON, Max at 60 C
				2.2	5.5		VDDD = 1.8 to 3.3 V, LDO, max at 60 C
SIDLPA2	IDD17	Execute from Cache; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. Dhrystone.	-	0.9	1.5	mA	VDDD=3.3V, Buck ON, Max at 60 C
				1.27	2		VDDD=1.8V, Buck ON, Max at 60 C
				2.2	5.5		VDDD = 1.8 to 3.3 V, LDO, max at 60 C
Cortex M0+. Minimum Regulator Current Mode							
SIDLPA3	IDD18	Execute from Flash; CM4 Off, CM0+ Active 8 MHz. With IMO. While (1)	-	0.8	1.5	mA	VDDD=3.3V, Buck ON, Max at 60 C
				1.14	2		VDDD=1.8V, Buck ON, Max at 60 C
				2.1	5.5		VDDD = 1.8 to 3.3 V, LDO, max at 60 C
SIDLPA4	IDD19	Execute from Cache; CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone.	-	0.8	1.5	mA	VDDD=3.3V, Buck ON, Max at 60 C
				1.15	2		VDDD=1.8V, Buck ON, Max at 60 C
				2.1	5.5		VDDD = 1.8 to 3.3 V, LDO, max at 60 C
Cortex M4. Minimum Regulator Current Mode							
SIDLPS1	IDD20	CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz. With IMO.	-	0.65	1.2	mA	VDDD=3.3V, Buck ON, Max at 60 C
				0.95	1.7		VDDD=1.8V, Buck ON, Max at 60 C
				1.6	5		VDDD = 1.8 to 3.3 V, LDO, max at 60 C
Cortex M0+. Minimum Regulator Current Mode							

Table 9. CPU Current and Transition Times *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SIDLPS3	IDD22	CM4 Off, CM0+ Sleep 8 MHz. With IMO.	-	0.64	1.2	mA	VDDD=3.3V, Buck ON, Max at 60 C
				0.93	1.7		VDDD=1.8V, Buck ON, Max at 60 C
				1.6	5		VDDD = 1.8 to 3.3 V, LDO, max at 60 C
ULP RANGE POWER SPECIFICATIONS (for VCCD = 0.9V using the Buck). ULP mode is valid from -20 to +85 C.							
Cortex M4. Active Mode							
Execute with Cache Disabled (Flash)							
SIDF5	IDD3	Execute from Flash; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. While(1).	-	2.15	2.9	mA	VDDD=3.3V, Buck ON, Max at 60 C
				2.85	3.4		VDDD=1.8V, Buck ON, Max at 60 C
SIDF6	IDD4	Execute from Flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While (1)	-	0.65	1.2	mA	VDDD=3.3V, Buck ON, Max at 60 C
				0.8	1.4		VDDD=1.8V, Buck ON, Max at 60 C
Execute with Cache Enabled							
SIDC8	IDD10	Execute from Cache; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. Dhrystone.	-	1.85	2.5	mA	VDDD=3.3V, Buck ON, Max at 60 C
				2.9	3.5		VDDD=1.8V, Buck ON, Max at 60 C
SIDC9	IDD11	Execute from Cache; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. Dhrystone.	-	0.65	1.2	mA	VDDD=3.3V, Buck ON, Max at 60 C
				0.8	1.3		VDDD=1.8V, Buck ON, Max at 60 C
Cortex M0+. Active Mode							
Execute with Cache Disabled (Flash)							
SIDF7	IDD16	Execute from Flash; CM4 Off, CM0+ Active 25 MHz. With IMO & FLL. Write(1).	-	1.1	1.5	mA	VDDD=3.3V, Buck ON, Max at 60 C
				1.55	2.2		VDDD=1.8V, Buck ON, Max at 60 C
SIDF8	IDD17	Execute from Flash; CM4 Off, CM0+ Active 8 MHz. With IMO. While(1)	-	0.55	1.2	mA	VDDD=3.3V, Buck ON, Max at 60 C
				0.73	1.4		VDDD=1.8V, Buck ON, Max at 60 C
Execute with Cache Enabled							
SIDC10	IDD18	Execute from Cache; CM4 Off, CM0+ Active 25 MHz. With IMO & FLL. Dhrystone.	-	1	1.5	mA	VDDD=3.3V, Buck ON, Max at 60 C
				1.5	2		VDDD=1.8V, Buck ON, Max at 60 C
SIDC11	IDD19	Execute from Cache; CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone.	-	0.55	0.95	mA	VDDD=3.3V, Buck ON, Max at 60 C
				0.73	1.3		VDDD=1.8V, Buck ON, Max at 60 C
Cortex M4. Sleep Mode							

Table 9. CPU Current and Transition Times *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SIDS7	IDD21	CM4 Sleep 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL		0.85	1.2	mA	VDDD=3.3V, Buck ON, Max at 60 C
				1.2	1.8		VDDD=1.8V, Buck ON, Max at 60 C
SIDS8	IDD22	CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz. With IMO		0.45	0.9	mA	VDDD=3.3V, Buck ON, Max at 60 C
				0.59	1		VDDD=1.8V, Buck ON, Max at 60 C
Cortex M0+. Sleep Mode							
SIDS9	IDD23	CM4 Off, CM0+ Sleep 25 MHz. With IMO & FLL.		0.62	1.2	mA	VDDD=3.3V, Buck ON, Max at 60 C
				0.88	1.5		VDDD=1.8V, Buck ON, Max at 60 C
SIDS10	IDD24	CM4 Off, CM0+ Sleep 8 MHz. With IMO.		0.41	0.72	mA	VDDD=3.3V, Buck ON, Max at 60 C
				0.58	1.3		VDDD=1.8V, Buck ON, Max at 60 C
Cortex M4. Minimum Regulator Current Mode							
SIDLPA5	IDD25	Execute from Flash. CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While(1).	-	0.65	1.2	mA	VDDD=3.3V, Buck ON, Max at 60 C
				0.8	1.4		VDDD=1.8V, Buck ON, Max at 60 C
SIDLPA6	IDD26	Execute from Cache. CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. Dhrystone.	-	0.6	1	mA	VDDD=3.3V, Buck ON, Max at 60 C
				0.78	1.4		VDDD=1.8V, Buck ON, Max at 60 C
Cortex M0+. Minimum Regulator Current Mode							
SIDLPA7	IDD27	Execute from Flash. CM4 Off, CM0+ Active 8 MHz. With IMO. While (1).	-	0.55	1	mA	VDDD=3.3V, Buck ON, Max at 60 C
				0.75	1.4		VDDD=1.8V, Buck ON, Max at 60 C
SIDLPA8	IDD28	Execute from Cache. CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone.	-	0.5	1	mA	VDDD=3.3V, Buck ON, Max at 60 C
				0.7	1.4		VDDD=1.8V, Buck ON, Max at 60 C
Cortex M4. Minimum Regulator Current Mode							
SIDLPS5	IDD29	CM4 Sleep 8 MHz, CM0 Sleep 8 MHz. With IMO.	-	0.45	1	mA	VDDD=3.3V, Buck ON, Max at 60 C
				0.57	1.1		VDDD=1.8V, Buck ON, Max at 60 C
Cortex M0+. Minimum Regulator Current Mode							
SIDLPS7	IDD31	CM4 Off, CM0+ Sleep 8 MHz. With IMO.	-	0.4	1	mA	VDDD=3.3V, Buck ON, Max at 60 C
				0.56	1.1		VDDD=1.8V, Buck ON, Max at 60 C
Deep Sleep Mode							
SIDDS1	I_{DD33A}	With internal Buck enabled and 64-KB SRAM retention	–	7	–	µA	Max value is at 85 °C

Table 9. CPU Current and Transition Times *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SIDDS1_B	I_{DD33A_B}	With internal Buck enabled and 64-KB SRAM retention	–	7	–	µA	Max value is at 60 °C
SIDDS2	I_{DD33B}	With internal Buck enabled and 256-KB SRAM retention	–	9	–	µA	Max value is at 85 °C
SIDDS2_B	I_{DD33B_B}	With internal Buck enabled and 256-KB SRAM retention	–	9	–	µA	Max value is at 60 °C
Hibernate Mode							
SIDHIB1	I_{DD34}	V_{DDD} = 1.8 V	–	300	–	nA	No clocks running
SIDHIB2	I_{DD34A}	V_{DDD} = 3.3 V	–	800	–	nA	No clocks running
Power Mode Transition Times							
SID12	T_{LPACT_ACT}	Minimum Regulator Current to Active transition time	–	–	35	µs	Including PLL lock time
SID13	T_{DS_LPACT}	Deep Sleep to Active transition time	–	–	25	µs	Guaranteed by design
SID14	T_{HIB_ACT}	Hibernate to Active transition time	–	500	–	µs	Including PLL lock time

XRES

Table 10. XRES

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
XRES (Active Low) Specifications							
XRES AC Specifications							
SID15	T_{XRES_ACT}	POR or XRES release to Active transition time	–	850	–	µs	Normal mode, 50 MHz CM0+.
SID16	T_{XRES_PW}	XRES pulse width	5	–	–	µs	–
XRES DC Specifications							
SID17	T_{XRES_IDD}	I_{DD} when XRES asserted	–	300	–	nA	V_{DDD} = 1.8 V
SID17A	$T_{XRES\_IDD\_1}$	I_{DD} when XRES asserted	–	2100	–	nA	V_{DDD} = 3.3 V
SID77	V_{IH}	Input voltage HIGH threshold	0.7 * V_{DD}	–	–	V	CMOS input
SID78	V_{IL}	Input voltage LOW threshold	–	–	0.3 * V_{DD}	V	CMOS input
SID80	C_{IN}	Input capacitance	–	3	–	pF	–
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	–
SID82	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–

GPIO

Table 11. GPIO Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
GPIO DC Specifications							
SID57	V_{IH}	Input voltage HIGH threshold	0.7 * V_{DD}	–	–	V	CMOS Input
SID57A	I_{IHS}	Input current when Pad > V_{DDIO} for OVT inputs	–	–	10	µA	Per I^2C Spec
SID58	V_{IL}	Input voltage LOW threshold	–	–	0.3 * V_{DD}	V	CMOS Input
SID241	V_{IH}	LVTTL input, V_{DD} < 2.7 V	0.7 * V_{DD}	–	–	V	–
SID242	V_{IL}	LVTTL input, V_{DD} < 2.7 V	–	–	0.3 * V_{DD}	V	–
SID243	V_{IH}	LVTTL input, V_{DD} ≥ 2.7 V	2.0	–	–	V	–
SID244	V_{IL}	LVTTL input, V_{DD} ≥ 2.7 V	–	–	0.8	V	–
SID59	V_{OH}	Output voltage HIGH level	V_{DD} – 0.5	–	–	V	I_{OH} = 8 mA
SID62A	V_{OL}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 8 mA
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	–
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DD} = 3.0 V
SID66	C_{IN}	Input capacitance	–	–	5	pF	–
SID67	V_{HYSTTL}	Input hysteresis LVTTL V_{DD} > 2.7 V	100	0	–	mV	–
SID68	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05*V_{DD}	–	–	mV	–
SID69	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–
SID69A	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	–
GPIO AC Specifications							
SID70	T_{RISEF}	Rise time in Fast Strong Mode. 10% to 90% of V_{DD}.	–	–	2.5	ns	Cload = 15 pF, 8mA drive strength
SID71	T_{FALLF}	Fall time in Fast Strong Mode. 10% to 90% of V_{DD}.	–	–	2.5	ns	Cload = 15 pF, 8 mA drive strength
SID72	T_{RISES_1}	Rise time in Slow Strong Mode. 10% to 90% of V_{DD}.	52	–	142	ns	Cload = 15 pF, 8 mA drive strength, V_{DD} ≤ 2.7 V
SID72A	T_{RISES_2}	Rise time in Slow Strong Mode. 10% to 90% of V_{DD}.	48	–	102	ns	Cload = 15 pF, 8 mA drive strength, 2.7 V < V_{DD} ≤ 3.6 V
SID73	T_{FALLS_1}	Fall time in Slow Strong Mode. 10% to 90% of V_{DD}.	44	–	211	ns	Cload = 15 pF, 8 mA drive strength, V_{DD} ≤ 2.7 V
SID73A	T_{FALLS_2}	Fall time in Slow Strong Mode. 10% to 90% of V_{DD}.	42	–	93	ns	Cload = 15 pF, 8 mA drive strength, 2.7 V < V_{DD} ≤ 3.6 V
SID73G	T_{FALL_I2C}	Fall time (30% to 70% of V_{DD}) in Slow Strong mode.	20 * V_{DDIO} / 5.5	–	250	ns	Cload = 10 pF to 400 pF, 8-mA drive strength
SID74	$F_{GPIOUT1}$	GPIO Fout. Fast Strong mode.	–	–	100	MHz	90/10%, 15-pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO Fout; Slow Strong mode.	–	–	1.5	MHz	90/10%, 15-pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO Fout; Fast Strong mode.	–	–	100	MHz	90/10%, 25-pF load, 60/40 duty cycle

Table 11. GPIO Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID245	$F_{GPIOUT4}$	GPIO Fout; Slow Strong mode.	–	–	1.3	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V_{DD} ≤ 3.6 V	–	–	100	MHz	90/10% V_{IO}

Analog Peripherals

Low-Power (LP) Comparator

Table 12. Low-Power (LP) Comparator Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
LP Comparator DC Specifications							
SID84	$V_{OFFSET1}$	Input offset voltage. Normal power mode.	–10	–	10	mV	–
SID85A	$V_{OFFSET2}$	Input offset voltage. Low-power mode.	–25	±12	25	mV	–
SID85B	$V_{OFFSET3}$	Input offset voltage. Ultra low-power mode.	–25	±12	25	mV	–
SID86	V_{HYST1}	Hysteresis when enabled in Normal mode	–	–	60	mV	–
SID86A	V_{HYST2}	Hysteresis when enabled in Low-power mode	–	–	80	mV	–
SID87	V_{ICM1}	Input common mode voltage in Normal mode	0	–	V_{DDIO1} – 0.1	V	–
SID247	V_{ICM2}	Input common mode voltage in Low power mode	0	–	V_{DDIO1} – 0.1	V	–
SID247A	V_{ICM3}	Input common mode voltage in Ultra low power mode	0	–	V_{DDIO1} – 0.1	V	–
SID88	CMRR	Common mode rejection ratio in Normal power mode	50	–	–	dB	–
SID89	I_{CMP1}	Block current, Normal mode	–	–	150	µA	–
SID248	I_{CMP2}	Block current, Low-power mode	–	–	10	µA	–
SID259	I_{CMP3}	Block current in Ultra low-power mode	–	0.3	0.85	µA	–
SID90	ZCMP	DC input impedance of comparator	35	–	–	MΩ	–
LP Comparator AC Specifications							
SID91	T_{RESP1}	Response time, Normal mode, 100 mV overdrive	–	–	100	ns	–
SID258	T_{RESP2}	Response time, Low power mode, 100 mV overdrive	–	–	1000	ns	–
SID92	T_{RESP3}	Response time, Ultra-low power mode, 100 mV overdrive	–	–	20	µs	–
SID92E	T_CMP_EN1	Time from Enabling to operation	–	–	10	µs	Normal and low-power modes
SID92F	T_CMP_EN2	Time from Enabling to operation	–	–	50	µs	Ultra-low-power mode

Temperature Sensor

Table 13. Temperature Sensor Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID93	$T_{SENSACC}$	Temperature sensor accuracy	–5	±1	5	°C	–40 to +85 °C

Internal Reference

Table 14. Internal Reference Specification

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID93R	V_{REFBG}	–	1.188	1.2	1.212	V	–

SAR ADC

Table 15. 12-bit SAR ADC DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID94	A_RES	SAR ADC Resolution	–	–	12	bits	–
SID95	A_CHNLS_S	Number of channels - single ended	–	–	16	–	8 full speed
SID96	A-CHNKS_D	Number of channels - differential	–	–	8	–	Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–	–	Yes
SID98	A_GAINERR	Gain error	–	–	±0.2	%	With external reference.
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V reference
SID100	A_ISAR_1	Current consumption at 1 Msps	–	–	1	mA	At 1 Msps. External bypass cap.
SID100A	A_ISAR_2	Current consumption at 1 Msps. Reference = V_{DD}	–	–	1.25	mA	At 1 Msps. External bypass cap.
SID101	A_VINS	Input voltage range - single-ended	Vss	–	V_{DDA}	V	–
SID102	A_VIND	Input voltage range - differential	Vss	–	V_{DDA}	V	–
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	–
SID104	A_INCAP	Input capacitance	–	–	10	pF	–

Table 16. 12-bit SAR ADC AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
12-bit SAR ADC AC Specifications							
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	–
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
One Megasample per second mode							
SID108	A_SAMP_1	Sample rate with external reference bypass cap.	–	–	1	Msps	–
SID108A	A_SAMP_2	Sample rate with no bypass cap; Reference = V_{DD}	–	–	250	ksps	–
SID108B	A_SAMP_3	Sample rate with no bypass cap. Internal reference.	–	–	100	ksps	–
SID109	A_SINAD	Signal-to-noise and Distortion ratio (SINAD). V_{DDA} = 2.7 to 3.6 V, 1 Msps.	64	–	–	dB	Fin = 10 kHz
SID111A	A_INL	Integral non linearity. V_{DDA} = 2.7 to 3.6 V, 1 Msps	–2	–	2	LSB	Measured with internal V_{REF} = 1.2 V and bypass cap.
SID111B	A_INL	Integral non-linearity. V_{DDA} = 2.7 to 3.6 V, 1 Msps	–4	–	4	LSB	Measured with external $V_{REF} \geq 1$ V and V_{IN} common mode < 2 * V_{REF}
SID112A	A_DNL	Differential non linearity. V_{DDA} = 2.7 to 3.6 V, 1 Msps	–1	–	1.4	LSB	Measured with internal V_{REF} = 1.2 V and bypass cap.
SID112B	A_DNL	Differential non linearity. V_{DDA} = 2.7 to 3.6 V, 1 Msps	–1	–	1.7	LSB	Measured with external $V_{REF} \geq 1$ V and V_{IN} common mode < 2 * V_{REF}
SID113	A_THD	Total harmonic distortion. V_{DDA} = 2.7 to 3.6 V, 1 Msps.	–	–	–65	dB	Fin = 10 kHz

CSD

Table 17. CapSense Sigma-Delta (CSD) Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
CSD V2 Specifications							
SYS.PER#3	V_{DD_RIPPLE}	Max allowed ripple on power supply, DC to 10 MHz	–	–	±50	mV	V_{DDA} > 2 V (with ripple), 25 °C T_A, Sensitivity = 0.1 pF
SYS.PER#16	$V_{DD\_RIPPLE\_1.8}$	Max allowed ripple on power supply, DC to 10 MHz	–	–	±25	mV	V_{DDA} > 1.75 V (with ripple), 25 ° C T_A, Parasitic Capacitance (C_P) < 20 pF, Sensitivity ≥ 0.4 pF
SID.CSD.BLK	I_{CSD}	Maximum block current			4500	µA	–
SID.CSD#15	V_{REF}	Voltage reference for CSD and Comparator	0.6	1.2	V_{DDA} – 0.6	V	$V_{DDA} - V_{REF} \geq 0.6$ V
SID.CSD#15A	V_{REF_EXT}	External Voltage reference for CSD and Comparator	0.6		V_{DDA} – 0.6	V	$V_{DDA} - V_{REF} \geq 0.6$ V
SID.CSD#16	$I_{DAC1IDD}$	IDAC1 (7-bits) block current	–	–	1900	µA	–
SID.CSD#17	$I_{DAC2IDD}$	IDAC2 (7-bits) block current	–	–	1900	µA	–
SID308	V_{CSD}	Voltage range of operation	1.7	–	3.6	V	1.71 to 3.6 V
SID308A	$V_{COMPIDAC}$	Voltage compliance range of IDAC	0.6	–	V_{DDA} – 0.6	V	$V_{DDA} - V_{REF} \geq 0.6$ V
SID309	$I_{DAC1DNL}$	DNL	–1	–	1	LSB	–
SID310	$I_{DAC1INL}$	INL	–3	–	3	LSB	If V_{DDA} < 2 V then for LSB of 2.4 µA or less
SID311	$I_{DAC2DNL}$	DNL	–1	–	1	LSB	–
SID312	$I_{DAC2INL}$	INL	–3	–	3	LSB	If V_{DDA} < 2 V then for LSB of 2.4 µA or less
SNRC of the following is Ratio of counts of finger to noise. Guaranteed by characterization.							
SID313_1A	SNRC_1	SRSS Reference. IMO + FLL Clock Source. 0.1-pF sensitivity.	5	–	–	Ratio	9.5 pF max. capacitance
SID313_1B	SNRC_2	SRSS Reference. IMO + FLL Clock Source. 0.3-pF sensitivity.	5	–	–	Ratio	31 pF max. capacitance
SID313_1C	SNRC_3	SRSS Reference. IMO + FLL Clock Source. 0.6-pF sensitivity.	5	–	–	Ratio	61 pF max. capacitance
SID313_2A	SNRC_4	PASS Reference. IMO + FLL Clock Source. 0.1-pF sensitivity.	5	–	–	Ratio	12 pF max. capacitance
SID313_2B	SNRC_5	PASS Reference. IMO + FLL Clock Source. 0.3-pF sensitivity.	5	–	–	Ratio	47 pF max. capacitance
SID313_2C	SNRC_6	PASS Reference. IMO + FLL Clock Source. 0.6-pF sensitivity.	5	–	–	Ratio	86 pF max. capacitance
SID313_3A	SNRC_7	PASS Reference. IMO + PLL Clock Source. 0.1-pF sensitivity.	5	–	–	Ratio	27 pF max. capacitance
SID313_3B	SNRC_8	PASS Reference. IMO + PLL Clock Source. 0.3-pF sensitivity.	5	–	–	Ratio	86 pF max. capacitance
SID313_3C	SNRC_9	PASS Reference. IMO + PLL Clock Source. 0.6-pF sensitivity.	5	–	–	Ratio	168 pF Max. capacitance

Table 17. CapSense Sigma-Delta (CSD) Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID314	$IDAC_{1CRT1}$	Output current of IDAC1 (7 bits) in low range	4.2		5.7	µA	LSB = 37.5-nA typ.
SID314A	$IDAC_{1CRT2}$	Output current of IDAC1 (7 bits) in medium range	33.7		45.6	µA	LSB = 300-nA typ.
SID314B	$IDAC_{1CRT3}$	Output current of IDAC1 (7 bits) in high range	270		365	µA	LSB = 2.4-µA typ.
SID314C	$IDAC_{1CRT12}$	Output current of IDAC1 (7 bits) in low range, 2X mode	8		11.4	µA	LSB = 37.5-nA typ. 2X output stage
SID314D	$IDAC_{1CRT22}$	Output current of IDAC1 (7 bits) in medium range, 2X mode	67		91	µA	LSB = 300-nA typ. 2X output stage
SID314E	$IDAC_{1CRT32}$	Output current of IDAC1 (7 bits) in high range, 2X mode. V_{DDA} > 2 V	540		730	µA	LSB = 2.4-µA typ. 2X output stage
SID315	$IDAC_{2CRT1}$	Output current of IDAC2 (7 bits) in low range	4.2		5.7	µA	LSB = 37.5-nA typ.
SID315A	$IDAC_{2CRT2}$	Output current of IDAC2 (7 bits) in medium range	33.7		45.6	µA	LSB = 300-nA typ.
SID315B	$IDAC_{2CRT3}$	Output current of IDAC2 (7 bits) in high range	270		365	µA	LSB = 2.4-µA typ.
SID315C	$IDAC_{2CRT12}$	Output current of IDAC2 (7 bits) in low range, 2X mode	8		11.4	µA	LSB = 37.5-nA typ. 2X output stage
SID315D	$IDAC_{2CRT22}$	Output current of IDAC2 (7 bits) in medium range, 2X mode	67		91	µA	LSB = 300-nA typ. 2X output stage
SID315E	$IDAC_{2CRT32}$	Output current of IDAC2 (7 bits) in high range, 2X mode. V_{DDA} > 2V	540		730	µA	LSB = 2.4-µA typ. 2X output stage
SID315F	$IDAC_{3CRT13}$	Output current of IDAC in 8-bit mode in low range	8		11.4	µA	LSB = 37.5-nA typ.
SID315G	$IDAC_{3CRT23}$	Output current of IDAC in 8-bit mode in medium range	67		91	µA	LSB = 300-nA typ.
SID315H	$IDAC_{3CRT33}$	Output current of IDAC in 8-bit mode in high range. V_{DDA} > 2V	540		730	µA	LSB = 2.4-µA typ.
SID320	$IDAC_{OFFSET}$	All zeroes input	–	–	1	LSB	Polarity set by Source or Sink
SID321	$IDAC_{GAIN}$	Full-scale error less offset	–	–	±15	%	LSB = 2.4-µA typ.
SID322	$IDAC_{MISMATCH1}$	Mismatch between IDAC1 and IDAC2 in Low mode	–	–	9.2	LSB	LSB = 37.5-nA typ.
SID322A	$IDAC_{MISMATCH2}$	Mismatch between IDAC1 and IDAC2 in Medium mode	–	–	6	LSB	LSB = 300-nA typ.
SID322B	$IDAC_{MISMATCH3}$	Mismatch between IDAC1 and IDAC2 in High mode	–	–	5.8	LSB	LSB = 2.4-µA typ.
SID323	$IDAC_{SET8}$	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID324	$IDAC_{SET7}$	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

Table 18. CSD ADC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
CSDv2 ADC Specifications							
SIDA94	A_RES	Resolution	–	–	10	bits	Auto-zeroing is required every milli-second
SID95	A_CHNLS_S	Number of channels - single ended	–	–	–	16	–
SIDA97	A-MONO	Monotonicity	–	–	Yes	–	V_{REF} mode
SIDA98	A_GAINERR_VREF	Gain error	–	0.6	–	%	Reference Source: SRSS (V_{REF} = 1.20 V, V_{DDA} < 2.2 V), (V_{REF} = 1.6 V, 2.2 V < V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)
SIDA98A	A_GAINERR_VDDA	Gain error	–	0.2	–	%	Reference Source: SRSS (V_{REF}=1.20 V, V_{DDA} < 2.2V), (V_{REF}=1.6 V, 2.2 V < V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)
SIDA99	A_OFFSET_VREF	Input offset voltage	–	0.5	–	LSb	After ADC calibration, Ref. Src = SRSS, (V_{REF} = 1.20 V, V_{DDA} < 2.2 V), (V_{REF} = 1.6 V, 2.2 V < V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)
SIDA99A	A_OFFSET_VDDA	Input offset voltage	–	0.5	–	LSb	After ADC calibration, Ref. Src = SRSS, (V_{REF} = 1.20 V, V_{DDA} < 2.2 V), (V_{REF} = 1.6 V, 2.2 V < V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)
SIDA100	A_ISAR_VREF	Current consumption	–	0.3	–	mA	CSD ADC Block current
SIDA100A	A_ISAR_VDDA	Current consumption	–	0.3	–	mA	CSD ADC Block current
SIDA101	A_VINS_VREF	Input voltage range - single ended	V_{SSA}	–	V_{REF}	V	(V_{REF} = 1.20 V, V_{DDA} < 2.2 V), (V_{REF} = 1.6 V, 2.2 V < V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)
SIDA101A	A_VINS_VDDA	Input voltage range - single ended	V_{SSA}	–	V_{DDA}	V	(V_{REF} = 1.20 V, V_{DDA} < 2.2 V), ($V_{RE\ F}$ = 1.6 V, 2.2 V < V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)
SIDA103	A_INRES	Input charging resistance	–	15	–	kΩ	–
SIDA104	A_INCAP	Input capacitance	–	41	–	pF	–
SIDA106	A_PSRR	Power supply rejection ratio (DC)	–	60	–	dB	–
SIDA107	A_TACQ	Sample acquisition time	–	10	–	µs	Measured with 50-Ω source impedance. 10 µs is default software driver acquisition time setting. Settling to within 0.05%.
SIDA108	A_CONV8	Conversion time for 8-bit resolution at conversion rate = Fhclk / (2"(N + 2)). Clock frequency = 50 MHz.	–	25	–	µs	Does not include acquisition time.
SIDA108A	A_CONV10	Conversion time for 10-bit resolution at conversion rate = Fhclk / (2"(N + 2)). Clock frequency = 50 MHz.	–	60	–	µs	Does not include acquisition time.

Table 18. CSD ADC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SIDA109	A_SND_VRE	Signal-to-noise and Distortion ratio (SINAD)	–	57	–	dB	Measured with 50-Ω source impedance
SIDA109A	A_SND_VDDA	Signal-to-noise and Distortion ratio (SINAD)	–	52	–	dB	Measured with 50-Ω source impedance
SIDA111	A_INL_VREF	Integral non-linearity. 11.6 ksps	–	–	2	LSB	Measured with 50-Ω source impedance
SIDA111A	A_INL_VDDA	Integral non-linearity. 11.6 ksps	–	–	2	LSB	Measured with 50-Ω source impedance
SIDA112	A_DNL_VREF	Differential non-linearity. 11.6 ksps	–	–	1	LSB	Measured with 50-Ω source impedance
SIDA112A	A_DNL_VDDA	Differential non-linearity. 11.6 ksps	–	–	1	LSB	Measured with 50-Ω source impedance

Digital Peripherals

Timer/Counter/PWM

Table 19. Timer/Counter/PWM (TCPWM) Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.1	I_{TCPWM1}	Block current consumption at 8 MHz	–	–	70	µA	All modes (TCPWM)
SID.TCPWM.2	I_{TCPWM2}	Block current consumption at 24 MHz	–	–	180	µA	All modes (TCPWM)
SID.TCPWM.2A	I_{TCPWM3}	Block current consumption at 50 MHz	–	–	270	µA	All modes (TCPWM)
SID.TCPWM.2B	I_{TCPWM4}	Block current consumption at 100 MHz	–	–	540	µA	All modes (TCPWM)
SID.TCPWM.3	$TCPWM_{FREQ}$	Operating frequency	–	–	100	MHz	Maximum = 100 MHz
SID.TCPWM.4	$TPWM_{ENEXT}$	Input trigger pulse width for all trigger events	2/Fc	–	–	ns	Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected. FC is counter operating frequency.
SID.TCPWM.5	$TPWM_{EXT}$	Output trigger pulse widths	1.5/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs. FC is counter operating frequency..
SID.TCPWM.5A	TC_{RES}	Resolution of counter	1/Fc	–	–	ns	Minimum time between successive counts. FC is counter operating frequency.
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–	ns	Minimum pulse width of PWM output. FC is counter operating frequency.
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	2/Fc	–	–	ns	Minimum pulse width between Quadrature phase inputs. Delays from pins should be similar. FC is counter operating frequency.

Serial Communication Block (SCB)

Table 20. Serial Communication Block (SCB) Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
Fixed I^2C DC Specifications							
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	30	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	80	µA	–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	180	µA	–
SID152	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	–	1.7	µA	At 60°C.
Fixed I^2C AC Specifications							
SID153	F_{I2C1}	Bit Rate	–	–	1	Mbps	–
Fixed UART DC Specifications							
SID160	I_{UART1}	Block current consumption at 100 kbps	–	–	30	µA	–
SID161	I_{UART2}	Block current consumption at 1000 kbps	–	–	180	µA	–
Fixed UART AC Specifications							

Table 20. Serial Communication Block (SCB) Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID162A	F_{UART1}	Bit Rate	–	–	3	Mbps	ULP Mode
SID162B	F_{UART2}		–	–	8		LP Mode
Fixed SPI DC Specifications							
SID163	I_{SPI1}	Block current consumption at 1 Mbps	–	–	220	µA	–
SID164	I_{SPI2}	Block current consumption at 4 Mbps	–	–	340	µA	–
SID165	I_{SPI3}	Block current consumption at 8 Mbps	–	–	360	µA	–
SID165A	I_{SP14}	Block current consumption at 25 Mbps	–	–	800	µA	–
Fixed SPI AC Specifications for LP Mode (1.1 V) unless noted otherwise.							
SID166	F_{SPI}	SPI Operating frequency externally clocked slave	–	–	25	MHz	12-MHz max for ULP (0.9 V) mode
SID166B	F_{SPI_EXT}	SPI operating frequency master (F_{scb} is SPI clock).	–	–	$F_{scb}/4$	MHz	F_{scb} max is 100 MHz in LP (1.1 V) mode, 25 MHz in ULP mode.
SID166A	F_{SPI_IC}	SPI slave internally clocked	–	–	15	MHz	5 MHz max for ULP (0.9 V) mode
Fixed SPI Master mode AC Specifications for LP Mode (1.1 V) unless noted otherwise.							
SID167	T_{DMO}	MOSI valid after SClock driving edge	–	–	12	ns	20 ns max for ULP (0.9 V) mode
SID168	T_{DSI}	MISO valid before SClock capturing edge	5	–	–	ns	Full clock, late MISO sampling
SID169	T_{HMO}	MOSI data hold time	0	–	–	ns	Referred to Slave capturing edge
Fixed SPI Slave mode AC Specifications for LP Mode (1.1 V) unless noted otherwise.							
SID170	T_{DMI}	MOSI valid before Sclock capturing edge	5	–	–	ns	–
SID171A	T_{DSO_EXT}	MISO valid after Sclock driving edge in Ext. Clk. mode	–	–	20	ns	35 ns max. for ULP (0.9 V) mode
SID171	T_{DSO}	MISO valid after Sclock driving edge in Internally Clk. mode	–	–	TDSO_EXT + 3 * Tscb	ns	Tscb is Serial Comm. Block clock period.
SID171B	T_{DSO}	MISO Valid after Sclock driving edge in Internally Clk. Mode with median filter enabled.	–	–	TDSO_EXT + 4 * Tscb	ns	Tscb is Serial Comm. Block clock period.
SID172	T_{HSO}	Previous MISO data hold time	5	–	–	ns	–
SID172A	$TSSEL_{SCK1}$	SSEL Valid to first SCK valid edge	65	–	–	ns	–
SID172B	$TSSEL_{SCK2}$	SSEL Hold after Last SCK valid edge	65	–	–	ns	–

LCD Specifications

Table 21. LCD Direct Drive DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID155	C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	–
SID156	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	–
SID157	I_{LCDOP1}	PWM Mode current. 3.3 V bias. 8 MHz IMO. 25°C.	–	0.6	–	mA	32 × 4 segments 50 Hz
SID158	I_{LCDOP2}	PWM Mode current. 3.3 V bias. 8 MHz IMO. 25°C.	–	0.5	–	mA	32 × 4 segments 50 Hz

Table 22. LCD Direct Drive AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID159	F_{LCD}	LCD frame rate	10	50	150	Hz	–

Memory

Flash Specifications[4]

Table 23. Flash Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Flash DC Specifications							
SID173	VPE	Erase and program voltage	1.71	–	3.6	V	–
Flash AC Specifications							
SID174	$T_{ROWWRITE}$	Row (Block) write time (erase and program)	–	–	16	ms	Row (Block) = 512 bytes
SID175	$T_{ROWERASE}$	Row erase time	–	–	11	ms	–
SID176	$T_{ROWPROGRAM}$	Row program time after erase	–	–	5	ms	–
SID178	$T_{BULKERASE}$	Bulk erase time (1024 KB)	–	–	11	ms	–
SID179	$T_{SECTORERASE}$	Sector erase time (256 KB)	–	–	11	ms	512 rows per sector
SID178S	$T_{SSERIAE}$	Sub-sector erase time	–	–	11	ms	8 rows per sub-sector
SID179S	$T_{SSWRITE}$	Sub-sector write time; 1 erase plus 8 program times	–	–	51	ms	–
SID180S	T_{SWRITE}	Sector write time; 1 erase plus 512 program times	–	–	2.6	seconds	–
SID180	$T_{DEVPROG}$	Total device program time	–	–	30	seconds	–
SID181	F_{END}	Flash endurance	100K	–	–	cycles	–
SID182	F_{RET1}	Flash retention. Ta ≤ 25°C, 100K P/E cycles	10	–	–	years	–
SID182A	F_{RET2}	Flash retention. Ta ≤ 85°C, 10K P/E cycles	10	–	–	years	–
SID182B	F_{RET3}	Flash retention. Ta ≤ 55°C, 20K P/E cycles	20	–	–	years	–
SID256	T_{WS100}	Number of Wait states at 100 MHz	3	–	–		–
SID257	T_{WS50}	Number of Wait states at 50 MHz	2	–	–		–

Note

4. It can take as much as 16 milliseconds to write to flash. During this time, the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

System Resources

Table 24. System Resources

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Power-On-Reset with Brown-out DC Specifications							
Precise POR (PPOR)							
SID190	$V_{FALLPPOR}$	BOD trip voltage in Active and Sleep modes. V_{DDD}.	1.54	–	–	V	BOD Reset guaranteed for levels below 1.54 V
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep. V_{DDD}.	1.54	–	–	V	–
SID192A	V_{DDRAMP}	Maximum power supply ramp rate (any supply)	–	–	100	mV/µs	Active mode
POR with Brown-out AC Specification							
SID194A	V_{DDRAMP_DS}	Maximum power supply ramp rate (any supply) in Deep Sleep	–	–	10	mV/µs	BOD operation guaranteed
Voltage Monitors DC Specifications							
SID195R	V_{HVD0}	–	1.18	1.23	1.27	V	–
SID195	V_{HVDI1}	–	1.38	1.43	1.47	V	–
SID196	V_{HVDI2}	–	1.57	1.63	1.68	V	–
SID197	V_{HVDI3}	–	1.76	1.83	1.89	V	–
SID198	V_{HVDI4}	–	1.95	2.03	2.1	V	–
SID199	V_{HVDI5}	–	2.05	2.13	2.2	V	–
SID200	V_{HVDI6}	–	2.15	2.23	2.3	V	–
SID201	V_{HVDI7}	–	2.24	2.33	2.41	V	–
SID202	V_{HVDI8}	–	2.34	2.43	2.51	V	–
SID203	V_{HVDI9}	–	2.44	2.53	2.61	V	–
SID204	V_{HVDI10}	–	2.53	2.63	2.72	V	–
SID205	V_{HVDI11}	–	2.63	2.73	2.82	V	–
SID206	V_{HVDI12}	–	2.73	2.83	2.92	V	–
SID207	V_{HVDI13}	–	2.82	2.93	3.03	V	–
SID208	V_{HVDI14}	–	2.92	3.03	3.13	V	–
SID209	V_{HVDI15}	–	3.02	3.13	3.23	V	–
SID211	LVI_IDD	Block current	–	5	15	µA	–
Voltage Monitors AC Specification							
SID212	$T_{MONTRIP}$	Voltage monitor trip time	–	–	170	ns	–

SWD Interface

Table 25. SWD and Trace Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SWD and Trace Interface							
SID214	F_SWDCLK2	1.7 V ≤ V_{DDD} ≤ 3.6 V	–	–	25	MHz	LP Mode. V_{CCD} = 1.1 V.
SID214L	F_SWDCLK2L	1.7 V≤ V_{DDD} ≤ 3.6 V	–	–	12	MHz	ULP Mode. V_{CCD} = 0.9 V.
SID215	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 * T	–	–	ns	–
SID216	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 * T	–	–	ns	–
SID217	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5 * T	ns	–
SID217A	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	–
SID214T	F_TRCLK_LP1	With Trace Data setup/hold times of 2/1 ns respectively	–	–	50	MHz	LP Mode. V_{DD} = 1.1 V.
SID215T	F_TRCLK_LP2	With Trace Data setup/hold times of 3/2 ns respectively	–	–	50	MHz	LP Mode. V_{DD} = 1.1 V.
SID216T	F_TRCLK_ULP	With Trace Data setup/hold times of 3/2 ns respectively	–	–	20	MHz	ULP Mode. V_{DD} = 0.9 V.

Internal Main Oscillator

Table 26. IMO DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 8 MHz	–	9	15	µA	–

Table 27. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	$F_{IMOTOL1}$	Frequency variation centered on 8 MHz	–	–	±2	%	–
SID227	T_{JITR}	Cycle-to-Cycle and Period jitter	–	250	–	ps	–

Internal Low-Speed Oscillator

Table 28. ILO DC Specification

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_{ILO2}	ILO operating current at 32 kHz	–	0.3	0.7	µA	–

Table 29. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	$T_{STARTILO1}$	ILO startup time	–	–	7	µs	Startup time to 95% of final frequency
SID236	TLIODUTY	ILO Duty cycle	45	50	55	%	–
SID237	$F_{ILOTRIM1}$	32 kHz trimmed frequency	28.8	32	36.1	kHz	

Crystal Oscillator Specifications

Table 30. ECO Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
MHz ECO DC Specifications							
SID316	I_{DD_MHz}	Block operating current with Cload up to 18 pF	–	800	1600	µA	Max = 33 MHz, Type = 16 MHz
MHz ECO AC Specifications							
SID317	F_MHz	Crystal frequency range	4	–	35	MHz	–
kHz ECO DC Specification							
SID318	I_{DD_kHz}	Block operating current with 32-kHz crystal	–	0.38	1	µA	–
SID321E	ESR32K	Equivalent series resistance	–	80	–	kΩ	–
SID322E	PD32K	Drive level	–	–	1	µW	–
kHz ECO AC Specification							
SID319	F_kHz	32 kHz trimmed frequency	–	32.768	–	kHz	–
SID320	Ton_kHz	Startup time	–	–	500	ms	–
SID320E	F_{TOL32K}	Frequency tolerance	–	50	250	ppm	–

External Clock Specifications

Table 31. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305	$EXTCLK_{FREQ}$	External clock input frequency	0	–	100	MHz	–
SID306	$EXTCLK_{DUTY}$	Duty cycle; measured at $V_{DD}/2$	45	–	55	%	–

PLL Specifications

Table 32. PLL Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305P	PLL_LOCK	Time to achieve PLL lock	–	16	35	µs	–
SID306P	PLL_OUT	Output frequency from PLL block	–	–	150	MHz	–
SID307P	PLL_IDD	PLL current	–	0.55	1.1	mA	Typ. at 100 MHz out.
SID308P	PLL_JTR	Period jitter	–	–	150	ps	100 MHz output frequency

Table 33. Clock Source Switching Time

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID262	$TCLK_{SWITCH}$	Clock switching from clk1 to clk2 in clock periods; for example, from IMO (clk1) to FLL (clk2).	–	–	4 clk1 + 3 clk2	periods	–

FLL Specifications

Table 34. Frequency Locked Loop (FLL) Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
Frequency Locked Loop (FLL) Specifications							
SID450	FLL_RANGE	Input frequency range.	0.001	–	100	MHz	Lower limit allows lock to USB SOF signal (1 kHz). Upper limit is for External input.
SID451	FLL_OUT_DIV2	Output frequency range. V_{CCD} = 1.1 V	24.00	–	100.00	MHz	Output range of FLL divided-by-2 output
SID451A	FLL_OUT_DIV2	Output frequency range. V_{CCD} = 0.9 V	24.00	–	50.00	MHz	Output range of FLL divided-by-2 output
SID452	FLL_DUTY_DIV2	Divided-by-2 output; High or Low	47.00	–	53.00	%	–
SID454	FLL_WAKEUP	Time from stable input clock to 1% of final value on Deep Sleep wakeup	–	–	7.50	µs	With IMO input, less than 10 °C change in temperature while in Deep Sleep, and Fout ≥ 50 MHz.
SID455	FLL_JITTER	Period jitter (1 sigma) at 100 MHz	–	–	35.00	ps	50 ps at 48 MHz, 35 ps at 100 MHz
SID456	FLL_CURRENT	CCO + Logic current	–	–	5.50	µA/MHz	–

USB

Table 35. USB Specifications (USB requires LP Mode 1.1-V internal supply)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
USB Block Specifications							
SID322U	Vusb_3.3	Device supply for USB operation	3.15	–	3.6	V	USB Configured, USB Reg. bypassed
SID323U	Vusb_3.3	Device supply for USB operation (functional operation only)	2.85	–	3.6	V	USB Configured, USB Reg. bypassed
SID325U	Iusb_config	Device supply current in Active mode	–	8	–	mA	VDDD = 3.3 V
SID328	Isub_suspend	Device supply current in Sleep mode	–	0.5	–	mA	VDDD = 3.3 V, PICU wakeup
SID329	Isub_suspend	Device supply current in Sleep mode	–	0.3	–	mA	VDDD = 3.3 V, Device disconnected
SID330U	USB_Drive_Res	USB driver impedance	28	–	44	Ω	Series resistors are on chip
SID331U	USB_Pulldown	USB pull-down resistors in Host mode	14.25	–	24.8	kΩ	–
SID332U	USB_Pullup_Idle	Idle mode range	900	–	1575	Ω	Bus idle
SID333U	USB_Pullup	Active mode	1425	–	3090	Ω	Upstream device transmitting

QSPI

Table 36. QSPI Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SMIF QSPI Specifications. All specs with 15-pF load.							
SID390Q	Fsmifclock	SMIF QSPI output clock frequency	–	–	80	MHz	LP mode (1.1 V)
SID390QU	Fsmifclocku	SMIF QSPI output clock frequency	–	–	50	MHz	ULP mode (0.9 V). Guaranteed by Char.
SID397Q	Idd_qspi	Block current in LP mode (1.1 V)	–	–	1900	µA	LP mode (1.1 V)
SID398Q	Idd_qspi_u	Block current in ULP mode (0.9 V)	–	–	590	µA	ULP mode (0.9 V)
SID391Q	Tsetup	Input data set-up time with respect to clock capturing edge	4.5	–	–	ns	Guaranteed by characterization
SID392Q	Tdatahold	Input data hold time with respect to clock capturing edge	0	–	–	ns	–
SID393Q	Tdataoutvalid	Output data valid time with respect to clock falling edge	–	–	3.7	ns	7.5-ns max for ULP mode (0.9 V)
SID394Q	Tholdtime	Output data hold time with respect to clock rising edge	3	–	–	ns	–
SID395Q	Tseloutvalid	Output Select valid time with respect to clock rising edge	–	–	7.5	ns	15-ns max for ULP mode (0.9 V)
SID396Q	Tselouthold	Output Select hold time with respect to clock rising edge	0.5*Tsclk	–	–	ns	Tsclk = Fsmifclk cycle time

Audio Subsystem

Table 37. Audio Subsystem Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
Audio Subsystem specifications							
PDM Specifications							
SID400P	PDM_IDD1	PDM Active current, stereo operation, 1-MHz clock	–	175	–	µA	16-bit audio at 16 ksps
SID401	PDM_IDD2	PDM Active current, stereo operation, 3-MHz clock	–	600	–	µA	24-bit audio at 48 ksps
SID402	PDM_JITTER	RMS jitter in PDM clock	–200	–	200	ps	–
SID403	PDM_CLK	PDM clock speed	0.384	–	3.072	MHz	–
SID403A	PDM_BLK_CLK	PDM block input clock	1.024	–	49.152	MHz	–
SID403B	PDM_SETUP	Data input set-up time to PDM_CLK edge	10	–	–	ns	–
SID403C	PDM_HOLD	Data input hold time to PDM_CLK edge	10	–	–	ns	–
SID404	PDM_OUT	Audio sample rate	8	–	48	ksps	–
SID405	PDM_WL	Word length	16	–	24	bits	–
SID406	PDM_SNR	Signal-to-Noise Ratio (A-weighted)	–	100	–	dB	PDM input, 20 Hz to 20 kHz BW
SID407	PDM_DR	Dynamic range (A-weighted)	–	100	–	dB	20 Hz to 20 kHz BW, -60 dB FS
SID408	PDM_FR	Frequency response	–0.2	–	0.2	dB	DC to 0.45f, DC Blocking filter off.
SID409	PDM_SB	Stop band	–	0.566	–	f	–

Table 37. Audio Subsystem Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID410	PDM_SBA	Stop band attenuation	–	60	–	dB	–
SID411	PDM_GAIN	Adjustable gain	–12	–	10.5	dB	PDM to PCM, 1.5 dB/step
SID412	PDM_ST	Startup time	–	48	–		WS (Word Select) cycles
I2S Specifications. The same for LP and ULP modes unless stated otherwise.							
SID413	I2S_WORD	Length of I2S Word	8	–	32	bits	
SID414	I2S_WS	Word clock frequency in LP mode	–	–	192	kHz	12.288-MHz bit clock with 32-bit word
SID414M	I2S_WS_U	Word clock frequency in ULP mode	–	–	48	kHz	3.072-MHz bit clock with 32-bit word
SID414A	I2S_WS_TDM	Word clock frequency in TDM mode for LP	–	–	48	kHz	Eight 32-bit channels
SID414X	I2S_WS_TDM_U	Word clock frequency in TDM mode for ULP	–	–	12	kHz	Eight 32-bit channels
I2S Slave Mode							
SID430	TS_WS	WS setup time to the following rising edge of SCK for LP mode	5	–	–	ns	–
SID430U	TS_WS_U	WS setup time to the following rising edge of SCK for ULP mode	11	–	–	ns	–
SID430A	TH_WS	WS hold time to the following edge of SCK	TMCLK_SOC+5	–	–	ns	–
SID432	TD_SDO	Delay time of TX_SDO transition from edge of TX_SCK for LP mode	-(TMCLK_SOC+25)	–	TMCLK_SOC+25	ns	Associated clock edge depends on selected polarity
SID432U	TD_SDO_U	Delay time of TX_SDO transition from edge of TX_SCK for ULP mode	-(TMCLK_SOC+70)	–	TMCLK_SOC+70	ns	Associated clock edge depends on selected polarity
SID433	TS_SDI	RX_SDI setup time to the following edge of RX_SCK in LP mode	5	–	–	ns	–
SID433U	TS_SDI_U	RX_SDI setup time to the following edge of RX_SCK in ULP mode	11	–	–	ns	–
SID434	TH_SDI	RX_SDI hold time to the rising edge of RX_SCK	TMCLK_SOC+5	–	–	ns	–
SID435	TSCKCY	TX/RX_SCK bit clock duty cycle	45	–	55	%	–
I2S Master Mode							
SID437	TD_WS	WS transition delay from falling edge of SCK in LP mode	–10	–	20	ns	–
SID437U	TD_WS_U	WS transition delay from falling edge of SCK in ULP mode	–10	–	40	ns	–
SID438	TD_SDO	SDO transition delay from falling edge of SCK in LP mode	–10	–	20	ns	–
SID438U	TD_SDO	SDO transition delay from falling edge of SCK in ULP mode	–10	–	40	ns	–
SID439	TS_SDI	SDI setup time to the associated edge of SCK	5	–	–	ns	Associated clock edge depends on selected polarity

Table 37. Audio Subsystem Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID440	TH_SDI	SDI hold time to the associated edge of SCK	TMCLK_SOC+5	–	–	ns	T is TX/RX_SCK Bit Clock period. Associated clock edge depends on selected polarity.
SID443	TSCKCY	SCK bit clock duty cycle	45	–	55	%	–
SID445	FMCLK_SOC	MCLK_SOC frequency in LP mode	1.024	–	98.304	MHz	FMCLK_SOC = 8*Bit-clock
SID445U	FMCLK_SOC_U	MCLK_SOC frequency in ULP mode	1.024	–	24.576	MHz	FMCLK_SOC_U = 8 * Bit-clock
SID446	TMCLKCY	MCLK_SOC duty cycle	45	–	55	%	–
SID447	TJITTER	MCLK_SOC input jitter	–100	–	100	ps	–

Smart I/O

Table 38. Smart I/O Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID420	SMIO_BYP	Smart I/O bypass delay	–	–	2	ns	–
SID421	SMIO_LUT	Smart I/O LUT prop delay	–	8	–	ns	–

SDHC and eMMC

Table 39. SDHC and eMMC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SDHC and eMMC Specifications (Block Clock must be divided by 2 or more when used as source in DDR modes. Use Drive select 1; Refer to Errata for details)							
SID_SD391	SD_TR	Input transition time	0.7	–	3	ns	–
SD:DS Timing							
SID_SD392	SD_CLK	Interface clock period (LP mode)	–	–	25	MHz	(40 ns period)
SID_SD393	SD_CLK	Interface clock period (ULP mode)	–	–	8	MHz	(125 ns period)
SID_SD394	SD_DCMD_CL	I/O loading at DATA/CMD pins	30	–	30	pF	–
SID_SD395	SD_CLK_CL	I/O loading at CLK pins	30	–	30	pF	–
SID_SD396	SD_TS_OUT	Output: Setup time of CMD/DAT prior to CLK	5.1	–	–	ns	–
SID_SD397	SD_HLD_OUT	Output: Hold time of CMD/DAT after CLK	5.1	–	–	ns	–
SID_SD398	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (LP mode)	24	–	–	ns	–
SID_SD399	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (ULP mode)	109	–	–	ns	–
SID_SD400	SD_HLD_IN	Input: Hold time of CMD/DAT after CLK	2.1	–	–	ns	–
SD:HS Timing							
SID_SD401	SD_CLK	Interface clock period (LP mode)	–	–	45	MHz	(20 ns period)
SID_SD402	SD_CLK	Interface clock period (ULP mode)	–	–	16	MHz	(62.5 ns period)
SID_SD403	SD_DCMD_CL	I/O loading at DATA/CMD pins	30	-	30	pF	–
SID_SD404	SD_CLK_CL	I/O loading at CLK pins	30	–	30	pF	–
SID_SD405	SD_TS_OUT	Output: Setup time of CMD/DAT prior to CLK	6.1	–	–	ns	–
SID_SD406	SD_HLD_OUT	Output: Hold time of CMD/DAT after CLK	2.1	–	–	ns	–
SID_SD407	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (LP mode)	8	–	–	ns	–
SID_SD408	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (ULP mode)	48	–	–	ns	–
SID_SD409	SD_HLD_IN	Input: Hold time of CMD/DAT after CLK	2.5	–	–	ns	–
SD:SDR-12 Timing							
SID_SD410	SD_CLK	Interface clock period (LP mode)	–	–	25	MHz	(40 ns period)
SID_SD411	SD_CLK	Interface clock period (ULP mode)	–	–	8	MHz	(125 ns period)
SID_SD412	SD_CLK_DC	Duty cycle of output CLK	30	–	70	%	–
SID_SD413	SD_DCMD_CL	I/O loading at DATA/CMD pins	30	–	30	pF	–
SID_SD414	SD_CLK_CL	I/O loading at CLK pins	30	–	30	pF	–
SID_SD415	SD_TS_OUT	Output: Setup time of CMD/DAT prior to CLK	3.1	–	–	ns	–
SID_SD416	SD_HLD_OUT	Output: Hold time of CMD/DAT after CLK	0.9	–	–	ns	–
SID_SD417	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (LP mode)	24	–	–	ns	–
SID_SD418	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (ULP mode)	109	–	–	ns	–

Table 39. SDHC and eMMC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID_SD419	SD_HLD_IN	Input: Hold time of CMD/DAT after CLK	1.85	–	–	ns	–
SD:SDR-25 Timing							
SID_SD420	SD_CLK	Interface clock period (LP mode)	–	–	50	MHz	(20 ns period)
SID_SD421	SD_CLK	Interface clock period (ULP mode)	–	–	16	MHz	(62.5 ns period)
SID_SD422	SD_CLK_DC	Duty cycle of output CLK	30	–	70	%	–
SID_SD423	SD_DCMD_CL	I/O loading at DATA/CMD pins	30	–	30	pF	–
SID_SD424	SD_CLK_CL	I/O loading at CLK pins	30	–	30	pF	–
SID_SD425	SD_TS_OUT	Output: Setup time of CMD/DAT prior to CLK	3.1	–	–	ns	–
SID_SD426	SD_HLD_OUT	Output: Hold time of CMD/DAT after CLK	0.9	–	–	ns	–
SID_SD427	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (LP mode)	5.8	–	–	ns	–
SID_SD428	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (ULP mode)	48	–	–	ns	–
SID_SD429	SD_HLD_IN	Input: Hold time of CMD/DAT after CLK	1.8	–	–	ns	–
SD:SDR-50 Timing							
SID_SD430	SD_CLK	Interface clock period (LP mode)	–	–	80	MHz	(12.5 ns period)
SID_SD431	SD_CLK	Interface clock period (ULP mode)	–	–	32	MHz	(31.25 ns period)
SID_SD432	SD_CLK_DC	Duty cycle of output CLK	30	–	70	%	–
SID_SD433	SD_DCMD_CL	I/O loading at DATA/CMD pins	20	–	20	pF	–
SID_SD434	SD_CLK_CL	I/O loading at CLK pins	20	–	20	pF	–
SID_SD435	SD_TS_OUT	Output: Setup time of CMD/DAT prior to CLK	3.1	–	–	ns	–
SID_SD436	SD_HLD_OUT	Output: Hold time of CMD/DAT after CLK	0.9	–	–	ns	–
SID_SD437	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (LP mode)	5	–	–	ns	–
SID_SD438	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (ULP mode)	23	–	–	ns	–
SID_SD439	SD_HLD_IN	Input: Hold time of CMD/DAT after CLK	1.8	–	–	ns	–
SD:DDR-50 Timing							
SID_SD440	SD_CLK	Interface clock period (LP mode)	–	–	40	MHz	(25 ns period).
SID_SD441	SD_CLK	Interface clock period (ULP mode)	–	–	16	MHz	(62.5 ns period)
SID_SD442	SD_CLK_DC	Duty cycle of output CLK	45	–	55	%	–
SID_SD443	SD_DCMD_CL	I/O loading at DATA/CMD pins	30	–	30	pF	–
SID_SD444	SD_CLK_CL	I/O loading at CLK pins	30	–	30	pF	–
SID_SD445	SD_TS_OUT	Output: Setup time of CMD/DAT prior to CLK	3.1	–	–	ns	–
SID_SD446	SD_HLD_OUT	Output: Hold time of CMD/DAT after CLK	0.9	–	–	ns	–
SID_SD447	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (LP mode)	5.75	–	–	ns	–
SID_SD448	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (ULP mode)	24	–	–	ns	–
SID_SD449	SD_HLD_IN	Input: Hold time of CMD/DAT after CLK	1.8	–	–	ns	–

Table 39. SDHC and eMMC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
eMMC:BWC Timing							
SID_SD450	SD_CLK	Interface clock period (LP mode)	–	–	26	MHz	(38.4 ns period)
SID_SD451	SD_CLK	Interface clock period (ULP mode)	–	–	8	MHz	(125 ns period)
SID_SD452	SD_DCMD_CL	I/O loading at DATA/CMD pins	30	–	30	pF	–
SID_SD453	SD_CLK_CL	I/O loading at CLK pins	30	–	30	pF	–
SID_SD454	SD_TS_OUT	Output: Setup time of CMD/DAT prior to CLK	3.1	–	–	ns	–
SID_SD455	SD_HLD_OUT	Output: Hold time of CMD/DAT after CLK	3.1	–	–	ns	–
SID_SD456	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (LP mode)	9.7	–	–	ns	–
SID_SD457	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (ULP mode)	96	–	–	ns	–
SID_SD458	SD_HLD_IN	Input: Hold time of CMD/DAT after CLK	8.3	–	–	ns	–
eMMC:SDR Timing							
SID_SD459	SD_CLK	Interface clock period (LP mode)	–	–	52	MHz	(19.2 ns period)
SID_SD460	SD_CLK	Interface clock period (ULP mode)	–	–	16	MHz	(62.5 ns period)
SID_SD461	SD_DCMD_CL	I/O loading at DATA/CMD pins	30	–	30	pF	–
SID_SD462	SD_CLK_CL	I/O loading at CLK pins	30	–	30	pF	–
SID_SD463	SD_TS_OUT	Output: Setup time of CMD/DAT prior to CLK	3.1	–	–	ns	–
SID_SD464	SD_HLD_OUT	Output: Hold time of CMD/DAT after CLK	3.1	–	–	ns	–
SID_SD465	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (LP mode)	5.3	–	–	ns	–
SID_SD466	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (ULP mode)	48	–	–	ns	–
SID_SD467	SD_HLD_IN	Input: Hold time of CMD/DAT after CLK	2.5	–	–	ns	–
eMMC:DDR Timing							
SID_SD468	SD_CLK	Interface clock period (LP mode)	–	–	52	MHz	–
SID_SD469	SD_CLK	Interface clock period (ULP mode)	–	–	16	MHz	(62.5 ns period)
SID_SD470	SD_CLK_DC	Dutycycle requirement at output CLK	40	–	60	%	–
SID_SD471	SD_DCMD_CL	I/O loading at DATA/CMD pins	20	–	20	pF	–
SID_SD472	SD_CLK_CL	I/O loading at CLK pins	20	–	20	pF	–
SID_SD473	SD_TS_OUT	Output: Setup time of CMD/DAT prior to CLK	2.6	–	–	ns	–
SID_SD474	SD_HLD_OUT	Output: Hold time of CMD/DAT after CLK	2.6	–	–	ns	–
SID_SD475	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (LP mode)	10	–	–	ns	–
SID_SD476	SD_TS_IN	Input: Setup time of CMD/DAT prior to CLK (ULP mode)	32	–	–	ns	–
SID_SD477	SD_HLD_IN	Input: Hold time of CMD/DAT after CLK	1.5	–	–	ns	–

JTAG Boundary Scan

Table 40. JTAG Boundary Scan

Spec ID#		Parameter	Description	Min	Typ	Max	Units
JTAG Boundary Scan Parameters							
JTAG Boundary Scan Parameters for 1.1 V (LP) Mode Operation:							
SID468	TCKLOW	TCK LOW	52	–	–	ns	–
SID469	TCKHIGH	TCK HIGH	10	–	–	ns	–
SID470	TCK_TDO	TCK falling edge to output valid		–	40	ns	–
SID471	TSU_TCK	Input valid to TCK rising edge	12	–	–	ns	–
SID472	TCk_THD	Input hold time to TCK rising edge	10	–	–	ns	–
SID473	TCK_TDOV	TCK falling edge to output valid (High-Z to Active).	40	–	–	ns	_
SID474	TCK_TDOZ	TCK falling edge to output valid (Active to High-Z).	40	–	–	ns	_
JTAG Boundary Scan Parameters for 0.9 V (ULP) Mode Operation:							
SID468A	TCKLOW	TCK low	102	–	–	ns	–
SID469A	TCKHIGH	TCK high	20	–	–	ns	–
SID470A	TCK_TDO	TCK falling edge to output valid		–	80	ns	–
SID471A	TSU_TCK	Input valid to TCK rising edge	22	–	–	ns	–
SID472A	TCk_THD	Input hold time to TCK rising edge	20	–	–	ns	–
SID473A	TCK_TDOV	TCK falling edge to output valid (high-Z to active).	80	–	–	ns	_
SID474A	TCK_TDOZ	TCK falling edge to output valid (active to high-Z).	80	–	–	ns	_

Ordering Information

Table 41 lists the CY8C62x8 and CY8C62xA part numbers and features. All devices include the following standard features:

- Dual CPU
- 13 Serial Communication Blocks
- 32 Timer/Counter/Pulse-Width Modulators
- 2 Secure Digital Host Controllers
- 12-bit Successive Approximation ADC
- Full-Speed USB

Table 41. Ordering Information

Family	Base Features	MPN	CM4 CPU Speed (LP/ULP)	CM0+ CPU Speed (LP/ULP)	Power Modes	Flash (KB)	SRAM (KB)	CapSense	Crypto	GPIO	Pin	Package
62	Arm CM4/CM0+, DC-DC converter 12-bit SAR ADC, 2 LPCOMPs, 13 SCBs, 2 I2S, 2 PDM, 2 SDHC, 1 FS-USB	CY8C624ABZI-S2D04	150/50	100/25	FLEX	2048	1024	–	–	104	124	BGA
		CY8C624ABZI-S2D14	150/50	100/25	FLEX	2048	1024	Y	–	104	124	BGA
		CY8C624AAZI-S2D14	150/50	100/25	FLEX	2048	1024	Y	–	104	128	TQFP
		CY8C624ABZI-S2D44	150/50	100/25	FLEX	2048	1024	Y	Y	104	124	BGA
		CY8C624AAZI-S2D44	150/50	100/25	FLEX	2048	1024	Y	Y	104	128	TQFP
		CY8C624AFNI-S2D43	150/50	100/25	FLEX	2048	1024	Y	Y	80	100	WLCSP
		CY8C624ALQI-S2D42	150/50	100/25	FLEX	2048	1024	Y	Y	51	68	QFN
		CY8C6248AZI-S2D14	150/50	100/25	FLEX	1024	512	Y	–	104	128	TQFP
		CY8C6248BZI-S2D44	150/50	100/25	FLEX	1024	512	Y	Y	104	124	BGA
		CY8C6248AZI-S2D44	150/50	100/25	FLEX	1024	512	Y	Y	104	128	TQFP
		CY8C6248FNI-S2D43	150/50	100/25	FLEX	1024	512	Y	Y	80	100	WLCSP

The nomenclature used in the preceding table is based on the following part numbering convention:
CY8C 6 A B C DD E – (FF) G H I (JJ) (K) (L)

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
6	Architecture	6	PSoC 6
A	Family	0	Value
		1	Programmable
		2	Performance
		3	Connectivity
B	Speed[5]	2	100 MHz
		3	150 MHz
		4	150/50 MHz
C	Memory Size (Flash/SRAM)	6	512 KB/128 KB
		7	1024 KB/288 KB
		8	1024 KB/512 KB
		A	2048 KB/1024 KB
DD	Package	AX	TQFP I (0.8-mm pitch)
		AZ	TQFP II (0.5-mm pitch)
		LQ	QFN
		BZ	BGA
		FM	M-CSP
		FN	WLCSP
E	Temperature Range	C	Consumer
		I	Industrial
		Q	Extended Industrial
FF	Feature Code		Standard MCU
		BL	Integrated BLE
G	CPU core	F	Single CPU
		D	Dual CPU
H	Attribute code	0-9	Feature set
I	GPIO count	1	31-50
		2	51-70
		3	71-90
		4	91-110
JJ	Engineering sample (optional)	ES	Engineering samples or not
K	Silicon revision		A0 (Base rev)
		1-9	A1, A2, A3 ...
L	Tape/reel shipment (optional)	T	Tape and reel shipment

Note
5. When two numbers are shown, they are the maximum CPU speed in System Low Power mode and System Ultra Low Power mode, respectively

Packaging

PSoC 62 will be offered in 124-BGA, 128-TQFP, and 100-WLCSP packages.

Table 42. Package Dimensions

Spec ID#	Package	Description	Package Dwg #
PKG_1	124-BGA	124 BGA, 9 mm × 9 mm × 1 mm height with 0.65-mm pitch	001-97718
PKG_2	128-TQFP	128 TQFP, 14 mm × 20 mm × 1.4 mm height with 0.5-mm pitch	51-85101
PKG_3	100-WLCSP	100 WLCSP, 4.1 mm × 3.9 mm × 0.5 mm height with 0.5-mm pitch	002-23991

Table 43. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	–	–40	25	85	°C
T_J	Operating junction temperature	–	–40	–	100	°C
T_{JA}	Package θ_{JA} (124-BGA)	–	–	32	–	°C/watt
T_{JA}	Package θ_{JA} (128-TQFP)	–	–	34	–	°C/watt
T_{JA}	Package θ_{JA} (100-WLCSP)	–	–	19	–	°C/watt

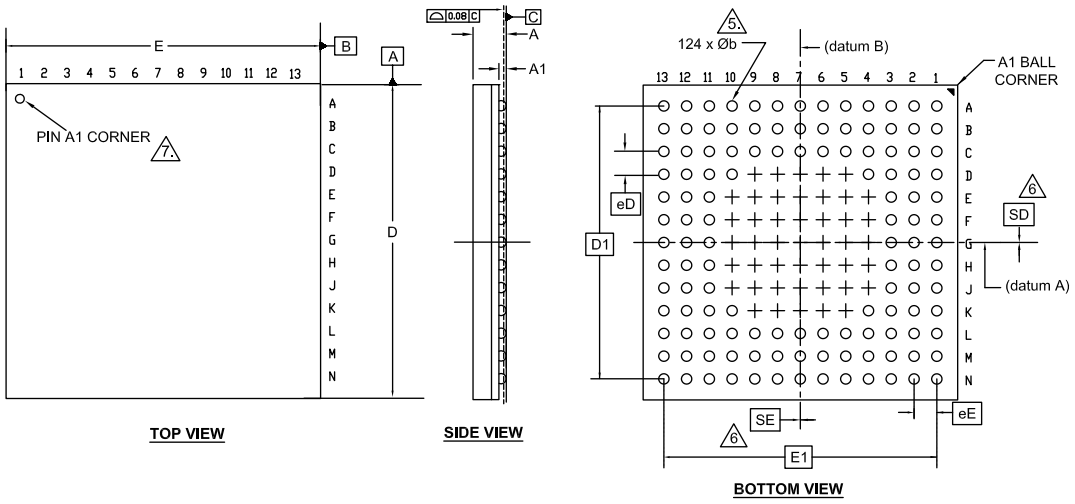
Table 44. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
All packages	260°C	30 seconds

Table 45. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
124-BGA and 128-TQFP	MSL 3
100-WLCSP	MSL 1

Figure 8. 124-BGA 9.0 × 9.0 ×1.0 mm



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	0.21	0.26
D	8.90	9.00	9.10
E	8.90	9.00	9.10
D1	7.80 BSC		
E1	7.80 BSC		
MD	13		
ME	13		
N	124		
Ø b	0.25	0.30	0.35
eD	0.65 BSC		
eE	0.65 BSC		
SD	0		
SE	0		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF. : MO-280.

001-97718 *B

Figure 9. 128-TQFP 14.0 × 20.0 ×1.4 mm

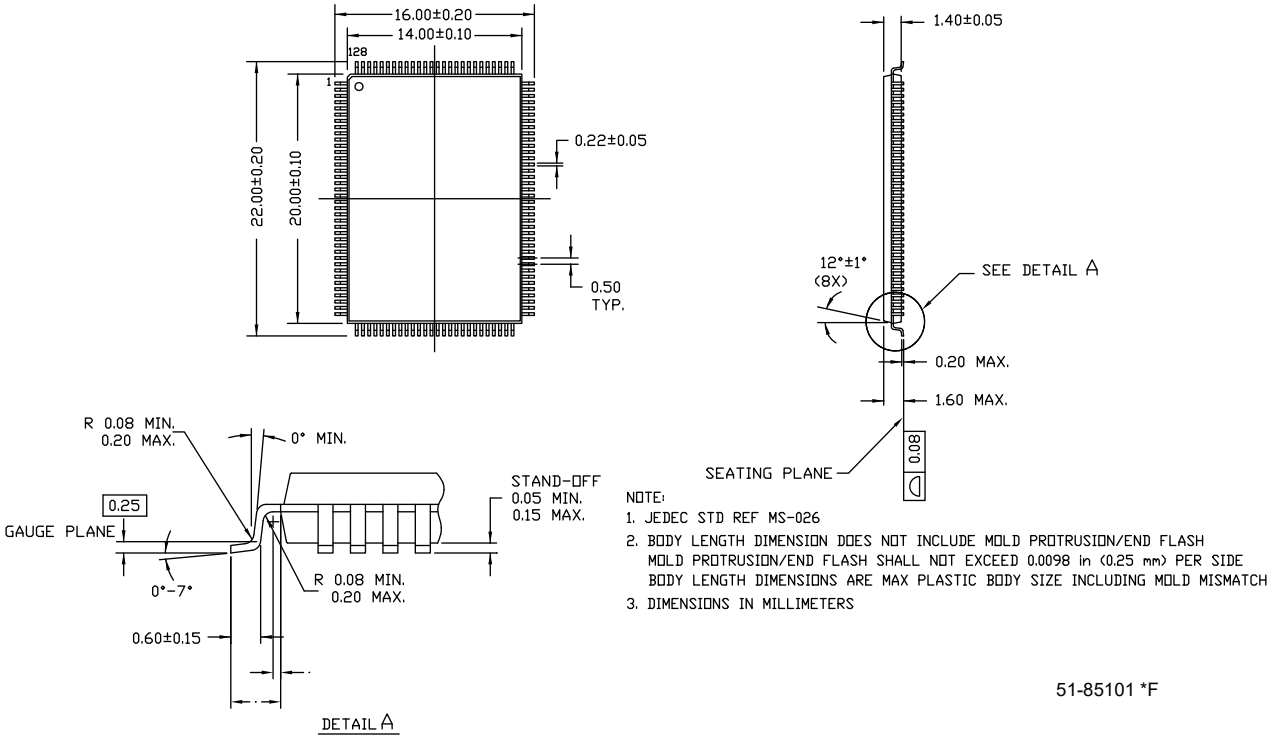
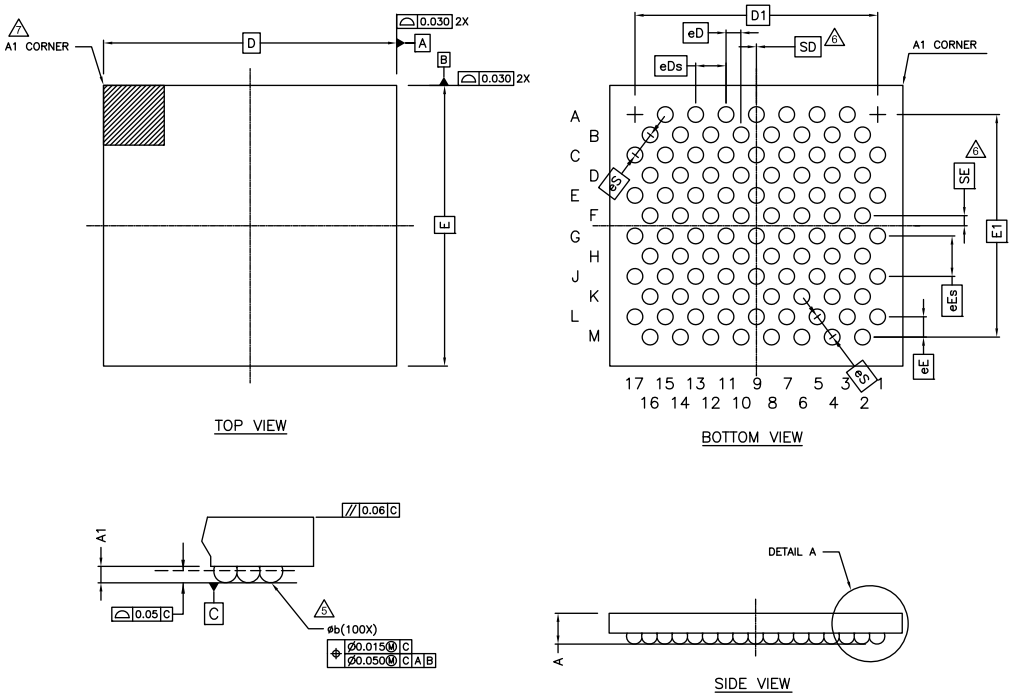


Figure 10. 100-WLCSP 4.1068 × 3.9025 × 0.467mm



SYMBOL	DIMENSIONS		
	MIN	NOM	MAX
A	-	-	0.467
A1	0.122	-	-
D	4.1068 BSC		
E	3.9025 BSC		
D1	3.36 BSC		
E1	3.08 BSC		
MD	17		
ME	12		
N	100		
Øb	0.188	0.218	0.248
eD	0.21 BSC		
eE	0.28 BSC		
eDs	0.42 BSC		
eEs	0.56 BSC		
eS	0.35 BSC		
SD	0.00 BSC		
SE	0.14 BSC		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF. : N/A.

002-23991 *A

Errata

This section describes the errata for the PSoC 62 devices. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Compare this document to the device's datasheet for a complete functional description.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Device Characteristics
PSoC 62	PSoC 62 Product Family

PSoC 62 Qualification Status

Engineering Samples

PSoC 62 Errata Summary

Noise is caused in supply and ground traces when multiple outputs switch. The amount of noise is dependent on the number of outputs, the drive strength of the output drivers, the frequency of the switching, and the impact on specific ports. The noise is worse at higher voltages (V_{DD} = 2.7 V and higher) and should not be an issue with 1.8 V externally regulated (that is, V_{DD} = 1.8 V ±5%) designs.

For cases where there are large numbers of GPIOs switching simultaneously, the following errata conditions are applicable. Note that the exact number cannot be specified as there are too many system-dependent conditions.

This table defines the errata applicability to available PSoC 62 family devices.

Items	PSoC 62	Silicon Revision	Fix Status
[1] Drive mode strength must be limited.	All	First silicon	No fix planned
[2] CapSense use is restricted to Ports 6 and 7 with switching restrictions on other ports.	All	First silicon	No fix planned
[3] Switching noise can cause ADC errors due to voltage reference noise.	All	First silicon	No fix planned
[4] Port Usage restrictions must be applied.	All	First silicon	No fix planned

1. Drive mode strength must be limited.	
Problem Definition	There are four Drive mode strengths: DM0, DM1, DM2, and DM3, DM0 being the strongest and DM3 the weakest in order. Usage of DM0 can cause noise in supply and ground lines for simultaneous outputs switching. Drive mode strength must be limited to DM2 for all GPIOs except for the 80 MHz QSPI clock which may use DM1. The V_{OL} and V_{OH} specs are affected as follows (also applies to V_{DDIO}, V_{DDIOA}, and V_{DDA} pins): V_{DD} < 2.7 V: V_{OL} = 0.5 V @ I_{OL} = 6 mA. V_{OH} = V_{DD} – 0.5 V, I_{OH} = 6 mA. V_{DD} ≥ 2.7 V: V_{OL} = 0.4 @ I_{OL} = 6 mA. V_{OH} = V_{DD} – 0.5 V, I_{OH} = 6 mA.
Parameters Affected	Drive mode settings.
Trigger Condition(s)	Simultaneous outputs switching with high drive strength
Scope of Impact	Causes supply and ground noise, which can affect ADC and CapSense operation
Workaround	Follow drive mode strength restrictions. Drive Mode 2 (DM2) should be used for all ports except for the 80-MHz QSPI clock, which should be DM1
Fix Status	No fix planned.

2. CapSense use is restricted to Ports 6 and 7 with switching restrictions on other ports.	
Problem Definition	GPIO simultaneous switching creates noise which can affect CapSense accuracy in unrestricted use
Parameters Affected	CapSense sensitivity and accuracy
Trigger Condition(s)	Noise caused by GPIO simultaneous output switching during CapSense operation
Scope of Impact	CapSense may produce erroneous results due to noise coupling from switching GPIOs.
Workaround	For CapSense usage, the following restrictions apply: a. Limit switching on Port 1 to 1 MHz (no more than 2 outputs) with slow slew rate. b. CapSense pins are restricted to Ports 6 and 7. No other GPIO output activity is allowed on Ports 6 and 7. c. Switching in Ports 5 and 8 is restricted to 1 MHz (no more than 2 outputs) with slow slew rate setting. CapSense must use the SRSS reference.
Fix Status	No fix planned.

3. Switching noise can cause ADC errors due to voltage reference noise.	
Problem Definition	12-bit SAR ADC Counts are affected by switching noise
Parameters Affected	ADC accuracy
Trigger Condition(s)	Switching noise caused by GPIO simultaneous switching
Scope of Impact	ADC accuracy will be impacted
Workaround	Restrict switching on Ports 9 and 10 (analog input ports). The Programmable Analog Sub-System (PASS), including the SAR ADC, is connected to Ports 9 and 10. With no switching on Ports 9 and 10, the ADC error may be up to 4 LSB counts. Switching in Ports 9 and 10 is restricted to 1 MHz (no more than 2 outputs) with slow slew rate setting and, in this case, the ADC error may be up to 12 counts.
Fix Status	No fix planned.

4. Port Usage restrictions must be applied.	
Problem Definition	GPIO simultaneous switching causes supply and ground noise that adversely affects other on-chip subsystems).
Parameters Affected	CapSense and ADC results
Trigger Condition(s)	GPIO simultaneous switching with unrestricted strengths and frequency.
Scope of Impact	Incorrect results may cause false sensing or failure to sense for CapSense and inaccurate results for the SAR ADC (may not deliver 12-bit accuracy).
Workaround	Follow Port Usage restrictions: a. Switching on Port 0 must be restricted to less than 8 MHz. b. Switching on Port 1 must be restricted to less than 1 MHz with slow rate and no more than 2 outputs. c. Ports 9 and 10 must be restricted to 8 MHz when not using the ADC and the restrictions stated earlier used when the ADC is used. d. Use VREF from System Resource Subsystem (SRSS) for CapSense
Fix Status	No fix planned.

Acronyms

Acronym	Description
3DES	triple DES (data encryption standard)
ADC	analog-to-digital converter
ADMA3	advanced DMA version 3, a Secure Digital data transfer mode
AES	advanced encryption standard
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm data transfer bus
AMUX	analog multiplexer
AMUXBUS	analog multiplexer bus
API	application programming interface
Arm®	advanced RISC machine, a CPU architecture
BGA	ball grid array
BOD	brown-out detect
BREG	backup registers
BWC	backward compatibility (eMMC data transfer mode)
CAD	computer aided design
CCO	current controlled oscillator
ChaCha	a stream cipher
CM0+	Cortex-M0+, an Arm CPU
CM4	Cortex-M4, an Arm CPU
CMAC	cypher-based messge authentication code
CMOS	complementary metal-oxide-semicondutor, a process technology for IC fabrication
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CSD	CapSense Sigma-Delta
CSV	clock supervisor
CSX	Cypress mutual capacitance sensing method. See also CSD
CTI	cross trigger interface
DAC	digital-to-analog converter, see also IDAC, VDAC
DAP	debug access port
DDR	double data rate
DES	data encryption standard
DFT	design for test
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DSI	digital system interconnect
DU	data unit
DW	data wire, a DMA implementation
ECC	error correcting code

Acronym	Description
ECC	elliptic curve cryptography
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
eMMC	embedded MultiMediaCard
ESD	electrostatic discharge
ETM	embedded trace macrocell
FIFO	first-in, first-out
FLL	frequency locked loop
FPU	floating-point unit
FS	full-speed
GND	Ground
GPIO	general-purpose input/output, applies to a PSoC pin
HMAC	Hash-based message authentication code
HSIOM	high-speed I/O matrix
I/O	input/output, see also GPIO, DIO, SIO, USBIO
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
I^2S	inter-IC sound
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
IOSS	input output subsystem
IoT	internet of things
IPC	inter-processor communication
IRQ	interrupt request
ISR	interrupt service routine
ITM	instrumentation trace macrocell
JTAG	Joint Test Action Group
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol
LP	low power
LS	low-speed
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit

Acronym	Description
MISO	master-in slave-out
MMIO	memory-mapped input output
MOSI	master-out slave-in
MPU	memory protection unit
MSL	moisture sensitivity level
Msps	million samples per second
MTB	micro trace buffer
MUL	multiplier
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
OTP	one-time programmable
OVP	over voltage protection
OVT	overvoltage tolerant
PASS	programmable analog subsystem
PCB	printed circuit board
PCM	pulse code modulation
PDM	pulse density modulation
PHY	physical layer
PICU	port interrupt control unit
PLL	phase-locked loop
PMIC	power management integrated circuit
POR	power-on reset
PPU	peripheral protection unit
PRNG	pseudo random number generator
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
QD	quadrature decoder
QSPI	quad serial peripheral interface
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
ROM	read-only memory
RSA	Rivest–Shamir–Adleman, a public-key cryptography algorithm
RTC	real-time clock
RWW	read-while-write
RX	receive
S/H	sample and hold
SAR	successive approximation register
SARMUX	SAR ADC multiplexer bus

Acronym	Description
SC/CT	switched capacitor/continuous time
SCB	serial communication block
SCL	I^2C serial clock
SD	Secure Digital
SDA	I^2C serial data
SDHC	Secure Digital host controller
SDR	single data rate
Sflash	supervisory flash
SHA	secure hash algorithm
SINAD	signal to noise and distortion ratio
SMPU	shared memory protection unit
SNR	signal-to-noise ration
SOF	start of frame
SONOS	silicon-oxide-nitride-oxide-silicon, a flash memory technology
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SROM	supervisory read-only memory
SRSS	system resources subsystem
SWD	serial wire debug, a test protocol
SWJ	serial wire JTAG
SWO	single wire output
SWV	single-wire viewer
TCPWM	timer, counter, pulse-width modulator
TDM	time division multiplexed
THD	total harmonic distortion
TQFP	thin quad flat package
TRM	technical reference manual
TRNG	true random number generator
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
ULP	ultra-low power
USB	Universal Serial Bus
WCO	watch crystal oscillator
WDT	watchdog timer
WIC	wakeup interrupt controller
WLCSP	wafer level chip scale package
XIP	execute-in-place
XRES	external reset input pin

Document Conventions

Units of Measure

Table 46. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
W	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Revision History

Description Title: PSoC 6 MCU: CY8C62X8, CY8C62XA Datasheet Document Number: 002-23185 Rev. *H			
Revision	**ECN**	**Submission Date**	**Description of Change**
**	6085299	03/01/2018	New datasheet for PSoC 6A-2M.
*A	6100523	03/16/2018	Updated the number of SCBs and removed CAN feature and specifications. Updated Multiple Alternate Functions.
*B	6169663	05/16/2018	Updated Features. Updated Block Diagram. Updated IMO Clock Source, Watchdog Timer (WDT), Clock Dividers, Serial Communication Blocks (SCB). Updated GPIO. Updated Quad-SPI/Serial Memory Interface (SMIF). Added a note in Pinouts. Removed pins P14.1 and P14.0. Updated typ value for SID15. Updated Notes 2 and 3. Updated description for SID246. Updated Conditions for SID.CSD#15, SID.CSD#15A, and SID308A. Updated min and max values for SID314A, SID315A, and SID172B. Added SID308P Updated specs SID454, SID455, and SID408. Added Table 41.
*C	6184665	05/24/2018	Updated Block Diagram. Updated CPU and Memory Subsystem. Updated SDHC Controllers. Updated SID262 description. Updated SDHC and eMMC Specifications.
*D	6235143	07/10/2018	Added Security information (Protection Contexts and Protection Units). Changed Power Mode nomenclature to reflect Minimum Regulator Current mode instead of LPA/LPS. Revised SDHC and eMMC specs based on STA. Added note on drive setting valid for all AC specs. Added JTAG Boundary scan specs.
*E	6340009	10/09/2018	Added 128 TQFP and 100 WLCSP pin and package information. Removed SID65A. Updated SID75, SID76, and SID245 max values. Updated SID421 typ value. Added CY8C624ABZI-D44ES(T) in Ordering Information. Added part numbering nomenclature table. Added Errata

Description Title: PSoC 6 MCU: CY8C62X8, CY8C62XA Datasheet Document Number: 002-23185 Rev. *H			
*F	6420256	01/21/2019	Updated the title and replaced PSoC 6A-2M with PSoC 62 PSoC 6 MCU: CY8C62X8, CY8C62XA Datasheet. Updated Features and Blocks and Functionality. Updated Development Ecosystem. Replaced “component” with “driver”. Updated System Resources and Fixed-Function Digital. Updated Pinouts Updated Power Supply Considerations. Updated Power Connections diagram. Updated CPU Current and Transition Times table. Removed spec SID13A Updated Ordering Information.
*G	6564322	05/03/2019	Replaced “dual core” with “dual CPU.” Updated Block Diagram. Updated CY8C62x8, CY8C62xA Pinouts and Multiple Alternate Functions.
*H	6660660	09/16/2019	Updated the title. Updated Ordering Information.

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