AN80555

72-Mbit RH QDR®-II+ Interface Controller Implementation Details

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Associated Part Family: CYRS154*AV18

Related Application Notes: AN4065, AN69702

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Application note AN80555 describes the architecture and timing details of an RH QDR®-II+ memory interface controller implementation for the Cypress Radiation-Hardened QDR-II+ SRAMs. The referenced synthesizable RTL design targets the Xilinx Virtex-5QV family of FPGA devices.

Contents

1 Introduction

The Cypress Radiation-Hardened 72-Mbit QDR-II+ is a source synchronous pipelined Static RAM equipped with the 1.8-V QDR-II+ architecture with RadStop™ technology. The QDR-II+ architecture has separate data inputs and data outputs along with a common multiplexed address port. To maximize data throughput, both read and write ports are equipped with DDR interfaces, which transfer data on both rising and falling edges of the clock signal. The result is that two/four bus widths of data are transferred during each clock period for burst 2 and burst 4 configurations.

Figure 1 depicts the 72-Mbit RH QDR-II+ architecture (X18 configuration).

Figure 1. RH QDR-II+ Architecture

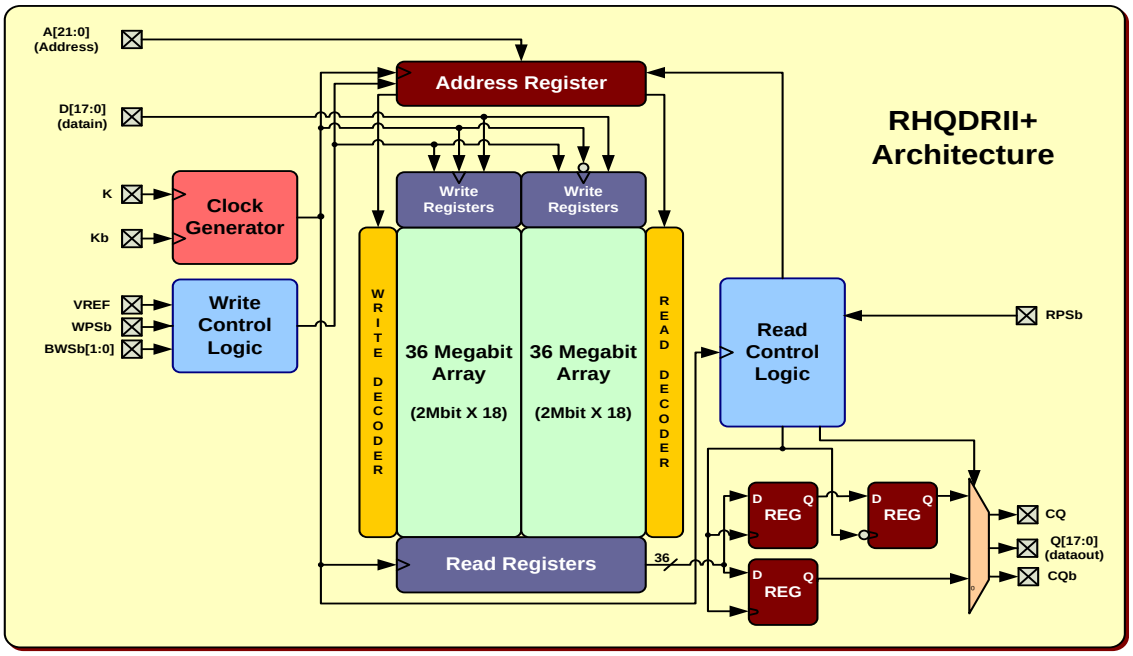


Table 1 summarizes the performance characteristics of the 72-Mbit RH QDR-II+ SRAM.

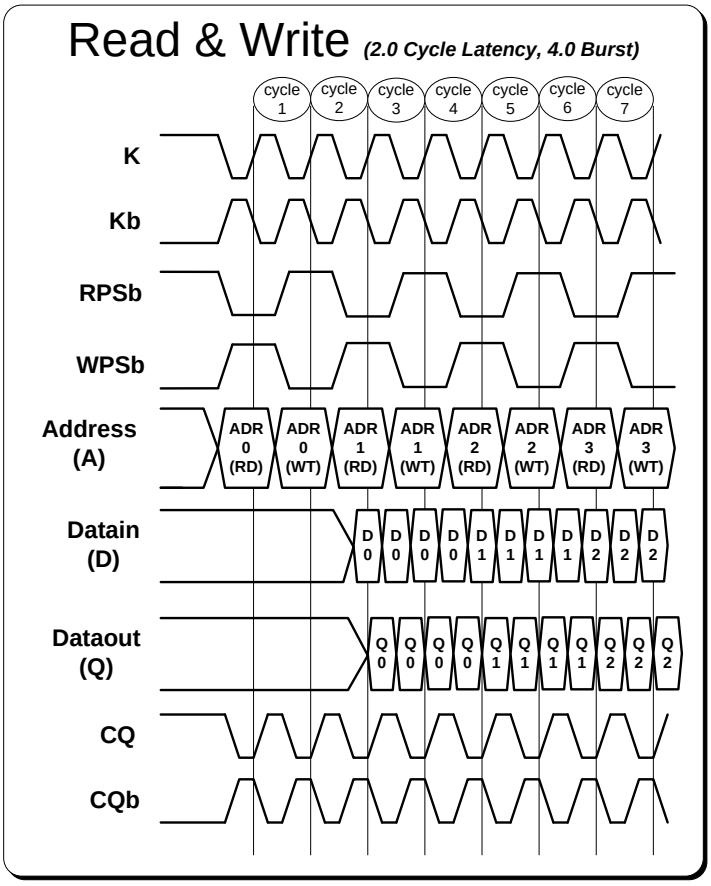
Table 1. 72-Mbit RH QDR-II+ Performance Characteristics

Parameter	Specification
Frequency	250 MHz
Latency	2.0 Cycle Read, 1.0 Cycle Write
Burst Options	2.0 Word-Burst, 4.0 Word-Burst
I/O Standard	HSTL-15
Bus Width	X18, X36

A major built-in architectural feature of RH QDR-II+ is the output echo-clocks (CQ, CQb). These echo-clocks are frequency locked to the master clock (K) but edge-aligned with respect to data outputs (Q). CQ and CQb are used as strobe signals to capture read data from RH QDR-II+ memory. However, CQ/CQb must be center-aligned with respect to data for optimum timing margins. This feature is incorporated in the RH QDR-II+ interface controller using delay calibration functionality built in to the Virtex 5-QV ISERDES block.

Figure 2 shows the timing waveforms with concurrent read and write operations. This configuration provides the maximum performance.

Figure 2. Four-Word Burst RH QDR-II+ Timing



As can be seen, the address bus is shared between the read and write operations. The read address along with read enable RPSb is presented on clock cycle 1, whereas the write address along with the write enable WPSb is presented on clock cycle 2. With a read latency of 2 clock cycles, the read bus data out (Q) values are transmitted from the RH QDR-II+ memory in DDR mode edge aligned to CQ/CQb echo clocks on clock cycle 3. The write data in (D) values are also transmitted to the RH QDR-II+ memory again in DDR mode on clock cycle 3 due to a write latency of 1 clock cycle. The two-word burst mode is similar to the four-word burst except the address bus is also DDR; read and write addresses are presented on different edges of the same clock cycle. Data follows its appropriate latencies with respect to initiated commands.

2 RH QDR-II+ Controller Design

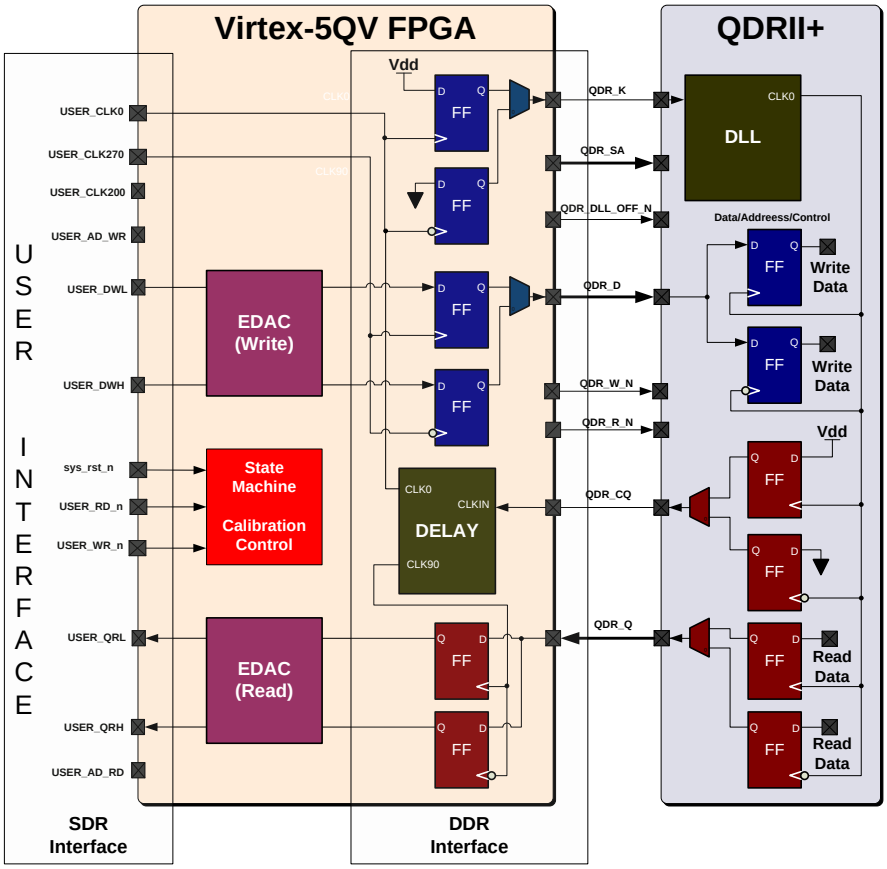
The RH QDR-II+ interface controller uses SDR signals to make read/write requests. The requests are then executed by the state machine which in turn initiates the actual read/write commands to the external RH QDR-II+ device. SDR data is correctly concatenated to maintain DDR relationships with proper timings. The state machine also ensures that the read/write operations are executed concurrently for maximum performance.

Figure 3 is a high-level functional block diagram of the Virtex-5QV based RH QDR-II+ memory interface controller.

The RH QDR-II+ controller has four main components:

- User interface
- State machine
- Error detection and correction (EDAC)
- Physical interface

Figure 3. Virtex-5QV FPGA Based QDR-II+ Controller Block Diagram



2.1 User Interface

The user interface (UI) is a simple SDR-based protocol making read and write command requests. This module utilizes Virtex-5QV FPGA Block RAM memories to queue read/write commands and store their corresponding address and data values. This information is then used to commence operations to the external RH QDR-II+ SRAM memory. Table 2 shows the user interface pin list.

Table 2. User Interface Pin List

Name	I/O	Type	Function
sys_rst_n	I	Reset input	Asynchronous master reset
user_rst_0_tb	O	Reset output	Reset output to higher modules
clk0	I	Clock	Master clock with 0º phase shift
clk270	I	Cock	Master clock with 270º phase shift
clk200	I	Clock	200-MHz clock for IDELAYctrl primitives
clk0_tb	O	Clock	User interface signals to be synchronous to this clock
locked	O	Enable	Indicates all input clocks are stable and PLL/DCM used to generate the input clocks have locked
cal_done	O	Enable	Asserts once calibration is complete. User interface can initiate transaction after this signal asserts.
user_nop	I	NOP enable	User can force NOP cycle toward RHQDRII+ by asserting this signal
user_ad_w_n	I	Enable	Write enable for user write address
user_d_w_n	I	Enable	Write enable for user write data
user_r_n	I	Enable	Write enable for user read address
user_dwl	I	Data	Write data input signals – lower word
user_dwh	I	Data	Write data input signals – higher word
user_ad_wr	I	Address	Write address
user_ad_rd	I	Address	Read address
user_grl	O	Data	Read data output signals – lower word
user _grh	O	Data	Read data output signals – higher word
user_grh_err	O	Status	Indicates error status of Hamming ECC
user_grl_err	O	Status	Indicates error status of Hamming ECC
user_gr_valid	O	Data valid	Indicates data read from RHQDRII+ memory is valid
user_wr_full	O	Status	Indicates that internal write Q is full. When asserted, any writes to user write address or user write data are invalid.
user_rd_full	O	Status	Indicates that internal read Q is full. When asserted, any writes to user read address are invalid.

Write requests are made by issuing an active-low on user_ad_w_n and user_d_w_n signals during the rising edge of clk0. The write address user_ad_wr must be presented on the same clk0 clock edge. The two data words to be written to the RH QDR-II+ memory are also presented to the user_dwh and user_dwl data buses respectively on the same clk0 clock edge. For burst of four, the third and fourth words are presented to the data buses on the next rising edge of clk0. Read requests are made similarly by issuing an active-low on user_r_n signal during the rising edge of clk0. The read address user_ad_rd must be presented on the same clk0 clock edge. The read data words are presented in clk0 domain on user_qrh and user_qrl data buses after 16 clock cycles. Figure 4 shows the timing details for a four-word burst configuration.

2.2 Read/Write State Machine

The read/write state machine coordinates the flow of data between the controller and the RH QDR-II+ SRAM memory. It initiates the actual read/write commands to RH QDR-II+ and ensures that the execution of read/write operations is performed concurrently for maximum bandwidth.

Figure 4. Four-Word Burst User Interface Timing

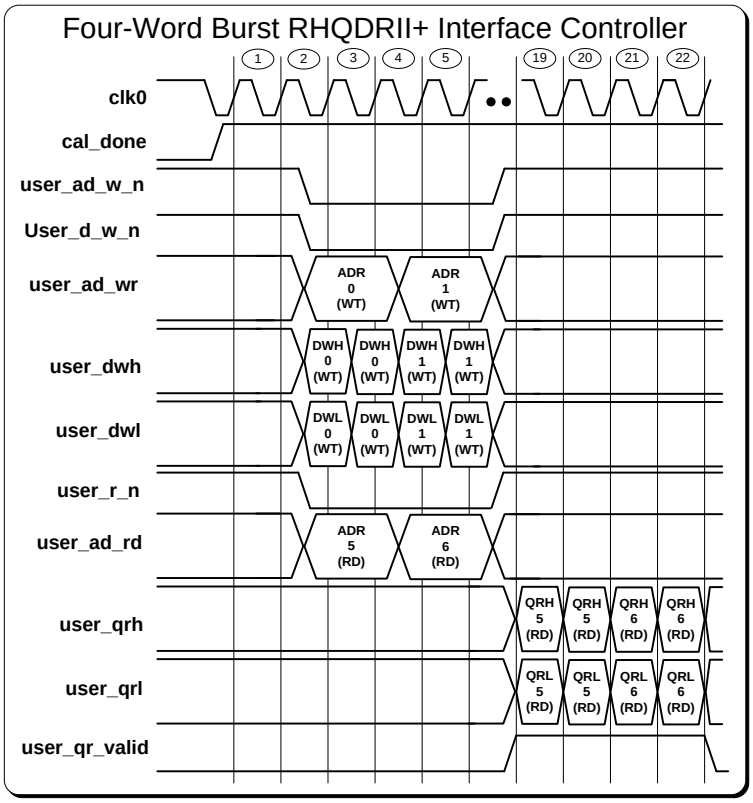


Figure 4 and Figure 6 show the state machines for two-word burst and four-word bursts.

Figure 5. Two-Word Burst State Machine

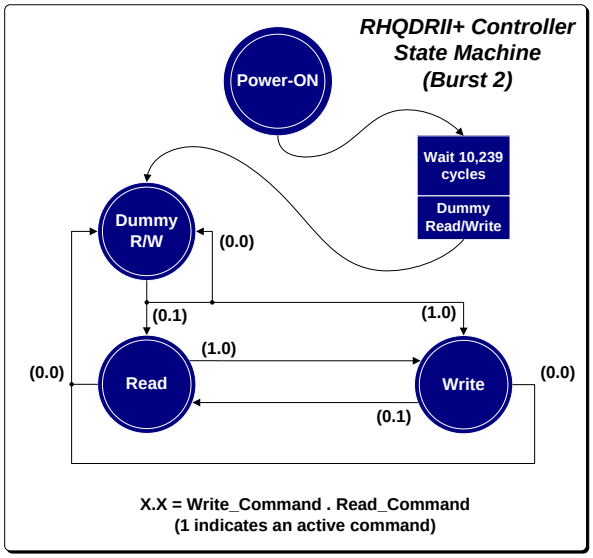
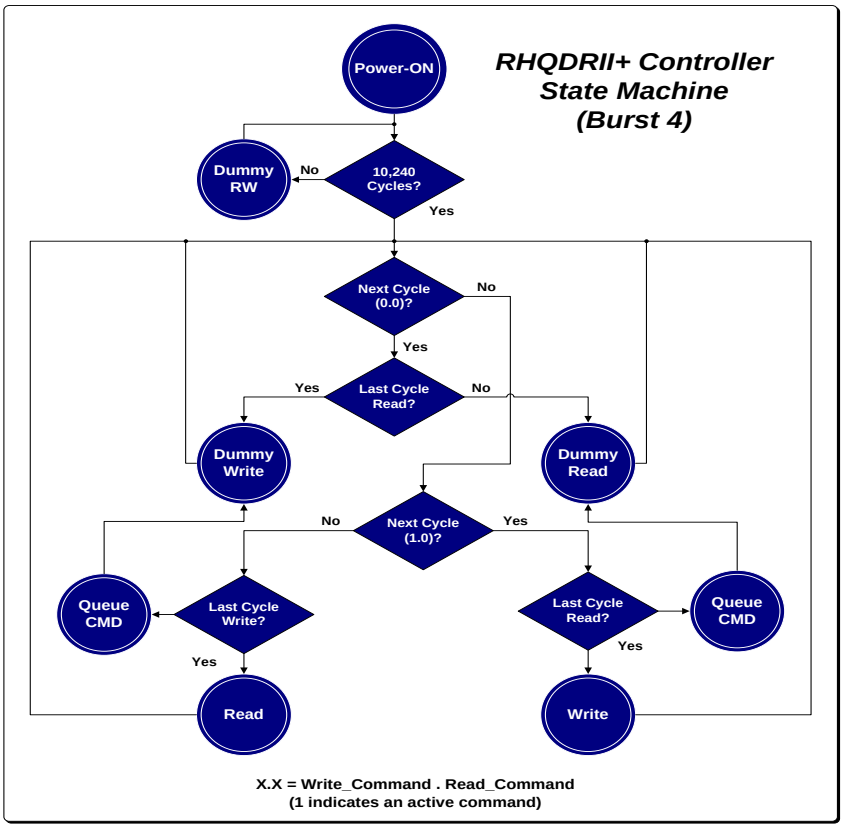


Figure 6. Four-Word Burst State Machine



The two state machines are similar, except that in the four-burst RH QDR-II+ memory case, two consecutive writes or two consecutive reads are not allowed; two clock cycles are needed to complete read/write.

A write request transitions the state machine to the write state, where a write command is initiated with the correct signal execution to the RH QDR-II+ memory. Similarly, a read request transitions the state machine to the read state, where a read command is initiated.

The state machine continually monitors for any pending read or write commands. During idle periods, dummy read and write commands are initiated to keep the RH QDR-II+ memory in the correct power mode (active). An active_low on sys_rst_n brings the state machine to the dummy read/write state by resetting all of the registers.

The state machine also performs delay calibration on the physical interface used to achieve maximum performance while greatly simplifying the task of read data capture inside the FPGA. Each input pin on a Virtex-5QV device has a programmable delay element (IDELAY) that can be dynamically adjusted to control the amount of delay on the input path across a 5-ns window. The state machine leverages this unique capability to adjust the timing of the read data returning from the memory device with respect to strobe signals (CQ, CQb). This ensures optimum data capture window.

2.3 Error Detection and Correction (EDAC)

72-Mbit RH QDR-II+ memory guarantees only single-bit upsets in every word, including bursts, due to proprietary RadStop architectural implementation. To mitigate these word-based single-bit errors, industry-standard single-bit error correction and double-bit error detection EDAC schemes can be used to improve the intrinsic SEU error rate of Radiation Hardened 72-Mbit QDR-II+ memory (1E-10 errors/bit-day). In general, EDAC schemes contain a Hamming code encoder and a Hamming code decoder, which are used to add or remove redundant bits of data for error detection and correction. Figure 7 shows the functional EDAC implementation.

An important EDAC parameter is the minimum Hamming distance (MD). MD determines the random error detecting and random error correcting capabilities of EDAC. The greater the distance, the less likely it is that an error will be made in the decoding process. A Hamming distance of at least four is required for single error correction and double error detection. Table 3 lists the parity bits implemented for the different data widths supported.

Figure 7. EDAC Implementation

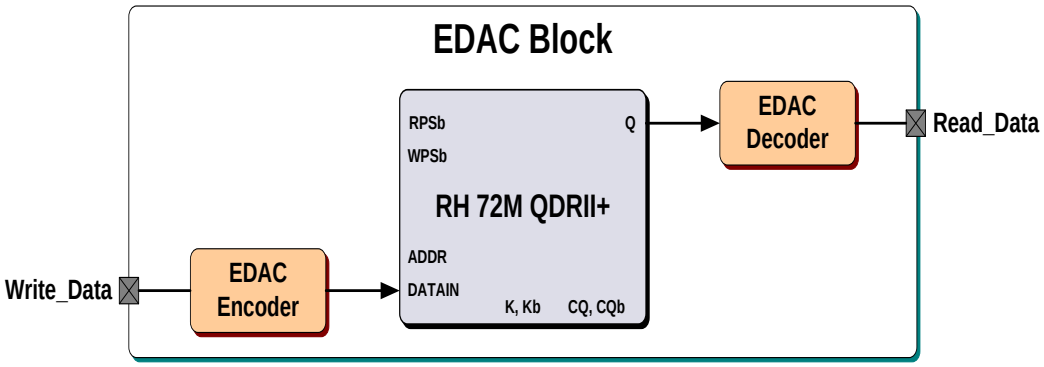


Table 3. EDAC Parity Bits

Interface Size	Data Bits	Parity Bits
X 18	12	6
X 36	29	7
X 72 (2 RH QDR-II+)	64	8

2.4 Physical Interface

The physical interface that is part of the I/Os in Virtex-5QV generates the actual I/O signaling and timing relationships for read/write commands to RH QDR-II+ SRAM memory. It has built-in SDR to DDR and DDR to SDR conversion registers and the appropriate I/O standards (HSTL-15) required to meet the design specifications. Table 4 shows the physical interface pin list.

The write path includes address, data, and control signals required to execute write operations. The write address qdr_sa uses DDR formatting for two-word burst and SDR formatting for four-word burst. Write control strobe qdr_w_n always uses SDR formatting. The write data values qdr_d utilize DDR signaling to achieve the required two-word or four-word burst with their associated clock periods. All write path signals are center-aligned with respect to master clock qdr_k and qdr_k_n clock edges. Clk270 is used to synchronize the built-in OSERDES registers in Virtex-5QV I/Os to output the write data values to the RH QDR-II+ memory.

Table 4. Physical Interface Pin List

Name	I/O	Type	# of Pins	Function
qdr_d	O	RH QDR-II+ data	18, 36	Write data for RH QDR-II+
qdr_bw_n	O	RH QDR-II+ byte enable	2, 4	Byte enables for write data for RH QDR-II+
qdr_q	I	RH QDR-II+ data	18, 36	Read data from RH QDR-II+
qdr_sa	O	RH QDR-II+ address	20, 21	Address for RH QDR-II+
qdr_w_n	O	RH QDR-II+ enable	1	Write port enable for RH QDR-II+
qdr_r_n	O	RH QDR-II+ enable	1	Read port enable for RH QDR-II+
qdr_dll_off_n	O	RH QDR-II+ DLL	1	DLL off signal for RH QDR-II+
qdr_k	O	RH QDR-II+ clock	1	Master clock for RH QDR-II+ – True
qdr_k_n	O	RH QDR-II+ clock	1	Master clock for RH QDR-II+ – Complement
qdr_cq	I	RH QDR-II+ echo clock	1	Echo clock from RH QDR-II+ – True
qdr_cq_n	I	RH QDR-II+ echo clock	1	Echo clock from RH QDR-II+ – Complement

The read path is similar to the write path. Once the read address qdr_sa and read control strobe qdr_r_n have been executed, qdr_cq and qdr_cq_n echo clocks are used as strobes to capture the DDR read data values qdr_q from the RH QDR-II+ memory. The timing and synchronization of DDR data to SDR format is handled by built-in ISERDES block in Virtex-5QV I/Os.

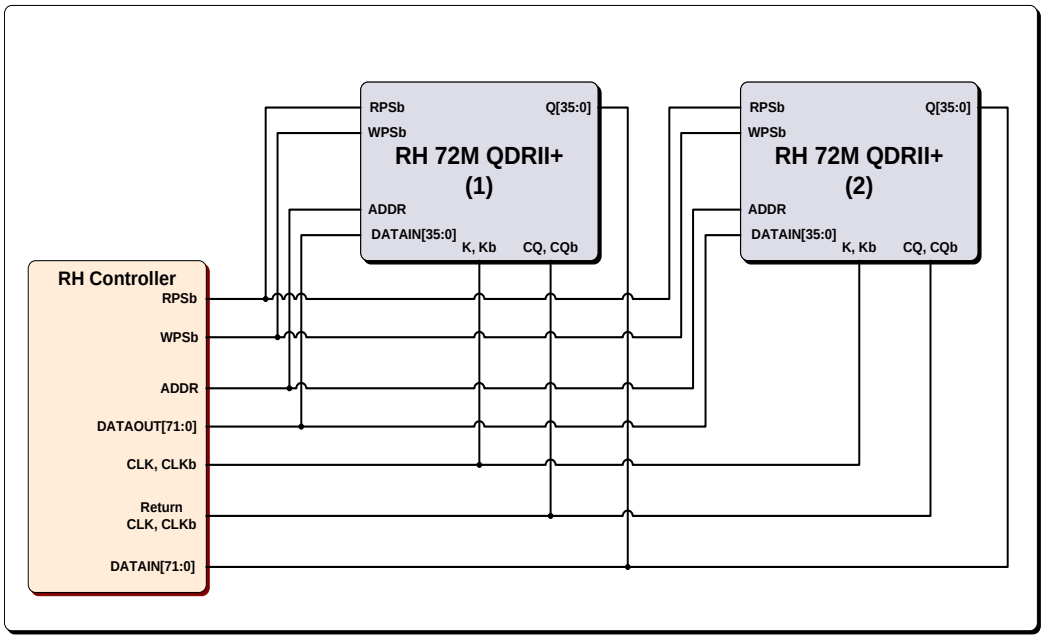
An important aspect of ISERDES is delay calibration. This calibration ensures that the read data qdr_q is center-aligned with respect to echo clocks qdr_cq and qdr_cq_n.

The RH QDR-II+ controller state machine handles this task. Reading from RH QDR-II+ memory should not proceed until delay calibration is complete; cal_done goes high.

2.5 RH QDR-II+ Controller with 72-bit Data Width Design

A common industry practice is to use 64 bits for data and 8 bits for parity. This forms a 72-bit EDAC word. Figure 8 shows a 72-bit implementation.

Figure 8. SECDED 72-Bit EDAC Implementation



Two RH 72-Mbit QDR-II+ memories are grouped together and driven by a Radiation Hardened controller. Both are configured as 36-bit I/Os with a burst of four. An advantage of using two separate devices is further reduction in multibit upset probability in a 72-bit word, because the word is based on two independent devices. Reduced probability is carried over in burst words. The Hamming encoder/decoder embedded in the RH controller adds and removes parity bits during write/read cycles.

3 Specifications

Table 5 shows the interface controller timing.

Table 5. Controller Timing

Spec ID	Parameter	Description	Value	Units
C1	Pipelining	Pipeline registers between the memory controller and the address, command, data outputs, and data inputs	1	Register stage
C2	Read latency	The number of clock cycles needed to get the read data at the local interface after the read command is issued	16	Clock cycles
C3	Write latency	The number of clock cycles needed to issue the write data at the local interface after the write command is issued	0	Clock cycles

Table 6 shows the device utilization of the Virtex-5QV device for the interface controller design.

Table 6. Device Utilization

Spec ID	Parameter	Description	Units
D1	Slices	Configurable logic blocks	590
D2	GCLK buffers	Clocks	3
D3	Block RAMs	Memory blocks	5

4 Reference Design Summary

Table 7 provides the design summary.

Table 7. Reference Design Matrix

Parameter	Description
Developer name	Xilinx Corporation Cypress Semiconductor
Target devices	Virtex-5QV FPGA
Source code provided	Yes
Source code format	Verilog
Functional simulation performed	Yes
Timing simulation performed	Yes
Testbench provided	Yes
Simulator	ModelSim
RTL design types	Burst: 2, 4 Port widths: x18, x36, x72

5 Transitioning Between Power Modes

High-speed source synchronous designs rely on clock synthesis circuits (DLL/PLL) to mitigate device-based skews. 72-Mbit RH QDR-II+ uses a DLL to ensure that output data and echo clocks (strobe) are edge aligned and de-skewed with respect to the source (K, Kb) clock. The disadvantage of using a DLL is the number of clock cycles needed to attain a lock during which the device will not reliably operate. Application note AN69702 discusses the steps needed to effectively transition between active and power-saving modes.

6 Clocking and Termination Design Guide

Design guide AN4065 assists designers in using the QDR-II, QDR-II+, DDR-II, and DDR-II+ SRAM devices and includes guidelines on clocking and termination techniques for the QDR-II, QDR-II+, DDR-II, and DDR-II+ SRAM devices.

7 Synthesizable RTL Design

For information on how to obtain the synthesizable RTL design, contact us at radstop@cypress.com.

8 Summary

This application note describes the implementation and timing details of two- and four-word burst RH QDR-II+ SRAM interfaces based on the Xilinx Virtex-5QV FPGA. The referenced synthesizable RTL design utilizes built-in Virtex-5QV structures to provide a high-performance solution.

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**	3650131	SZZX	06/19/2012	New application note.
*A	3750134	SZZX	09/20/2012	No technical updates. Post to external web.
*B	3879851	SZZX	02/11/2013	Added RH QDR-II+ Architecture. Clarified Interface boundaries.
*C	4088853	SZZX	08/06/2013	Added link to the synthesizable reference design.
*D	4115842	SZZX	09/09/2013	Removed synthesizable reference design mention from Cypress website. Updated to new template.
*E	4817489	SZZX	06/30/2015	Updated to new template.
*F	5849728	HARA	08/17/2017	Updated logo and copyright.

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