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Spec No: 002-18467

Spec Title: AN218467 - MIGRATING FROM 65-NM S26KL512S/S26KS512S HYPERFLASH (TM) PRODUCTS TO 45-NM S26KL512T/S26KS512T HYPERFLASH PRODUCTS

Replaced by: 002-23680

AN218467

Migrating from 65-nm S26KL512S/S26KS512S HyperFlash™ Products to 45-nm S26KL512T/S26KS512T HyperFlash Products

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Associated Part Families: S26KL-S, S26KS-S, S26KL-T, S26KS-T

AN218467 provides guidelines for migrating from Cypress's 65-nm, 512-Mb S26KL-S/S26KS-S HyperFlash™ product family to the 45-nm, 512-Mb S26KL-T/S26KS-T HyperFlash product family. It describes the similarities and differences in the configuration of address spaces and command codes to facilitate the conversion.

Contents

1 Introduction

This document provides guidelines for migrating from Cypress's S26KL512S/S26KS512S serial NOR flash family of products to the S26KL512T/S26KS512T serial NOR flash family of products. It discusses the known issues that may be encountered when facilitating this conversion.

S26KL512S/S26KS512S is a 3.0-V/1.8-V flash memory device based on 65-nm MirrorBit® process technology. S26KL512T/S26KS512T is also a 3.0-V/1.8-V flash memory device, but it is based on an advanced 45-nm MirrorBit process technology. The S26KL/S512T family of flash devices represents the effort committed by Cypress to continually improve its product line. Among the advances are higher bandwidth through higher frequency (400 MB/s, 200 MHz), interface data integrity through Interface CRC, and enhanced endurance/retention through wear leveling (EnduraFlex™). Refer to the S26KL/S512T datasheet for a full description of all the new features and functions included in these devices.

2 Feature Comparison

S26KL/S512T supports a superset of the S26KL/S512S feature set. Table 1 summarizes the similarities and differences in features. Command Set Comparison discusses these differences in more detail.

Table 1. Feature Comparison

Feature/Parameter	S26KL/S512T	S26KL/S512S
Technology Node	45 nm MirrorBit	65 nm MirrorBit
Architecture	NOR Flash	NOR Flash
Density	512 Mb	512 Mb
Interface Width	x1, x8	x8
Supply Voltage	1.70 V – 2.00 V 2.70 V – 3.60 V	1.70 V – 1.95 V 2.70 V – 3.60 V
Read Bandwidth (1.8 V)	400 MB/s (200 MHz)	333 MB/s (166 MHz)
Read Bandwidth (3.0 V)	400 MB/s (200 MHz)	200 MB/s (100 MHz)
Program Buffer Size	512 Bytes	512 Bytes
Erase Sector Size	4 KB / 256 KB	4 KB / 256 KB
Parameter Sector Size	4 KB	4 KB
Number of Parameter Sectors	32	8
Secure Silicon Region (SSR)	1024B	1024B
Advanced Sector Protection (ASP)	Yes	Yes
Suspend / Resume	Erase / Program	Erase / Program
Addressing	HyperBus™ – 5 Bytes SPI – 3 / 4 Bytes	HyperBus – 5 Bytes
Hardware Reset	Yes	Yes
Standard Operating Temperature	–40°C to +85°C	–40°C to +85°C
	–40°C to +105°C	–40°C to +105°C
Automotive Operating Temperature	–40°C to +85°C	–40°C to +85°C
	–40°C to +105°C	–40°C to +105°C
	–40°C to +125°C	–40°C to +125°C
Deep Power Down	Yes	Yes
ID and Common Flash Interface	Yes	Yes
Serial Flash Discoverable Parameters (SFDP)	Yes	No
Unique Identification	Yes	No
AutoBoot	Yes	No
Memory Array CRC	Yes	Yes
Interface CRC	Yes	No
EnduraFlex	Yes	No
Error Correcting Code (ECC – SECDED)	Yes	Yes
Packages	24-ball BGA (6x8 mm, 5x5-ball)	24-ball BGA (6x8 mm, 5x5-ball)
Legacy Single SPI Boot Mode	Yes	No

3 New Feature Set Summary

This section summarizes the new features in the S26KL/S512T devices. For detailed information, consult the device datasheet.

3.1 Serial Flash Discoverable Parameters

Serial Flash Discoverable Parameter (SFDP) is a JEDEC standard that provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables are interrogated by the host system software to enable any adjustments needed to accommodate divergent features from multiple vendors.

Cypress supports SFDP in all its SPI NOR flash devices. S26KL/S512T is the first HyperBus based NOR flash product that supports SFDP.

3.2 AutoBoot

HyperFlash devices require 48 cycles of command and address shifting to initiate a read command. To read boot code, the host memory controller or processor must supply the read command from a hardwired state machine or from internal ROM code. The AutoBoot feature allows the host memory controller to receive boot code from an S26KL/S512T device immediately after the end of reset, without having to send a read command. This saves 48 cycles and simplifies the logic needed to initiate the reading of boot code.

3.3 Interface CRC

One of the most critical aspects of communication between a host and a slave device is ensuring the integrity of transferred information. A cyclic redundancy check (CRC) is an error-detecting code commonly used in devices to detect unintentional changes to raw data. An Interface CRC–enabled slave device calculates a fixed-length binary sequence, known as a CRC checksum, for each block of data transferred (host to slave or slave to host). The host device must also calculate its own CRC checksum on the same data block transferred. If the host-calculated CRC checksum does not match the slave-generated checksum, then the block transferred incurs a data error, and the host device can take corrective action such as requesting the data block to be sent again.

Note: The CRC polynomial must be identical between the slave and the host.

S26KL/S512T supports the Interface CRC functionality. It calculates the CRC checksum of all interface data (instruction, address, and data) and stores the checksum in a register that the host can access. This enables the host to take the appropriate actions in the event of an error.

3.4 EnduraFlex

Flash devices, when subjected to a high number of program/erase cycles, can potentially suffer from degraded data retention and/or shortened device lifespan. To increase device reliability, Cypress has incorporated EnduraFlex in S26KL/S512T devices, which enhances program/erase cycling endurance and data retention by distributing program/erase cycles over a larger number of sectors. EnduraFlex also allows you to configure high-endurance and/or long-retention regions for storing different types of data.

3.5 Legacy SPI Boot Mode

S26KL/S512T supports the single SPI (1S-1S-1S) interface mode with a limited set of instructions to enable access to SFDP, reading of the memory array for accessing boot code, device configuration, and transitioning to HyperBus interface mode.

Note: For details on all the SPI instructions supported, consult the device's datasheet.

4 Command Set Comparison

Table 2 summarizes the supported commands for each device. Pertinent differences are discussed in subsequent sections.

Table 2. Command Set Comparison

Command Function	Command Description	Cycles	S26KL/S512T	S26KL/S512S
Read Memory Array	Read	1	Yes	Yes
Interface Mode	Enter SPI Mode	3	Yes	–
Reset	Reset – Address Space Overlay (ASO) Exit	1	Yes	Yes
Power Modes	Enter Deep Power Down	3	Yes	Yes
Register Access	Status Register Read	2	Yes	Yes
	Status Register Clear	1	Yes	Yes
	POR Timer Register Program	4	Yes	Yes
	POR Timer Register Read	4	Yes	Yes
	Interrupt Configuration Register Load	4	Yes	Yes
	Interrupt Configuration Register Read	4	Yes	Yes
	Interrupt Status Register Load	4	Yes	Yes
	Interrupt Status Register Read	4	Yes	Yes
	Volatile Configuration Register 0 Load	4	Yes	Yes
	Volatile Configuration Register 1 Load	4	Yes	–
	Volatile Configuration Register 0 Read	4	Yes	Yes
	Volatile Configuration Register 1 Read	4	Yes	–
	Nonvolatile Configuration Register 0 Program	4	Yes	Yes
	Nonvolatile Configuration Register 1 Program	4	Yes	–
	Nonvolatile Configuration Registers Erase	3	Yes	Yes
	Nonvolatile Configuration Register 0 Read	4	Yes	Yes
	Nonvolatile Configuration Register 1 Read	4	Yes	–
Program Array	Word Program	4	Yes	Yes
	Write to Buffer – 256 Byte	6	Yes	Yes
	Program Write Buffer to Flash (Confirm)	1	Yes	Yes
	Write to Buffer Abort – Reset	3	Yes	Yes
Erase Array	Chip Erase	6	Yes	Yes
	Sector Erase	6	Yes	Yes
	Blank Check	1	Yes	Yes
	Erase Status Evaluation	1	Yes	Yes
Erase Suspend / Resume	Erase Suspend	1	Yes	Yes
	Erase Resume	1	Yes	Yes
Program Suspend / Resume	Program Suspend	1	Yes	Yes
	Program Resume	1	Yes	Yes
Address Space Overlay	RESET ASO Exit – 1 Cycle F0	1	Yes	Yes
	RESET ASO Exit – 1 Cycle FF	1	Yes	Yes

Command Function	Command Description		Cycles	S26KL/S512T	S26KL/S512S
Address Space Overlay	RESET	ASO Exit – 2 Cycle	2	Yes	Yes
	RESET	ASO Exit – 4 Cycle	4	Yes	Yes
	ID/CFI	ASO Entry – Identification / Common Flash Interface (ID/CFI) (3 cycle)	3	Yes	Yes
	ID/CFI	ASO Entry – Identification / Common Flash Interface (ID/CFI) (1 cycle)	1	Yes	Yes
	ID/CFI	Identification / Common Flash Interface Read	1	Yes	Yes
	SSR	ASO Entry – Secure Silicon Region (SSR)	3	Yes	Yes
	SSR	SSR Read	1	Yes	Yes
	SSR	SSR Word Program	4	Yes	Yes
	SSR	SSR Write to Buffer – 512 Byte	5	Yes	Yes
	SSR	SSR Program Write Buffer to Flash	1	Yes	Yes
	SSR	SSR Write to Buffer Abort – Reset	3	Yes	Yes
	ASP	ASO Entry – Advanced Sector Protection (ASP) Register	3	Yes	Yes
	ASP	ASP Register Program	2	Yes	Yes
	ASP	ASP Register Read	1	Yes	Yes
	PSWD	ASO Entry – Password (PSWD)	3	Yes	Yes
	PSWD	Password Program	2	Yes	Yes
	PSWD	Password Read	1	Yes	Yes
	PSWD	Password Unlock	7	Yes	Yes
	PPB	ASO Entry – Nonvolatile Persistent Sector Protection (PPB)	3	Yes	Yes
	PPB	PPB Bits Program	2	Yes	Yes
	PPB	All PPB Bits Erase	2	Yes	Yes
	PPB	PPB Bits Read	1	Yes	Yes
	PPB	Sector Address (SA) Protection Status	2	Yes	Yes
	PPBL	ASO Entry – Persistent Protection Lock (PPBL)	3	Yes	Yes
	PPBL	Persistent Protection Lock Bit Clear	2	Yes	Yes
	PPBL	Persistent Protection Lock Status Read	1	Yes	Yes
	DYB	ASO Entry – Volatile Dynamic Sector Protection (DYB)	3	Yes	Yes
	DYB	DYB Set	2	Yes	Yes
	DYB	DYB Clear	2	Yes	Yes
	DYB	DYB Status Read	1	Yes	Yes
	DYB	Sector Address (SA) Protection Status	2	Yes	Yes
	ECC	ASO Entry – ECC	3	Yes	Yes
	ECC	ECC Status Read	1	Yes	Yes
	ECC	Error Address Trap Register Read (Lower)	2	Yes	Yes
	ECC	Error Address Trap Register Read (Upper)	2	Yes	Yes
	ECC	ECC Count Register Read (Lower)	2	Yes	Yes
	ECC	ECC Count Register Read (Upper)	2	Yes	Yes
	ECC	Clear ECC Status and Interrupts	1	Yes	Yes

Command Function	Command Description		Cycles	S26KL/S512T	S26KL/S512S
Address Space Overlay	ICRC	ASO Entry – Interface CRC	3	Yes	–-
	ICRC	Interface CRC Register Read	1	Yes	–
	CRC	ASO Entry – CRC	3	Yes	Yes
	CRC	CRC Start Address Load	1	Yes	Yes
	CRC	CRC End Address Load	1	Yes	Yes
	CRC	CRC Suspend	1	Yes	Yes
	CRC	Array Read (During Suspend)	1	Yes	Yes
	CRC	CRC Resume	1	Yes	Yes
	CRC	Result Check Value Register Read (Lower)	2	Yes	Yes
	CRC	Result Check Value Register Read (Upper)	2	Yes	Yes
	ATB	ASO Entry – AutoBoot (ATB) Register	3	Yes	–
	ATB	AutoBoot Register Program / Write	2	Yes	–
	ATB	AutoBoot Register Read	1	Yes	–
	SEC	ASO Entry – Sector Erase Count (SEC) Register	3	Yes	–
	SEC	SEC Command	2	Yes	–
	SEC	SEC Register Read	1	Yes	–
	HDRP	ASO Entry – High Data Retention Pointer (HDRP) Register	3	Yes	–
	HDRP	HDRP Pointer Program	2	Yes	–
	HDRP	HDRP Pointer Read	1	Yes	–

4.1 SFDP

S26KL/S512T supports SFDP in addition to manufacturer/device identification and Common Flash Interface (CFI) tables as in S26KL/S512S. SFDP is defined by JEDEC (JEDEC-216B) and consists of a header table, which identifies SFDP. Table 3 provides the address map overview for both device families.

Table 3. S26KL/S512T and S26KL/S512S SFDP, ID, CFI Address Map Overview

Address	S26KL/S512T	S26KL/S512S
(SA) + 0000h to 0000Fh	–	Device ID
(SA) + 0010h to 00079h	–	CFI Data
(SA) + 0000h to 03FFh	SFDP	–
(SA) + 1000h to 1000Fh	Device ID	–
(SA) + 1010h to 10079h	CDI Data	–

4.2 Unique Identification

S26KL/S512T provides a 64-bit unique number for each device. S26KL/S512S does not support unique identification. Table 4 shows the address map for unique identification of S26KL/S512T.

Table 4. S26KL/S512T Unique ID Address Map Overview

Address	S26KL/S512T	S26KL/S512S
(SA) + 0400h to 0440h	Unique ID	–

4.3 Status and Configuration Registers

The working state of S26KL/S512T and S26KL/S512S devices is set by internal configuration registers. Status registers, on the other hand, provide the device's status during embedded algorithmic operations. Table 5 summarizes the supported registers for each device.

Table 5. Status and Configuration Register Set Comparison

Register Type	S26KL/S512T	S26KL/S512S	Identical
Status Register	Yes	Yes	Yes
Configuration Register 1	Yes	Yes	No
Configuration Register 2	Yes	–	N/A

For the type and functionality of each configuration/status bit, consult each device's respective datasheet.

4.4 ECC Status Registers

S26KL/S512T and S26KL/S512S devices both have ECC-protected memory cores and provide registers for ECC status reporting. Table 6 summarizes the supported registers for each device.

Table 6. ECC Register Set Comparison

Register Type	S26KL/S512T	S26KL/S512S	Identical
ECC Status Register	Yes	Yes	No
Address Trap Register	Yes	Yes	Yes
ECC Count Register	Yes	Yes	Yes

For the type and functionality of each register bit, consult each device's respective datasheet.

4.5 Data Protection Registers

S26KL/S512T and S26KL/S512S devices both support Advanced Sector Protection (ASP) data protection against erase/program operations. Table 7 summarizes the supported registers for each device.

Table 7. ASP Register Set Comparison

Register Type	S26KL/S512T	S26KL/S512S	Identical
ASP Register	Yes	Yes	No
Password Register	Yes	Yes	Yes
PPB Lock Register	Yes	Yes	Yes
PPB Access Register	Yes	Yes	Yes
DYB Access Register	Yes	Yes	Yes

For the type and functionality of each register bit, consult each device's respective datasheet.

4.6 AutoBoot Registers

S26KL/S512T supports an AutoBoot feature, with which the host master controller can execute boot code immediately after the end of reset (POR, hardware reset, software reset, default recovery) without having to send a read instruction. S26KL/S512S does not support AutoBoot. Table 8 summarizes the supported registers for each device.

Table 8. AutoBoot Register Set Comparison

Register Type	S26KL/S512T	S26KL/S512S	Identical
AutoBoot Register	Yes	–	N/A

For the type and functionality of each register bit, consult each device's respective datasheet.

4.7 Sector Erase Count Registers

S26KL/S512T supports the Sector Erase Count (SEC) feature, which provides the capability to read the number of times each sector has been erased. The SEC command outputs the number of successful erase cycles for the addressed sector. S26KL/S512S does not support SEC. Table 9 summarizes the supported registers for each device.

Table 9. SEC Register Set Comparison

Register Type	S26KL/S512T	S26KL/S512S	Identical
SEC Register	Yes	–	N/A

For the type and functionality of each register bit, consult each device's respective datasheet.

4.8 Interface CRC Registers

S26KL/S512T supports the Interface CRC (ICRC) feature, with which the device calculates a fixed-length binary sequence, known as the CRC checksum, for each block of interface data and puts it in the ICRC register for interface integrity. S26KL/S512S does not support ICRC. Table 10 summarizes the supported registers for each device.

Table 10. ICRC Register Set Comparison

Register Type	S26KL/S512T	S26KL/S512S	Identical
ICRC Register	Yes	–	N/A

For the type and functionality of each register bit, consult each device's respective datasheet.

4.9 EnduraFlex (Wear Leveling) Registers

S26KL/S512T supports the EnduraFlex feature, whereby data endurance is improved through wear leveling. Wear leveling spreads the program/erase cycles of the device evenly across all the sectors that are part of the wear leveling pool in the device. S26KL/S512S does not support EnduraFlex. Table 11 summarizes the supported registers for each device.

Table 11. EnduraFlex Register Set Comparison

Register Type	S26KL/S512T	S26KL/S512S	Identical
PNT_ADR_0 Register	Yes	–	N/A
PNT_ADR_1 Register	Yes	–	N/A
PNT_ADR_2 Register	Yes	–	N/A
PNT_ADR_3 Register	Yes	–	N/A
PNT_ADR_4 Register	Yes	–	N/A

For the type and functionality of each register bit, consult each device's respective datasheet.

5 Hardware Comparison

Pertinent hardware differences between S26KL/S512T and S26KL/S512S are discussed in subsequent sections.

5.1 Hardware Reset

The hardware pin based reset (RESET#) behavior in S26KL/S512T is different from that in S26KL/S512S. In S26KL/S512T, RESET#, once initiated, duplicates the power-on reset (POR) sequence. In S26KL/S512S, the RESET# behavior is a subset of the POR sequence—that is, all blocks are not initialized.

From a timing perspective, S26KL/S512T uses the rising edge of RESET# to trigger, whereas S26KL/S512S uses the falling edge to trigger. Figure 1 shows the RESET# timing waveforms for S26KL/S512T. Table 12 summarizes the timing details.

Figure 1. RESET# Timing Sequence

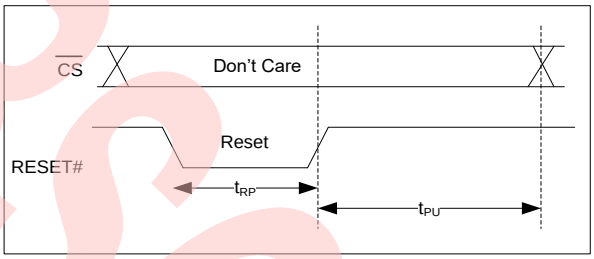

Table 12. RESET# Timing Details

Parameter	S26KL/S512T	S26KL/S512S	Units
t_{RP} – RESET# Pulse Width	200	–	ns
t_{PU} – Internal Device Reset Duration	300	–	µs

5.2 DC Parameters

Table 13 provides a comparison of the DC parameters for S26KL/S512T and S26KL/S512S. While most parameter differences should not cause performance issues when migrating, it is highly recommended that you carefully review all the parameter differences for any potential impact.

Table 13. DC Parameter Comparison

		S26KL/S512T			S26KL/S512S			
DC Parameters	**Description / Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
V_{IH}	Input voltage HIGH threshold, GPIO, CMOS Configuration	$V_{CC}Q$ * 0.7		$V_{CC}Q$ + 0.4	$V_{CC}Q$ * 0.7		$V_{CC}Q$ + 0.4	V
V_{IL}	Input voltage LOW threshold, GPIO, CMOS Configuration	–0.50		$V_{CC}Q$ * 0.3	–0.50		$V_{CC}Q$ * 0.3	V
V_{OH}	Output High Voltage Conditions: @ –0.1 mA	$V_{CC}Q$ – 0.2			$V_{CC}Q$ – 0.2			V
V_{OL}	Output Low Voltage Conditions: @ 0.1 mA			0.20			$V_{CC}Q$ * 0.15	V
I_{LI}	Input Leakage Current Conditions: $V_{CC}Q$ = MAX, VIN = VIH or VSS, CS# = VIH			±4.00				µA
I_{LO}	Output Leakage Current Conditions: $V_{CC}Q$ = MAX, VIN = VIH or VSS, CS# = VIH			±4.00				µA
I_{CC1}	V_{CC} Active Read Current (core current only, IO switching current is not included) CS# = V_{IL}, @200 MHz, V_{CC} = 1.95 V		125.00			130.00	180.00	mA
I_{CC1}	V_{CC} Active Read Current (core current only, IO switching current is not included) CS# = V_{IL}, @200 MHz, V_{CC} = 3.6 V		125.00			80.00	100.00	mA
I_{IO1}	$V_{CC}Q$ Active Read Current of IOs CS# = V_{IL}, @200 MHz, $V_{CC}Q$ = 1.95 V, CLOAD = 15 pf					80.00	100.00	mA
I_{IO1}	$V_{CC}Q$ Active Read Current of IOs CS# = V_{IL}, @200 MHz, $V_{CC}Q$ = 3.6 V, CLOAD = 15 pf					80.00	100.00	mA
I_{CC3P}	Active Page Program Current Conditions: CS# = V_{IH}, V_{CC} = max		50.00			60.00	100.00	mA
I_{CC4}	Active Sector Erase (256 KB) Conditions: CS# = V_{IH}, V_{CC} = max		50.00			60.00	100.00	mA
I_{SB1}	Standby Current (–40°C to +85°C) Conditions: CS# = V_{IH}, RESET# = V_{IH}, All I/Os = V_{IH} or V_{SS}					25.00	100.00	µA
I_{SB2}	Standby Current –40°C to +105°C) Conditions: CS# = V_{IH}, RESET# = V_{IH}, All I/Os = V_{IH} or V_{SS}					25.00	300.00	µA
I_{SB3}	Standby Current –40°C to +125°C) Conditions: CS# = V_{IH}, RESET# = V_{IH}, All I/Os = V_{IH} or V_{SS}		11.00			25.00	300.00	µA
I_{DPD1}	Deep Power Down Current (–40°C to +85°C) Conditions: CS# = V_{IH}, CS# = V_{IH}, RESET# = V_{IH}, All I/Os = V_{IH} or V_{SS}					30.00	50.00	µA
I_{DPD2}	Deep Power Down Current (–40°C to +105°C) Conditions: CS# = V_{IH}, CS# = V_{IH}, RESET# = V_{IH}, All I/Os = V_{IH} or V_{SS}					95.00	150.00	µA
I_{DPD3}	Deep Power Down Current (–40°C to +125°C) Conditions: CS# = V_{IH}, CS# = V_{IH}, RESET# = V_{IH}, All I/Os = V_{IH} or V_{SS}		1.30			150.00	250.00	µA
I_{RESET}	Reset Current Conditions: CS# = VIH, All I/Os = V_{IH} or VSS					10.00	20.00	mA

		S26KL/S512T			S26KL/S512S			
DC Parameters	**Description / Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
$I_{CLKSTOP1}$	Active Clock Stop Mode V_{CC} = 1.95 V Conditions: CS# = VIH, IO3/RESET# = V_{IH}, All I/Os = V_{IH} or VSS					6.00	12.00	mA
$I_{CLKSTOP2}$	Active Clock Stop Mode V_{CC} = 3.6 V Conditions: CS# = VIH, IO3/RESET# = V_{IH}, All I/Os = V_{IH} or VSS					6.00	12.00	mA

5.3 Pin Capacitance Values

Table 14 provides a comparison of pin capacitance values for S26KL/S512T and S26KL/S512S. While most parameter differences should not cause performance issues when migrating, it is highly recommended that you carefully review all the parameter differences for any potential impact.

Table 14. Pin Cap Value Comparison

		S26KL/S512T			S26KL/S512S			
Cap Parameters	**Description**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
CI	Input Capacitance (CK, CK#, CS#, PSC, PSC#)	–	–	6.50	3.50	–	4.50	pF
CID	Delta Input Capacitance (CK, CK#, CS#, PSC, PSC#)	–	–	–	–	–	0.25	pF
CO	Output Capacitance (RWDS)	–	–	6.50	5.00	–	6.00	pF
CIO	I/O Pin Capacitance (DQx)	–	–	6.50	5.00	–	6.00	pF
CIOD	I/O Pin Capacitance Delta (DQx)	–	–	–	–	–	0.80	pF
COP	INT#, RSTO# Pin Capacitance	–	–	6.50	5.00	–	6.00	pF
CIP	WP#, RESET# Pin Capacitance	–	–	6.50	6.50	–	9.00	pF

5.4 AC Parameters

Table 15 provides a comparison of AC parameters for S26KL/S512T and S26KL/S512S. While most parameter differences should not cause performance issues when migrating, it is highly recommended that you carefully review all the parameter differences for any potential impact.

Table 15. AC Parameter Comparison

		S26KL/S512T			S26KL/S512S			
AC Parameters	**Description / Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
f_{SCK}	SPI Clock Frequency	0.00	–	200.00	–	–	166.00	MHz
P_{SCK}	SCK Period	$1/f_{SCK}$	–	–	6.00	–	–	ns
t_{CSHI}	Chip Select High Between Transactions	5.00	–	–	6.00	–	–	ns
t_{CSS}	CS# Active Setup Time (w.r.t SCK)	3.00	–	–	3.00	–	–	ns
t_{DSV}	Data Strobe Valid	–	–	5.00	–	–	12.00	ns
t_{IS}	Input Data Setup Time (w.r.t SCK)	0.40	–	–	0.60	–	–	ns
t_{IH}	Input Data Hold Time (w.r.t SCK)	0.40	–	–	0.60	–	–	ns
t_{ACC}	Read Initial Access Time	–	–	80.00	–	–	96.00	ns
t_{DQLZ}	Clock to DQs Low Z	0.00	–		0.00	–	–	ns

		S26KL/S512T			S26KL/S512S			
AC Parameters	**Description / Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
t_{CKD}	CK Transition to DQ Valid	1.20	–	5.00	1.00	–	5.50	ns
t_{CKDI}	CK Transition to DQ Invalid	0.40	–	4.20	0.00	–	4.60	ns
t_{DV}	Data Valid (tDV min = the lesser of: tCKHP min – tCKD max + tCKDI max) or tCKHP min – tCKD min + tCKDI min)	1.45	–	–	1.70	–	–	ns
t_{CKDS}	CK Transition to RWDS Valid	1.20	–	5.00	1.00	–	5.50	ns
t_{DSS}	RWDS Transition to DQ Valid	–0.40	–	0.40	–0.45	–	0.45	ns
t_{DSH}	RWDS Transition to DQ Invalid	–0.40	–	0.40	–0.45	–	0.45	ns
t_{CSH}	Chip Select Hold After CK Falling Edge	0.00	–	–	0.00	–		ns
t_{DSZ}	Chip Select Inactive to RWDS High-Z	–	–	5.00	–	–	6.00	ns
t_{OZ}	Chip Select Inactive to DQ High-Z	–	–	5.00	–	–	6.00	ns
t_{DSZ}	Chip Select Inactive or Clock to RWDS High-Z	–	–	5.00	–	–	6.00	ns
$t_{PSCRWDS}$	PSC Transition to RWDS Transition @ 133 MHz	–	–	–	1.00	–	5.50	ns
$t_{PSCRWDS} - t_{CKD}$	Time Delta Between CK to DQ Valid and PSC to RWDS	–	–	–	–1.00	–	0.50	ns

5.5 Embedded Algorithm Performance

Table 16 provides a comparison of the embedded algorithm performance parameters for S26KL/S512T and S26KL/S512S. While most parameter differences should not cause performance issues when migrating, it is highly recommended that you carefully review all the parameter differences for any potential impact.

Table 16. Embedded Algorithm Performance Parameter Comparison

		S26KL/S512T			S26KL/S512S			
Embedded Parameters	**Description / Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
t_W	Nonvolatile Register Write Time		40.00					ms
$t_{PP}1$	Page Programming Time (256 Bytes)		315.00					µs
$t_{PP}2$	Page Programming Time (512 Bytes)		435.00					µs
$t_{SE}1$	Sector Erase Time (4 KB)		40.00			240.00	725.00	ms
$t_{SE}2$	Sector Erase Time (256 KB)		700.00			930.00	2900.00	ms
$t_{BE}1$	Bulk Erase Time (512 Mb)		179.00			220.00	462.00	s
$t_{EES}1$	Evaluate Erase Status Time (4-KB Sector)		20.00			70.00	100.00	µs
$t_{EES}2$	Evaluate Erase Status Time (256-KB Sector)		80.00			70.00	100.00	µs
t_{EES_RATES}	Evaluate Erase Status Time (256-KB Sector)	60.00	65.00					MB/s
t_{CRC_SETUP}	ECRC Calculation Setup Time		10.00			10.00		µs
t_{CRC_RATES}	ECRC Calculation Rate	60.00	65.00		60.00	65.00		MB/s
t_{SEC}	Sector Erase Count Time							µs
t_{ESL}	Erase Suspend / Resume						50.00	µs
t_{PSL}	Erase Suspend / Resume						50.00	µs
t_{CSL}	CRC Suspend / Resume						50.00	µs
t_{PSWD}	Password Comparison				80.00	100.00	120.00	µs

6 Summary

Migration from Cypress S26KL512S/S26KS512S to S26KL512T/S26KS512T is straightforward and requires minimal accommodation with regard to system software or hardware. Moreover, once accommodations are made, if required, KL-T/KS-T flash can enable the use of higher density devices, resulting in greater performance of existing systems.

7 Related Documents

Table 17. Cypress NOR Flash Product Specific Datasheets

Product Family	Spec. Number	Title
S26KL-S/KS-S Family	001-99198	512 Mbit (64 Mbyte) /256 Mbit (32 Mbyte) / 128 Mbit (16 Mbyte), 1.8V/3.0V HyperFlash™ Family
S26KL-T/KS-T Family	002-12337	512 Mbit (64 Mbyte), 1 Gbit (128 Mbyte) 1.8V/3.0V HyperFlash Family

Document History

Document Title: AN218467 – Migrating from 65-nm S26KL512S/S26KS512S HyperFlash™ Products to 45-nm S26KL512T/S26KS512T HyperFlash Products

Document Number: 002-18467

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5662405	SZZX	03/16/2017	New application note.
*A	6819982	BWHA	02/28/2020	Obsolete document. Completing Sunset Review.

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