AN46982

PLL Considerations in QDR®-II/II+/DDR-II/II+ SRAMs

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Associated Project: No

Associated Part Family: CY7C1*KV18, CY7C2*KV18

Software Version: N/A

Related Application Notes: None

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AN46982 provides an overview of the operation of QDR-II/II+/DDR-II/II+ SRAMs in PLL disabled mode.

1 Introduction

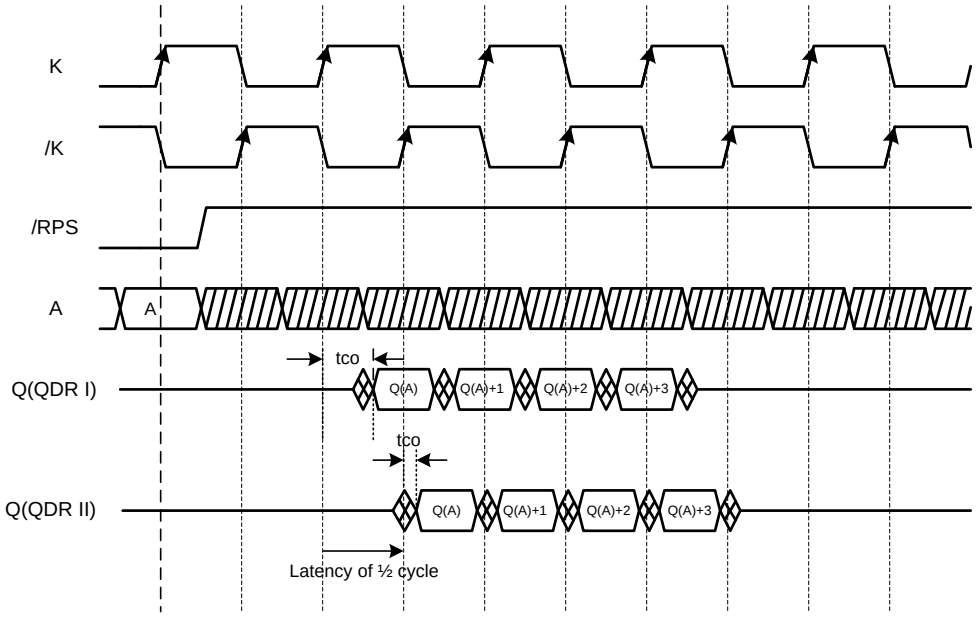
QDR SRAM family of devices has a phase-locked loop (PLL) within the device to synchronize the output data to the input clocks thereby enabling the device to operate at higher frequencies.

QDR-II/II+/DDR-II/II+ devices can be operated with PLL enabled or PLL disabled. This application note provides an overview of the operation of the device when the PLL is disabled.

2 Overview of PLL in QDR-II/QDR-II+ DDR-II/DDR-II+ SRAMs

A PLL is implemented on QDR-II/II+ DDR-II/II+ SRAMs with the purpose of placing the output data coincident with the rising edge of C and $\overline{C}$ (input clocks for output data), or K and $\overline{K}$ when in single clock mode. The first piece of data begins to output a half clock cycle later than the first generation QDR. Figure 1 shows this scenario for a read operation. Write operation is unaffected by the presence of PLL.

Figure 1. QDR-I and QDR-II Output Data



As illustrated in Figure 1 the t_{CO} for QDR-II is very small compared to the t_{CO} on QDR-I.

When $\overline{DOFF}$ signal is tied HIGH, PLL is enabled. In this mode the QDRII device operates with a read latency of 1.5 clock cycles (see Figure 1). When PLL is locked to a specific frequency in the range 120 MHz to the specified maximum clock frequency, the entire timings specific to the designated frequency of the part are valid. These timings are guaranteed by design. Figure 2 shows the scenario during power-up sequence with PLL enabled.

System designers typically operate the QDR-II/II+/DDR-II/II+ devices in PLL disabled mode in the following scenarios:

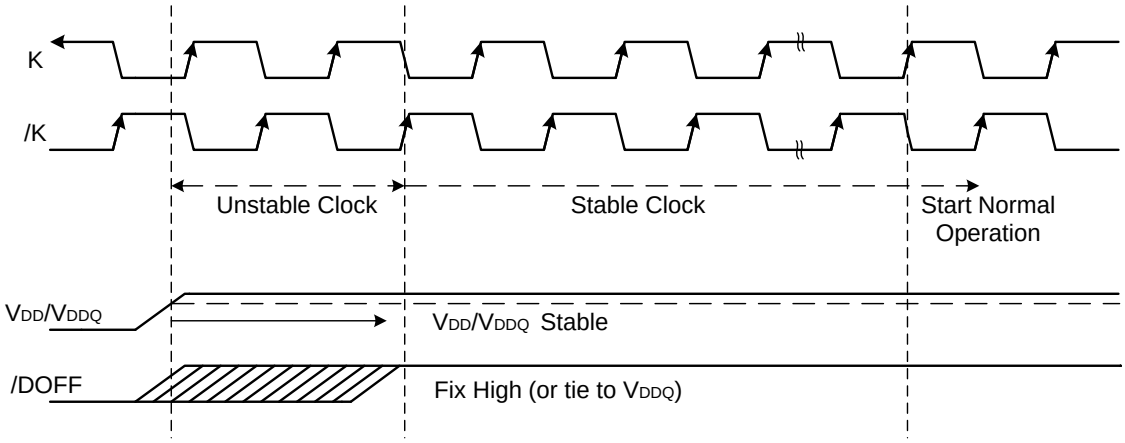
1. At operating frequencies below 120 MHz
2. During power up sequence [1]
3. Debug mode when full operational speed of SRAM is not required

During the initial design, it is natural to run the system at lower frequencies, which makes the data capturing easy. There is a constraint on the lower end of the frequency at which the PLL can operate, which is 120 MHz. To operate the system below this frequency, PLL is bypassed by strapping the $\overline{DOFF}$ signal LOW.

In this mode, the read latency for QDR-II/II+/DDR-II/II+ devices is 1.0 clock cycle(see Figure-1) and the timings are guaranteed by design but not tested.

Figure 3 shows the scenario during power-up sequence with PLL disabled. Normal operation can be started early in this case.

Figure 2. Power-Up Waveforms for Frequency Greater Than 120 MHz (PLL Enabled)



[1] Refer to the knowledge base article link for $\overline{DOFF}$ control input power-up sequence: http://www.cypress.com/?id=4&rID=40999

Figure 3. Power-Up Waveforms for Frequency Less Than 120 MHz (PLL Disabled)

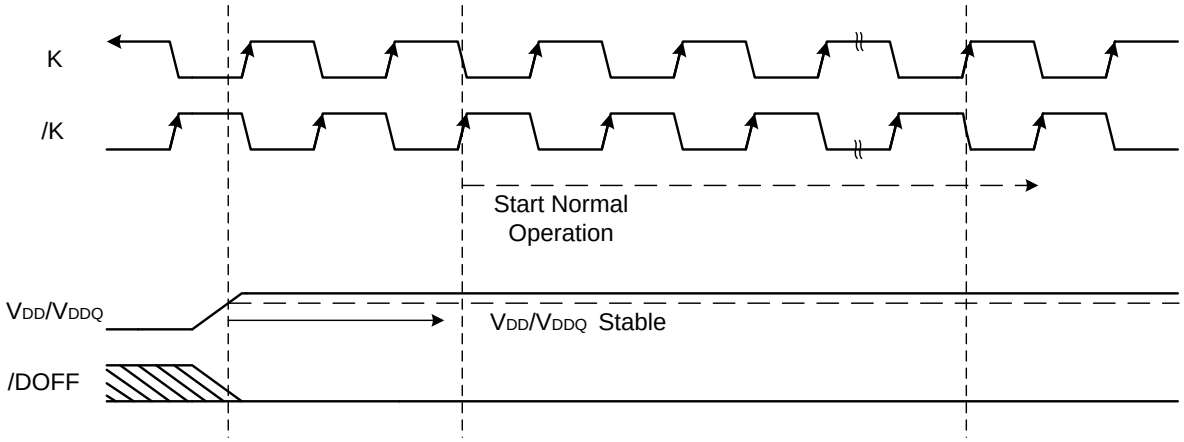


Table-1 shows the timings when the PLL is disabled.

Table-1. Timing Parameters in PLL Disabled Mode [2, 3]

Parameter	Description	167 MHz		Unit
		Min	Max	
Timings Pertaining to Clock				
t_{CYC}	K Clock and C Clock Cycle Time	6.0	8.4	ns
t_{KH}	Input Clock (K/$\overline{K}$ and C/$\overline{C}$) HIGH	2.4	-	ns
t_{KL}	Input Clock (K/$\overline{K}$ and C/$\overline{C}$) LOW	2.4	-	ns
t_{KHKH}	K/$\overline{K}$ Clock rise to $\overline{K}$ /K Clock rise and C/$\overline{C}$ to C/$\overline{C}$ rise (rising edge to rising edge)	2.7	-	ns
t_{KHCH}	K/$\overline{K}$ Clock rise to C/C clock rise (rising edge to rising edge)	0.0	3.55	ns
t_{KC}	Clock Phase Jitter (K, $\overline{K}$, C, $\overline{C}$)	-	0.2	ns
$t_{KC\ lock}$	PLL lock time (K, C)	20	-	µs
Setup times				
t_{SA}	Address Setup to K Clock Rise	0.7	-	ns
t_{SC}	Control Setup to K Clock Rise ($\overline{LD}$, R/$\overline{W}$)	0.7	-	ns
t_{SCDDR}	DDR Control Setup to Clock (K/$\overline{K}$) Rise ($\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$)	0.7	-	ns
t_{SD}	Data Setup to Clock (K/$\overline{K}$) Rise	0.7	-	ns
Hold times				
t_{HA}	Address Hold to K Clock Rise	0.7	-	ns
t_{HC}	Control Hold to K Clock Rise ($\overline{LD}$, R/$\overline{W}$)	0.7	-	ns
t_{HCDDR}	DDR Control Hold to Clock (K/$\overline{K}$) Rise ($\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$)	0.7	-	ns
t_{HD}	Data Hold to Clock (K/$\overline{K}$) Rise	0.7	-	ns
t_{CQD}	Echo clock high to data change	-	0.40	ns

[2] These parameters are only guaranteed by design and are not tested in production.
[3] The C and $\overline{C}$ input clocks and dual clock mode are applicable only to the QDR-II/DDR-II SRAMs and not for the QDR-II+/DDR-II+ SRAMs.

Parameter	Description	167 MHz		Unit
		Min	Max	
t_{CQDOH}	Echo clock high to data change	–0.40	-	ns
t_{CLZ}	Clock (C and $\overline{C}$) rise to Low-Z	–0.50	-	ns
t_{CHZ}	Clock (C and $\overline{C}$) rise to High-Z (Active to High-Z)	-	0.50	ns
Output Timings when the PLL is Bypassed				
t_{CO}	C/$\overline{C}$ Clock rise (or K/$\overline{K}$ in single clock mode) to Data Valid	-	3.0	ns
t_{DOH}	Data Output Hold After Output C/$\overline{C}$ clock Rise (Active to Active)	1.2	-	ns
t_{CCQO}	C/C Clock rise to echo clock valid	-	3.0	ns
t_{CQOH}	Echo clock hold after C/$\overline{C}$ Clock rise	0.5	-	ns
t_{CQD}	Echo clock high to data change	-	0.40	ns
t_{CQDOH}	Echo clock high to data change	–0.40	-	ns
t_{CLZ}	Clock (C and $\overline{C}$) rise to Low-Z	0.5	-	ns
t_{CHZ}	Clock (C and $\overline{C}$) rise to High-Z (Active to High-Z)	-	3.0	ns

3 Summary

This application note outlines the operation of QDR-II/II+/DDR-II/II+ SRAMs specifically when the PLL is disabled. Please note that the timing parameters values are guaranteed only by design and not tested.

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Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2521141	NJY / AESA	06/25/2008	New Spec.
*A	3285879	OSN	06/17/2011	No technical updates.
*B	3339963	DSG	08/08/2011	No technical updates. Release to web.
*C	3667953	PRIT	07/09/2012	No technical updates. Completing Sunset Review.
*D	3734403	PRIT	09/12/2012	Updated Abstract. Updated Introduction. Removed “Overview of PLL in QDRII/II+DDRII/II+ SRAMs”. Removed “PLL Timings when Enabled and Disabled”. Removed “PLL Constraints”. Added “PLL disabled mode”. Updated Summary.
*E	4484246	DEVM	08/28/2014	Removed “PLL disabled mode”. Added “Overview of PLL in QDR-II/QDR-II+ DDR-II/DDR-II+ SRAMs”.
*F	4812440	PRIT	06/26/2015	Updated to new template. Completing Sunset Review.
*G	5850026	AJU	08/10/2017	Updated to new template. Completing Sunset Review.

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QDR SRAMs are a family of products defined and developed by the members of the QDR Consortium comprised of Cypress, Hitachi, IDT, NEC & Samsung.

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