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AN52433

# Advantages of Serial Peripheral Interface (SPI) nvSRAM over SPI EEPROM in Metering Applications

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**Related Application Note: AN64574**

**If you have a question, or need help with this application note, contact the author at zsk@cypress.com.**

Cypress's SPI nvSRAM nonvolatile memory technology has significant advantages when compared to conventional SPI EEPROMs. This application note describes the benefits of using SPI nvSRAM in metering applications and is aimed at designers and architects of the latest 'smart' electrical energy meters.

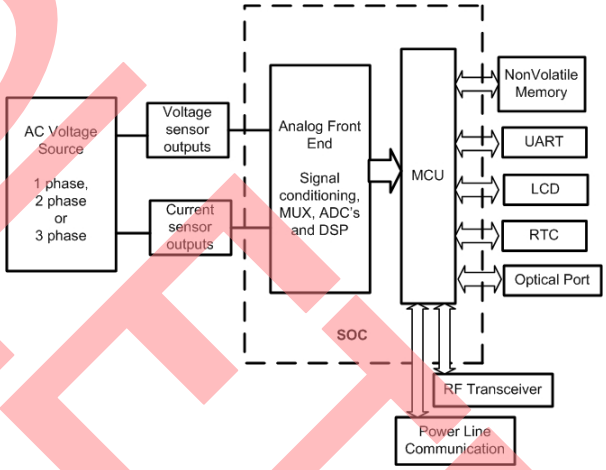


## Introduction

Cypress's nvSRAM is a proven, established combination of fast SRAM cells and silicon-oxide-nitride-oxide-silicon (SONOS)-based nonvolatile memory cells. You can rapidly transfer the entire contents of the SRAM to nonvolatile storage automatically (AutoStore) if the power supply fails, or transfer on demand by issuing the relevant software command (Software Store). The nvSRAM requires a small (typically 47 uF) capacitor connected to its $V_{CAP}$ pin to complete its AutoStore operation. When the main power supply ($V_{CC}$) is applied to the nvSRAM, it charges the capacitor connected to its $V_{CAP}$ pin. When the power supply falls below a threshold ($V_{SWITCH}$), the nvSRAM automatically switches from $V_{CC}$ to $V_{CAP}$ and completes the AutoStore cycle.

This application note provides an architectural overview of smart energy meters and elaborates the benefits of using serial (SPI) nvSRAMs over SPI EEPROMs in such meter designs. Figure 1 shows a simplified block diagram of a smart energy meter. Nonvolatile memory is one of the critical components of the energy meter. The nonvolatile memory stores the valuable energy consumption and environmental data in a time slot when the smart meter uploads information over the network that links it to the supply infrastructure. Valuable information includes periodic power readings and suspicious physical changes which may signify an attempt to tamper with the meter. reduce energy consumption and improve the efficient use of electric energy, different metrics of energy consumption (active power, reactive power, apparent power, sometimes both imported and exported) are recorded at fine granularity. Size requirements for nonvolatile memory have, therefore, grown rapidly with the latest focus being on smart metering. The dependability and integrity requirements for this data are very important.

Figure 1. Energy Meter Block Diagram




## Benefits of nvSRAM over EEPROM in Metering Applications

### Faster Serial Data Transfer

Cypress's serial nvSRAM products operate for both reads and writes similar to a standard SRAM, at continuous clock speeds in excess of 40 MHz under all combinations of temperature and supply voltage. This is much faster (2x) than EEPROM technology, and therefore reduces the amount of time needed to transfer blocks of data down the serial interface. In a heavily loaded microcontroller system that supports critical time dependent tasks such as energy management, this reduction in interfacing overhead using nvSRAM is beneficial.

### Zero Clock Cycle Write Latency in nvSRAM

A typical EEPROM device in the 1 Mbit density requires a write cycle of approximately 6 ms for every 256-byte page of data sent to the memory. This results in long write times when several kilobytes of data need to be written. The nvSRAM does not suffer from this write slowdown; all writes occur at bus speed and there is no memory based latency.

For example:

- It takes 24 ms to backup 1 Kbit of data from the controller's memory to the SPI EEPROM. The controller will take 50 µs to transfer the entire 1-Kbit data from its memory to the EEPROM page buffer over 20 MHz SPI, and will take 24 ms to write four page data from the page buffer to the EEPROM.
- It takes 25 µs to backup 1 Kbit of data from the controller's memory to the SPI nvSRAM. The controller will take only 25 µs to transfer the entire 1-Kbit data from its memory to the nvSRAM over 40 MHz SPI. The nvSRAM does not require a page write cycle, unlike EEPROM.

Therefore, zero clock cycle write latency in nvSRAM significantly improves its write performance over EEPROM.

### No Need to Architect Memory Usage to Match Page Size

Another result of the page mode is that the page size can vary with the different architectures and sizes of EEPROM. The routines to interface to the memory must be flexibly written to accommodate this and continuously tested over a range of storage conditions. The nvSRAM imposes no page size restriction; therefore, you can write arbitrary-sized blocks of data, independent of the total size of memory in use.

### No Need for Wear Leveling or Blockage Tracking

Every page or part-page (for example, byte) write to an EEPROM counts towards the finite endurance limit of nonvolatile technology. This is critical in a smart meter in which, depending on the required settings from the energy supplier, data may have to be recorded once every few seconds.

Careful address management is used in all EEPROM systems that write regularly to the memory. This is called 'wear leveling' and it aims to equalize the number of times to which each page is written. This process requires a fairly sophisticated driver routine present in the controller, through which all nonvolatile accesses are managed. This routine translates the internal addressing of data structures into a physical addressing scheme for the memory. It usually maintains an 'aging table' on the memory array to keep track of how the device is being used.

This consumes a significant amount of code space of a miniature filing system. Because of the fundamental importance of data integrity in a smart meter application (this is legally prescribed in many territories), there is a substantial testing burden on such routines. During an architectural change, this adds to the design cycle time when migrating to a new processor family.

Cypress's nvSRAM does not require any form of wear leveling or aging tracking. The fundamental nonvolatile storage physical layer is very similar to EEPROM. However, it is only exercised when the power needs to be removed from the device, not continuously as in the case of EEPROM use. Therefore, you can use more basic interfacing protocols to connect internal data structures with their organization in external memory. This makes it easier to conform to the requirements on the security, location, format, and accessibility of any stored information that is used for billing purposes.

### No Action needed on an Unexpected Power Down

This is the main benefit of using an nvSRAM device that leads to improved confidence in system data integrity under extreme fault conditions.

When the nvSRAM device detects a power-down, that is, when its power supply voltage drops below a threshold value, it ignores further activity on the link to the processor and automatically initiates a complete store of its entire contents to the local nonvolatile SONOS memory. This process is powered by the energy stored in the capacitor connected to $V_{CAP}$.

In contrast to saving valuable data in an EEPROM-based system, the controller must initiate and carry through a complete write cycle to the desired data block size when a power fault is detected. The main power supply must store enough energy to reliably power the controller and its peripherals throughout this process. The controller must be well protected against crashes that can occur as a result of 'thrashing' on the power supply during power failure. The system firmware must be thoroughly tested over a wide range of error conditions to ensure that the correct action is carried out at whatever system state existed before power failure.

On power-up, the data stored in the nonvolatile portion is copied back into the SRAM portion. This process takes about 20 ms and the contents of the nonvolatile portion are not affected by this recall process.

## nvSRAM Usages

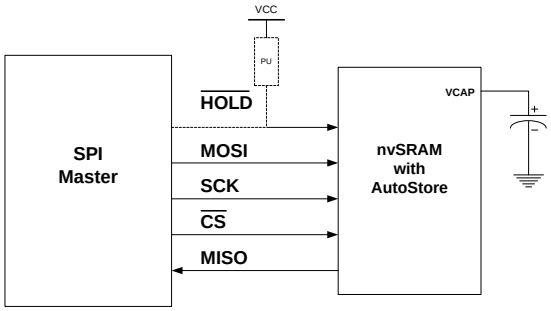
### Using nvSRAM with a Storage Capacitor

Cypress's nvSRAM devices transfer data from the SRAM portion into the nonvolatile portion using energy stored in a small size external capacitor, $V_{CAP}$. This is shown in Figure 2. The recommended nominal value for this capacitor is 47 µF, which enables substantial reductions in value due to initial tolerance, aging, and temperature. Tantalum and Niobium oxide types are particularly suitable from a size and lifetime viewpoint.

The capacitor's static voltage equals the chip supply voltage and it does not need to deliver high currents (the average current is about 3 mA over the period of the store operation). This means that there is no stringent leakage current requirement. The capacitor is connected to, and charged from, the main power supply rail through an internal switch which acts as an ideal diode and disconnects from the supply when it falls below the capacitor voltage.

The capacitor's purpose is not to deliver a sustaining voltage to the SRAM array, as is the case of a battery or capacitor-backed SRAM. After the nonvolatile store operation is completed, data retention is typically 20 years and is completely independent of the capacitor voltage, which gradually discharges to zero after the store operation is complete.

Figure 2. Typical SPI nvSRAM (with storage capacitor) Interface



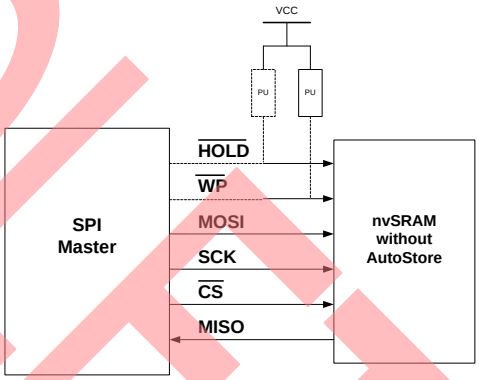

### Using nvSRAM without a Storage Capacitor

It is possible to use nvSRAM even without the local storage capacitor on the $V_{CAP}$ pin, as shown in Figure 3. This is a different package option (without AutoStore feature) in which the $V_{CAP}$ pin is not available, but is replaced by the $\overline{WP}$ (Write Protect); for more information, refer to the section Footprint Compatibility with EEPROM. In this case, the software programming alternative is used. A command sent to the device through the serial interface can trigger the storage of the entire SRAM content into the nonvolatile memory. This process relies on the system's capability to predict power failure in advance and executes nonvolatile store on demand by issuing a software command (STORE or Software STORE). The Software STORE takes a maximum of 8 ms to complete a nonvolatile store operation. The system must ensure that the device power $V_{CC}$ is stable during the Software STORE operation. You can initiate the STORE command by sending the one-byte opcode (0x3C) down the SI line of the serial peripheral interface (SPI). Memory accesses to the nvSRAM are inhibited during this period.

Cypress recommends that you use the storage capacitor method (AutoStore enabled) for electricity meters and other systems operating in difficult power environments where the microcontroller operation cannot be relied upon.

The corresponding 'Software RECALL' command allows the user to trigger a RECALL operation to restore the contents of the nonvolatile memory into the SRAM. The Software RECALL operation is initiated by sending the one-byte RECALL opcode (0x60) down the SI line of the SPI interface. It takes a maximum of 600 µs to complete this operation, during which memory accesses to the nvSRAM are inhibited.

Figure 3. Typical SPI nvSRAM (without storage capacitor) Interface




## Benefits of nvSRAM Versus Other Memory Technologies

Other memory technologies have been recently advocated as alternatives superior to EEPROM for use in meter data storage applications. Devices based on these technologies typically address the same EEPROM shortcomings as Cypress's nvSRAM.

Cypress's nvSRAM technology is built on standard CMOS processes, is in volume production at a number of foundries, and can be licensed to almost any CMOS 'backplane'. Consequently, the nvSRAM devices typically have lower total cost of design-in over time. They are highly suited to design-in over lengthy engineering projects, and the technology has proven its reliability in challenging avionics and communications applications for nearly two decades.

### Footprint Compatibility with EEPROM

Cypress's serial nvSRAM devices are currently available in 8-pin SOIC and 16-pin SOIC packages as shown in Table 1. The Serial EEPROM devices in 1-Mbit density are often supplied in 8-pin SOIC packages. The nvSRAM can be used to 'upgrade' an EEPROM design, but the correct management of the storage capacitor connection is important and involves a PCB change. A standard EEPROM offers additional control through the $\overline{WP}$ (Write Protect) pin. In some systems which use EEPROM, you can drive this pin LOW to provide additional write interlock. This pin has been used to provide the $V_{CAP}$ option in case of nvSRAM with AutoStore feature. Figure 4 shows the difference between SPI EEPROM and SPI nvSRAM (with AutoStore) pin diagram, and Figure 5 shows the difference between SPI EEPROM and SPI nvSRAM (without AutoStore) pin diagram. The $\overline{WP}$ of EEPROM must be disconnected from the microcontroller and connected to the storage capacitor.

Figure 4. Pin Diagram of SPI EEPROM and SPI nvSRAM (with AutoStore)

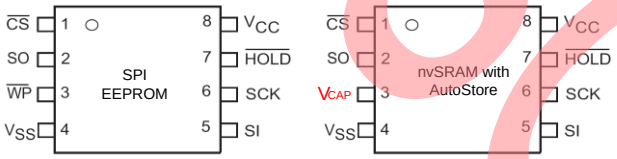
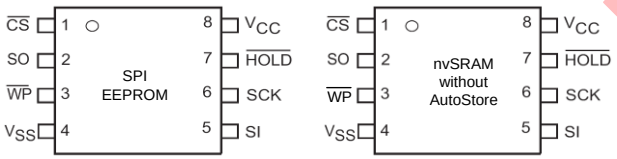



Figure 5. Pin Diagram of SPI EEPROM and SPI nvSRAM (without AutoStore)




### Additional Functions in the 16-pin SOIC Package

Cypress's serial nvSRAM devices are also available in a 16-pin SOIC package. The additional pins facilitate functionality such as real time clock (RTC), square wave output, watchdog timer, timing, and power fail interrupts. The RTC enables the logging of metering data stamped with accurate timing. The nvSRAM RTC chip uses an industry standard 32.768-kHz watch crystal on its X1 and X2 pins to generate a reference input clock for the RTC block. The nvSRAM RTC also has built-in calibration circuitry where it automatically corrects the PPM drift in the crystal. PPM drift occurs due to external factors and affects the system timing accuracy. The calibration circuitry enables you to set appropriate values in the calibration register and achieve clock accuracy up to +1 / -2 ppm. The 16-pin SOIC package also provides a bidirectional $\overline{HSB}$ (Hardware Store Busy) pin and configures it as input to the chip. This is to initiate a nonvolatile store by pulling it LOW using the external controller. While a STORE or RECALL operation is in progress, the $\overline{HSB}$ as an output pin indicates the ready ($\overline{HSB}$ is HIGH) or busy ($\overline{HSB}$ pulled LOW by the nvSRAM) status of the device. Table 1 lists all the serial nvSRAM packages that Cypress currently offers:

Table 1. SPI nvSRAM Packages

| Part Number | Density | RTC | Package |
|---|---|---|---|
| CY14x101PA | 1 Mbit | Yes | 16-pin SOIC |
| CY14x101QxA | 1 Mbit | No | 8-pin SOIC,<br>16-pin SOIC |
| CY14x512PA | 512 Kbit | Yes | 16-pin SOIC |
| CY14x512QxA | 512 Kbit | No | 8-pin SOIC,<br>16-pin SOIC |
| CY14x256PA | 256 Kbit | Yes | 16-pin SOIC |
| CY14x256QxA | 256 Kbit | No | 8-pin SOIC,<br>16-pin SOIC |
| CY14x064PA | 64 Kit | Yes | 16-pin SOIC |
| CY14Mx064QxA | 64 Kbit | No | 8-pin SOIC,<br>16-pin SOIC |

## Summary

Cypress's serial nvSRAM offers easy integration to all metering ICs and MCUs with standard SPI interface available in the market. It allows infinite read and write cycles. With its rich feature set, it significantly improves the overall system performance of the energy meter. Cypress serial nvSRAMs are drop-in replacements for most serial nonvolatile memories used in metering. Serial nvSRAM devices are a cost-effective alternative to slower, lower endurance technologies, with improved system performance.

## Document History

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| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| ** | 2712588 | KVCP/SKUV | 05/29/09 | New application note |
| *A | 2754282 | ZSK | 08/20/09 | Table 1 is updated to show the current status of the serial nvSRAM parts.<br>Removed CY14B064X from the list. |
| *B | 2944753 | ZSK | 06/09/10 | Updated the Using nvSRAM without a Storage Capacitor section. |
| *C | 3045094 | ZSK | 10/07/10 | Updated Table 1 with the addition of 8-pin SOIC package options.<br>Application note title changed from “nvSRAM in Metering Applications “to “Advantages of nvSRAM over EEPROM in Metering Applications”. |
| *D | 3281260 | ZSK | 06/13/2011 | Updated title from ‘Advantages of nvSRAM over EEPROM in Metering Applications’ to ‘Advantages of Serial Peripheral Interface (SPI) nvSRAM over SPI EEPROM in Metering Applications’.<br>Updated Table 1 with the additional 64 Kbit density SPI nvSRAM part numbers.<br>Removed obsolete parts CY14B101P/Qx, CY14B512P/Qx, and CY14B256P/Qx.<br>Removed DFN package option from all definition fields. |
| *E | 3651613 | ZSK | 06/21/2012 | Added Figure 3 and updated template. Completing sunset review. |
| *F | 4020942 | ZSK | 06/05/2013 | Added example on data transfer time in section “Zero Clock Cycle Write Latency in nvSRAM”.<br>Added Figure 3 “Typical SPI nvSRAM (without storage capacitor) Interface”.<br>Added Figure 5 Pin Diagram of SPI EEPROM and SPI nvSRAM (without AutoStore). |
| *G | 5281352 | ZSK | 06/09/2016 | Sunset ECN.<br>Obsolete AN52433 because all parts/package options discussed in this AN and obsolete.<br>All 8-pin package, non RTC nvSRAM parts are obsolete. All RTC nvSRAMs are 16-SOIC only parts and are not direct replacement for the EEPROM sockets. |

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