AN60580

SIO Tips and Tricks in PSoC® 3 / PSoC 5LP

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Associated Project: Yes
Associated Part Family: All PSoC 3 and PSoC 5LP parts
Software Version: PSoC® Creator™ 3.1 SP2 or higher
Related Application Notes: AN54181, AN72382, AN77759

The special input/output (SIO) pins provide differential input buffer and a means to regulate the high-level output voltage (V_{OH}). The SIO pins are tolerant to input voltages higher than the I/O supply voltage and can sink up to 25 mA current. This application note explains the following applications of SIO pins: comparator, charge pump, Salen-key filter, level shifter, half wave rectifier, peak detector, and sleep wakeup using SIO comparator.

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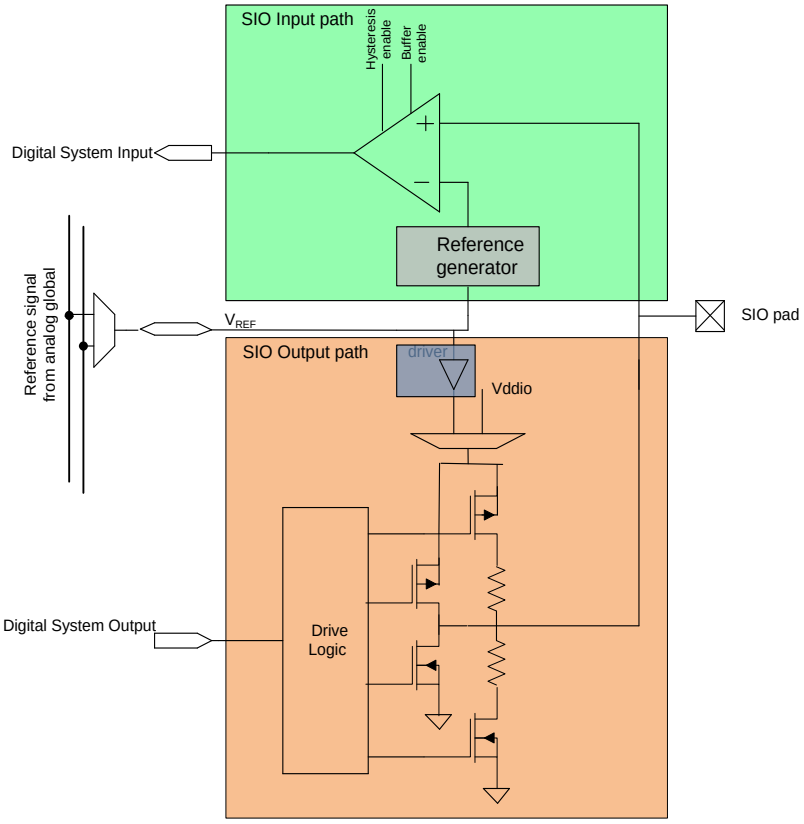
1 Introduction

The SIO input can be set as a single ended or a differential input. When configured as a single ended input, the SIO acts similar to a normal GPIO with standard CMOS and LVTTL input levels. However, when configured as a differential input it acts as a comparator. The reference generator block provides the threshold for the comparator.

The SIO output level can be set as a standard CMOS output or a regulated output. In regulated output mode, the V_{REF} signal selected from Analog Global sets the V_{OH} level. The SIO architecture is shown in Figure 1.

PSoC® 3 and PSoC 5LP devices have eight SIO pins that are organized as four pin pairs. A pair of SIO pins shares a common reference generator block. See the Technical Reference Manual (TRM) for SIO architecture details and PSoC 3 or PSoC 5LP device datasheet for SIO AC/DC specifications.

Figure 1. SIO Architecture

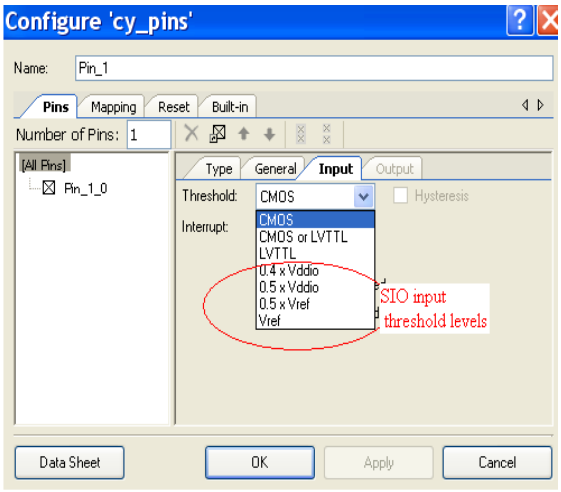


2 SIO Configuration in PSoC Creator™

2.1 SIO Input Configuration

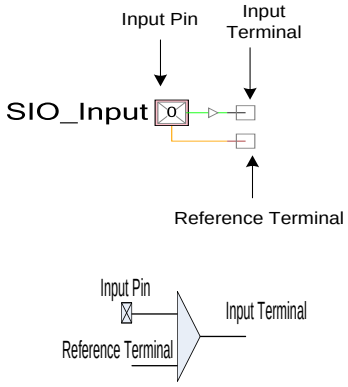
The Digital Input Pin component configuration screen is shown in Figure 2. Selecting one of the four threshold options circled in red configures the pin as SIO in differential input mode.

Figure 2. Digital Input Pin Configuration



Selecting 0.5 x V_{REF} and V_{REF} threshold options add Reference Terminal to the Digital Input Pin component. This allows to route external reference from other components such as DAC or Pin.

Figure 3. Routing External Reference for Differential Input

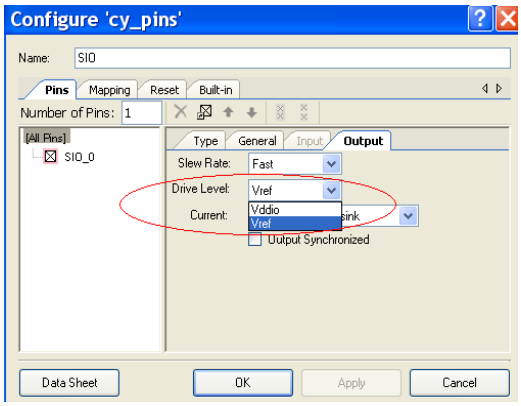


This component uses SIO pin if Hot Swap is enabled and threshold is set to anything other than LVTTL or CMOS. **Note** The outline in pink indicates that the Digital Input Pin component uses SIO pin.

2.2 SIO Output Configuration

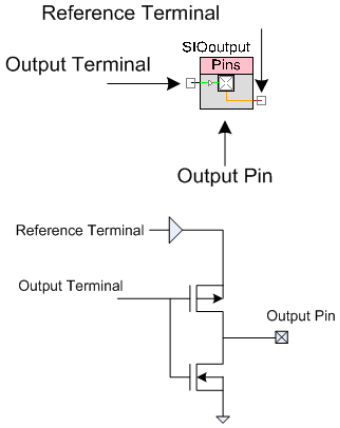
The Digital Output Pin component configuration screen is shown in Figure 4.

Figure 4. Digital Output Pin Configuration



Select V_{REF} Drive Level option to configure the pin as SIO in regulated output mode. It adds reference terminal to the Digital Output Pin component. This allows to route external reference from other components such as DAC or Pin.

Figure 5. Routing External Reference for Regulated Output



GPIO pins can source 4 mA and sink 8 mA; SIO pins can source 4 mA and sink 25 mA.

This component uses SIO pin if Drive Level is set to VREF, and Drive Current is set to a 25 mA sink.

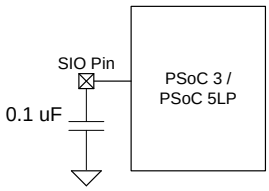
Note The outline in pink indicates that the Digital Output Pin component uses SIO pin.

3 Tip 1: Comparator

When the SIO pin is configured as a differential input, it acts as a comparator. The reference generator block provides the threshold for the comparator. This comparator compares the input signal against the threshold voltage.

SIOs are not ideal comparators hence SIOs are good to be used as comparators when application does not have strict requirements. The dedicated comparators in PSoC 3 and PSoC 5LP devices have faster response and smaller offset voltage (see PSoC 3 or PSoC 5LP device datasheet). Use dedicated comparators when application requires fast response and small offset. Also, it is recommended to use 0.1 µF on SIO input pin as shown in Figure 6. This capacitor filters out any system noise coupling to the signals on the SIO.

Figure 6. External Capacitor on SIO Pin to Remove System Noise

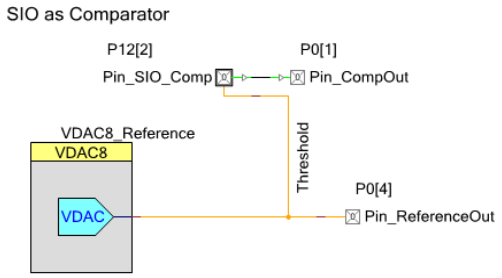


3.1 Top Design

The Digital Input Pin component is placed on the top design and the input threshold is set to V_{REF} to enable external reference routing. This component is named as Pin_SIO_Comp. The VDAC output is connected to the reference terminal of SIO. The Digital Output Pin component is connected to the SIO input terminal and renamed as Pin_CompOut. The analog pin Pin_ReferenceOut is also connected to VDAC to see the reference.

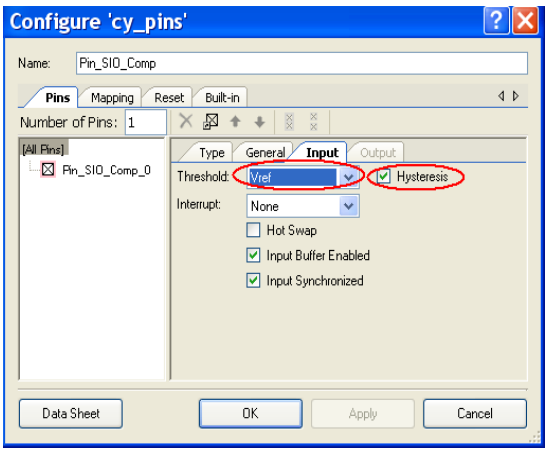
In design wide resources *(*.cydwr)* file, the pins Pin_SIO_Comp, Pin_CompOut, and Pin_ReferenceOut are mapped to P12[2], P0[1], and P0[4] pins.

Figure 7. Top Design for Comparator



3.2 Digital Input Pin Configuration

Figure 8. Digital Input Pin Configuration

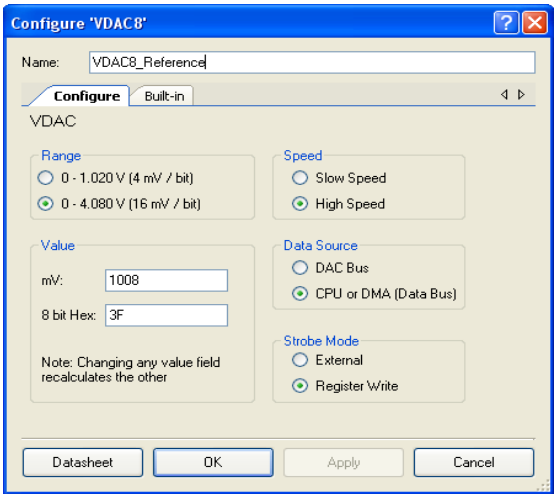


In the input tab, the threshold is set to V_{REF} and hysteresis is enabled. Hysteresis of ±50 mV is provided on the SIO input buffer to remove the noise effects. The SIO_HYST_EN register enables the hysteresis individually for each SIO pin. See the TRM for more details.

3.3 VDAC Configuration

The VDAC voltage is set to 1 V.

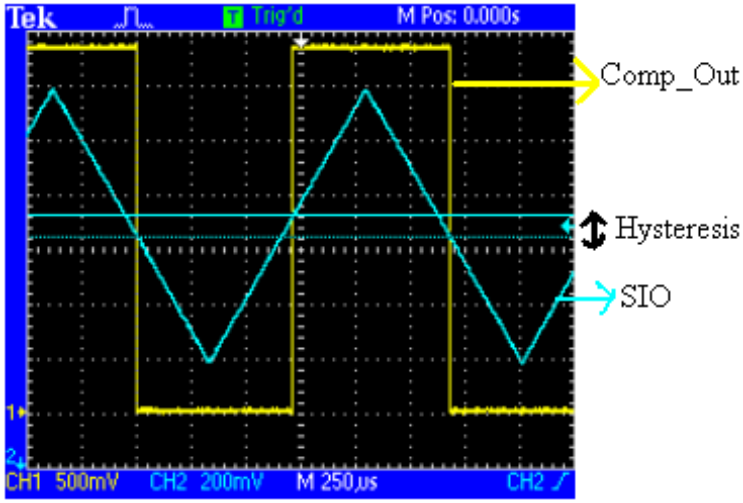
Figure 9. VDAC Configuration



The project details are as follows:

1. Open the project SIO_Comparator, build, and program the PSoC 3 and PSoC 5LP on CY8CKIT-001 Development Kit.
2. The ramp wave with amplitude 1 Vp-p and offset 1 V is given to P12[2].
3. The comparator output is seen on pin P0[1]. Waveforms are shown in the following figure.

Figure 10. Comparator Waveforms



4 Tip 2: Comparator Wakeup

The SIO comparator remains active in sleep and hibernate modes. It can be used to wake up the device from these modes to active mode. The reference signal from the comparator should be routed from external pins as the internal circuits are disabled in these modes.

Note The current with SIO comparator is around 100 µA.

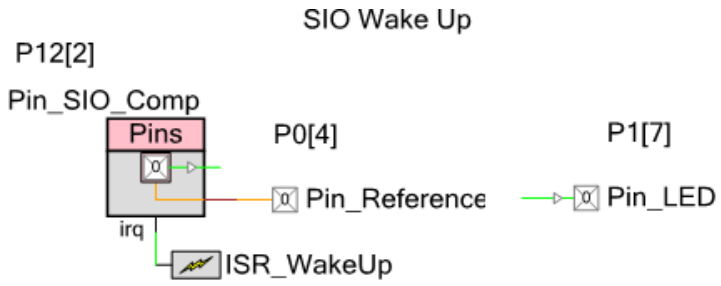
4.1 Top Design

The SIO is configured as comparator as shown in the previous example. The reference to SIO is given externally and this terminal is connected to analog pin named Reference. The interrupt on the rising edge is set in the SIO pin configuration. An Interrupt component is named ISR_WakeUp and connected to the 'irq' terminal of SIO.

In design wide resources (**.cydwr*) file, the pins Pin_SIO_Comp, Pin_Reference, and Pin_LED are mapped to P12[2], P0[4], and P1[7] pins.

Also for device to go in sleep mode, the debug ports must be disabled. In the design wide resources (**.cydwr*) click on the system tab and disable the debug ports select (DPS).

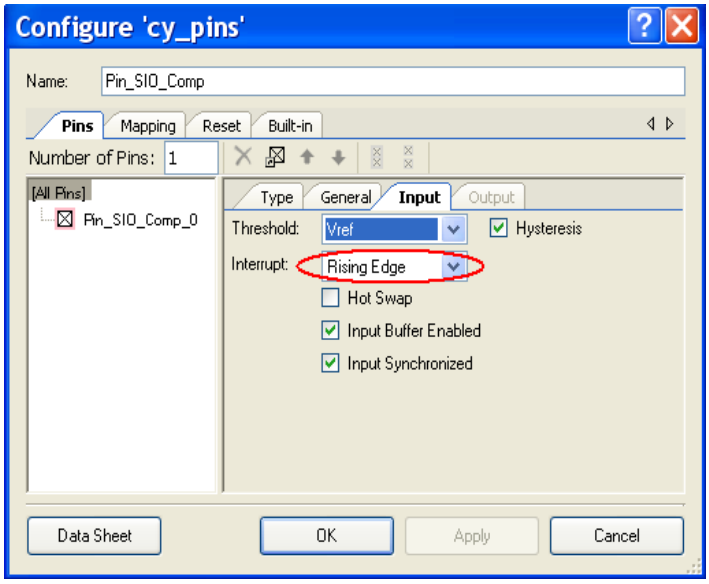
Figure 11. Comparator WakeUp



4.2 Configuration

The interrupt on SIO pin is set as rising edge interrupt.

Figure 12. SIO Interrupt Configuration



In the background loop, the device is put to sleep using CyPmSleep() API. When the SIO voltage crosses the reference, it generates rising edge at comparator output and wakes up the device from sleep. After wakeup, the device enters the ISR routine inside ISR and the interrupt flag is cleared. In the background loop, it toggles the pin Pin_LED before going to sleep again. The same code can be written for the hibernate mode too using CyHibernate().

```
for(;;)
    {
        /* Save all the clocks before going to sleep mode*/
        CyPmSaveClocks();

        /* Puts the device in sleep */
        CyPmSleep(PM_SLEEP_TIME_NONE,PM_SLEEP_SRC_PICU);

        /* Restores all the clocks after coming to Active mode*/
        CyPmRestoreClocks();

        /* When the device wakes up, it toggles the LED */
             Pin_LED_Write(Pin_LED_Read() ^ 1);

        /* Delays between next time the device goes to sleep */
             CyDelay(20);

    }
```

The project details are as follows:

1. Open the project SIO_WakeUp, build, and program the PSoC 3 and PSoC 5LP on CY8CKIT-001 DVK.
2. The potentiometer output VR (on P14 of DVK) is connected to P12[2]. Power the potentiometer by setting J11 to ON position.
3. The VADJ on DVK is set to 1.5 V by varying adjustable resistor R11 on DVK. The VADJ (on P14 of DVK) is connected to P0[4].
4. P1[7] is connected to LED1.
5. Vary the potentiometer VR on the DVK; whenever it crosses the 1.5 V the LED is toggled.

5 Tip 3: Charge Pump

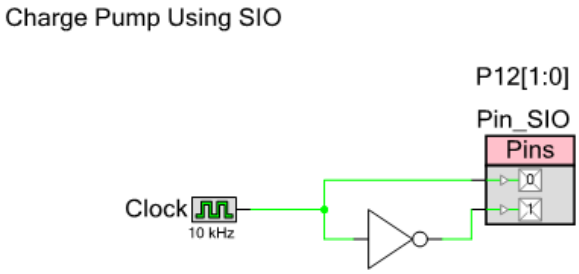
Charge pump is a kind of DC to DC converter that uses capacitors as energy storage elements to create a higher voltage power source.

5.1 Top Design

The Digital Output Pin component is placed in the top design, the number of pins is set to two, and the component is renamed as Pin_SIO. The Pin_SIO_0 pin is configured as an Open Drain, Drive High and the Pin_SIO_1 is configured as a strong drive. A clock of 10 kHz is given to the input terminal of Pin_SIO_0 and the inverted clock is given to input terminal of Pin_SIO_1.

In design wide resources (**.cydwr*) file, these two SIO pins are mapped to P12[1:0] pins.

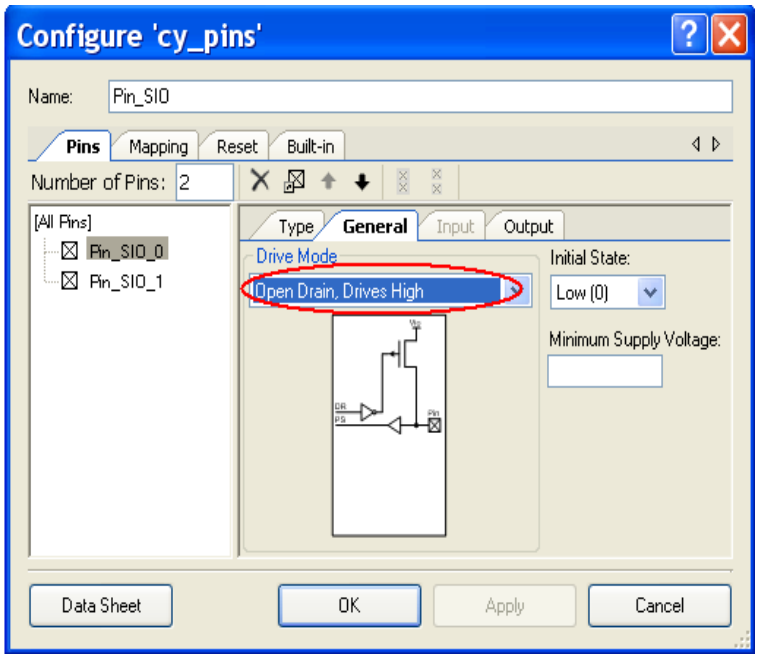
Figure 13. Top Design for SIO Charge Pump

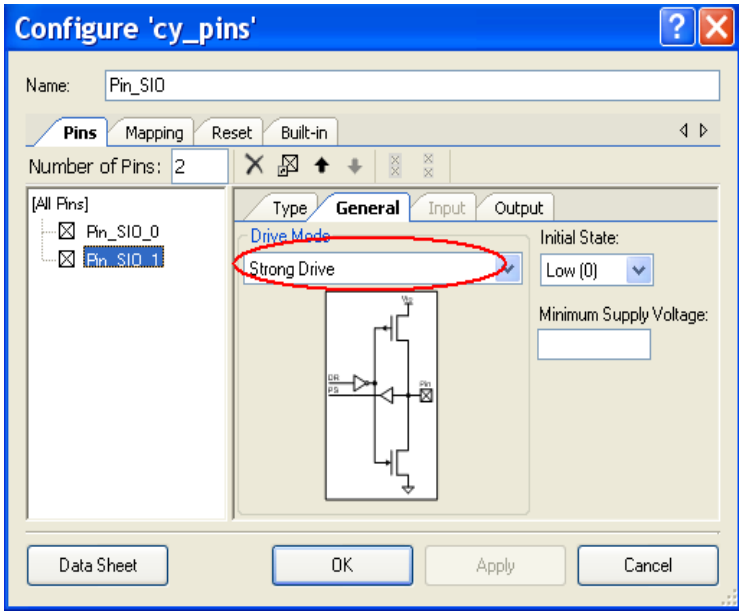


5.2 Configuration

The Pin_SIO_0 and Pin_SIO_1 pin drive mode configuration is as follows.

Figure 14. SIO Pins Drive Mode Configuration

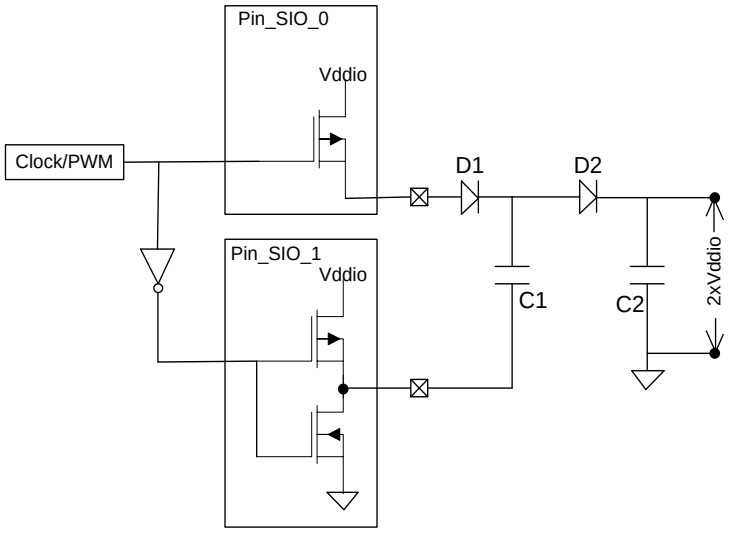




5.3 Equivalent Schematic

Connect an external capacitor to this SIO pair and make a circuit as follows.

Figure 15. Schematic for Charge Pump



When the clock or PWM goes high, the Pin_SIO_0 charges the capacitor C1 to V_{DDIO} referenced against GND on the Pin_SIO_1. When the clock is low the Pin_SIO_0 is floating because of the open drain connection. But the low side of C1 is now V_{DDIO}; this makes C1 to have a 2 X V_{DDIO} voltage developed at its high side. This makes the diode to conduct and thus charges the capacitor C2 to 2 x V_{DDIO}.

Note The capacitor C2 is referenced to GND and hence can see the entire voltage, 2 V_{DDIO}.

This implements a charge pump to double the voltage. There is no need of diode D1 for voltage output up to 5 V because the SIO can withstand maximum of 5 V regardless of V_{DDIO}. To achieve voltages higher than 5 V, the diode is used on the pin. PWM can also be used in place of the clock control. The PWM with a comparator feedback can achieve a feedback controlled voltage.

The project details are as follows:

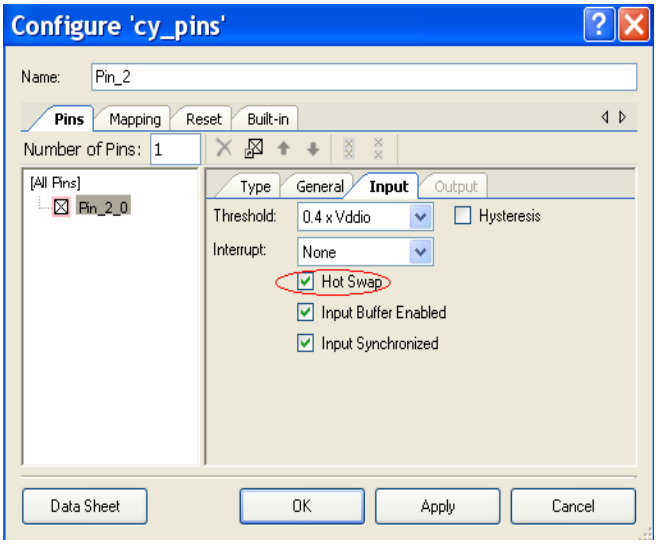
1. Open the project SIO_ChargePump, build, and program the PSoC 3 and PSoC 5LP on the CY8CKIT-001 (DVK).
2. The diodes and capacitors are connected as shown in Figure 15.
3. The voltage of 2 x V_{DDIO} is seen on the capacitor C2.

6 Tip 4: Level Shifter

The SIO pins are tolerant to input voltages higher than the I/O supply voltage. The hot swap feature prevents input from being clamped to the I/O supply level, when the input voltage is above the I/O supply voltage. Each SIO pin can tolerate any input voltage up to 5 V, regardless of I/O supply voltage. In cases where the input voltage exceeds I/O supply voltage, the DC input leakage current is < 100 µA. This feature allows the SIO to be connected to an external bus that can be switched to voltage levels higher than the I/O supply voltage.

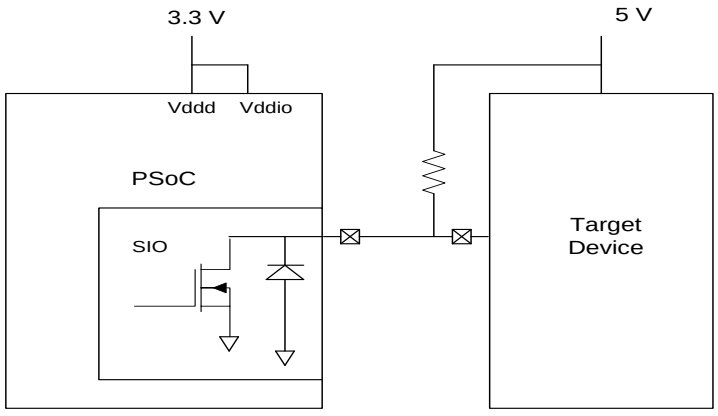
The Digital Input Pin configuration enables Hot Swap feature is shown in Figure 16.

Figure 16. Hot Swap Configuration



Use the hot swap capability to interface to peripherals that operate at different voltage levels. The following example shows how to interface to peripheral operating at 5 V while the PSoC 3 or PSoC 5LP device runs at 3.3 V. The SIO pin Drive Mode is configured to Open Drain, Drive Low mode.

Figure 17. Application using Hot Swap



7 Tip 5: Half Wave Rectifier

The half wave rectifier is achieved with a pair of SIO pins.

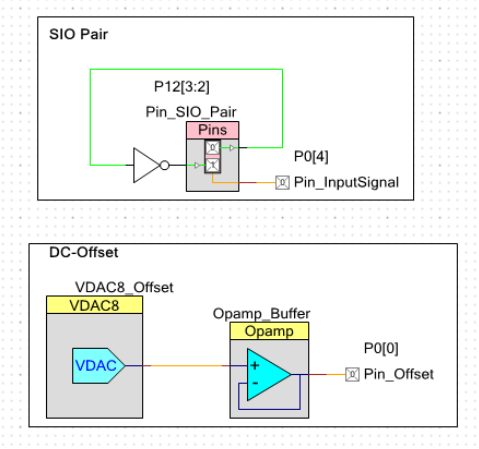
7.1 Top Design

The Digital Output Pin component is placed in the top design, the number of pins is set to two, and the component is renamed as Pin_SIO_Pair. The Pin_SIO_Pair_0 pin is configured as input pin and the threshold is set to V_{REF}. The Pin_SIO_Pair_1 is configured as output pin, the Drive Level is set to 'V_{REF}', and drive mode is set to Open Drain, Drive High. An analog pin is named as Pin_InputSignal and connected to reference terminal of SIO. SIO_Pair_0 input terminal is inverted and then connected to the SIO_pair_1 output terminal.

The VDAC component is placed and named to VDAC8_Offset; it is set to give output of 1 V. The VDAC output is buffered using the opamp component; the opamp is named Opamp_Buffer. The analog pin Pin_Offset connected to the opamp, gives the DC offset for the input signal.

In design wide resources (**.cydwr*) file, the pins Pin_SIO_Pair[1:0], Input_Signal, and Offset are mapped to P12[3:2], P0[4], and P0[0] pins.

Figure 18. Top Design for Half Wave Rectifier



7.2 Pairing SIO pins

To map the pins as SIO pair, click on [All Pins] and select 'Pair Selected SIOs' option.

Figure 19. SIO Pair Configuration

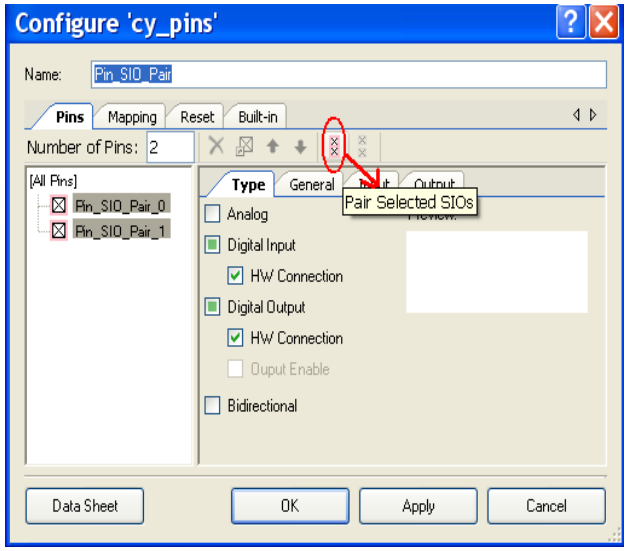
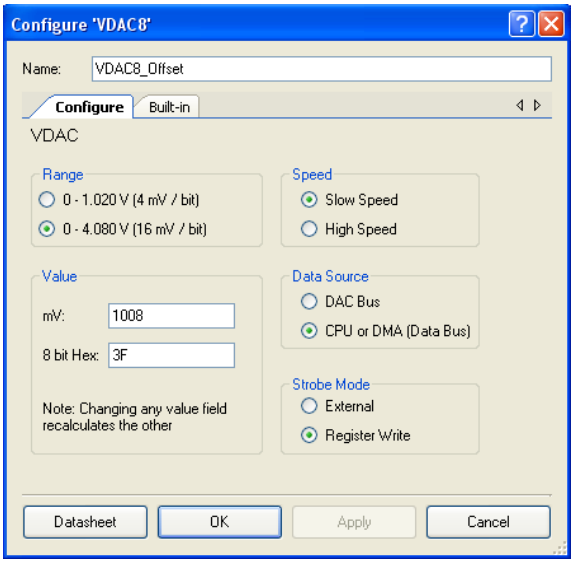
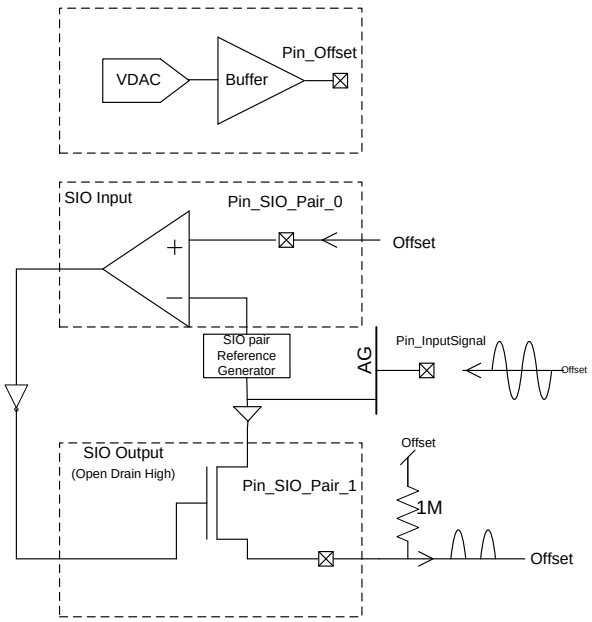


Figure 20. DAC Configuration



7.3 Equivalent Schematic

Figure 21. Equivalent Schematic



The analog input signal is biased on the offset and is given to SIO reference terminal. The Pin_SIO_Pair_0 is connected to offset voltage. Whenever the signal is in positive half cycle the SIO_Pair_0 input is logic 'Low'. This input is inverted and used to drive the other SIO pin Pin_SIO_Pair_1. The Pin_SIO_Pair_1 gives the reference as output as it is configured in regulated mode. Thus in positive half cycle of the input signal, the output of the SIO_Pair_Ref is the signal itself. For negative cycle, the Pin_SIO_Pair_1 outputs High-Z as it is configured in Open Drain, Drive High configuration. The pull-up resistor is connected to make the output equal to Offset during negative cycles.

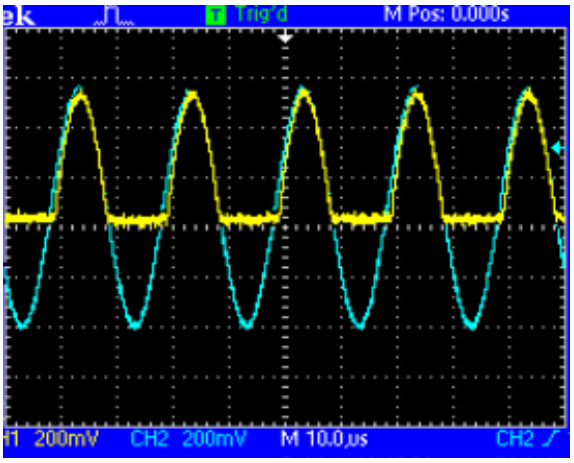
Note The signal should be less than $V_{DDIO}/2$ because the maximum limit on the SIO input threshold in differential mode is $V_{DDIO}/2$.

The project details are as follows:

1. Open the project ‘SIO_HalfWaveRectifier’, build, and program the PSoC 3 and PSoC 5LP on the CY8CKIT-001 DVK.
2. The analog signal is given to pin P0[4] with respect to P0[0]. This makes the input signal biased at ‘Offset’.
3. Connect offset voltage P0[0] to P12[2].
4. The pull up resistor of 1 M is connected between P12[3] and P0[0].
5. Observe the half wave rectified output on pin P12[3].

Waveforms: At 50 kHz, with input 1 Vp-p, offset of 0 V.

Figure 22. Waveforms for Half Wave Rectifier



8 Tip 6: Peak Detector

This section explains how a single SIO can function as a peak detector of an analog signal. It gives the digital signal with transitions at the peaks of the analog signal. The analog signal amplitude level should be less than $V_{DDIO}/2$ peak to peak, because threshold of SIO should be less than $V_{DDIO}/2$.

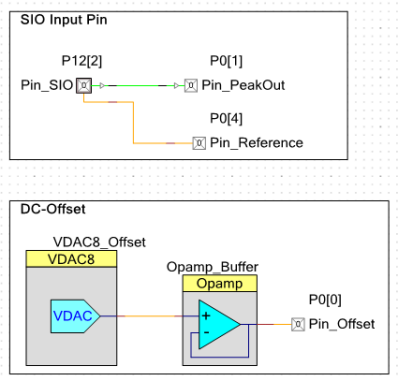
8.1 Top Design

The Digital Input Pin is placed in the top design; the threshold is set to V_{REF} and the pin is named as ‘Pin_SIO’. The Reference terminal of the SIO is connected to the analog pin named Pin_Reference.

The VDAC component is placed and named to ‘VDAC8_Offset’; it is set to give output of 2 V. The VDAC output is buffered using the opamp component; the opamp is named Opamp_Buffer. The analog pin Pin_Offset connected to the opamp, gives the DC offset for the input signal.

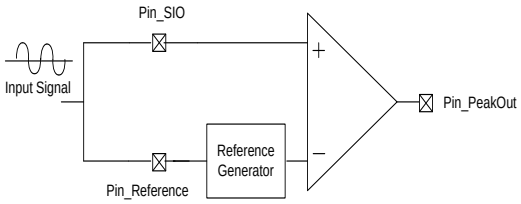
In design wide resources (**.cydwr*) file, the pins Pin_SIO, Pin_Reference, Pin_PeakOut, and Pin_Offset are mapped to P12[2], P0[4], P0[1] and P0[0] pins.

Figure 23. Top Design for Peak Detector



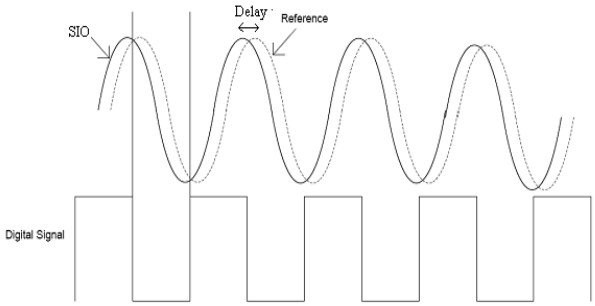
8.2 Equivalent Schematic

Figure 24. Equivalent Schematic



The analog signal is biased at the Offset voltage. This signal is connected to both the SIO pin and also to the reference of the SIO. The reference of SIO goes to the reference generator and it experiences a small delay in reaching the threshold input of the comparator. This delay between the SIO input and the reference input makes it a peak detector. The input signal is compared at the SIO input buffer against the delayed version of the signal and the comparator output crosses zero at the peaks, as shown in Figure 25.

Figure 25. Waveforms Showing Input and Delayed Signals

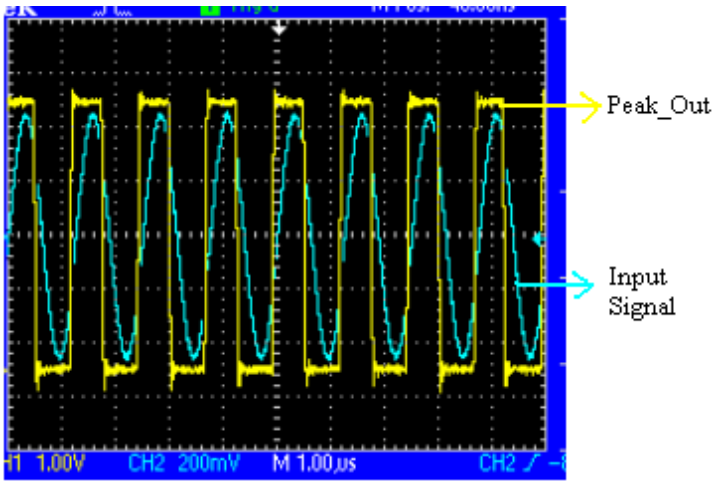


The project details are as follows:

1. Open the project SIO_PeakDetector, build, and program the PSoC 3 and PSoC 5LP on the CY8CKIT-001 DVK.
2. The analog signal is biased on P0[0] and given to both P12[2] and P0[4].
3. The digital output is seen on the pin P0[1].
4. Waveforms are shown in the following figure.

The input signal is at 800 kHz, 1 Vp-p and offset is 2 V. The V_{DDIO} = 5 V.s

Figure 26. Peak Detector Waveforms



9 Tip 7: SIO as SPST/SPDT Switch

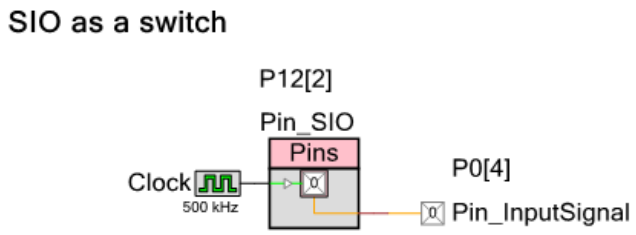
The SIO can be used as a hardware analog switch.

9.1 Top Design

The Digital Output Pin is placed in the Top Design. The drive level is set to V_{REF} and the pin is named as Pin_SIO. An analog pin named as 'Pin_InputSignal' is connected to SIO's Reference terminal. The clock component is set to frequency 500 kHz and connected to output terminal of SIO.

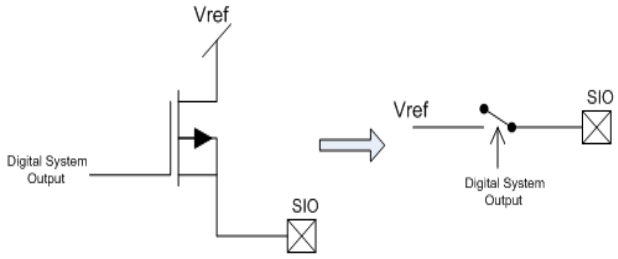
In design wide resources (*.*cydwr*) file, the pins Pin_SIO and Pin_InputSignal are mapped to P12[2] and P0[4] pins.

Figure 27. Top Design for SIO Switch



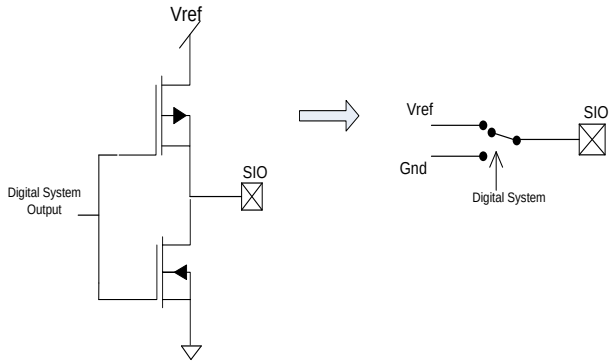
Single Pole Single Throw switch (SPST): SIO pin drive mode is configured as Open Drain, Drives High. The digital output to the SIO connects/disconnects the V_{REF} and SIO pin.

Figure 28. Equivalent Circuit for SPST Switch



Single Pole Double Throw (SPDT): SIO pin drive mode is configured as Strong Drive. The digital output to the SIO connects or disconnects the SIO pin between V_{REF} and Gnd.

Figure 29. Equivalent Circuit for SPDT Switch



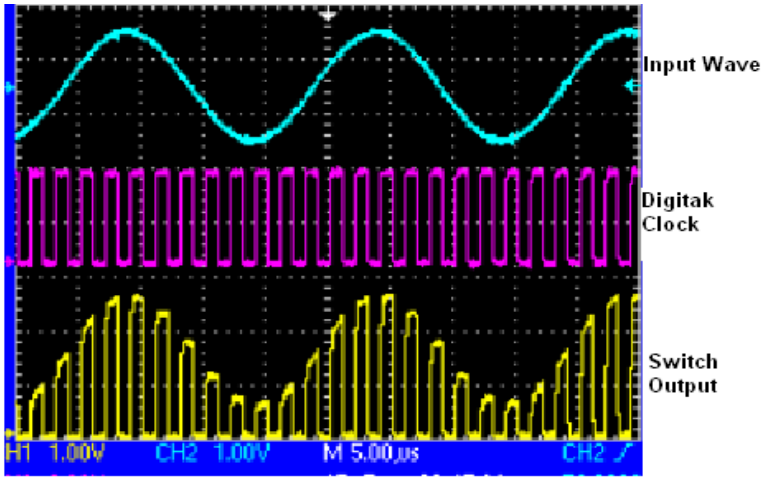
The project details are as follows:

1. Open the project 'SIO_Switch', build, and program the PSoC 3 / PSoC 5LP on the CY8CKIT-001 DVK.
2. The input signal is given to P0[4].

3. The output, which is switched at 500 kHz is seen at P12[2]. The output of P12[2] switches between signal and ground giving the SPDT functionality.
4. Waveforms are shown in the following figure.

A clock of 500 kHz is made to drive the SIO pin configured in ‘Strong Drive’ mode.

Figure 30. Waveforms showing SIO Switch



10 Tip 8: Handling SIOs in sleep mode

SIO input pins should be put in single ended mode before putting PSoC device in sleep mode to reduce PSoC sleep current. SIO’s in differential mode consume high current of 100 uA. To put SIO’s in single ended mode, use the register PRT12_SIO_CFG and set the bits for the specific SIO pair to zero. After coming out of sleep, the bits should be set back to previous values.

PRT12_SIO_CFG:

SIO[7:6]		SIO[5:4]		SIO[3:2]		SIO[1:0]	
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

11 Summary

The SIO pin on PSoC 3 and PSoC 5LP is designed to perform some special tasks. These are level translator, hot swap capability, and high current capability as explained in PSoC Creator configuration section. However, the SIO pin is so resourceful and flexible that many designs can be accomplished with this, making it a powerful feature. Thus, it is useful to consider how to exploit the features of the SIO in every design.

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Document History

Document Title: AN60580 - SIO Tips and Tricks in PSoC® 3 / PSoC 5LP

Document Number: 001-60580

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2901596	PVKV	03/30/2010	New Application Note
*A	2967030	PVKV	07/01/2010	Updated for PSoC Creator 4.1, updated the project and document to work with PSoC 3 / PSoC 5.
*B	3013833	PVKV	08/23/2010	The API Cy_Sleep() is changed to Cy_pm_Sleep(). TIP 2: Comparator Wakeup updated according to a new code.
*C	3443801	PVKV	11/21/2011	Project Updates for PSoC Creator 2.0. Updated template.
*D	3564190	PVKV	03/28/2012	Added a paragraph in Tip 1: Comparator Updated template. Completing sunset review.
*E	3811571	PHAL	11/12/2012	Updated for PSoC 5LP
*F	4015097	PVKV	06/05/2013	Updated Introduction (Updated Figure 1, added Tip 8: Handling SIOs in sleep mode). Updated in new template.
*G	4734347	KRIS	04/23/2015	Updated associated projects to work with PSoC Creator 3.1 SP2
*H	5700420	AESATP12	04/26/2017	Updated logo and copyright.
*I	6328274	SNVN	10/01/2018	Updated template

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