AN221988

Migrating from CY15B104Q to CY15B104QN

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Associated Part Family: CY15B104Q, CY15B104QN

Related Documents: For a complete list, click here

AN221988 discusses the key differences that need to be considered when migrating from CY15B104Q to CY15B104QN. CY15B104Q is now "Not Recommended for New Designs"; this application note explains how CY15B104QN is a replacement for CY15B104Q.

1 Introduction

CY15B104QN, a 4-Mbit Serial (SPI) F-RAM, is a replacement device for CY15B104Q, which is now "Not recommended for new designs". For all designs, CY15B104QN can be considered as a superset of CY15B104Q. The two devices are identical in terms of package composition and dimensions, and read/write functionality. The pinout is almost identical except for one pin (highlighted in Figure 2). This application note discusses the key differences between the two devices that need to be considered when migrating from CY15B104Q to CY15B104QN.

2 Drop-In Replacement or Not?

From a hardware point of view, the key difference is change in the PCB for package pinout (pin 7). From a software point of view, the key difference between the two devices are pin 7 functionality, sleep mode (Hibernate mode) entry time, and Device ID. Refer to the Critical Considerations section for more details.

CY15B104QN adds many features like operation down to 1.8 V, deep power down capability, lower standby current and higher speed capability. Table 1 shows the compatibility chart of CY15B104Q and CY15B104QN. For a detailed comparison of the devices, see Table 3.

Table 1. Compatibility Chart

CY15B104Q Feature or Spec	CY15B104QN Compatible?
Package	Yes
Pinout*	No
Temperature Range	Yes
Operating Voltage	Yes
Operating Current	Yes
Standby Current	Yes
Read / Write Function	Yes
Timing / Frequency	Yes
Data Retention	Yes
Endurance	Yes

* Pin 7 on the CY15B104QN is RESET# and on the CY15B104Q is HOLD#.

3 Ordering Part Numbers

Table 2 lists the recommended CY15B104QN ordering part numbers that correspond to CY15B104Q (Not Recommended for New Designs) ordering part numbers.

Table 2. Recommended Ordering Part Numbers for Migration

CY15B104Q		CY15B104QN		Comments
Ordering Part Number	**Status**	**Ordering Part Number**	**Status**	
CY15B104Q-SXI	Not Recommended for New Designs	CY15B104QN -50SXI	In Sampling	Hardware change is required for pinout difference. System software update is required if you wish to use the Device ID feature and other features supported in CY15B104QN. For more details, refer to section “Critical Considerations”.
CY15B104Q-SXIT		CY15B104QN -50SXIT		

4 Detailed Comparison of CY15B104Q and CY15B104QN

Table 3. Detailed Comparison Table

	CY15B104Q	CY15B104QN	Comments
Package type	-G	-S	Identical “Green (RoHS)” package for SOIC.
Pinout/package Outline	SOIC-8	SOIC-8	Identical outline and board footprint. CY15B104QN has RESET# functionality on pin 7 versus HOLD# functionality on CY15B104Q. Refer “Pinout” section for more details on the pin 7 difference.
Temperature Range	–40 ºC to +85 ºC	–40 ºC to +85 ºC	Identical
Operating Voltage Range	2.0 V to 3.6 V	1.8 V to 3.6 V	CY15B104QN allows operation down to 1.8 V.
Active Supply Current (typ)	300 µA @ 1 MHz - 3.0 mA @ 40 MHz -	250 µA @ 1 MHz 1.0 mA @ 20 MHz 2.0 mA @ 40 MHz 2.4 mA @ 50 MHz	CY15B104QN offers a little higher active current.
Active Supply Current (Max)	300 µA @ 1 MHz - 3.0 mA @ 40 MHz -	400 µA @ 1 MHz 1.4 mA @ 20 MHz 2.6 mA @ 40 MHz 3.2 mA @ 50 MHz	
Standby Current	250 µA @ 85 ºC	54 µA @ 85 ºC	CY15B104QN offers lower standby current
Sleep Mode or Hibernate Current	8 µA	0.9 µA	CY15B104QN offers lower sleep mode current. Sleep function is called Hibernate in CY15B104QN.
CS# high to enter hibernate (t_{ENTHIB})	-	3 µs	Different. Refer to Hibernate Mode section in “Critical Considerations” for more details. Sleep mode of CY15B104Q is refereed as Hibernate mode in CY15B104QN.
Read / Write Function	3-byte addressing, op-codes	3-byte addressing, op-codes	Identical
Clock Frequency	40 MHz	50 MHz	Higher speed offered in CY15B104QN
Data Retention	10 years (+85 ºC)	10 years (+85 ºC)	Identical
Endurance (Write/Read Cycles)	1E+14	1E+14	Identical
V_{DD} Power-Up Ramp Rate (t_{VR})	50 µs / V	50 µs / V	Identical
V_{DD} Power-Down Ramp Rate (t_{VF})	100 µs / V	100 µs / V	Identical
Power-Up to First Access (t_{PU})	1 ms	450 µs	Better power-up to first access specification in CY15B104QN
Device ID	7F7F7F7F7F7FC22608h	7F7F7F7F7F7FC22C00h	Different. Refer to Device ID section in “Critical Considerations” for more details.

5 Critical Considerations

You should consider all the parameter differences mentioned in Table 3 during the migration to CY15B104QN. This section discusses the critical differences between CY14B104Q and CY14B104QN. System designers should also review the datasheet when migrating to the new part.

5.1 Device ID

The CY15B104Q and CY15B104QN incorporate a 9-byte read-only Device ID to identify the product uniquely. The Device ID allows the host to determine the manufacturer, product density, and product revision. Table 4 gives the Device IDs of CY15B104Q and CY15B104QN, where the difference is highlighted in red.

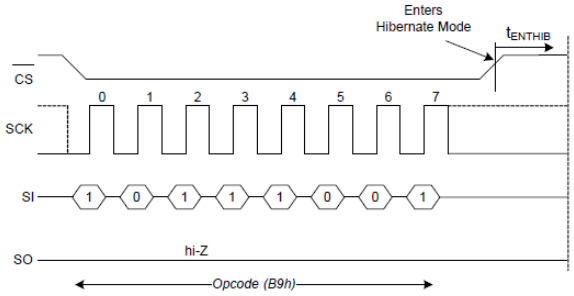
Table 4. Device ID

Device ID	
CY15B104Q	**CY15B104QN**
7F7F7F7F7F7FC22608h	7F7F7F7F7F7FC22C00h

5.2 Hibernate/Sleep Mode

CS# HIGH to enter Hibernate (t_{ENTHIB}) specification is added in CY15B104QN. Note that CY15B104QN will enter Hiberante/Sleep mode after t_{ENTHIB} time (3 µs) after the HBN opcode B9h is clocked in and a rising edge of CS# is applied in your system as shown below in Figure 1.

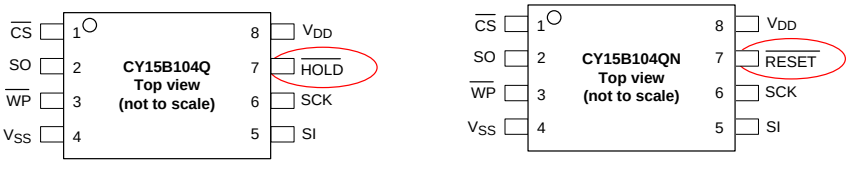
Figure 1: Hibernate Mode Entry



5.3 Pinout

The two parts, CY15B104Q and CY15B104QN have difference in pin 7 functionality. The older part, CY15B104Q has HOLD# on pin 7 while CY15B104QN has RESET# on pin 7 as shown in Figure 2.

Figure 2. Pinout Details Comparison



HOLD, RESET, CS pin names are referred as HOLD# , RESET# , CS# respectively throughout the document.

From the hardware point of view, when replacing CY15B104Q with CY15B104QN, the PCB will not likely require any change, but software change is required to enable RESET# function on the CY15B104QN.

Pin 7 – HOLD# (CY15B104Q): The HOLD# pin is used when the host CPU must interrupt a memory operation for another task. When HOLD# is LOW, the current operation is suspended. The device ignores any transition on SCK or CS#. All transitions on HOLD# must occur while SCK is LOW. This pin must be tied to V_{DD} if not used.

Pin 7 – RESET# (CY15B104QN): This active LOW pin resets the device to default power on status. When RESET# is LOW, the device self-initializes and returns to the standby state. This pin has an internal weak pull-up resistor that keeps this pin HIGH if left floating (not connected on the board). This pin can also be tied to V_{DD} if not used.

Hardware change is required in addition with software change to enable RESET functionality if HOLD# is not used and pin is NC (No connect) in the existing design.

6 Related Documents

Datasheets

- CY15B104Q: 4-Mbit (512 K × 8) Serial (SPI) F-RAM datasheet
- CY15B104QN: 4-Mbit (512 K × 8) Serial (SPI) F-RAM datasheet

Application Note

- AN304 – SPI Guide for F-RAM

Document History

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