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16-Mbit (1M × 16/2M × 8) Static RAM

Features

- TSOP I package configurable as 1M × 16 or 2M × 8 SRAM
- Very high speed: 45 ns
- Temperature ranges
  - Industrial: –40 °C to +85 °C
- Wide voltage range: 2.20 V to 3.60 V
- Ultra-low standby power
  - Typical standby current: 1.5 µA
  - Maximum standby current: 12 µA
- Ultra-low active power
  - Typical active current: 7 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ Features
- Automatic power-down when deselected
- CMOS for optimum speed and power
- Offered in Pb-free 48-ball VFBGA and 48-pin TSOP I packages

Functional Description

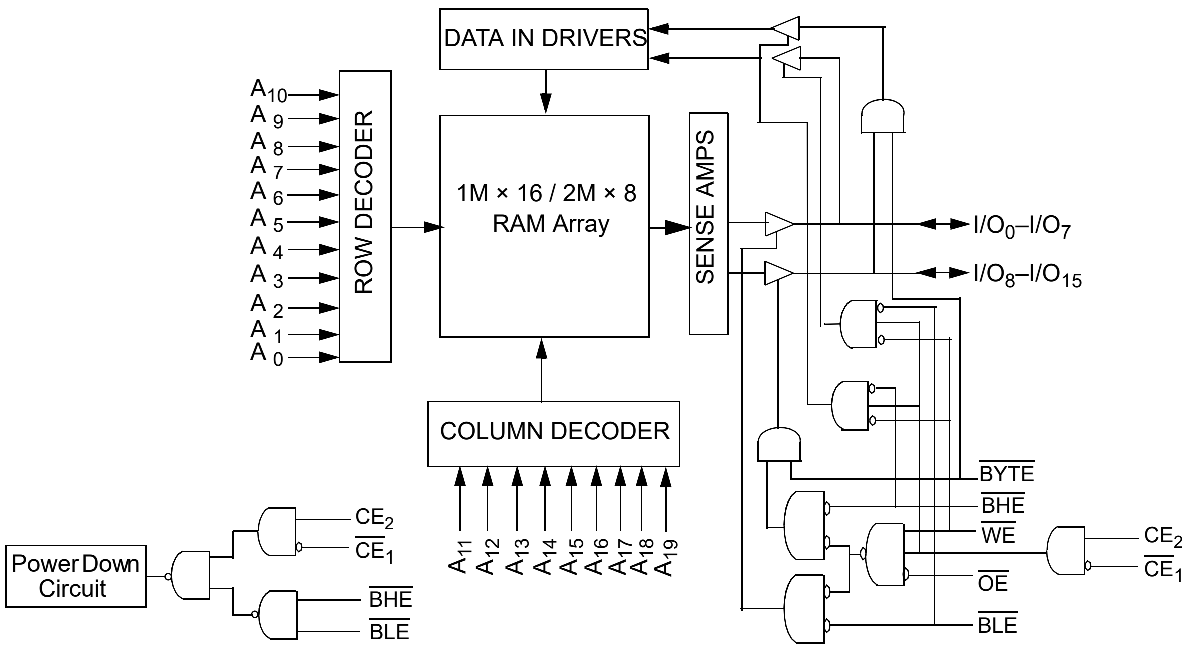
The CY62167EV30 is a high-performance CMOS static RAM organized as 1M words by 16 bits or 2M words by 8 bits. This device features an advanced circuit design that provides an ultra low active current. Ultra low active current is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that reduces power consumption by 99 percent when addresses are not toggling. Place the device in standby mode when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or a write operation is in progress ($\overline{CE}_1$ LOW, CE_2 HIGH and $\overline{WE}$ LOW).

To write to the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{19}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from the I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{19}).

To read from the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See Truth Table on page 13 for a complete description of read and write modes.

For a complete list of related documentation, click here.

Logic Block Diagram



Contents

Pin Configuration

Figure 1. 48-ball VFBGA Pinout (Top View)[1, 2]

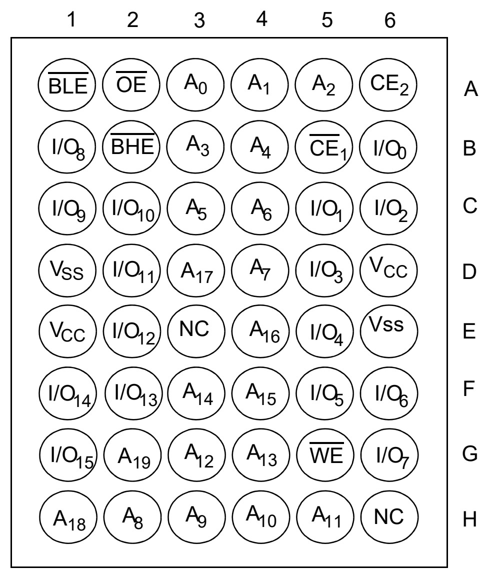
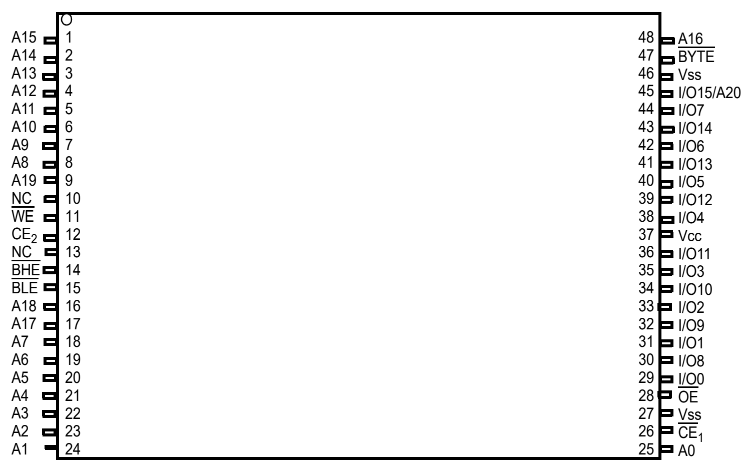


Figure 2. 48-pin TSOP I Pinout (Top View)[2, 3]



Product Portfolio

Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
						f = 1 MHz		f = f_{max}			
		Min	Typ[4]	Max		Typ[4]	Max	Typ[4, 5]	Max[5]	Typ[4]	Max
CY62167EV30LL	Industrial	2.2	3.0	3.6	45	7	9	29	35	1.5	12

Notes
1. Ball H6 for the VFBGA package can be used to upgrade to a 32M density.
2. NC pins are not connected on the die.
3. The BYTE pin in the 48-pin TSOP I package has to be tied to V_{CC} to use the device as a 1M × 16 SRAM. The 48-pin TSOP I package can also be used as a 2M × 8 SRAM by tying the BYTE signal to V_{SS}. In the 2M × 8 configuration, Pin 45 is A20, while BHE, BLE and I/O_8 to I/O_{14} pins are not used.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
5. Refer to PIN#183401 for details of changes.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature .... –65 °C to + 150 °C

Ambient temperature with power applied .... –55 °C to + 125 °C

Supply voltage to ground potential [6, 7] ... –0.3 V to 3.9 V ($V_{CC(max)}$ + 0.3 V)

DC voltage applied to outputs in High Z state [6, 7] .... –0.3 V to 3.9 V ($V_{CC(max)}$ + 0.3 V)

DC input voltage [6, 7] .... –0.3 V to 3.9 V ($V_{CC(max)}$ + 0.3 V)

Output current into outputs (LOW) .... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) .... >2001 V

Latch-up current .... >140 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[8]
CY62167EV30LL	Industrial	–40 °C to +85 °C	2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		45 ns (Industrial) Min	Typ[9]	Max	Unit
V_{OH}	Output HIGH voltage	$2.2 \le V_{CC} \le 2.7$	I_{OH} = –0.1 mA	2.0	–	–	V
		$2.7 \le V_{CC} \le 3.6$	I_{OH} = –1.0 mA	2.4	–	–	V
V_{OL}	Output LOW voltage	$2.2 \le V_{CC} \le 2.7$	I_{OL} = 0.1 mA	–	–	0.4	V
		$2.7 \le V_{CC} \le 3.6$	I_{OL} = 2.1 mA	–	–	0.4	V
V_{IH}	Input HIGH voltage	$2.2 \le V_{CC} \le 2.7$		1.8	–	V_{CC} + 0.3	V
		$2.7 \le V_{CC} \le 3.6$		2.2	–	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage	$2.2 \le V_{CC} \le 2.7$		–0.3	–	0.6	V
		$2.7 \le V_{CC} \le 3.6$	For VFBGA package	–0.3	–	0.8	V
			For TSOP I package	–0.3	–	0.7[10]	V
I_{IX}	Input leakage current	$GND \le V_I \le V_{CC}$		–1	–	+1	µA
I_{OZ}	Output leakage current	$GND \le V_O \le V_{CC}$, Output disabled		–1	–	+1	µA
I_{CC}[11]	V_{CC} operating supply current	$f = f_{max} = 1/t_{RC}$	$V_{CC} = V_{CC(max)}$ I_{OUT} = 0 mA CMOS levels	–	29	35	mA
		f = 1 MHz		–	7.0	9.0	mA
I_{SB1}[12]	Automatic power down current – CMOS inputs	$\overline{CE}_1 \ge V_{CC} - 0.2$ V or $CE_2 \le 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\ge V_{CC} - 0.2$ V, $V_{IN} \ge V_{CC} - 0.2$ V, $V_{IN} \le 0.2$ V, $f = f_{max}$ (address and data only), f = 0 ($\overline{OE}$, and $\overline{WE}$), $V_{CC} = V_{CC(max)}$		–	1.5	12	µA
I_{SB2}[12]	Automatic power down current – CMOS inputs	$\overline{CE}_1 \ge V_{CC} - 0.2$ V or $CE_2 \le 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\ge V_{CC} - 0.2$ V, $V_{IN} \ge V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V, f = 0	$V_{CC} = V_{CC(max)}$ Temperature = 25 °C	–	1.5	3.0[13]	µA
			V_{CC} = 3.0 V, Temperature = 40 °C	–	–	3.5[13]	
			$V_{CC} = V_{CC(max)}$ Temperature = 85 °C	–	–	12	

Notes

6. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
7. $V_{IH(max)} = V_{CC}$ + 0.75 V for pulse durations less than 20 ns.
8. Full Device AC operation assumes a 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after V_{CC} stabilization.
9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
10. Under DC conditions the device meets a V_{IL} of 0.8 V. However, in dynamic conditions Input LOW Voltage applied to the device must not be higher than 0.7 V. This is applicable to TSOP I package only.
11. Refer to PIN#183401 for details of changes.
12. Chip enables ($\overline{CE}_1$ and CE_2), byte enables ($\overline{BHE}$ and $\overline{BLE}$) and $\overline{BYTE}$ must be tied to CMOS levels to meet the $I_{SB1}/I_{SB2}/I_{CCDR}$ spec. Other inputs can be left floating
13. This parameter is guaranteed by design.

Capacitance

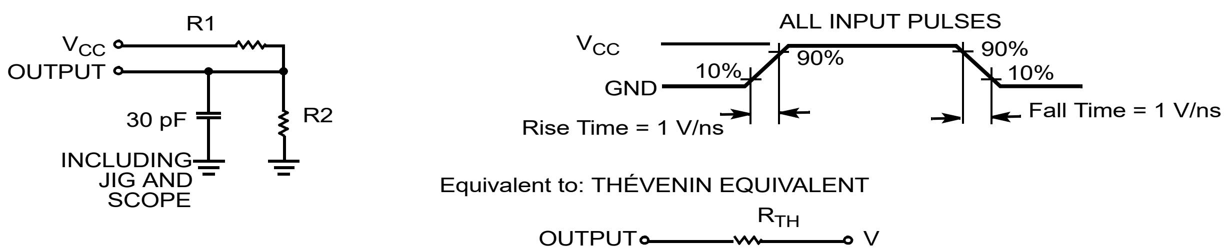
Parameter [14]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [14, 15]	Description	Test Conditions	48-ball VFBGA	48-pin TSOP I	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	31.50	57.99	°C/W
Θ_{JC}	Thermal resistance (junction to case)		15.75	13.42	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Parameters	2.2 V to 2.7 V	2.7 V to 3.6 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Note
14. Tested initially and after any design or process changes that may affect these parameters.
15. Refer to PIN#183401 for details of changes.

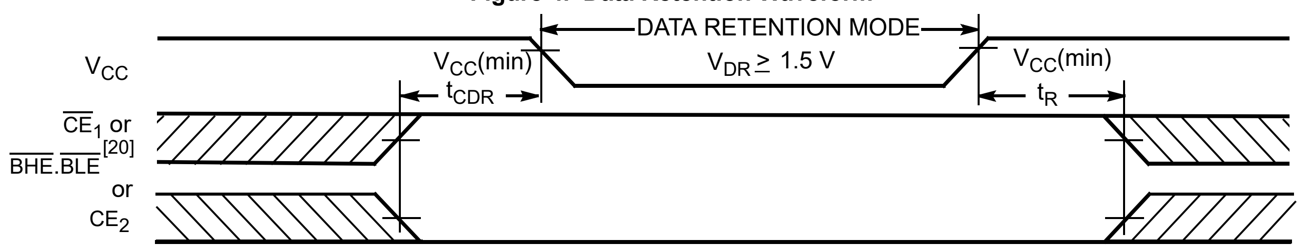
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ [16]	Max	Unit
V_{DR}	V_{CC} for data retention		1.5	–	–	V
I_{CCDR}[17]	Data retention current	V_{CC} = 1.5 V to 3.0 V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	–	10	µA
t_{CDR}[18]	Chip deselect to data retention time	–	0	–	–	–
t_R[19]	Operation recovery time	–	45	–	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform



Notes

16. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
17. Chip enables ($\overline{CE}_1$ and CE_2), byte enables ($\overline{BHE}$ and $\overline{BLE}$) and $\overline{BYTE}$ must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
18. Tested initially and after any design or process changes that may affect these parameters.
19. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
20. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics

Parameter [21, 22]	Description	45 ns (Industrial/ Automotive-A)		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z [22]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [22, 23]	–	18	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z [22]	10	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to High Z [22, 23]	–	18	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to power-up	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to power-down	–	45	ns
t_{DBE}	BLE / BHE LOW to data valid	–	45	ns
t_{LZBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low Z [22]	10	–	ns
t_{HZBE}	$\overline{BLE}$ / $\overline{BHE}$ HIGH to High Z [22, 23]	–	18	ns
Write Cycle[24, 25]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{BW}	$\overline{BLE}$ / $\overline{BHE}$ LOW to write end	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [22, 23]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [22]	10	–	ns

Notes

21. Test conditions for all parameters other than tristate parameters assume signal transition time of 1 V/ns, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in Figure 3 on page 6.
22. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
23. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
24. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
25. The minimum pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 5. Read Cycle No. 1 (Address Transition Controlled)[26, 27]

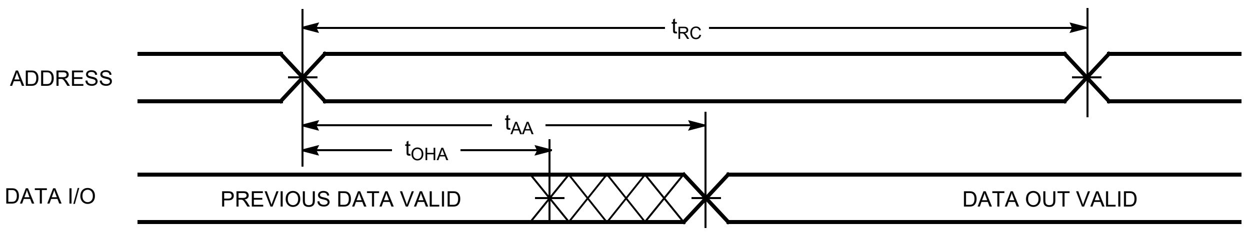
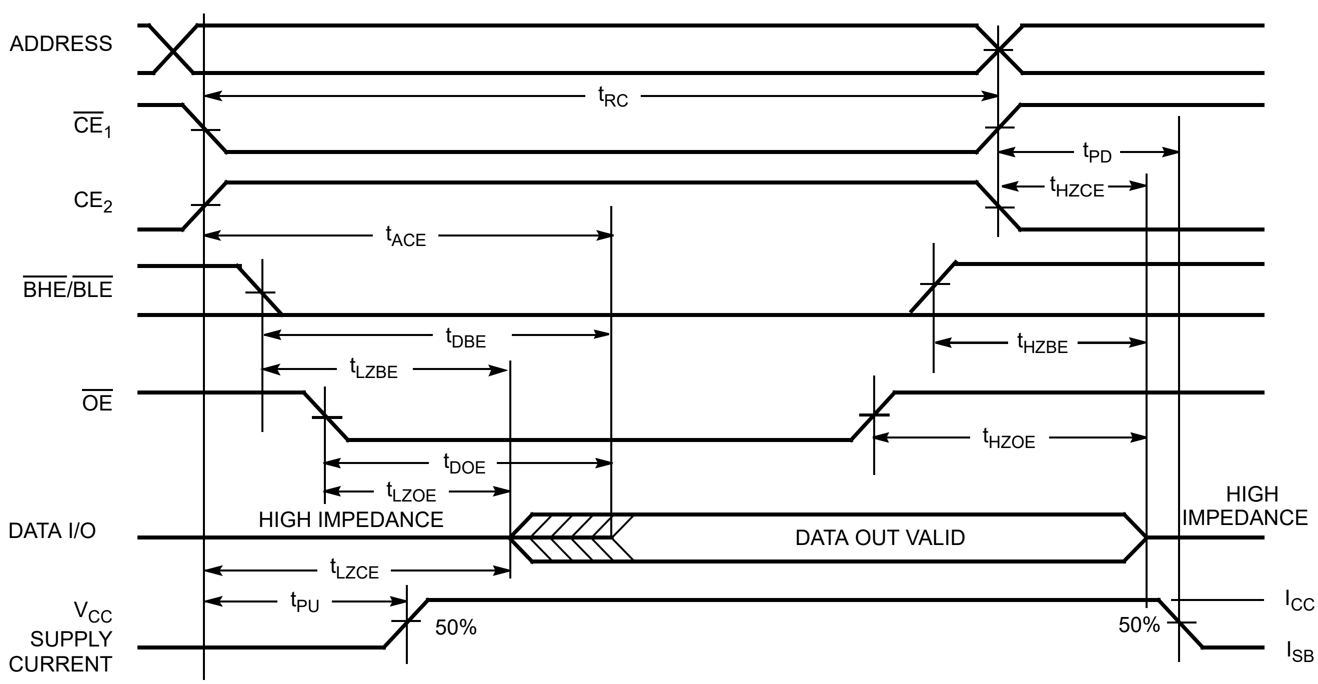


Figure 6. Read Cycle No. 2 ($\overline{OE}$ Controlled)[27, 28]



Notes

26. The device is continuously selected. $\overline{OE}$, $\overline{CE}_1$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}.
27. $\overline{WE}$ is HIGH for read cycle.
28. Address valid before or similar to $\overline{CE}_1$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

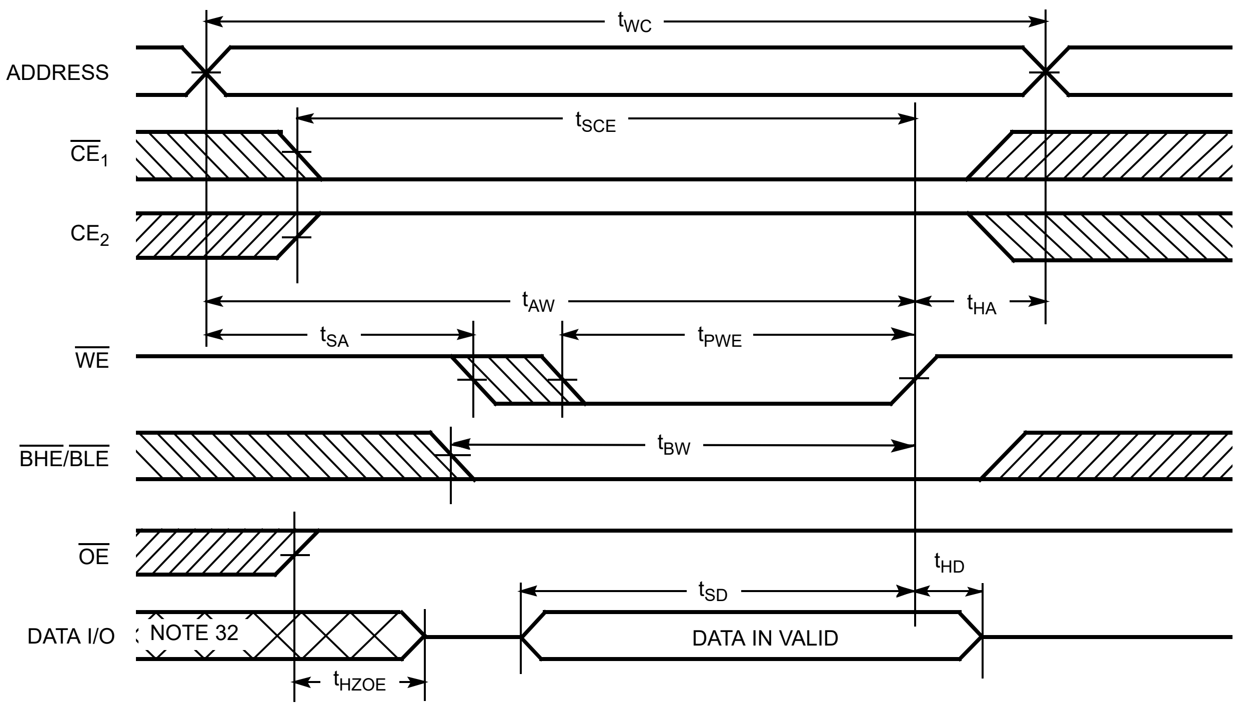


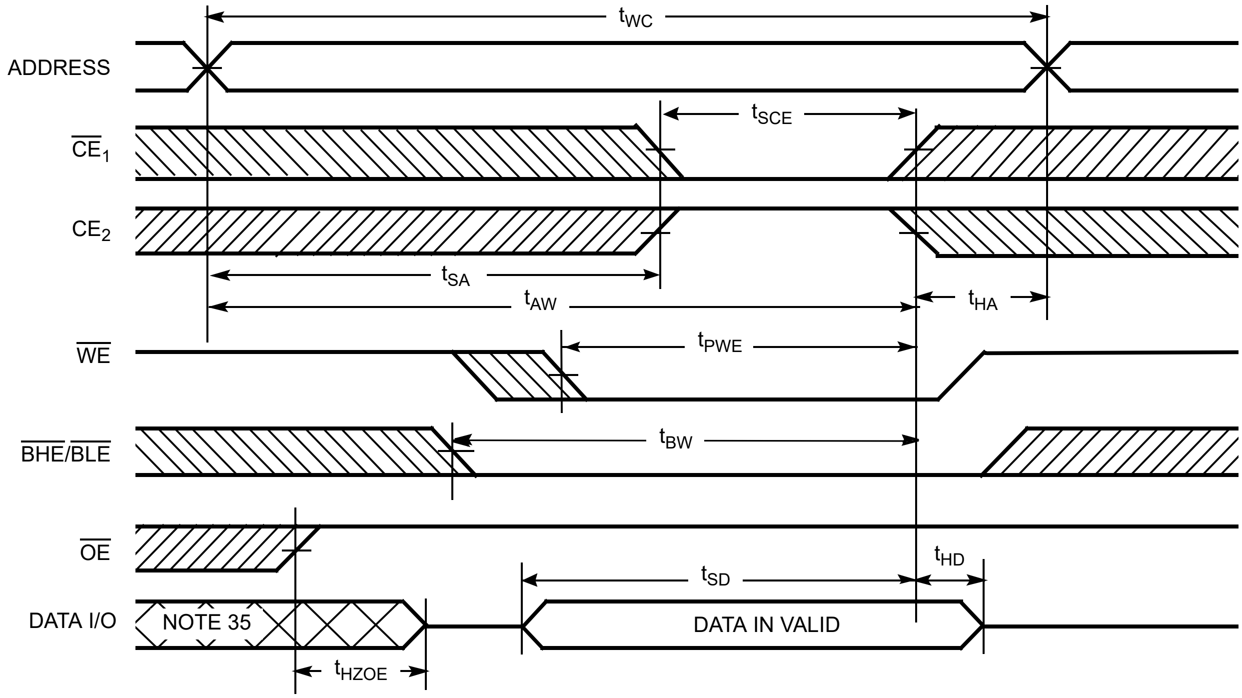
Figure 7. Write Cycle No. 1 ($\overline{WE}$ Controlled)[29, 30, 31]

Notes

29. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
30. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
31. If $\overline{CE}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
32. During this period the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 2 ($\overline{CE_1}$ or CE_2 Controlled)[33, 34]



Notes

33. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE_1}$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
34. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
35. During this period the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW)[36]

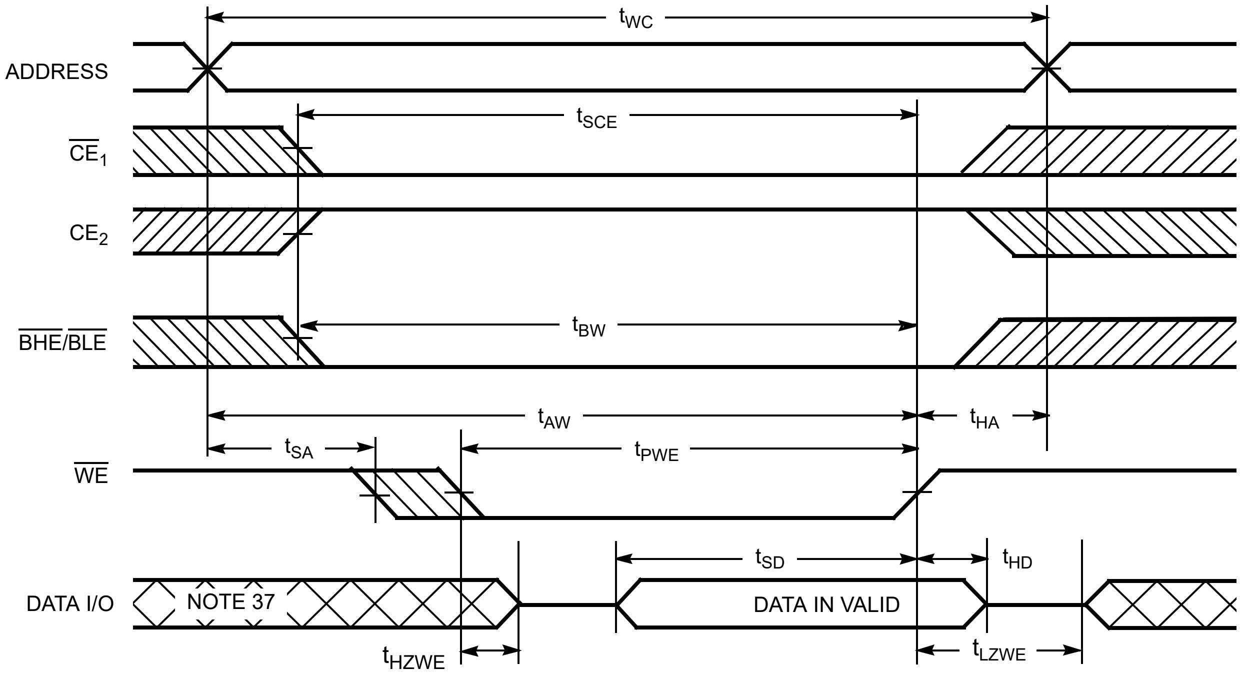
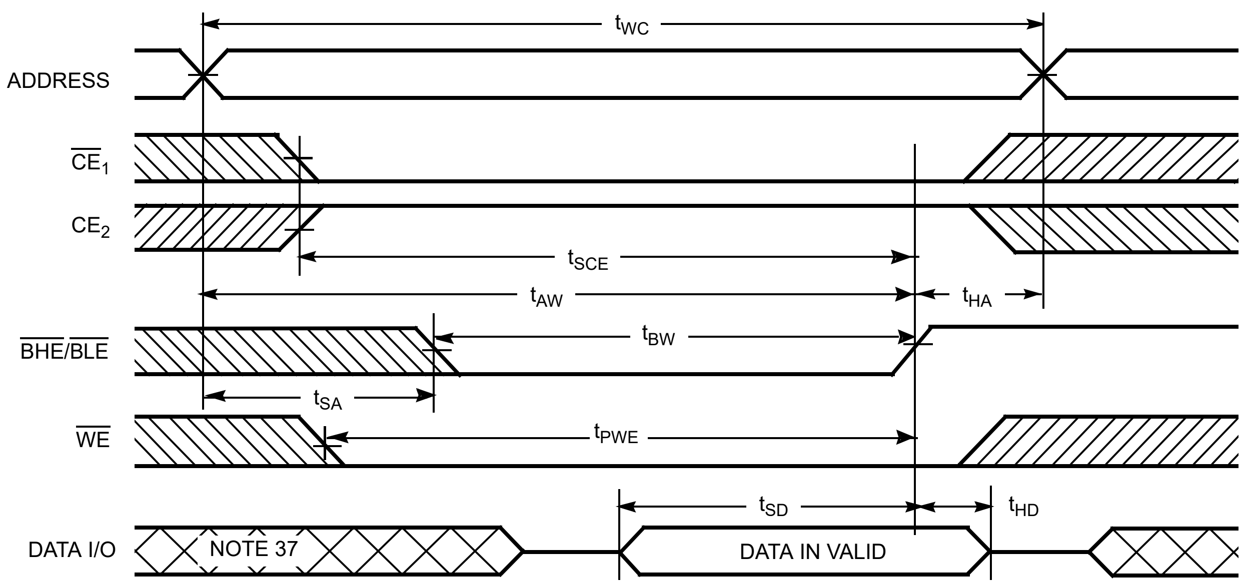


Figure 10. Write Cycle No. 4 ($\overline{BHE}$/$\overline{BLE}$ controlled, $\overline{OE}$ LOW)[36]



Notes

36. If $\overline{CE}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
37. During this period the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X[38]	X	X	X[38]	X[38]	High Z	Deselect/Power-down	Standby (I_{SB})
X[38]	L	X	X	X[38]	X[38]	High Z	Deselect/Power-down	Standby (I_{SB})
X[38]	X[38]	X	X	H	H	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O_0–I/O_7); High Z (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	L	H	High Z (I/O_0–I/O_7); Data Out (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	Data In (I/O_0–I/O_7); High Z (I/O_8–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	L	H	High Z (I/O_0–I/O_7); Data In (I/O_8–I/O_{15})	Write	Active (I_{CC})

Note

38. The ‘X’ (Don’t care) state for the chip enables and Byte enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62167EV30LL-45BVI	51-85150	48-ball VFBGA (6 × 8 × 1 mm), Package Code: BV48	Industrial
	CY62167EV30LL-45BVXI	51-85150	48-ball VFBGA (6 × 8 × 1 mm) (Pb-free), Package Code: BZ48	
	CY62167EV30LL-45ZXI	51-85183	48-pin TSOP I (Pb-free)	

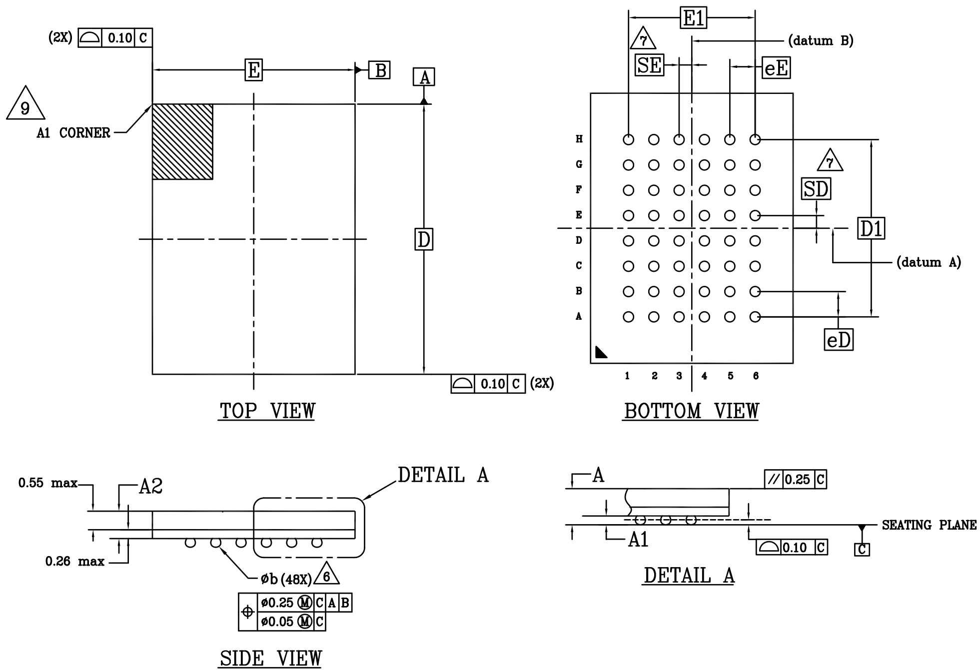
Ordering Code Definitions

CY 621 6 7 E V30 LL - 45 XX X X

- Temperature Grade: X = I
  I = Industrial;
- Pb-free
- Package Type: XX = BV or Z
  BV = 48-ball VFBGA
  Z = 48-pin TSOP I
- Speed Grade: 45 ns
- LL = Low Power
- Voltage Range: V30 = 3 V typical
- Process Technology: Low Power
- Bus Width = × 16
- Density = 16-Mbit
- Family Code: 621 = MoBL SRAM family
- Company ID: CY = Cypress

Package Diagrams

Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) Package Outline, 51-85150



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	-	-
A2	-	-	0.81
D	8.00 BSC		
E	6.00 BSC		
D1	5.25 BSC		
E1	3.75 BSC		
MD	8		
ME	6		
n	48		
Ø b	0.25	0.30	0.35
eE	0.75 BSC		
eD	0.75 BSC		
SD	0.375 BSC		
SE	0.375 BSC		

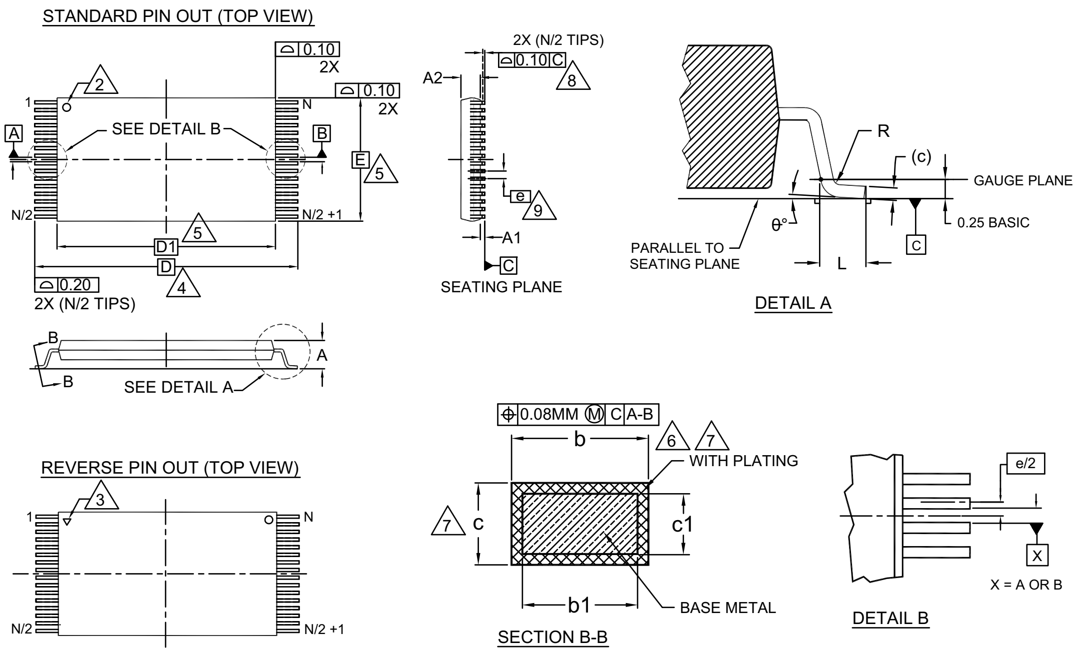
NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.

51-85150 *I

Package Diagrams (continued)

Figure 12. 48-pin TSOP I (18.4 × 12 × 1.2 mm) Package Outline, 51-85183



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	20.00 BASIC		
D1	18.40 BASIC		
E	12.00 BASIC		
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	—	8
R	0.08	—	0.20
N	48		

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS (mm).
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C- . THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm .
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
10. JEDEC SPECIFICATION NO. REF: MO-142(D)DD.

51-85183 *F

Acronyms

Table 1. Acronyms Used in this Document

Acronym	Description
$\overline{BHE}$	byte high enable
$\overline{BLE}$	byte low enable
$\overline{CE}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{OE}$	output enable
SRAM	static random access memory
TSOP	thin small outline package
VFBGA	very fine-pitch ball grid array
$\overline{WE}$	write enable

Document Conventions

Units of Measure

Table 2. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62167EV30 Industrial MoBL, 16-Mbit (1M × 16/2M × 8) Static RAM Document Number: 002-24706			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
**	6267677	07/31/2018	New data sheet.
*A	6294735	08/29/2018	Updated Product Portfolio: Added Note 5 and referred the same note in “Typ” and “Max” columns under “Operating I_{CC}”. Updated Electrical Characteristics: Added Note 11 and referred the same note in I_{CC} parameter. Updated Thermal Resistance: Added Note 15 and referred the same note in “Parameter” column.
*B	6843831	04/01/2020	Updated Maximum Ratings: Updated Note references in “Supply voltage to ground potential”, “DC voltage applied to outputs in High Z state”, and “DC input voltage” (Replaced “9” with “6”). Updated Package Diagrams: spec 51-85150 – Changed revision from *H to *I. Updated to new template.

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