



**Please note that Cypress is an Infineon Technologies Company.**

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

**Continuity of document content**

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

**Continuity of ordering part numbers**

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

## S25FL129P Programming Guide

Every flash device supports three fundamental operations: Read, Erase, and Program. The Read operation enables access to digital data contents of the flash memory array. The Erase operation converts bits from '0' (programmed) to '1' (erased) and are performed on a sector basis. The Programming operation sets a bit or group of bits from '1' (erased) to '0' (programmed). The S25FL (032/064/129) P Flash Family offers both Single and Multi I/O read and write access modes which provides access bandwidths (BW) up to 40 Mbytes/s. The S25FL129P supports standard Page Programming and Quad Page Programming operations. This document investigates the S25FL-P standard Page Programming and Quad Programming performance and highlights recommended programming practices and verification methods.

### 1. S25FL129P SPI Flash

SPI Flash supports the fundamental flash Read, Erase, and Program operations. The S25FL-P Multi I/O SPI Family supports standard SPI features and provides additional features like increased read and write BW accesses speeds up to 40 Mbytes/s. The S25FL-P faster read and write speeds BW provide for an expanded command set including an enhanced Quad Page Program (QPP) command. The QPP allows the flash input buffer to be filled much faster than standard Page Programming. The next sections compare the S25FL-P standard Page Programming and Quad Programming performance along with recommended programming practices and verification.

#### 1.1 Page Programming vs. Quad Programming

As previously stated a programming operation sets a bit or group of bits from '1' (erased state) to '0' (programmed state). A complete program operation has multiple steps consisting of sending the program command sequence including program address, filling the input buffer with program data, and performing the internal flash program operation. The following investigates these program steps for the S25FL129P both PP and QPP operations.

##### 1.1.1 S25FL129P Programming

- Performs programming on a full page or partial page basis (Page: 256 bytes)
- Page Programming (PP) and Quad Page Programming (QPP)
  - PP fills input page buffer a single bit of data/Clock cycle (PP 2079 clock cycles)
  - QPP fills input page buffer with 4 bits of data/Clock cycle (QPP 543 clock cycles)
- Typical Page program time is 1.5 ms for PP and QPP operations

Table 1. Comparison of Page and Quad Page Buffer Fill Times (8 MByte File: 32K Pages)

SPI Clk	Single Buffer Fill		32K Buffer Fills (8 MB) <sup>(1, 2)</sup>		Cell Programming (s) <sup>2</sup>	Buffer Fill + Prog (s)		Time Delta (s)	Comment
	PP (s)	QPP (s)	PP (s)	QPP (s)	PP/ QPP (s)	PP (s)	QPP (s)		
1	2.1E-03	5.4E-04	66.53	17.38	~48	114.53	65.38	49.15	Time deltas decrease as SPI Clock increases
5	4.2E-04	1.1E-04	13.31	3.48		61.31	51.48	9.83	
10	2.1E-04	5.4E-05	6.65	1.74		54.65	49.74	4.92	
20	1.0E-04	2.7E-05	3.33	0.87		51.33	48.87	2.46	
40	5.2E-05	1.4E-05	1.66	0.43		49.66	48.43	1.23	
80	2.6E-05	6.8E-06	0.83	0.22		48.83	48.22	0.61	

<sup>1</sup> SPI Clock Cycles to fill buffer: PP 2079 clock cycles and QPP 543 clock cycles.

<sup>2</sup> The flash internal Page program time is the same for PP and QPP operations.

This example shows that QPP improves overall program performance. However, systems with faster clock speed will not realize as much benefit for the QPP instruction since the internal page program time is greater than the time it takes to clock data into the input buffer.

## 1.2 Programming Recommendations and Verification

### 1.2.1 Efficient Programming

The most efficient flash programming is achieved when writing full 256 Byte pages, once per page. It is recommended to program 256 bytes at a time, aligned on 256 byte boundaries. Programming data in full, aligned pages is the most efficient method to store data. Using misaligned buffer can force alignment at some level of software or firmware, which can slow down some systems. Please consult the processors documentation to understand any impact on your platform. Some applications require writes that are less than 256 bytes. In this case, the recommended program size is at least 16 bytes aligned on a 16 byte boundary.

Manufacturing environments enable additional efficiencies where production programmers can access multiple flash devices in parallel. This avoids bus contention by only allowing access to a single device at a time. Note accelerated programming is typically used in production environments to further reduce programming times.

### 1.2.2 Flash Operating Environment

Cypress recommends a flash  $V_{CC}$  be maintained within the flash data sheet specification to ensure reliable flash operations. Many times  $V_{CC}$  Bias noise can be reduced via characterization and optimization of the module's signal integrity and power delivery network. These type investigations should be part of the early design planning and validation to ensure the power and ground voltage fluctuations are within an IC's  $V_{CC}$  specification across all operating conditions.

### 1.2.3 Flash Usage Model

Another topic related to flash programming is the flash usage model and product life expectancy. The following two Cypress application notes address flash programming and erasure operations as they relate understanding flash endurance, data retention, and system level tools to extend reliable flash operation if required.

- Practical Guide to Endurance and Data Retention  
<http://www.cypress.com/documentation/application-notes/an99121-practical-guide-endurance-and-data-retention>
- Wear Leveling  
<http://www.cypress.com/documentation/application-notes/an98521-wear-leveling>

### 1.2.4 Programming Verification

The following addresses another important aspect of programming; Programming Verification.

Programming validation starts with an assessment of the flash Read access integrity. Read access assessment is completed by performing basic Read Identification / Read ID check to determine if the system controller is communicating with the flash device correctly. Performing these tests enables first level verification that basic continuity, write timing, and voltage interface do not exhibit any major issues. If the flash Device fails Read assessment, it is highly recommended to re-verify these basic Read operations on a reference system such as an industry standard flash programmer and determine if the reference system can successfully access the flash device. If these first basic reads fail on both systems, the flash is exhibiting gross operational failures and should be examined for signs of mechanical stress or electrical over stress.

Once the device is shown to have good read integrity it is essential to understand the system programming algorithm, any block protection, and software time out constraints. Is the system using an auto timer with no periodic register polling for program operation status?

After sending a program command sequence it is recommended to read the Status Register WIP bit to confirm the device successfully accepted the programming command. To verify successful programming operation completions, it is useful to monitor the status register. The WIP and P\_ERR bits provide status if the Program Operation completed successfully or there was an error. In instances where P\_ERR = 1 (Program Error) is observed during a program operation it is an indication that there is a device fault. Once the program operation is successfully completed it is recommended to perform a 2x read verify operation at high and low flash  $V_{CC}$  range. Note a partially or incompletely programmed device/cell will typically fail read verification against its master pattern.

Please consult the device data sheet to ensure your flash hardware and software adhere to the specified requirements and note the [www.cypress.com](http://www.cypress.com) website can be accessed to obtain SW Driver, flash File Systems, along with numerous applications notes. If you have further questions about using Cypress SPI devices, please contact Cypress support.

## 2. Summary

This document shows the S25FL-P Multi I/O SPI Family supports standard SPI features and additional features like increased read and write BW access speeds up to 40 Mbytes/s, which enables programming option to improve the devices overall programming efficiency. Also highlighted was the concept that full Page programming is more efficient than word programming. To provide reliable flash operation, the designer should characterize the module design to provide an operating environment that at least meets or is better than the flash data sheet recommended operating conditions.

## 3. References

[Cypress S25FL129P data sheet](#)

## Document History

Document Title: AN99203 - S25FL129P Programming Guide

Document Number: 001-99203

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	-	07/09/2010	Initial release.
*A	6245752	BACD	07/18/2018	Updated in Cypress template

## Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

### Products

Arm® Cortex® Microcontrollers	<a href="http://cypress.com/arm">cypress.com/arm</a>
Automotive	<a href="http://cypress.com/automotive">cypress.com/automotive</a>
Clocks & Buffers	<a href="http://cypress.com/clocks">cypress.com/clocks</a>
Interface	<a href="http://cypress.com/interface">cypress.com/interface</a>
Internet of Things	<a href="http://cypress.com/iot">cypress.com/iot</a>
Memory	<a href="http://cypress.com/memory">cypress.com/memory</a>
Microcontrollers	<a href="http://cypress.com/mcu">cypress.com/mcu</a>
PSoC	<a href="http://cypress.com/psoc">cypress.com/psoc</a>
Power Management ICs	<a href="http://cypress.com/pmic">cypress.com/pmic</a>
Touch Sensing	<a href="http://cypress.com/touch">cypress.com/touch</a>
USB Controllers	<a href="http://cypress.com/usb">cypress.com/usb</a>
Wireless Connectivity	<a href="http://cypress.com/wireless">cypress.com/wireless</a>

### PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

### Cypress Developer Community

[Community](#) | [Projects](#) | [Videos](#) | [Blogs](#) | [Training](#) | [Components](#)

### Technical Support

[cypress.com/support](http://cypress.com/support)

All other trademarks or registered trademarks referenced herein are the property of their respective owners.



Cypress Semiconductor  
198 Champion Court  
San Jose, CA 95134-1709

© Cypress Semiconductor Corporation, 2010-2018. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress does not assume any liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit [cypress.com](http://cypress.com). Other names and brands may be claimed as property of their respective owners.