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1. Introduction

Cypress’ USB-C PPS 39W Dual Port Car Charger reference design is based on the EZ-PD™ CCG3PA product family of Cypress’s USB Type-C microcontroller and ActiveSemi ACT5101 buck-boost controller. **Figure 1-1** shows the picture of the reference design board.

**Figure 1-1. EZ-PD™ CCG3PA Car Charger Reference Design Board**

1.1 Overview

In this reference design, CCG3PA serves as highly integrated USB Type-C port controller that complies with latest USB Type-C, PD standards and USB Type-A. This solution supports PD 3.0, PPS, QC 4.0/4.0 +, QC 3.0/2.0, AFC, Apple charging and BC 1.2 on Type-C port. It also supports QC 2.0, Apple charging and BC 1.2 on Type-A port output simultaneously. The default application firmware in CCGX SDK 3.x supports all these features and any further customization can be done using the EZ-PD CCGx Power Software Development Kit (SDK) 3.2 and EZ-PD Configuration Utility (refer section 4.2 Firmware update through CC interface below for more details). The reference design board schematics, hardware design files and firmware example project can be found on the [CCG3PA USB-C 39W dual port Car Charger reference design webpage](#). This reference design has dual port (Type-C and Type-A) functionality and each of them is explained in the following sub-sections.
1.1.1 Type-C Port

On Type-C port of this reference design, CCG3PA device regulates the VBUS voltage by controlling the feedback node of DC-DC controller as shown in the block diagram below, in Figure 1-2.

![Figure 1-2. CCG3PA Type-C Voltage and Current Control Block Diagram](image)

Apart from the USB-PD PPS charging protocol on the Type-C port, it also supports other charging protocols like QC 4.0/4.0+, QC 3.0/2.0, AFC, Apple charging and BC 1.2. This reference design can support maximum power profile of 27W on Type-C port. It supports FIXED_5V@3A, FIXED_9V@3A, PPS_5VPROG@3A, PPS_9VPROG@3A.

In this reference design, CCG3PA device monitors and handles fault protections like Over-Voltage Protection(OVP), Under-Voltage Protection(UVP), Over-Current Protection(OCP) and Short-Circuit Protection(SCP). It also supports two modes of regulation—Constant Voltage(CV) and Constant Current(CC) mode. In the CV mode, CCG3PA regulates the VBUS voltage by controlling the feedback node of DC-DC. In the CC mode of operation, CCG3PA monitors the load current using the internal Low Side Current Sense Amplifier (LSCSA) and integrated error amplifier controls VBUS such that the load current stays at the set limit.

CCG3PA also drives external PFET and controls VBUS discharge with integrated discharge resistors.

1.1.2 Type-A Port

On the Type-A port of this reference design, CCG3PA regulates the VBUS voltage by controlling the PDC node of DC-DC controller as shown in the block diagram below, in Figure 1-3.

![Figure 1-3. CCG3PA Type-A VBUS Control Block Diagram](image)

In this design, the Type-A port supports Apple charging, QC 2.0, AFC and BC 1.2. This design supports power profile of 12W on the Type-A port. It supports FIXED_5V@2.4A, FIXED_9V@1.3A, FIXED_12V@1A.
1.2 Required Hardware & Software Tools

This section lists the hardware and software tools required to get started with this reference design.

- CCG3PA based 39W Car Charger Reference design board with pre-programmed CCG3PA device (not manufactured by Cypress; click here for reference design webpage).
- USBCEE Power Adapter Tester (PAT) board or a Type-C sink device (any Type-C sink device would work).
- Legacy USB sink device (any Type-A sink devices with legacy USB port would work)
- CY4500 EZ-PD™ Protocol Analyzer or Totalphase Analyzer to monitor the traffic on the CC line, the VBUS voltage and the output current.
- 12V to 24V DC Power Supply or Battery to power the CCG3PA board, should provide at least 39W.
- EZ-PD Analyzer Utility
- USBCEE - Tester GUI Software with PPS Support version
2. Basic Operation

This chapter describes how to use this reference design to demonstrate basic functionality using the USBCEE Tester Board.

2.1 Basic Functionality

1. Connect 12V DC power supply input to the EZ-PD CCG3PA Car Charger reference design board. Note that this reference design can work with power adapters with DC input voltages between 12V and 24V. The 12V DC reference has been used as a reference through this user guide to emulate the car-charger functionality.

2. Connect the CY4500 EZ-PD™ Protocol Analyzer to the Type-C port of the reference design board. If users do not have the CY4500 EZ-PD Protocol Analyzer kit, then skip steps 3, 4 and 5.

3. Connect the CY4500 EZ-PD™ Protocol Analyzer to the PC (USB host) using a Micro-USB cable.

4. Launch the EZ-PD Analyzer Utility from Windows > All Programs > Cypress > EZ-PD Analyzer Utility > EZ-PD Analyzer Utility.

5. Click the Start Capturing icon to keep it triggered and ready to start capturing CC traffic.

6. Connect the PAT test tool to the PC using a Micro-B USB cable. The LED on the PAT test tool board will turn ON indicating it is powered.

7. Launch the PAT tool utility from Windows > All Programs > USBCEE > PAT Tool Utility. The utility window will look like the utility screen shown in Figure 2-1.

Using a Type-C cable, connect the Type-C receptacle of the PAT test tool to the Type-C receptacle of the CY4500 EZ-PD™ Protocol Analyzer kit. The setup will look similar to the setup shown in Figure 2-2. Observe that the PD traffic is being captured on the EZ-PD Analyzer Utility. The EZ-PD Analyzer Utility running on the host PC should look similar to that in Figure 2-3.
A successful PD contract can be seen from the PD message sequence. From the messages, it can be seen that the reference design board is acting as DFP (Source/Power Provider), and the Type-C port of the PAT test board is acting as UFP (Sink/Power Consumer). Also, a successful power contract has been established between the two devices at 5V.
The same can be observed on the PAT tool utility that is running. As soon as the setup is completed as shown in Figure 2-2, the PAT tool utility gets updated and shows an output voltage of about 5V on the left-hand side of the utility. The text at the bottom of the utility also gets updated to “USB-PD contract established” as shown in Figure 2-4.

8. In the PAT tool utility, select the output PDO as PDO 4 in the list of PDOs as shown in Figure 2-5. A set of parameters that can be requested opens on the right side of the utility under Request Parameters.

9. In the Output Voltage box, enter any voltage between 3V and 11V in the units of mV. For example, to set the output voltage to 9V, enter “9000” next to the “Output Voltage” box as shown in Figure 2-6. Also observe that the Update Request button is now enabled as shown in Figure 2-6.
10. Click on the Update Request button in the PAT tool utility. Observe that the output voltage in the PAT tool utility changes to about 9V as shown in Figure 2-6.

11. In the EZ-PD Analyzer Utility that is running, additional CC traffic will be captured as shown in Figure 2-7. Observe that the sink device (PAT test board) first sends a request of updated voltage of 9V to the source device (EZ-PD CCG3PA Car Charger reference design board). The source device accepts the request, updates the output voltage to 9V and sends a PS_RDY message as an indication that it has reached the desired output voltage. The sink device responds with a GoodCRC message. Also, as shown in Figure 2-7, observe that the VBUS voltage is now set to about 9V as set in the PAT tool utility.

Figure 2-6. Entering Output Voltage in PPS Mode of PAT tool Utility

Figure 2-7. EZ-PD Analyzer Utility Capturing CC Traffic of Successful Power Contract
Note that the sink device (PAT test tool) repetitively sends the request of updated voltage every 10 seconds. These requests will also be seen from captured CC traffic in the EZ-PD Analyzer Utility (not shown in Figure 2-7). This is expected behavior as per the USB PD spec that as a part of PPS functionality, the sink device needs to keep sending the requested updated voltage on a regular basis to the source device.

12. Repeat steps 8 to 11 to enter another voltage between 3.3V and 11V in the PAT tool utility by selecting PDO 4 (or the appropriate one for your setup) and entering a desired output voltage.

### 2.2 PPS Current Limit Functionality Test

To perform the test, it need to connect E-Load as sink devices. Test setup could refer to Figure 2-8, PPS request could be sent out through PAT board, E-Load could be used to add external load for the testing. The test performs the PPS current limit function test which use below test pattern, Figure 2- shows the test result:

- 11V, 1A, current limit test with CR 7ohm;
- 9V, 2A, current limit test with CV mode 7V;
- 11V, 2A, current limit test with CC mode 2A;

**Figure 2-8. Reference Design Board PPS Current Limit Test with USBCEE Tester Board E-Load**
This shows a successful demonstration of the PPS feature that is supported by the CCG3PA device in the EZ-PD CCG3PA 39W Car Charger reference design project.

2.3 PPS Functionality of Reference Design with Nubia Z17 Phone

This section describes the use of this reference design with a Nubia Z17 phone (model #: Z17 NX563J) and showcasing PPS functionality.

1. Close the PAT tool utility and the EZ-PD Analyzer Utility running on the PC from the previous section.
2. Disconnect the PAT test tool from the CY4500 EZ-PD™ Protocol Analyzer by detaching the Type-C cable connected to the PAT test tool. Also disconnect the PAT test tool from the PC.
3. Launch the EZ-PD Analyzer Utility again from Windows > All Programs > Cypress > EZ-PD Analyzer Utility > EZ-PD Analyzer Utility.
4. Click the Start Capturing icon to keep it triggered and ready to start capturing CC traffic. For users not already familiar with the EZ-PD Analyzer Utility usage, clearing the captured data by clicking on icon will also work rather than closing, re-opening and restarting the data capture.
5. Connect the Nubia phone (model #: Z17 NX563J) to the Type-C receptacle of CY4500 EZ-PD™ Protocol Analyzer using a Type-C cable. The setup will look similar to the setup shown in Figure 2-. Observe that the PD traffic is being captured on the EZ-PD Analyzer Utility.
6. A successful PD contract can be seen from the PD message sequence. From the messages shown in Figure 2- and Figure 2-7 later, it can be seen that the EZ-PD CCG3PA Car Charger reference design board is acting as a DFP (Source/Power Provider), so the Type-C port of the Nubia Z17 phone locks as a UFP (Sink/Power Consumer). The entire message sequence can be summarized into two main set of events:
   a. The sink device (UFP, i.e. the Nubia Z17 phone) first settles down into a power contract with a fixed PDO, i.e. PDO at Object Position 1 with the source device (DFP, i.e. EZ-PD CCG3PA Car Charger reference design board.
   b. After that, the sink device starts a power negotiation with the source, requesting power for the PDO at Object Position 3. Requests are sent in steps of 20mV about every 10 seconds. This happens until an optimum voltage for charging the battery of the sink device (i.e. the Nubia Z17 phone) is reached.

7. As shown in the trace capture in Error! Reference source not found., the sink device, i.e. the Nubia Z17 phone, first sends the request for a power contract for source PDO at Object Position 1. The source device, i.e. the EZ-PD CCG3PA Car Charger reference design board, accepts it and sends a PS_RDY message. The VBUS voltage at this time can be observed to be about 5V.
8. After this power contract settlement, the sink device then starts sending a series of power requests for source PDO at Object Position 3. A request is sent about every 10 seconds, with a voltage increment of 20mV. The CC trace in Error! Reference source not found. shows the multiple requests from the sink device, the source accepting the request and sending the PS_RDY message, and then the sink device sending another request about 10 seconds later. The voltage shown in the VBUS Voltage column also increments by about 20mV upon completion of each request.

Figure 2-7. Sink Device Sending a Series of Requests Every 10 seconds in 20mV Increments
2.4 Charging the Mobile Phone through Type-A Port (Optional)

Disconnect all the hardware connections from the previous section and close the CY4500 EZ-PD Analyzer Utility. Next, connect a mobile phone using USB Type-A port, the reference design could charge any Type-A phones. Figure 2-13 shows the charging status, along with voltage, current values shown from USB Safety Tester.

Figure 2-13. Reference Design Board Charging a Type-A Mobile Phone

IMPORTANT NOTE: The current version of the firmware on the reference design board does not support bootloading over Type-C Interface to update the firmware use SWD interface, see section 4.1 for details.
3. Functionality with Legacy Charging Protocols

This chapter describes how to use customized firmware for this reference design to perform with different legacy charging protocols.

3.1 Required Tools

The tools required for this are:

- EZ-PD CCG3PA Car Charger reference design board,
- USBCEE tester board (optional).
- QC 2.0/3.0 tester board (optional).
- Type-C consumer devices—any consumer device with a Type-C port would work (optional).
- Type-A consumer devices—any consumer device with a Type-A port would work (optional).
- If needed, use the CY4500 EZ-PD or TotalPhase Protocol Analyzer to monitor the traffic on the CC line, the VBUS voltage and the output current.
Figure 3-1. Test Items Overview

- EZ-PD CCG3PA Car charger reference design board
- CY4500 EZ-PD Protocol Analyzer
- Totalphase Protocol Analyzer
- USBCEE Power Adapter Tester (PAT)
- Type-C sink device
3.2 Test Procedure

1. Connect the EZ-PD CCG3PA Car Charger reference design board to the 12V to 24V DC power supply.
2. Using a Type-C cable, connect the Type-C receptacle of this reference design board to any Type-C consumer device.
3. If using a consumer device like a mobile or laptop, the charging status over the Type-C interface can be monitored on the device.
4. Alternatively, connect the CY4500 EZ-PD Protocol Analyzer between the Power Adapter and the consumer device to monitor the CC traffic, the VBUS levels and output current.
5. For PPS voltage steps function test, follow the test procedure described in section 2.1.2.1 – 2.1.2.12.
6. For PPS current limit function test, follow the test procedure described in section 2.2.
7. For a simple function test with QC 2.0/3.0 tester board, follow the steps below:
   a. Connect QC 2.0/3.0 tester board through Type-C port, change to QC 2.0 test mode, use below test pattern to perform the test. Figure 3-2 shows the test results along with the voltage and current values.
      - 5V, 2A;
b. Connect QC 2.0/3.0 tester board through Type-C port, change to QC 3.0 test mode, use below test pattern to perform the test. Figure 3-3 shows the test result along with the voltage values.

- 5V, 2.5A -> 5.2V, 2.5A;
- 3.6V, 2.5A -> 3.8V, 2.5A;
- 11.8V, 2.5A -> 12V, 2.5A;

Figure 3-3. QC 3.0 Test Result Thru Type-C Port

c. Connect QC 2.0/3.0 tester board through Type-A port, test with QC 2.0 test mode, use below test pattern to perform the test. Figure 3-4 shows the test result along with the voltage, current value.

- 5V, 2A;
- 9V, 2A;
- 12V, 1.67A;
8. For PPS current limit function test, follow the test procedure described in section 2.2.
9. For charging the QC mobile phone through Type-C port by QC 2.0/3.0 protocol, connect QC mobile phone using USB Type-C port. As shown in Figure 3-5 the charging status, along with voltage and current values is observed.

Figure 3-5. Reference Design Board Charging QC2.0/3.0 mobile phone
10. For charging the Apple IPHONE through Type-C port in Apple charger 2.4A mode, connect the IPHONE using USB Type-C port. As shown in Figure 3-6 the charging status, along with voltage and current values is observed.

Figure 3-6. Reference Design Board Charging Apple Mobile phone over Type-C Port

11. For charging the Apple IPHONE through the Type-A port by Apple Charger 2.4A mode, connect the Apple IPHONE using USB Type-A port. As shown in Figure 3-7 the charging status, along with voltage and current values is observed.

Figure 3-7. Reference Design Board Charging Apple Mobile Phone over Type-A Port
4. Firmware Update

This chapter describes how to update the firmware for this reference design. This can be done over SWD interface or over CC interface.

4.1 Firmware Update Through SWD Interface

Connect MiniProg3 to the reference design board’s debug connector, figure 3-1 shows the connection, using PSoC programmer software to upgrade hex file to the reference design board. Details refer to PSoC® Programmer User Guide.

The steps to update firmware running on the reference design are as follows:

1. If the kit installation is not performed yet, or was not performed recently, install the latest version of PSoC Programmer software by downloading from the website www.cypress.com/files/psoc-programmer-3271.

2. Connect the USB Mini cable from the PC to the Mini-B receptacle on the MiniProg3 Rev*B device. Connect the 5-pin header of the MiniProg3 device to connector of the reference design shown Figure 4-1.

Figure 4-1. Firmware Update over SWD Interface

3. Open PSoC Programmer and note the enumeration of MiniProg3/xxxxx. In the Port Selection window, select the newly enumerated “MiniProg3.” A blue dot should appear, indicating the selection, as shown in Figure 4-2.
4. Check the following settings in the PSoC Programmer window. They should be the same as shown in Figure 4-2.
   - Programming Mode: Reset
   - Verification: On
   - AutoDetection: On
   - Protocol: SWD
   - Voltage: 3.3 V
   - Connector: 5p
   - Clock Speed: 1.6 MHz (default)

5. Load the new firmware (hex file) by choosing File > File Load. Browse to the location and select the file Activesemi_custom_CYPD3175-24LQXQ_pa.hex.

6. Click the toggle power button in PSoC Programmer to ensure that the MiniProg3 device is delivering power to the target. The red LED on the MiniProg3 device should be turned on and Power should be seen in a green box at the bottom right corner of the PSoC Programmer window as shown in Figure 4-2.

7. Program the new firmware by choosing File > Program.

8. When programming is complete, the message “Programming Succeeded” will appear in the Actions/Results tab of PSoC Programmer.

9. Disconnect the MiniProg3 from the reference design.
4.2 Firmware Update Over CC Interface

This method primarily applies to the CCG3PA family. In these applications, the PAT board can be used to send programming and configuration data as Cypress specific Vendor Defined Messages (VDMs) over the CC line. The PAT board is connected to a Windows PC running the EZ-PDTM Configuration Utility as shown in Figure 4-3 on the other end to program the CCG3PA device.

Figure 4-3. Application Firmware Update over CC Line

Connect PAT board to the reference design board's Type-C port, Figure 4-4 shows the connection, using EZ-PD Configuration Utility tools to upgrade cycad files to the reference design board. Details refer to EZ-PD Configuration Utility User Manual.

Figure 4-4. Firmware Update over CC Interface
A. Terminology

Terminology
This guide assumes that the user of the CY4532 EZ-PD CCG3PA EVK is familiar with the fundamentals of the Type-C connectivity and the USB Power Delivery protocol. A brief description of Type-C terms is provided here for reference.

- Alternate Modes: A feature of a USB Type-C system whereby one or both SuperSpeed lanes may be repurposed for use with a different serial protocol, such as a DisplayPort, eSATA, or Thunderbolt.
- Client: A USB peripheral such as a hub, docking station, or monitor.
- Configuration channel (CC): A USB Type-C bus wire used to transmit protocol signals. This is a half-duplex 300 kHz signal.
- Consumer: A Type-C port that sinks power from VBUS.
- DisplayPort: A digital display interface standard developed by the Video Electronics Standards Association. It is used primarily to connect a video source to a display such as a computer monitor.
- Downstream facing port (DFP): A USB Type-C port on a host or a hub to which devices are connected.
- Dp, Dn: USB Type-C bus wires used to transmit and receive USB 2.0 data.
- Dual-role port (DRP): A USB Type-C port that can operate as either a DFP or a UFP.
- Electronically Marked Cable Assembly (EMCA): A USB cable that includes an IC that reports cable characteristics (such as current rating) to the Type-C ports.
- Host: A USB Host system such as a PC, notebook, and laptop.
- Provider: A Type-C port that sources power over VBUS.
- Sideband use (SBU): A USB Type-C bus wire used for non-USB control signals, such as DisplayPort control signals.
- Type-C Transceiver: A transmitter/receiver that communicates over the CC.
- TX1p, TX1n, RX1p, RX1n, TX2p, TX2n, RX2p, and RX2n: USB Type-C bus wires used to transmit and receive SuperSpeed USB and PCIe or DisplayPort data.
- Upstream facing port (UFP): A USB Type-C port on a device or a hub that connects to a host or the DFP of a hub.
- USB Power Delivery (USB PD, PD): A new USB standard that increases maximum power delivery over USB from 7.5 W to 100 W.
- USB Type-C (Type-C): A new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power and supporting Alternate Modes.
- VBUS: A USB Type-C bus wire used for power; initially 5 V, but can be increased up to 20 V on USB PD systems.
- VCONN: A USB Type-C bus wire used to power the IC in the EMCA.
## Revision History

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