Crystal Parameters Recommendation for Cypress Frequency Synthesizers

Cypress Semiconductor White Paper

Executive Summary

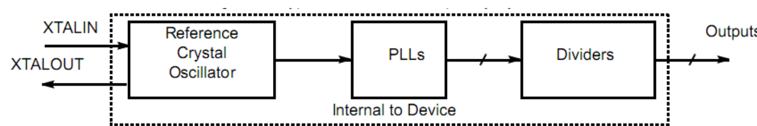
The document describes crystal oscillator of Cypress clock synthesizers. It explains about crystal parameters calculation and its recommendation for Cypress frequency synthesizers. At last general error budget analysis is given for PPM error.

The note applies specifically to Cypress frequency synthesizers and not to Cypress Clock Buffers.

Introduction

A PLL-based frequency synthesizer uses a reference input to generate output clocks. The reference can be provided by a quartz crystal or an external clock source. The accuracy and stability of the output clock is directly proportional to that of the reference. Thus, it is important to provide a stable, accurate, and appropriate reference input.

Figure 1. Typical PLL-based Frequency Synthesizer



Cypress's PLL-Based Frequency Synthesizers

Figure 1 shows the block diagram of a typical PLL-based frequency synthesizer. The reference input to the PLL comes from an on-chip crystal oscillator that is the architecture of all Cypress clock generators. Figure 2 on Page 2 shows the circuitry of the on-chip crystal oscillator (Pierce oscillator) that is formed by components R, G, Ci, and Co, where G is a linear inverter. For this circuit to produce an electrical clock, a quartz crystal needs to be connected between the XTALIN and XTALOUT pins.

The equivalent circuit of a quartz crystal is shown in Figure 3 on page 2. Co is the shunt or static capacitance of the crystal, R1 is the motional resistance, L1 is the motional inductance, and C1 is the motional capacitance of the crystal. R1, L1, and C1 are determined by the mechanical properties of the crystal (they are in the motional arm of the crystal and their circuit effects only exist when the crystal is oscillating). The effective reactance curve of the crystal is shown in Figure 4 on page 2.

Figure 2. On-Chip Crystal Oscillator Circuitry

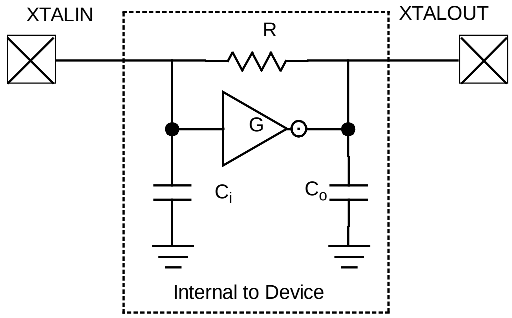


Figure 3. Equivalent Circuit of a Quartz Crystal

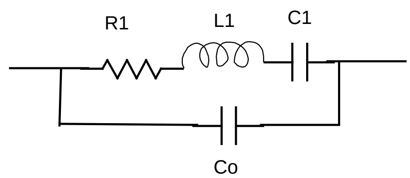
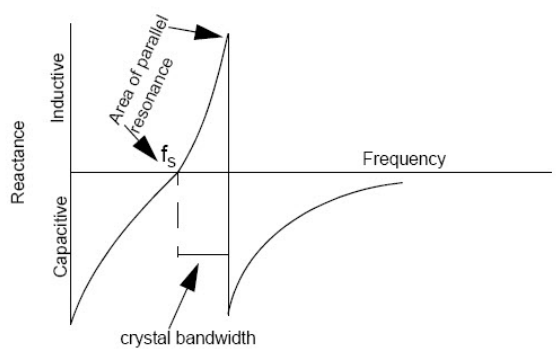


Figure 4. Crystal Reactance v/s Frequency



When connected as a feedback element in an oscillator circuit that has a no phase shift (O°), the crystal oscillates at the series resonating frequency (fs) given by

$$f_s = \frac{1}{2\Pi\sqrt{L_1 C_1}}$$

Equation 1

A Pierce oscillator has a 180° phase shift on the amplifier and needs another 180° phase shift from the feedback element. The feedback element in this case is a crystal along with a capacitive load, and the frequency of oscillation of the crystal (and oscillator circuit) is in the 'area of parallel resonance'. The actual value of the crystal oscillator is parallel to the resonating frequency that is dependent on the capacitive loading seen by the crystal and is given by

$$f_p = f_s\left\{\frac{C_1}{2(C_0 + C_L)} + 1\right\}$$

Equation 2

Where C_L = Capacitive loading seen by the crystal. For example, a 14.318 MHz parallel resonant crystal tuned to a Cload = 18 pF will oscillate at 14.318 MHz (not including tolerance) when it is placed in a Pierce oscillator (parallel oscillator) circuit that offers a capacitive loading C_L=18 pF. If the capacitive loading seen by the crystal in the Pierce oscillator circuit were different from the rated Cload, the change in frequency from the rated frequency is given in Equation 3.

$$\frac{f_{p(rated)} - f_{p(actual)}}{f_{p(rated)}} = \frac{C_1}{2}\left\{\frac{1}{C_0 + C_{load}} - \frac{1}{(C_0 + C_L)}\right\}$$ **Equation 3**

$f_{p(rated)}$ = frequency rating of crystal

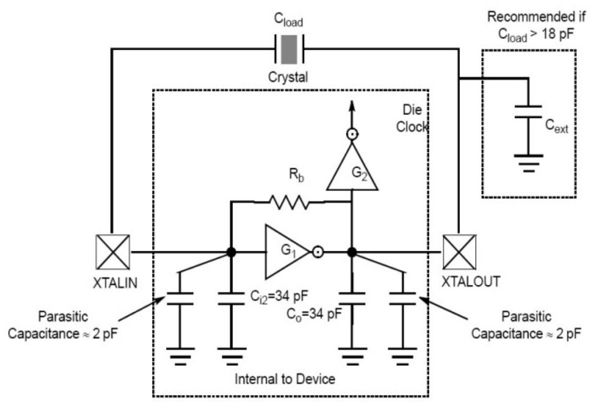
$f_{p(actual)}$ = actual frequency of oscillation in oscillator circuit

C_{load} = Capacitive loading rating of crystal

C_L = Capacitive loading seen by crystal in oscillator circuit.

If a series resonant crystal (which is a crystal whose rated frequency is f_s) is used in a Pierce oscillator circuit, the frequency of oscillation will be higher than the rated frequency by 0.02% or 200 ppm. The actual value of frequency can be calculated from Equation 2.

Figure 5. Using a Crystal as Reference



Crystals Recommended for Cypress Clock Generators

Figure 5 shows the required connection of a crystal to an on chip oscillator of a PLL-based frequency synthesizer. For best results in fundamental mode, a parallel resonant crystal should be used. The load capacitance of this crystal (C_{load}) must match the load capacitance of the oscillator circuitry (C_L), as seen by the crystal. As shown in Figure 5, under normal AC conditions, C_o will be in series with C_{i2}. Thus,

$$C_L = \frac{C_0 \times C_{i2}}{C_0 + C_{i2}}$$ **Equation 4**

C_L = 17 pF. However, if parasitics are accounted for,

$$C_L = \frac{C_{oeq} \times C_{i2eq}}{C_{oeq} + C_{i2eq}}$$ Equation 5

Where, $C_{oeq} = C_o + 2pF$ $C_{i2eq} = C_{i2} + 2pF$

Which results in C_L = 18 pF.

Hence, in fundamental mode, a parallel-resonant crystals with C_{load} = 17 to 18 pF should be used for best results with Cypress clock generators. If the C_{load} of the crystal does not equal 17 or 18 pF, the output frequency will be somewhat different from the target. Since capacitors C_{i2} and C_o are on-chip, no additional external components are required for operation, provided a crystal with matched C_{load} is used.

A Patch for Crystals with an Unmatched Cload

As shown in Figure 6 on page 5, Cypress recommends the addition of an external capacitor, C_{ext}, on or close to the XTAL OUT pin to compensate for a C_{load} > 18 pF. C_o and C_{ext} are in parallel that under AC conditions are in series with C_{i2}. Solving the following equation for C_{ext} that accounts for parasitic,

$$C_L = \frac{C_{i2eq} \times (C_{oeq} + C_{ext})}{C_{i2eq} + (C_{oeq} + C_{ext})}$$

Equation 6

Equation 6 gives the value of the external capacitor required for a crystal with C_{load}= 20 pF, C_{ext} = 9 pF. When C_{load} < 17 pF, solving *Equation 7* (does not account for parasitic) for C_{ext} results in a negative capacitance value.

$$C_L = \frac{C_{i2} \times (C_o + C_{ext})}{C_{i2} + (C_o + C_{ext})}$$

Equation 7

Thus, there is no patch available, instead the user needs to use a crystal with C_{load} = 17 to 18 pF. Using a capacitor in series with the XTALIN or XTALOUT pin will reduce the C_{load} seen by the crystal, but will cause start-up problems. This is because the crystal needs to have a DC voltage across it to start oscillations. And if a capacitor is used in series with the XTALIN and XTALOUT pins, this capacitor will block any DC voltage normally applied to the crystal on start-up.

Using a Series Resonant Crystal

In general, using a series resonant crystal with a parallel resonant circuit will introduce an error on the output frequencies of the device. For Cypress's on-chip oscillator, using a series resonant crystal will typically add a 500 ppm (.05%) error on the output frequencies. For some applications, such as time keeping, choosing the right crystal type is crucial. For example, a 50 ppm error in the reference frequency produces a real time clocking error of two minutes per month. Thus, the user must ensure that proper crystals are used with Cypress clock generators.

Special Case: 32.768 kHz Crystal

The CY2291 offer internal parallel resonant oscillation circuitry that can produce a 32.768-kHz signal, which is commonly used as a real time clock. Since the internal circuitry does not have a biasing resistor on-chip, a 10-M☐ resistor must be placed in parallel to the 32.768-kHz crystal, as shown in Figure 6 on page 5. Performing the calculations based on Equation 4 and Equation 5 results in a crystal requirement of Cload = 12 to 13 pF. If the crystal has Cload ☐13 pF, then a Cext, as calculated from Equation 6, is needed. If the Cload of the crystal is less than 12 or 13 pF, a capacitor cannot be placed in series with the 32XIN or 32XOUT pin, as explained before.

Using an External Signal Source

Frequently, a frequency synthesizer is driven by an external signal source rather than a crystal. In this case, the external clock should be driven in on the XTALIN pin, and the XTALOUT pin must be left floating. Cypress also recommends using a small coupling capacitor in series with the signal, as shown in Figure 7 on page 5. Such a capacitor provides the benefits of reduced loading of the signal source and restoration of duty cycle, as explained below.

Reduced Loading

As shown in Figure 7 on page 5, the two internal capacitors are each 34 pF. Without the coupling capacitor C_{i1}, the frequency source is effectively driving C_{eff}=34 pF (not accounting for parasitics), where C_{eff} is the effective load capacitance seen by the driver. C_{eff} is reduced by the addition of C_{i1} in series with C_{i2}. Now,

$$C_{eff} = \frac{C_{i1} \times C_{i2}}{C_{i1} + C_{i2}}$$

Equation 8

For example, C_{i1}=22 pF and C_{i2}=34 pF results in C_{eff}=13.4 pF. In this case, C_{eff} is reduced by 62%, which results in reduced loading of the frequency source, reduced power supply noise, and thus improved signal transition times. While the load is reduced, so is the amplitude of the signal at XTALIN according to the following equation:

$$V_{i2} = V_{i1}\frac{C_{i1}}{C_{i1} + C_{i2}}$$

Equation 9

Using the same numbers, as in the example above, and setting the input voltage V_{i1} = 5 V_{pp} results in V_{i2} = 2 V_{pp}. However, the reduction in amplitude is not a problem since the linear inverter, G1, helps bias and re-amplifies the signal. Specifically, the DC level of V_{in} equals the DC level of V_{out}, and thus the DC level is biased to V_{DD}/2 (CMOS threshold level). Furthermore, the amplifier circuit, consisting of G1 and feedback resistor R_b, results in an AC gain of the signal.

Figure 6. Using a 32.768 kHz Crystal

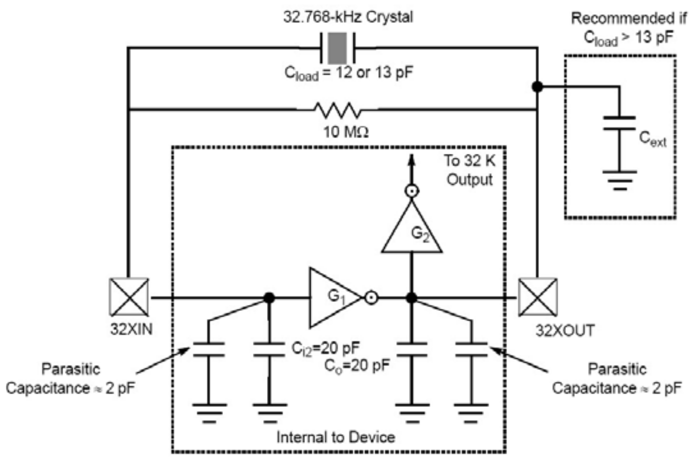
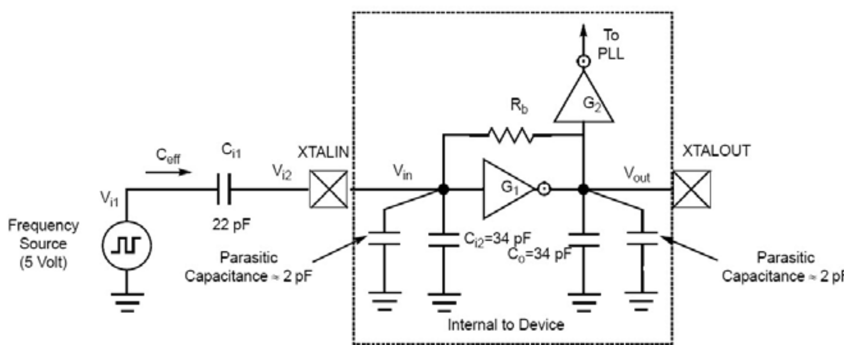


Figure 7. Using an External Driver as Reference



Restoration of Duty Cycle

Typically a waveform at XTALOUT, with a duty cycle of 35%–65%, can have the duty cycle restored close to 50%. This restoration can be seen on the output of G2, in Figure 7, which is typically the XBUF pin on most devices. Both the matched characteristics of G1 and G2, and the R-C components work to restore the duty cycle, the mechanism being an AC gain and their effect on DC biasing, as mentioned. However, duty cycle regulation is reduced by G1 saturating near V_{DD} or ground. To keep G1 in the linear region, C_{i1} should not be too large. A smaller C_{i1} reduces signal amplitude, thus improving linearity.

Coupling Capacitor Value

For Vi1= 5 Vpp applied to a Cypress device, a capacitor value of Cil= 22 to 24 pF, placed as close to the XTALIN pin as possible, is recommended. Using Ci1= 22 to 24 pF provides 2 Vpp around an average DC level of VDD/2 at XTALIN, as well as reduced loading and restored duty cycle. Cypress clock generators require Vi2 = 2 Vpp. Thus for 5 V input signal (Vi1= 5 Vpp), Vi2 = 2 Vpp, and Ci2 = 34 pF, solving *Equation 8* results in Ci1=22 pF. Accounting for parasitics by substituting Ci2eq= 36 pF for Ci2 = 34 pF, the result is Ci1=24 pF. For a 3.3 V input signal (Vi1 = 3.3 Vpp), Vi2 = 2 Vpp, and Ci2 = 34 pF, solving Equation 8 results in Ci1 = 52 pF. Accounting for parasitics results in Ci1=55 pF.

General Error Budget Analysis

As in any good design, an error budget should be calculated. Several sources of error must be taken into account.

- Reference source frequency tolerance (ppm); specified by manufacturer of reference
- Reference source temperature stability (ppm); specified by manufacturer of reference
- Crystal Oscillator process variation (ppm); specified by clock chip manufacturer
- Crystal Oscillator supply voltage and temperature stability (ppm); specified by clock chip manufacturer

The following example uses typical error values for crystals and Cypress clock devices.

Example: Addition of Relevant Sources of Error

Source of Error	Error in ppm
Reference Source, Crystal	
Frequency tolerance	±50 ppm
Temperature stability	±30 ppm
Crystal Oscillator in Cypress Clock Generator	
Process Variation	±20 ppm
Voltage and Temperature stability	±05 ppm
Total	±105 ppm

Summary

Cypress recommends the following for our clock generators. For designs that use a crystal for the input reference, the crystal should be parallel resonant, and must have Cload = 17 to 18 pF. If Cload > 18 pF, then use an external capacitor, as shown in Figure 5 on page 3, with Cext calculated from Equation 6. If Cload < 17 pF, then use a crystal with Cload = 17 to 18 pF. For designs using the 32.768-kHz circuitry, a parallel resonant crystal with Cload = 12 to 13 pF must be used. A 10 MΩ biasing resistor must be placed in parallel with the crystal. 5 V designs using an external clock source must AC couple the clock input with a 22- to 24-pF capacitor in series with the clock source. 3.3 V designs should use a 52- to 55-pF coupling capacitor instead.

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