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WHITEPAPER

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EMI and Spread Spectrum Technology

Abstract

EMI reduction can be achieved using Spread spectrum technique. Spread spectrum technology is discussed in detail and examples of SST supporting devices are included. Application diagram of hard disk drive using SST is discussed. This white paper describes about Electronic Magnetic Interference (EMI) and different EMI suppression techniques.

What is EMI? Why is it a Design Concern?

When electrical current flows in a circuit, an electromagnetic field is created. The strength of this field depends on the frequency and magnitude of the current flow. This field radiates outward from the wires and electronic traces in the equipment that it flows in. Any radiation that is an unwanted by-product of the electrical circuitry's desired function is called Electro-Magnetic Interference (EMI).

This radiation has the potential for either degrading the performance of the equipment that generates it or other (external) equipment in proximity to it. This occurs through the basic "generator" process that happens when there is relative motion between any conductor and any electro-magnetic field. If the levels of these induced currents are high, they can cause malfunctions in equipment, degrade performance, or render it totally useless. It is even worse when they cause other systems to degrade or malfunction. A good example of this is a piece of computing equipment interfering with (and therefore degrading the performance of) a common television or radio receiver. While some levels of EMI are considered acceptable others are clearly not. Determining whether one device impacts the functionality of another is too complex to include as an element in a user manual/guide. To protect consumers from experiencing these problems, federal regulatory agencies such as the FCC have established measurable limits on the amount of EMI that any piece of electronic equipment may emit at any frequency.

To sell an electronic product in the commercial market within the boundaries of the United States, the FCC requires that the product have its electromagnetic emissions measured in a specified environment called an EMI 'range'. Further, the device must have electro-magnetic emissions in very specific frequency bands well below specified values. Here the precise levels and amount of energy emitted in specified frequency bands are measured against set maximum limits and recorded. Europe, Japan, Asia, and the U.S. all have different sets of limits. To sell an electronic product in the world market, it must be tested to each of the corresponding governing bodies' specifications. The test facility may be a small room with a large number of antennae which are used to sense/measure the magnetic waves being emitted (called a closed site) or a large outdoor area taking up many acres (called an open site). These test facilities and the equipment and methods used must be approved and certified by the government. This is necessary for the results to be used in the legal certification of compliance with the emission standards they are required to comply.

Methods to Reduce EMI – Limitations

There are two established and unchanging trends in the electronics industry: Products are released to the market faster and they are cheaper. Each of these factors individually impacts a design's ability to pass federally mandated electromagnetic interference (EMI) testing. Faster speeds result in more EMI at higher frequencies, and lower cost structures reduce the budget, a designer has to meet EMI requirements. EMI is a growing problem and traditional methods of addressing it are not very effective. Many methods have been tried to reduce EMI emissions, each with existing permanent limitations or disadvantages.

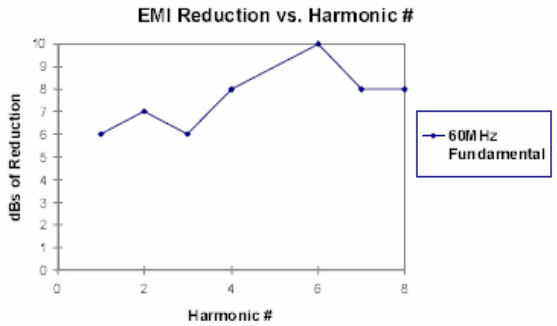
Al the methods that are used to reduce EMI have positive and negative effects on the overall product. Adding more power and ground layers to increase shielding is a good "correct by design" technique but it adds a cost that is usually restrained in mass produced consumer products. Metallic casing is not an option for handheld and portable systems in which weight is considered important; it also adds cost. May be the most familiar method of addressing EMI is by adding passive components or changing the values of existing ones to adjust edge rates to move energy from one harmonic to another. As system speeds rise, timing budgets become more constrained, preventing designers from altering the edge rate drastically. Here, signal performance (clean and fast edge rates) is sacrificed and the repeatability of the "fix" in production can often be poor due to component tolerance consideration.

Contrasted with these "fixes" is spread spectrum timing (SST) technology. This is a "correct by design" method that is implemented during the design effort. It is applied to the fundamental clock frequency at its source and, unlike adding passives, benefits every harmonic. In fact, the higher the harmonics, the more EMI suppressing effect it provides.

"Spread Spectrum" EMI Suppression

Because the FCC and other regulatory bodies are concerned with peak emissions, not average emissions, anything that can reduce the peak energy helps a product meet FCC requirements. In the spread spectrum technique, instead of concentrating all of a frequency reference's energy on a single frequency, the energy is spread out by modulating the frequency. This results in the energy being spread over a frequency range, instead of being concentrated on one particular frequency. The reduction in system EMI can be high up to 10 dB. The reduction is greatest at the higher harmonic frequencies (see Figure 1).

Figure 1. EMI Reduction vs. Harmonic #

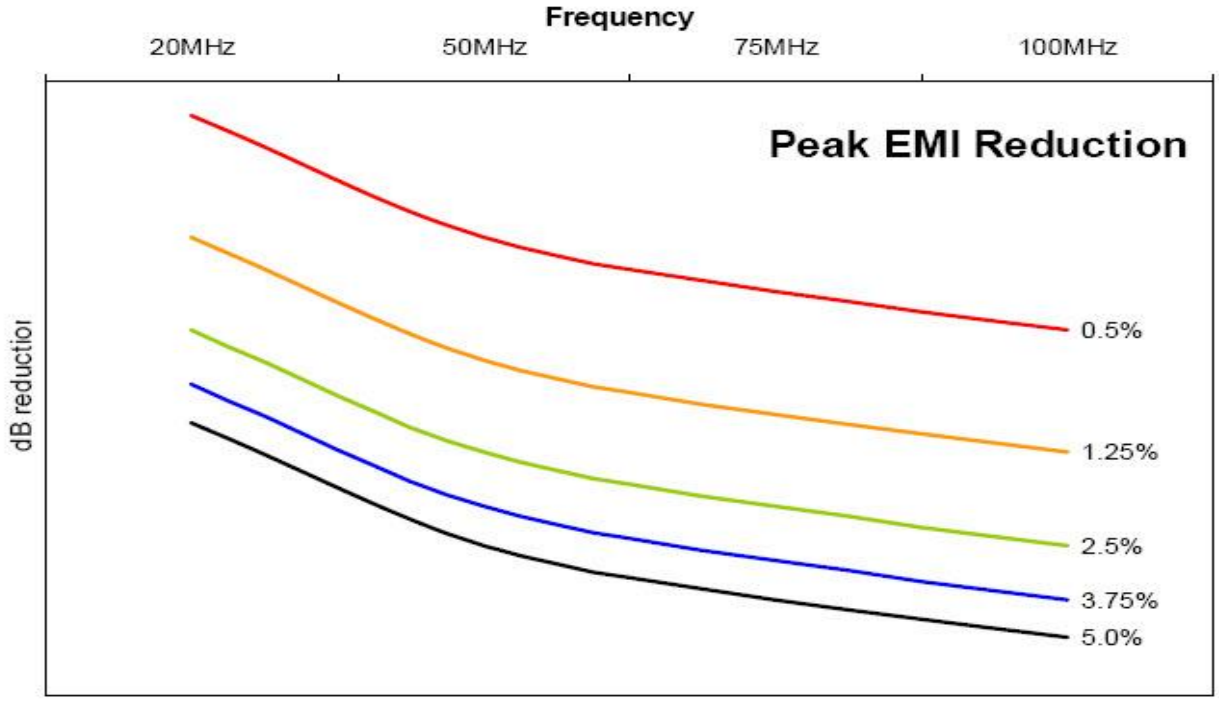


The same total amount of energy is still present; however, the peak value is reduced. In theory it would be possible to spread the signal so far that the energy density can be reduced all the way to thermal noise floor, in which case there would be no harmful emissions in the environment at all. Minimum signal to noise ratio requirements will of course dictate a higher level be used in practice.

Calling this technique "spread spectrum" is a different usage than is conventional in communications usage. Conventionally, spread spectrum means that information is being encoded in a way that it is distributed over a wide bandwidth, as with code division multiple access. With clock ICs, there is no "information" being spread over a bandwidth, we are simply modulating the frequency of a clock. Because it has become common practice to call these devices "spread spectrum clocks," we also use that nomenclature.

The amount of EMI reduction is related to the depth of modulation of the reference frequency. Typical modulation amounts are ±0.5%, or ±1%. The greater the modulation, the higher the EMI reduction. However, as shown in Figure 2 on page 3, the effect is non-linear. For example, each 1.25 percentage point increase in the amount of modulation does not result in the same amount of EMI reduction. The figure also shows that higher frequencies experience a great dB reduction in EMI for a given percentage of modulation.

Figure 2. EMI Reduction vs. Spread Amount and Clock Frequency



When center modulation (±) is used, system processing performance of a CPU will be the same as for a CPU using a non-modulated clock. Some system designers are concerned about overboosting processors; if you use a processor designed for a 100-MHz reference, and that reference spends a substantial part of its time at 100.5 MHz, the processor may be operating at a higher than rated speed during that period of time. To lighten this concern, modulation can be specified as “down only,” for example, –0.5%. A –0.5% modulation, in the same 100-MHz example, would only vary from 99.5 to 100 MHz. This is achieved by moving the center frequency down. What is specified as “100 MHz, with –0.5% modulation” could really be thought of as “99.75 MHz with ±0.25% modulation.” Using down spread only will result in some small performance degradation of a CPU, as the nominal 100-MHz signal is now something less than that.

The modulation frequency selected also affects the EMI suppression performance. Modulation frequencies selected are typically between 25 kHz and 100 kHz based on empirical observations as to the optimal compromise between EMI suppression performance, impact on jitter performance, and ability of the device receiving the reference to track the variations in frequency.

The best dispersion of energy does NOT come with a simple triangular modulation waveform. Research and experimental observation have shown that a complex modulation waveform with precise variations in the transition time actually results in significantly better performance. Cypress has a method for implementing this complex waveform which allows us to closely track the ideal waveform. Our technology allows Cypress to achieve EMI reductions typically 2–3 dB better than is available from competing devices.

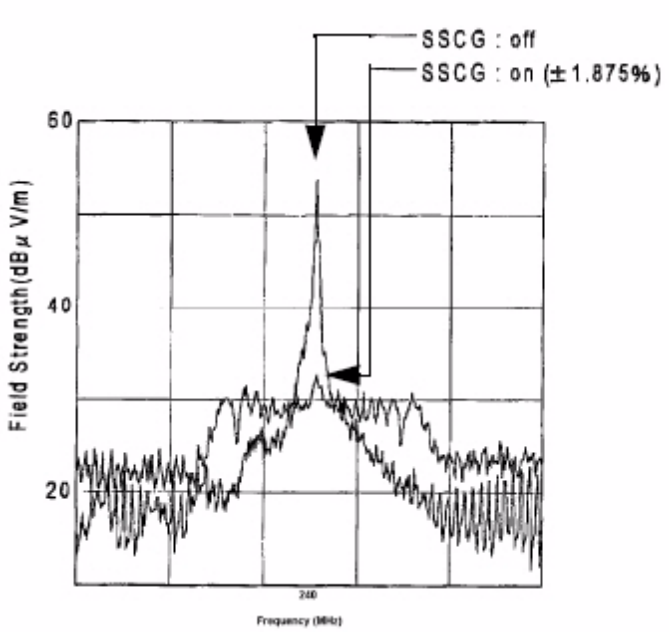
Cost Savings with EMI Suppression

Use of an EMI suppression-enabled clock IC can result in a reduction of system radiated EMI of 10 dB or more. This can result in important cost savings for the system, anywhere from less than $1, to $5–10 or more. Conventional techniques for reducing EMI include shielding ground planes, filtering components and shielding. Going from a two-layer board to a four-layer board to insert additional ground planes could easily cost $5–6. Filtering EMI typically uses ~$0.25 worth of resistors, inductors, and capacitors, and often $0.70 worth of common mode chokes and toroids. In many cases filtering will not be enough to allow a system to pass EMI tests, in which case costly shielding may be required. Shielding can easily add several dollars to the cost of a system.

Spread Spectrum Technology

The frequency of the output is slowly swept through a range of frequencies rather than being delivered at a single constant frequency. As a result, the peak energy emitted is time distributed across a wider band of frequencies, resulting in reduction in the averaged peak emissions as measured in regulatory testing (see Figure 3).

Figure 3. Measured EMI



The SST technology was developed solely for the purpose of reducing peak EMI. It eases passage of regulatory testing, and reduces total manufacturing costs. Historically, EMI problems arise after a board is designed and its functionality is proven. If prototype boards failed EMI tests, EMC engineers would step in and adjust with component values, add some combination of chokes, more shielding or better gaskets to address specific frequencies at which the board failed.

Designers who have utilized SST technology have typically found no less than 8 dB of reduction in peak EMI, and as much as 20 dB on higher order harmonics. Also, while most traditional methods of addressing EMI at the circuit level only benefit a specific harmonic, SST technology is applied to the fundamental frequency and affects every harmonic. The amount of benefit varies from design to design, and there are several factors that influence it.

Figure 4 on page 5 shows a block diagram of the concept, not an actual implementation. Although the method of implementation varies from supplier to supplier, the concept remains the same.

Basically, the frequency of the output is slowly swept through a range of frequencies rather than being delivered at a single constant frequency. Two factors (modulation width and modulation profile) significantly affect the amount of reduction in peak EMI that the system achieves through the addition of SST technology. The wider the modulation, the larger the band of frequencies over which the energy is distributed and therefore the more reduction from the peak can be seen. The effect of the modulation profile is less obvious, but in some cases it is equally important.

Three modulation profiles are explored, and two are commonly used in spread spectrum clock products. Figure 5 on page 5 shows the typical spectrum analyzer displays of the modulated output signals resulting from the three modulation profiles. Figure 5 (c) is the resultant spectrum when using a sine waveform for modulation; although easiest to implement, the extreme peaking at the edges reduces the benefit that nobody is using this profile in their products. Figure 5 (b) shows the spectrum when using a triangular (that is, linear) modulation waveform; again, you see a slight trough in the middle of the profile with peaking at the edges. Some Cypress clock products use this profile. Figure 5 (a) shows a flat profile, which is optimal, resulting from use of the modulation waveform shown in Figure 6 on page 5. Various terms have been used to describe this wave shape (optimized, Hershey's Kiss, non-linear, and so on.)

Figure 4. Simplified Block Diagram of Spread Spectrum Timing Technology

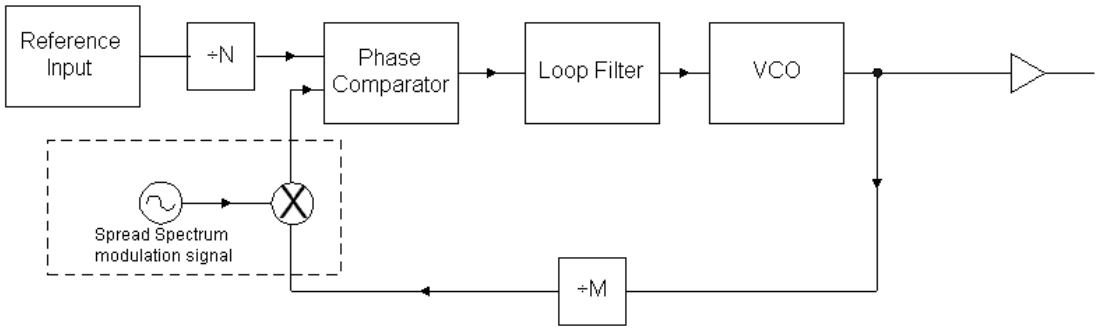
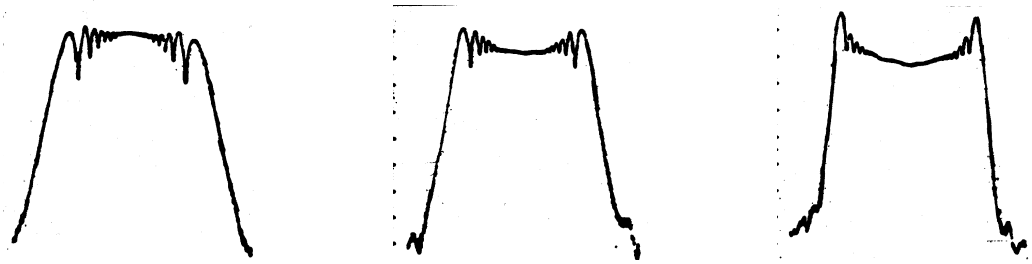


Figure 5. Frequency Spectra of Timing Signals Resulting from Different Modulation Profiles



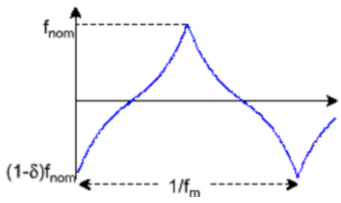
Optimized Modulation (b) Linear Modulation (C) Sinewave Modulation

Why is a flat spectral profile optimal? The band of frequencies over which the EMI energy is spread is fixed by the modulation width used, it does not vary with the modulation profile. Because EMI testing is concerned with peaks, you have to spread that energy evenly over this frequency band. A flat spectral profile with minimal peaking shows that the energy is evenly spread across the frequency band.

There are a variety of products on the market using the optimal profile. Some, like the Cypress CY25100, CY2556x series and CY2581x series, have small footprints and can easily be placed in an existing timing path to add the spread spectrum function to it. Others, like the Cypress CY24292, can use a reference crystal and provide multiple differential PCI Express clocks with spread, in addition to a non-spread reference clock. All of these devices use the optimized profile so they provide maximum peak reduction over the entire frequency band.

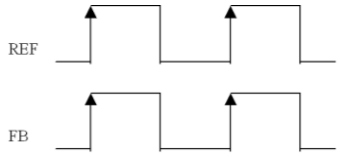
Spread spectrum timing is a very effective tool for reducing peak EMI, and may be easily integrated into many different systems without affecting other circuit elements. The one type of circuit element that may cause a timing problem when driven by a spread spectrum timing signal is a downstream PLL.

Figure 6. Optimized Modulation Profile



A downstream PLL is a device that receives a reference timing signal from another PLL-based device, including those that utilize SST technology. The term downstream may also indicate that data signals have been transmitted by a processor and the PLL must accurately recover the timing information to latch the data correctly. For this reason, tracking skew is very important in downstream PLL applications. Some examples of downstream PLLs are: a PLL cell in an application specific integrated circuit (ASIC) that receives an external reference signal, a PLL-based timing module that generates timing signals by multiplying an external reference, and a zero delay buffer used on a memory module to buffer the clock signal and provide the correct timing to Figure 7 (a) and (b).

Figure 7. (a) Ideal Tracking Skew



(b) Realistic Tracking Skew

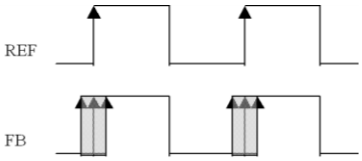


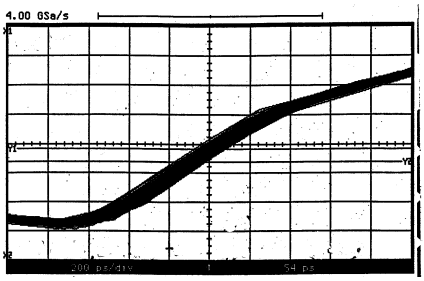
Figure 7 (a) and (b) show a comparison of an ideal and realistic downstream PLL performance when tracking an SST reference signal. In Figure 7 (a) the reference (REF) and feedback (FB) inputs to the phase detector are perfectly aligned and as the reference frequency changes the PLL loop responds instantly and the feedback signal perfectly 'tracks' the reference in phase and frequency.

In Figure 7 (b), the real-world PLL has a non-zero response time and as the reference frequency changes the feedback signal is slightly offset in phase as the loop responds. If we assume that the reference frequency slightly increases, then the feedback signal slightly lags in phase until the loop responds. That is, the change of the reference input is detected by the phase detector, filtered, applied to the VCO, divided by the feedback divider and then applied to the feedback input of the PLL. The tracking skew is shown as both leading and lagging the reference input for two reasons: (1) because we are assuming the reference frequency is modulated around a stable center frequency, and (2) because at the scale of measurement we are concerned with here, picoseconds, there is a statistical nature to at least a portion of the measurement. A typical measurement is made by triggering a very high-bandwidth digital oscilloscope on the reference signal and observing the feedback signal on a second channel. Using the infinite persistence mode of the oscilloscope, one is able to accumulate many traces of the feedback signal relative to the reference and measure the 'accumulated tracking skew.' Accumulated tracking skew is actually a combination of phase skew due to the PLL loop response and all sources of phase noise or jitter that are affecting the device, including input jitter.

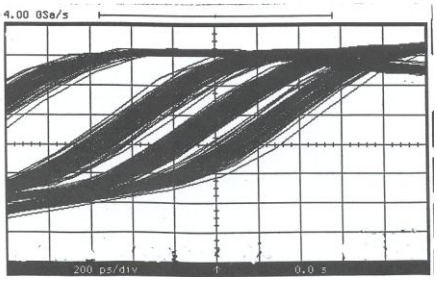
When a spread spectrum timing signal is used as the reference input for a downstream PLL it must be able to track the frequency modulation without excessive tracking skew. Cypress uses the term Spread Aware™ to describe a PLL device that can properly track a spread spectrum timing signal. Spread Aware timing devices are able to follow the frequency modulated input signal with minimal tracking skew. Therefore, the system designer is able to maintain the best possible timing margins for latching data. In addition, the downstream subsystem will be compatible with systems that utilize SST technology. Timing devices that are not spread aware either generate excessive tracking skew, thereby eroding the system timing budget, or does not lock to the spread spectrum reference signal at all, resulting in system failure.

Figure 8 (a) and (b) show test results for two zero delay buffers (ZDB) using spread spectrum timing signals as reference inputs. In both cases, the oscilloscope is triggered on the reference input signal and the buffer output signal is captured using infinite persistence mode. The traces show the accumulated tracking skew which results from the PLL's loop response to the modulated input signal and the phase jitter of the buffer. Figure 8 (a) is the output signal of a Cypress spread aware ZDB that is able to track the modulated input and has about ±80 ps of accumulated skew. Figure 8 (b) is the output signal of a competitor's buffer which is obviously not able to track the spread spectrum modulated input.

Figure 8. (a) Cypress Spread Aware Zero Delay Buffer



(b) Example of a ZDB That Cannot Track an SST Input



Effects on System Performance

Using the spread spectrum technique has minimal or no impact on other system performance considerations. It is commonly used for CPU reference clocks, and is specified for PCI Express and SATA interfaces. The slow, controlled modulation method used introduces relatively short term jitter. The spreading frequency range can be chosen to avoid clock periods shorter than system minimums.

Use of spread spectrum clocks in applications where they are placing a pixel position, such as printers or faxes may require additional application techniques to maintain the same level of apparent resolution.

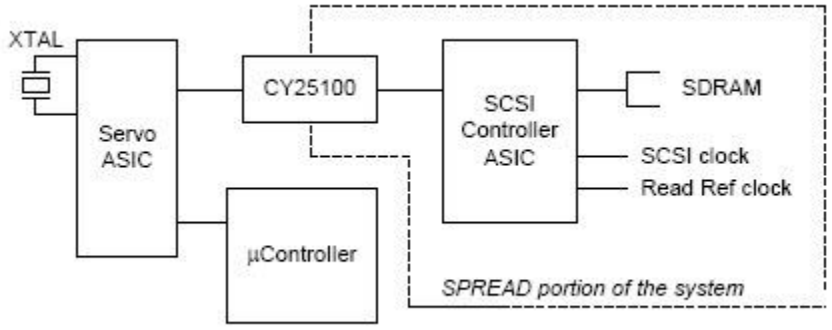
Using SST in a Hard Disk Drive

The first HDD vendor to implement Spread Spectrum Timing (SST) did so as a result of problems experienced when combining multiple hard drives in a single chassis. They developed a drive that functioned well and began large-scale manufacturing, but were unable to find a customer as a result of outstanding EMI issues. The EMI of all the drives was additive; even the prospect of redesigning the boards to add layers was considered, despite the fact that tens of thousands of drives were already built. Instead, by turning to SST, they were able to solve all their EMI problems simply by adding a single 8 pin PREMIS™ part which they managed to rework into those devices. Turning a profit from the then-EMI-compliant drives rather than scrapping them made the small added cost financially rewarding.

The benefits when applying SST to a subsection of the overall design were so dramatic that the technology is quickly migrating into additional designs and is soon becoming standard.

The system block diagram being manufactured now is described in Figure 9 on page 8.

Figure 9. System Block Diagram



By implementing SST in the SCSI/SDRAM portion of the design, this customer achieved a significant (>10 dB for many harmonics) amount of reduction in the measured speak EMI of the system. Because the microcontroller is used in part for drive control timing circuitry, it does not work well with a SST signal, but if that function is migrated to the Servo ASIC, additional reduction can be achieved by using the spread spectrum to drive the µC as well.

By designing with spread spectrum from inception, it is possible to save significant amounts of time and money.

Summary

The use of spread spectrum clocking to reduce peak EMI has become an effective way to meet emission standards while reducing components costs. Cypress spread spectrum-enabled clock products help system designers combat EMI issues using a “correct by design” solution that systematically reduces peak emissions in various applications including hard disk drives and other consumer electronics.

Cypress’s family of Spread Aware Zero Delay Buffers are specifically designed to receive a spread spectrum modulated input signal. The PLL characteristics of Spread Aware devices track the frequency modulation on the input signal with minimal accumulated tracking skew. Therefore, spread spectrum modulation present on the ZDB input signal also present on the output signals. This reduces the EMI emissions of the system. In addition, since the PLL tracking skew has been minimized, the system designer has the benefit of the greatest possible timing margins.

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