AN198537

Migration from AL-D to AL-J (8 - 16 Mb)

Two devices S29AL008D and S29AL016D manufactured with the 200 nm Floating-Gate technology are being migrated to the next generation AL-J 110 nm Floating-Gate technology.This application note explains the details of migration from AL-D to AL-J (8 - 16 Mb).

1 Introduction

The two devices S29AL008D and S29AL016D manufactured with the 200 nm Floating-Gate technology are being migrated to the next generation AL-J 110 nm Floating-Gate technology.

All hardware and software features, and most of the package options of the old devices have been maintained to ensure a seamless pin-to-pin compatible migration for the great majority of the applications.

In addition, the S29AL008J and S29AL016J devices offer improved access time (55 ns) with the regulated voltage option and faster erase/program speed.

As an additional security feature, the new devices offer an improved hardware boot sector protection via a dedicated hardware pin (WP#) and a 256 byte secure region, which can be either provided with a random serial number and factory locked or programmable and lockable by the user. The AL-J series Flash has Sector Group Protection security features that replace the individual Sector Protection feature of the AL-D.

2 Architectural/Feature Comparison

In Table 1, a feature comparison summary of the S29AL008/016D and S29AL008/016J devices is provided.

Table 1. Feature Comparison

Feature	S29AL008D / S29AL016D	S29AL008J / S29AL016J
Technology	200 nm Floating-Gate technology	110 nm Floating-Gate technology
Sector Architecture	4 Small boot sectors: One 16 KB, two 8 KB, one 32 KB. (AL008D) 15 Large sectors of 64 KB. (AL016D) 31 Large sectors of 64 KB. Small boot sectors can be located at either bottom or top of the address range.	Same sector organization for full software compatibility. Top/Bottom boot options maintained.
Access time and supply voltage range	70 ns Full V_{CC} 2.7V to 3.6V 90 ns Full V_{CC} 2.7V to 3.6V	55 ns Regulated V_{CC} 3.0V to 3.6V 70 ns Full V_{CC} 2.7V to 3.6V
Bus Architecture	X8 / X16	Same
Device ID	8 Mb: 22DAh, DAh, 225Bh, 5Bh 16 Mb: 22C4h, C4h, 2249h, 49h	Same
Program operation	Single Byte/Word programming	Same
Sector Protection/Unprotection	V_{ID} on RESET# pin V_{ID} on A9 /OE# pins	Sector Group Protection/Unprotection scheme with V_{ID} on RESET# pin
Temporary Sector Unprotection	V_{ID} on RESET# pin	Temporary Sector Group Unprotection scheme with V_{ID} on RESET# pin.
256 bytes Secure Silicon Sector region	Not available	Available
Data Polling	Software detection of write/erase embedded algorithms completion.	Same
Ready/Busy# pin	Hardware detection of write/erase embedded algorithms completion.	Same

Table 1. Feature Comparison

Feature	S29AL008D / S29AL016D	S29AL008J / S29AL016J
Erase suspend/resume	Command to suspend erase to program/ read	Same
Command interface	Set of commands to perform various device operations.	100% backward compatible plus superset commands to Enter and Exit the Secure Silicon Sector.
WP# pin	Not available	WP# pin to protect the lowest (bottom boot) highest (top boot) 16 KB sector. The pin has an internal pull-up, so it can be left unconnected in existing designs.
Package Summary	TS048, VBK048, SO044, KGD	TS048, VBK048, KGD (all with WP#). New LAE064 (16 Mb only) and SSOP56 packages. SO044 package not available.

Minor differences in the DC characteristics are summarized in Table 2. The absolute maximum parameter ratings are unchanged from AL-D to AL-J.

Table 2. DC Characteristics Comparison

Parameter	Description	AL-D	AL-J	Comments
I_{LI}	WP# Input Load Current (max)		± 25 µA	
I_{CC1}	Active Read Current @ 5 MHz	Typ: 9 mA Max: 16 mA	Typ: 7 mA Max: 12 mA	AL-J products have slightly lower power consumption in read mode.
I_{CC2}	V_{CC} Active Erase/Program. Current	Typ: 20 mA Max: 35 mA	Typ: 20 mA Max: 30 mA	AL-J products have slightly lower power consumption in write mode.
V_{IL}	Input Low Voltage	Min: -0.5V Max: 0.8V	Min: -0.1V Max: 0.8V	AL-J products have increased minimum V_{IL} to preserve I_{CC3}, I_{CC4}, and I_{CC5} current specifications.
V_{OH1} (min)	Output High voltage @ I_{OH} -2 mA, V_{CC} = V_{CC} min	2.4V	0.85 * V_{CC}	In case of V_{CC} (min) = 2.7V, AL-J has a V_{OH1} (min) = 2.3V, which is comparable with the AL-D products.
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect.	Typ: 11.5V Max: 12.5V	Typ: 8.5V Max: 12.5V	AL-J products can activate autoselect and temporary sector unprotection with a lower V_{ID} voltage level.
V_{LKO}	Low V_{CC} Lock-out voltage	Min: 2.3V Max: 2.5V	Min: 2.1V Max: 2.5V	AL-J products operate at slightly lower V_{CC} before disabling erase/program operations.

Table 3. AC Characteristics Comparison

Parameter	Description	AL-D	AL-J	Comments
t_{READY}	RESET# Pin Low (During Embedded Algorithms) to Read or Write (max)	20 µs	35 µs	Allow for a longer reset time pulse to the AL-J devices to insure proper embedded algorithm read/write operation.
t_{RPD}	RESET# low to standby mode (min)	20 µs	35 µs	Allow for a slightly longer reset time to drive the AL-J device into standby mode during a hardware reset operation.
t_{WPH}	Write Pulse Width High (min)	30 ns	25 ns	AL-J allows faster toggling of the write cycles. This parameter is relevant during subsequent write cycles.
t_{RRB}	RESET# Hold Time from RY/BY# High for Temporary Sector Unprotect (min)		4 µs	New AL-J parameter
t_{CPH}	CE# Pulse Width High (min)	30 ns	25 ns	AL-J allows faster toggling of the write cycles/CE# controlled. This parameter is relevant during subsequent write cycles.
	Erase Suspend during sector erase operation (max)	20 µs	35 µs	AL-J is slower to suspend when the Erase Suspend command is written during a sector erase operation.

3 Design Considerations

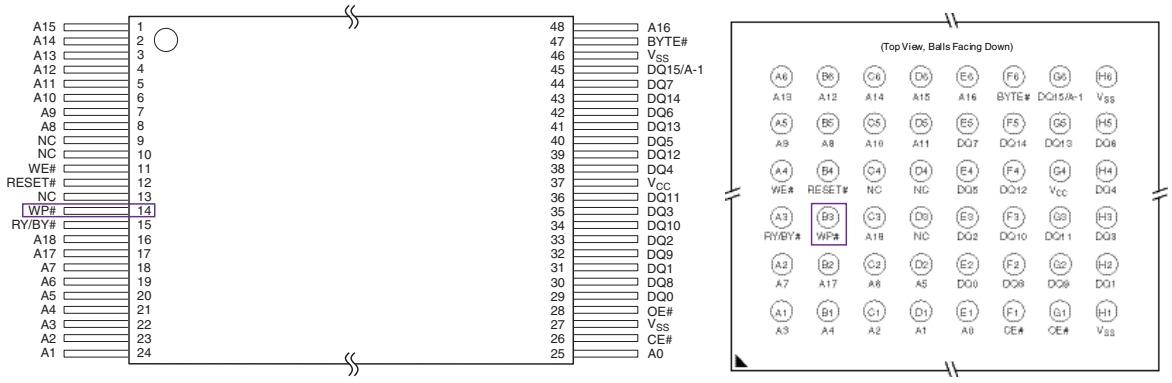
3.1 WP#, Write Protect

The AL-J adds the Write Protect input pin (WP#) in place of a No Connect on the AL-D as shown in Figure 1. This feature offers a hardware method to protect the boot block of the application. When WP# = V_{IL}, program and erase functions are disabled in the lowest (bottom boot) or highest (top boot) 16 KB sector.

The WP# pin has an internal pull-up, so it can be left unconnected in existing designs.

The S29AL016J TS048 and VBK048 packages are footprint backward compatible with S29AL016D designs if pin 14 of the TS048 48-pin TSOP or ball B3 of the VBK048 48-ball Fine-pitch BGA is treated as No Connect.

Figure 1. AL-J WP# Location In the TS048 and VBK048 Package Pinouts



3.2 DC Performance Characteristics

The DC characteristics are either mostly unchanged or improved. That means that the new AL-J device family has improved power consumption compared to the equivalent AL-D under certain operation conditions.

One major difference is that the minimum Input Low Voltage (V_{IL}) has changed to -0.5V to -0.1V. This change was necessary in the AL-J family to preserve the I_{CC3}, I_{CC4}, and I_{CC5} current specifications. If a customer were to use a minimum Input Low Voltage less than -0.1V but greater than -0.5V, the excess current consumption would negatively impact battery life but would not damage the circuit or cause logic 0 input judgment errors. It is recommended that customers follow the new AL-J minimum Input Low Voltage value of -0.1V to prevent the excess current consumption.

3.3 AC Performance Characteristics

The AC characteristics are mostly either unchanged or improved. That means that the new AL-J device family has improved speed compared to the equivalent AL-D except for a few parameters.

The AL-J requires 35s to Reset during an embedded algorithm (t_{READY}) or during suspend (t_{RPD}) compared to the 20s required by AL-D devices.

One of the major differences is the test condition for the slowest speed grade. AL-D had the 90 ns speed class able to match a maximum bus load of 100 pF.

The AL-J AC test conditions are now referring to a typical load of 30 pF for both the 55 ns and 70 ns speed grades. Consider that the driving strength of the AL-J device's output buffers can be slightly different compared to the AL-D ones. It is recommended to perform qualification experiments to validate AL-J on existing AL-D sockets. Boards with heavy bus loads (>30 pF) will require careful evaluation of the new AL-J devices. IBIS models are also available on the Cypress website to evaluate the new device on existing PCB designs.

3.4 Hardware Sector Protection

3.4.1 Sector Protection vs. Sector Group Protection

The AL-J supports hardware Sector Group Protection unlike the AL-D which supports independent hardware Sector Protection control of any sector or combination of sectors. AL-J Sector Group Protection permits independent sector protection control over boot sectors and the one adjacent 64 Kbyte sector while grouping the remaining 64 Kbyte sectors.

AL-J Sector Group Protection addressing requires the Sector group address with A6=0, A3=A2=0, A1=1, and A0=0 while AL-D Sector Protection addressing required the Sector address with A6=0, A1=1, and A0=0. Both the AL-J and AL-D use RESET# hardware circuitry to control the nominal 12V (V_{ID}) voltage that is required for the Sector Group Protection and Unprotection or Sector Protection and Unprotection operations respectively. For RESET# Pin circuitry implementation suggestions, see the “Reset Pin Circuitry for Flash Memory Sector Protection Management” Application Note.

3.4.2 Sector Group Unprotection

Sector unprotection is a reversed operation, which also needs a 12V V_{ID} on RESET# pin before the flow.

AL-J Sector Group Unprotection addressing requires the Sector group address with A6=1, A3=A2=0, A1=1, and A0=0 while AL-D Sector Unprotection addressing required the Sector address with A6=1, A1=1, and A0=0.

3.4.3 Temporary Sector Group Unprotect

The AL-J hardware Temporary Sector Group Unprotect feature is consistent with AL-D Temporary Sector Unprotect unless the WP# = V_{IL}, then the first or last 16 Kbyte AL-J sector remains protected.

This feature allows temporary unprotection of previously protected sector groups to change the data in system. The Sector Group Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sectors are protected again.

3.5 Secured Silicon Sector

The AL-J supports the Secured Silicon Sector feature unlike the AL-D.

The AL-J adds the Secured Silicon Sector feature providing a 256-byte OTP (One Time Programmable) Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). Cypress offers the device with the Secured Silicon Sector either factory-locked or customer-lockable. For details, see the data sheet.

RESET# = V_{ID} is required to program or verify the Customer Lockable version of the AL-J.

3.5.1 Autoselect Mode

The AL-J adds Address 03h to Autoselect Mode, and the DQ7 Indicator Bit (DQ7) of Address 03h indicates if the Secured Silicon Sector has been factory locked or not factory locked.

3.6 Command Set

The AL-J Command Sequences are backward software compatible with the AL-D. The AL-J adds two Command Sequences, Enter Secured Silicon Sector and Exit Secured Silicon Sector, to read the Secured Silicon Sector or program the Customer Lockable Version of the device once.

3.7 Common Flash Interface (CFI) Differences

S29AL008J includes a CFI option unlike S29AL008D which had no CFI support.

S29AL016J has minimal CFI changes versus S29AL016D. S29AL016J CFI locations 44h, Minor version number, and 45h, Process Technology Bits 5-2, in Word Mode can be used by software to distinguish between the AL-J and AL-D versions.

S29AL016J CFI locations 1Fh and 21h (Word Mode) contain shorter program and erase time-outs than the AL-D.

AL-J CFI location 49h indicates the device has Group Sector Protection with RESET# = V_{ID} unlike the AL-D which has Sector Protection with RESET# = V_{ID}.

AL-J CFI locations 4Dh to 50h (Word Mode) expose new device capabilities in the Primary Vendor-Specific Extended Query.

3.8 Erase and Programming Performance

The AL-J devices erase and programming performance has been improved compared to the AL-D devices.

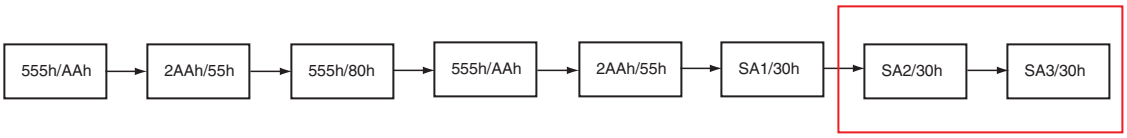
Table 4. Erase and Programming Timing

Parameter	AL-D	AL-J	Comments
Sector Erase time (typ)	0.7s	0.5s	
Sector Erase time (max)	10s	10s	A similar sector erase worst-case time out can be used with AL-D and AL-J.
Chip Erase time (typ)	25s	16s	
Byte programming time (typ)	7 µs	6 µs	
Word programming time (typ)	7 µs	6 µs	
Word programming time (max)	210 µs	150 µs	

3.9 Multiple Sector Erase

In AL-D or AL-J devices, multiple sectors can be erased together by entering additional sector erase commands before the Sector Erase Timer expires (50 µs from the last Sector Erase Command). However, there is a slight difference on the command sequence requirement between the AL-D and AL-J devices.

As indicated in the AL-J data sheet, the correct command sequence for doing multi-sector erase is shown in Address/Data format:



In this example, two additional sectors, SA2 and SA3 will be erased along with SA1.

When migrating from software that does multi-sector erase on AL-D devices, the software may have two unlock cycles before the red box in the above sequence. Any additional command cycle may cause the multi-sector erase malfunction in AL-J devices.

If no multi-sector erase function is used in AL-D software, no changes are required.

Note that multi-sector erase does not significantly improve the system performance because the actual erase time will be the sum of each individual sector erase time. The time saved by omitting a few command sequences are insignificant compared to the sector erase time.

3.10 First Read after Power Reset

For AL-J devices, during the power up sequence, CE# should only go LOW after RESET# has gone HIGH. Keeping CE# LOW from power up through the first read could cause the first read to retrieve erroneous data. This behavior does not exist in AL-D devices.

4 Package Comparison

Table 5 provides a matrix of the supported S29AL008/0016D and S29AL008/016J package options.

The AL-J devices continue to support the TS048 (48-pin Standard TSOP) and the VBK048 (48-ball Fine-pitch BGA) packages like the AL-D. However, the AL-J devices do not support the SO044, 44-Pin SOP (Small Outline

Package) 28.20 mm x 13.30 mm, unlike the AL-D. Instead, AL-J supports the smaller and higher pin count SSOP56 (56-pin Shrink Small Outline Package).

The S29AL016J also supports the LAE064, 64-Ball Fortified Ball Grid Array (BGA) 9 mm x 9 mm. The LAE064 package ball-out is a compatible subset of the Cypress Universal Footprint used by the GL MirrorBit family.

Table 5. AL-D and AL-J Package Options

Package Offered (Size)	S29AL008D	S29AL016D	S29AL008J	S29AL016J
TS048 (20 x 12 mm)	Supported	Supported	Supported	Supported
VBK048 (8.15 x 6.15 mm)	Supported	Supported	Supported	Supported
SO44 (16 x 28.20 mm)	Supported	Supported	Not Available	Not Available
SSOP56 (16 x 23.70 mm)	Not Available	Not Available	Supported	Supported
LAE064 (9 x 9 mm)	Not Available	Not Available	Not Available	Supported
KGD (Known-Good Die)	Supported	Supported	Supported	Supported

5 ROHS

AL-J Standard Products are only offered in RoHS compliant Pb-Free package material sets unlike the AL-D.

6 References

- S29AL008J Data Sheet (S29AL008J_00)
- S29AL016J Data Sheet (S29AL016J_00)
- S29AL008D Data Sheet (S29AL008D_00)
- S29AL016D Data Sheet (S29AL016D_00)
- “Reset Pin Circuitry for Flash Memory Sector Protection Management” Application Note

Document History Page

Section	Description
Revision 01 (November 18, 2008)	
	Initial release
Revision 02 (April 3, 2009)	
Global	Minor updates
Revision 03 (October 28, 2009)	
Architectural/Feature Comparison	DC Characteristics Comparison table: added comment for V_{IL}
Design Considerations	Added new section: DC Performance Characteristics
Revision 04 (October 19, 2010)	
Architectural/Feature Comparison	Removed invalid signals t_{ASO}, t_{OEPH}, t_{CEH}
Design Considerations	Added new sections: Multiple Sector Erase and First Read after Power Reset

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Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	–	–	18/11/2008	Initial release
*A	–	–	04/03/2009	Minor updates
*B	–	–	10/28/2009	Architectural/Feature Comparison > DC Characteristics Comparison table: added comment for V_{IL} Design Considerations > Added new section: DC Performance Characteristics
*C	–	–	10/19/2010	Architectural/Feature Comparison > Removed invalid signals t_{ASO}, t_{OEPH}, t_{CEH} Design Considerations > Added new sections: Multiple Sector Erase and First Read after Power Reset
*D	6060421	PRIT	02/06/2018	Migrated to Cypress Template Minor edits

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