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About This Document

This document discusses the hardware design guidelines for the CYW20719 kit.

Purpose and Audience

This document provides hardware guidance on how to design with CYW20719. This document is intended for hardware engineers creating schematic and layout designs with CYW20719.

Scope

This document covers some basic layout guidelines, component placement, and suggestions for power trace width.

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use. For a comprehensive list of acronyms and other terms used in Cypress documents, go to www.cypress.com/glossary.

IoT Resources and Technical Support

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).
1 Basic Layout Guidelines

Most Bluetooth devices use four-layer boards to minimize thickness. Components are placed on the top layer and the bottom layer is a solid ground fill. Most signal traces are routed on the top layer.

For RF traces, use a 50-ohm transmission to minimize mismatch losses and reflections, and therefore maximize the power transferred to the load.

There are two types of transmission lines: microstrip and stripline. The reference design uses the microstrip design.

Transmission lines require the proper geometry. Some parameters are highly dependent on the dielectric material – trace width, vertical distance to ground plane, and a solid ground plane of sufficient width. Different height and width solutions perform differently.

For the microstrip layer and its reference ground layer selections, two things should be considered:

1. Thinner traces have higher insertion loss—PCB fabrication requires adequate trace width for reliability and repeatability. The heights between the microstrip and ground should be thick enough to guarantee adequate trace width for the microstrip.

2. For the microstrip lines, avoid sharp corners; use a smooth radius to change directions. The coplanar ground follows the contour of these traces with a clearance distance of two to three line widths (2 W to 3 W). Surrounding the microstrip trace, connect the outer layer to the reference ground plane using vias.

The microstrip is used in this reference design is on Layer 1. The reference ground is Layer 2.

This reference design uses the four-layer technique as shown in Figure 1-1:

- Layer 1 is the main signal layer
- Layer 2 is a solid ground
- Layer 3 is the power signal layer
- Layer 4 is a solid ground layer

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Figure 1-1. Stack-up
2 Component Placement

As a rule, follow the receive signal flow from the antenna to the matching and filter circuits, then to the chip (LNA) input. Keep RF, PMU, and BB decoupling capacitors next to the chip pin pads.

2.1 Antenna Placement

Keep the antenna connection to the chip should as short as possible. Maintain a solid ground near the antenna and adequate ground clearance for the layers beneath antenna.

In the reference design, the antenna is on the top layer on the left side of the board next the Bluetooth chip.

![Antenna Placement and Microstrip Clearance](image)

*Figure 2-1. Antenna Placement and Microstrip Clearance*
2.2 PCB Antenna

For more details on antenna, see AN91445 - Antenna Design and RF Layout Guidelines. For the associated Gerber file, visit: http://www.cypress.com/go/AN91445.

2.3 Crystal Placement

Protect the crystal and related traces from noise sources, and use a solid ground used to separate the crystal from RF traces. The crystal ground plane should have direct vias to the reference ground plane.

You can find the crystal specification requirements in the CYW20719 datasheet. See the reference design BOM for the recommended vendor part numbers.

2.4 Decoupling Capacitors

See the reference schematic for the decoupling capacitor usage and values on the different power domains. It is recommended to use the vendor and part numbers shown in the reference design BOM.

2.5 Ground Vias

Do not use long thin traces to connect components to ground vias; doing so adds inductance that can significantly alter circuit performance. Use ground fill under the BGA to inter-connect all the ground pins.

2.6 Bandpass Filter

Place a chip bandpass filter between the antenna matching components and the CYW20719 chip to attenuate harmonics from CYW20719.

A microstrip is used for all the connections of the bandpass filter.

Insertion loss and out-of-band attenuation performance depend on PCB component layouts and tolerances. Filter layout should follow all the general RF layout rules.
Figure 2-2. Bandpass Filter and Decoupling Capacitors
2.7 Layer 2, Solid Ground Fill

Fill the layer immediately below the layer where CYW20719 is located (Layer 2), with solid ground for optimal ground return path.

![Layer 2, Solid Ground Fill](image)

Figure 2-3. Layer 2, Solid Ground Fill

2.8 Power Traces

Use wide traces for power supply lines. Know the maximum current to be carried on each trace and make the trace width proportionate to the current.

Route the main DC power supply line up the middle of the board like a spine, branching off left and right as needed.

Avoid routing DC power in a loop.

Protect the RF power supply from main power, noisy signals, and digital power by separating with ground fill.

- Make sure adequate power trace width and vias are available to minimize parasitic impedance:
  - CBUCK_OUT → Minimum 12 mils trace width
  - CBUCK_OUT to DIGLDO_VDDIN (pin 16) → Minimum 8 mils trace width
  - VDDIO → Minimum 12 mils trace width
  - VDDIO to LHL_VDDO (pin 39)/BT_VDDO (pin 25) → Minimum 8 mils trace width
  - BT_VDDC → Minimum 10 mils trace width
  - BT_VDDC to BT_VDDC (pin 26) → Minimum 8 mils trace width
  - VDDIO to SR_VDDBAT3V (pin 13) → Minimum 8 mils trace width
  - CBUCK_OUT to SR_VLX (pin 12)/RFLDOIN (pin 15) → Minimum 8 mils trace width
- RFLDO_OUT to RFLDO_VDDOUT (pin 14) → Minimum 8 mils trace width
- PA_2P5V → Minimum 12 mils trace width
- PA_2P5V to PAVDD2P5 (pin 17) → Minimum 8 mils trace width
- 1P2VRF → Minimum 12 mils trace width
- 1P2VRF to IFVDD1P2 (pin 19)/PLLVD1P2 (pin 21) / VCOVDD1P2 (pin 20) → Minimum 8 mils trace width

*Figure 2-4. Power Supply Traces*
2.9 Power Inductor

Place the power inductor further away from the RF area, but close to the CBUCK power pins. Remove the GND plane immediately underneath the power inductor. See the Recommended Component section in the CYW20719 datasheet and reference design files for the recommended component.

Figure 2-5. Power Inductor Routing
2.10 Layer 4

Layer 4 shows all non-critical signal routing. All non-critical signals can be routed on Layer 4.

*Figure 2-6. Layer 4*
## Document Revision History

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**Document Number:** 002-22478

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<td>**</td>
<td>6005625</td>
<td>01/09/2018</td>
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