AN61546

Nonvolatile Static Random Access Memory (nvSRAM) Real Time Clock (RTC) Design Guidelines and Best Practices

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Associated Part Family: CY14xxxxx (nvSRAM RTC)

Related Application Notes: AN53313

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AN61546 describes the RTC functionality, component selection criteria, and best layout design practices for the nvSRAM RTC design. The guidelines and best practices covered in this application note are intended to assist you in designing nvSRAM with RTC functions in your system design and to minimize timing errors, which mostly occur due to improper layout design and component selection.

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1 Introduction

The nvSRAM RTC integrates standard real time clock functions and nonvolatile SRAM functions. Applications such as servers, security and surveillance systems, industrial controllers, data loggers, and single-board computers are just a few system examples that require RTC functions to operate the system reliably and accurately. The integrated RTC functions along with the nvSRAM provide multiple advantages such as enabling infinite write into SRAM of nvSRAM, automatic data saving during power down, and allowing the systems to log critical information continuously into nonvolatile memory with time stamping.

The RTC block uses a 32.768-kHz crystal to produce a reference clock for timekeeping functions. It maintains system timing information regardless of whether it is in active mode or power-down mode. To keep the RTC block active during power-down mode requires a backup power source that keeps the clock oscillator running even though the VCC supply is switched OFF.

The accuracy of the RTC clock mainly depends upon the accuracy of the components used, layout design, component placement, and operating temperature. The clock accuracy can be improved further by enabling the on-chip clock calibration option. The RTC Clock Calibration section of this application note provides a brief description of RTC clock calibration.

This application note discusses the crystal operation, nvSRAM RTC component selection criteria, and layout design guidelines.

2 Crystal Basics

Crystals are made of quartz material, which contains silicon dioxide and exhibits piezoelectric properties. Quartz generates an electrical potential when pressure is applied on the surfaces of the quartz crystal. Inversely, when an electrical potential is applied to the surfaces of a quartz crystal, mechanical deformation or vibration is generated. These vibrations occur at a frequency determined by the following:

- Physical dimension of the piece of quartz crystal
- Cut of the crystal in relation to the crystalline axes of the quartz
- Operating temperature
- Oscillator circuit

The natural oscillation frequency is stable. Additionally, the resonance has a high quality factor (Q) ranging from tens of thousands to several hundred thousand.

Crystals have several fundamental characteristics that are important to the design of an oscillator circuit. A typical crystal symbol is shown in Figure 1 and its equivalent circuit is shown in Figure 2. The circuit consists of series components that include motional inductance L_1, motional resistance R_1, and motional capacitance C_1. The parallel component C_0 is the shunt capacitance of the crystal.

The equivalent series resistance (ESR), also known as motional resistance, is the impedance of the crystal when the reactive components of the crystal cancel at the resonant frequency. ESR and Q are inversely proportional. The lower the ESR, the less energy that is lost in the crystal. A crystal with a high ESR requires more power to operate and takes longer to start.

Figure 1. Crystal Symbol

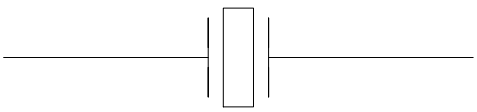
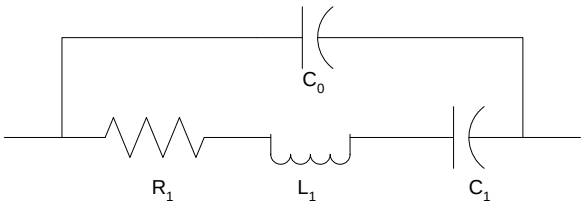


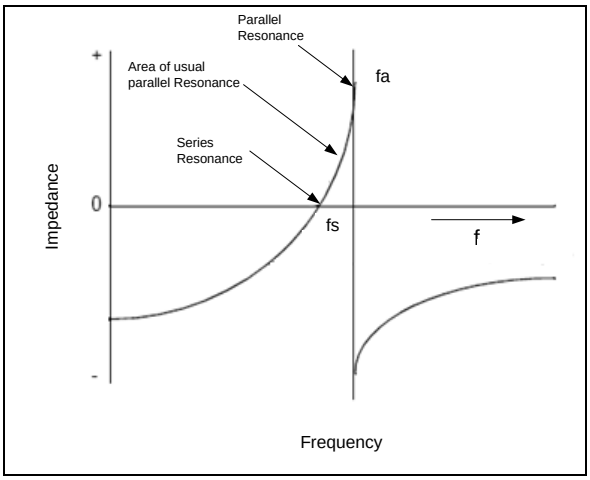
Figure 2. Crystal Equivalent Circuit



3 Crystal Resonant Frequencies

Figure 3 shows the reactance frequency plot of the crystal. A crystal has two resonant frequencies: series resonance and parallel resonance.

Figure 3. Crystal Resonant Frequencies



When a crystal is operating at series resonance, it looks purely resistive, and the inductive reactance of L_1 equals the capacitive reactance of C_1. Since these impedances are 180° out of phase, they cancel out each other, leaving R_1 as the impedance between the crystal terminals.

The series resonance frequency (fs) is determined by Equation 1.

Equation 1 $$fs = \frac{1}{2\pi\sqrt{L_1 C_1}}$$

When the series resonance occurs, the effect of reactive impedance is minimal, and the circuit behaves as a resistive circuit with minimum equivalent impedance, thus drawing maximum current.

When the crystal is operating in parallel resonant mode, the inductor L_1 reacts with the total capacitance between its terminals. This is also known as the antiresonant frequency and is defined by Equation 2.

Equation 2 $$fa = \frac{1}{2\pi\sqrt{L_1 \frac{C_1 (C_0 + C_L)}{C_1 + (C_0 + C_L)}}}$$

This equation combines the parallel capacitance of C_0 and C_L, where C_L is the load capacitance specified by the crystal manufacturer as shown in Figure 5.

When a crystal is operating at its antiresonant frequency, the impedance is at its maximum, and current flow is at its minimum. Crystals are mostly designed to resonate between fs < f < fa, and this range of frequencies between fs and fa is called the “area of usual parallel resonance” or “parallel resonance.”

3.1 Equivalent Series Resistance

The ESR is the resistance exhibited by the crystal at series resonant frequency (fs). This is not necessarily the R_1 value shown in Figure 2. The ESR of the oscillator circuit can be calculated using Equation 3.

Equation 3 $$ESR, R_S = R_1\left(1+\frac{C_0}{C_L}\right)^2$$

This value is typically monitored when tuning the quartz crystal to the specified resonant frequency. R_S is sometimes specified as a maximum resistance and should be used when determining the drive level of the oscillator (see Where,

ωL_1 = Reactance due to inductor (L1)

$1/\omega C_1$ = Reactance due to capacitor (C1) at the operating frequency of the crystal

Drive Level).

3.2 Crystal Quality Factor

Due to the piezoelectric effect of the crystal, a physical displacement occurs when an electric field is applied. The reverse effect happens when the crystal is deformed and electrical energy is produced across the crystal electrodes. A mechanically resonating crystal is seen from its electrodes as an electrically resonating circuit. Therefore, the crystal behaves like a tuned circuit and can store energy. You can quantify the amount of stored energy by stating the quality factor (Q) of the crystal. Crystal Q is defined as shown in Equation 4.

Equation 4 $$Q = \frac{\omega L_1}{R_1} = \frac{1}{\omega C_1 R_1}$$

Where,

ωL_1 = Reactance due to inductor (L_1)

$1/\omega C_1$ = Reactance due to capacitor (C_1) at the operating frequency of the crystal

3.3 Drive Level

Drive level refers to the power dissipated in the crystal. The crystal specification document defines the maximum drive level that the crystal can sustain. Overdriving the crystal can cause excessive aging, frequency shift, quartz fracture, and eventual failure. The designer should ensure that the maximum rated drive level of the crystal is not exceeded. Again, the drive should be maintained at the minimum level that is necessary for the oscillator to start up and maintain steady state operation.

You can compute power dissipation of the crystal by using Equation 5.

Equation 5 $$P=2R\_1\ [\ \pi\ f\ (C\_0\ +\ C\_L\ )\ V\_RMS]^2$$

Where,

VRMS = Root mean square (RMS) value of the voltage across the crystal

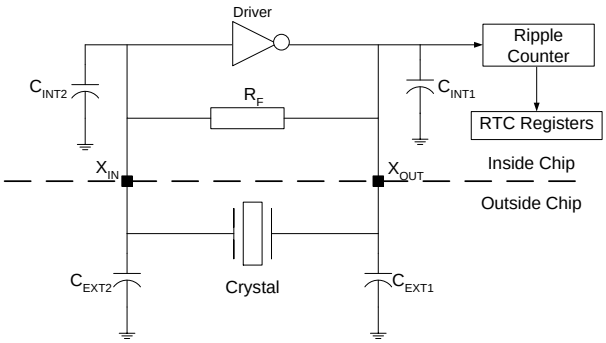
f = Nominal frequency of oscillation for the crystal

Most of the RTC crystals specify a maximum power dissipation of 1 µW.

4 nvSRAM RTC Clock Oscillator Circuit

The oscillator used in the nvSRAM RTC is a CMOS inverter-based Pierce-type oscillator as shown in Figure 4. The inverter acts as a class AB amplifier and provides approximately 180° phase shift from the input to the output, whereas the pi (π) network formed by crystal, C_{INT1}, and C_{INT2} provides an additional 180° phase shift from the output to the input. Therefore, the total phase shift around the loop is 360°. This satisfies one of the conditions required for sustained oscillation. The other condition for sustained oscillation is the closed loop gain, which must be greater than one. The resistor R_F around the inverter provides negative feedback and sets the bias point of the inverter near mid-supply voltage, thus operating the inverter in the high gain linear region. The value of the R_F resistor is high and is measured generally in the range of a few megaohms.

Figure 4. Pierce-Type Oscillator

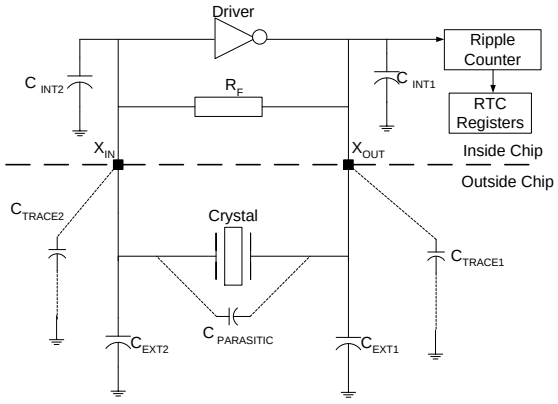


The Pierce-type oscillator uses a crystal that operates in parallel mode. The nominal frequency of oscillation for the crystal is defined under the specific load condition. To oscillate the crystal at its specified frequency, you should design the application board in such a way that the load capacitance across the crystal pads (X_{IN} and X_{OUT}) on the PCB is equal to the specified load for the crystal.

4.1 Load Capacitance

The load capacitance (C_L) is the capacitive load of the oscillating circuit as seen from the pins of the crystal. Figure 5 depicts C_L as a capacitance measured across the X_{IN} and X_{OUT} pins without crystal. C_{INT1}, C_{INT2}, and any stray capacitance in the circuit are combined to create overall load capacitance.

Figure 5. Oscillator Load Capacitance



An equivalent load capacitance C_{EQ2} on X_{IN} pin can be defined as shown in Equation 6.

Equation 5 $$C_{EQ2} = C_{INT2} + C_{TRACE2} + C_{EXT2}$$

Similarly, an equivalent load capacitance C_{EQ1}on X_{OUT} pin can be defined as shown in Equation 7.

Equation 7 $$C_{EQ1} = C_{INT1} + C_{TRACE1} + C_{EXT1}$$

The resultant load capacitance (C_L) is calculated as shown in Equation 8.

Equation 8 $$C_L = \frac{C_{EQ1}C_{EQ2}}{C_{EQ1}+C_{EQ2}} + C_{PARASITIC}$$

Where,

C_{INT1} = Input capacitance on the X_{OUT} pin

C_{INT2} = Input capacitance on the X_{IN} pin

C_{TRACE1} = Capacitance of the trace connecting pin X_{OUT}, crystal, and capacitor C_{EXT2}

C_{TRACE2} = Capacitance of the trace connecting pin X_{IN}, crystal, and capacitor C_{EXT1}

C_{EXT1} = External capacitor connected on X_{OUT} pin

C_{EXT2} = External capacitor connected on X_{IN} pin

$C_{PARASITIC}$ = Parasitic capacitance due to the crystal mount on the board

C_L = Total capacitive load of the circuit that must be applied across the crystal pins to oscillate at its nominal frequency

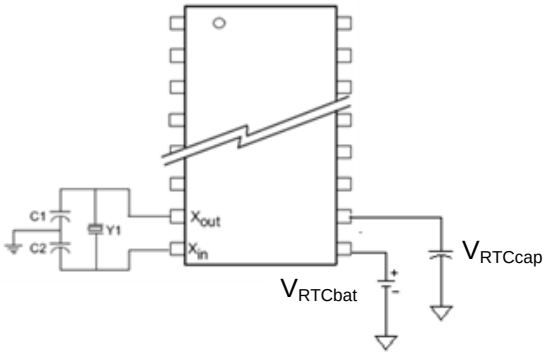
Any change in the load capacitance of the crystal circuit has an effect on the frequency of oscillation. The drift in frequency of the operation from nominal operation frequency can be characterized as follows.

- If the specified load capacitance of the crystal is larger than the load capacitance of the crystal circuit (C_L) on the PCB across the crystal pads, then this configuration causes the oscillator to run faster than specified nominal frequency.
- Reciprocally, using a crystal with a specified capacitive load smaller than the C_L causes the oscillator to run slower than the nominal frequency.
- If the specified capacitive load of a crystal equals the load capacitance of the C_L, then the crystal oscillates at its nominal frequency.

5 nvSRAM RTC Circuit Design

The nvSRAM RTC requires connecting an external 32.768-kHz crystal and C1, C2 load capacitance to build a RTC circuit as shown in Figure 6.

Figure 6. nvSRAM RTC Design



The load capacitances C1 and C2 are inclusive of the PCB parasitic components, including the capacitance due to the land pattern of crystal pads/pins, X_{IN}/X_{OUT} pads, and copper traces connecting crystal and device pins. Equation 9

$$CEXT1 = C1 - CPARASITIC1$$

Equation 10 $$CEXT2 = C2 - CPARASITIC2$$

Where,

CPARASITIC1 = Parasitic capacitance due to the land pattern of crystal pads/pins, the trace connecting the crystal pads and device pads XOUT, and the land pattern of XOUT

CPARASITIC2 = Parasitic capacitance due to the land pattern of crystal pads/pins, the trace connecting the crystal pads and device pads XIN, and the land pattern of XIN

Figure 7 illustrates the PCB parasitic components.

Effective capacitance that should be mounted additionally onto the board is calculated by using the following equations. These external load capacitors are defined as C_{EXT1} and C_{EXT2} in Figure 5.

Equation 9 $$C_{EXT1} = C1 - C_{PARASITIC}1$$

Equation 10 $$C_{EXT2} = C2 - C_{PARASITIC}2$$

Where,

$C_{PARASITIC}1$ = Parasitic capacitance due to the land pattern of crystal pads/pins, the trace connecting the crystal pads and device pads X_{OUT}, and the land pattern of X_{OUT}

$C_{PARASITIC}2$ = Parasitic capacitance due to the land pattern of crystal pads/pins, the trace connecting the crystal pads and device pads X_{IN}, and the land pattern of X_{IN}

Figure 7. PCB Parasitic Components

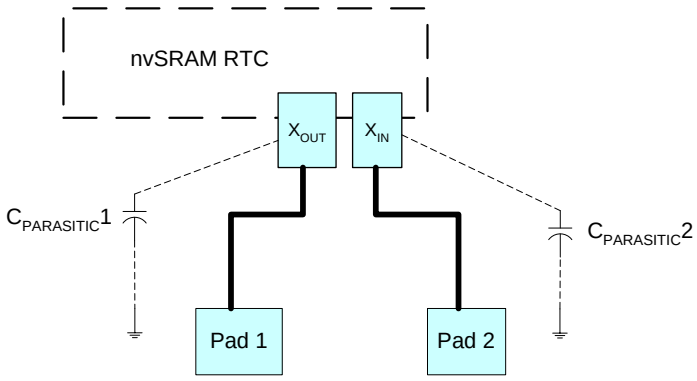


Table 1 provides the recommended component values for the nvSRAM RTC design.

Table 1. nvSRAM RTC Circuit Components

CY Part Number	C_1 (ext) (Typ)	C_2 (ext) (Typ)	Crystal Freq, C_L (Typ)	Production Status
CY14B101P CY14B512P CY14B256P	10 pF ±5%	68 pF ±5%	32.768 kHz, 12.5 pF	Not Recommended for New Designs
CY14B101KA/MA	10 pF ±5%	68 pF ±5%	32.768 kHz, 12.5 pF	In Production
CY14B064I/PA CY14B256I/PA CY14B512I/PA CY14B101I/PA CY14B104K/M CY14B108K/M CY14B116K/M	12 pF ±5%	68 pF ±5%	32.768 kHz, 12.5 pF	In Production

Table 2 provides a typical RTC crystal specification for the nvSRAM RTC.

Table 2. Crystal Specifications

Parameter	Symbol	Value (Typ)	Units
Frequency	f	32.768	kHz
Equivalent Series Resistance (ESR)	R_S	50	kΩ
Frequency Stability	K	-0.035	PPM/(Δ °C)²
Drive Level		1	µW
Aging (first year at 25 °C)		±3	PPM
Load Capacitance	C_L	12.5	pF
Q Factor	Q	60000	
Operating Temp Range	-40 °C to +85 °C		

5.1 RTC Backup Power Options

The nvSRAM RTC supports both capacitor and battery options as the RTC power backup in the absence of V_{CC} supply. The nvSRAM RTC design recommends using either a battery or a capacitor option for the RTC power backup. You should avoid mounting both of them together in an application.

The choice of battery or capacitor entirely depends on the application requirements. As a rule, if the system expects power down for less than 30 days, then a capacitor may be more suitable than a battery because of its smaller footprint and the reliability of capacitors at higher ambient temperatures. However, if the system's expected power-down period is longer than 30 days at a stretch, then battery is generally preferred because supercapacitors with a value greater than 1 farad and a voltage rating above 3.6 V are not easily available in small-footprint package options. If the application can allow larger capacitor packages, the RTC backup time for more than 30 days can be obtained with a capacitor value larger than 1 farad. The calculation for nvSRAM RTC backup time is shown in Equation 11 $Time = \frac{C\Delta V}{I}$

Where,
Time = Total discharge time in seconds

C = Value of supercap on VRTCcap pin in farad

ΔV = VCC – VRTCcap (min)

I = Supercap discharge current in amperes

Supercap discharge current (I) comprises nvSRAM RTC backup current (IBAK) and supercap self-leakage current (iL), as shown in Equation 12.

Equation 12 $I = IBAK + iL$
Example 1 for the capacitor option and Example 2 for the battery option. These two examples are valid for any rated value of a capacitor or battery used in applications.

When using a battery for the RTC power backup option, the V_{RTCbat} pin is directly connected to the lithium coin cell battery. Similarly, if a capacitor is used for the RTC power backup, then the V_{RTCcap} pin is directly connected to the supercap. The nvSRAM RTC has an internal automatic switching that disconnects itself from the backup power source and switches to the main V_{CC} whenever the main supply is available. It switches to the backup power source when power goes off. To determine the backup time duration achievable by different capacitor values or different battery ratings, use the equations provided in the following section.

5.2 Calculation of RTC Backup Time

This section describes equations that you can use to calculate battery and capacitor backup time for the RTC. The nvSRAM draws a constant current (I_{BAK}) to keep the oscillator running using a backup power supply source (either capacitor or battery). This constant current gradually discharges the capacitor or battery over the time period.

5.2.1 Discharge Time for Capacitor

Equation 11 $Time = \frac{C\Delta V}{I}$

Where,
Time = Total discharge time in seconds

C = Value of supercap on V_{RTCcap} pin in farad

ΔV = V_{CC} – V_{RTCcap} (min)

I = Supercap discharge current in amperes

Supercap discharge current (I) comprises nvSRAM RTC backup current (I_{BAK}) and supercap self-leakage current (i_L), as shown in Equation 12.

Equation 12 $I = I_{BAK} + i_L$

5.2.2 Example 1

If the application uses a 1-F capacitor on the V_{RTCcap} pin, with a typical power supply at 3 V (V_{CC}) and drawing a typical I_{BAK} of 350 nA at room temperature, then the capacitor can power the RTC for 49.6 days without recharging. To illustrate the backup time calculation, the following example considers the supercap discharge current (I) as the nvSRAM RTC backup current I_{BAK}.

Calculation

The minimum capacitor voltage required on the V_{RTCcap} pin to run the RTC is 1.5 V.

Therefore, Δ V is 1.5 V (3 V – 1.5 V).

Equation 13 $Time(hr) = \frac{1.0\ x\ 1.5}{350\ x(10)^{-9} x\ 60\ x\ 60}$ = 1,190 hours or 49.6 days

5.2.3 Discharge Time for Battery

Battery manufacturers provide the battery spec in milliampere hours (mAh). The RTC backup timing calculation for the battery is simpler than for the capacitor.

Equation 14 $Time\ (hrs) = \frac{mAhofbattery}{I\ (mA)}$

Where,

I (mA) = I_{BAK} in milliamperes

5.2.4 Example 2

If the application uses a 48-mAh BR1225 coin cell battery, then the battery can run the nvSRAM RTC for approximately 15.6 years without battery replacement. The nvSRAM RTC circuit draws a typical I_{BAK} of 350 nA at room temperature.

Calculation

Equation 15 $Time(hr) = \frac{48\ x(10)^{-3}}{350\ x(10)^{-9} x\ 24\ x\ 365}$ = 137,142 hours or 15.6 years

The nvSRAM RTC specifies 1.8 V as the minimum voltage at the battery pin (V_{RTCbat}). That is, the battery output voltage must be greater than 1.8 V to provide the sustained RTC oscillation throughout the life span of the system.

5.2.5 Example 2

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Calculation

Equation 15 $Time(hr) = \frac{48\ x(10)^{-3}}{350\ x(10)^{-9} x\ 24\ x\ 365}$ = 137,142 hours or 15.6 years

The nvSRAM RTC specifies 1.8 V as the minimum voltage at the battery pin (V_{RTCbat}). That is, the battery output voltage must be greater than 1.8 V to provide sustained RTC oscillation throughout the life span of the system.

5.2.6 Charging Time for Capacitor on V_{RTCcap}

The charging of the backup capacitor is also a critical parameter to consider in RTC circuit design.

If V_{RTCcap} > 0.5 V or if no capacitor is connected to the V_{RTCcap} pin, then the oscillator start time (t_{OCS}) is 1 to 2 seconds as defined in the datasheet.

If the capacitor on V_{RTCcap} is discharged to a voltage level lower than 0.5 V (V_{RTCcap} < 0.5 V), then after applying V_{CC}, the nvSRAM RTC does not start the oscillator immediately; it waits until the RTC capacitor on V_{RTCcap} is charged to 0.5 V. After the voltage on V_{RTCcap} reaches 0.5 V, the nvSRAM starts oscillation after t_{OCS} time.

The time nvSRAM takes to charge the RTC capacitor to 0.5 V depends upon the initial residual voltage on the RTC capacitor and the charging path resistance (R_{BKCHG}) of nvSRAM, which is typically 650 Ω.

The capacitor charging equation in a given RC network is defined as follows:

Equation 16 $Vc(t) = Vcc(1 - e^{-t/RC})$

Where,

Vc(t) = Voltage across the capacitor at a time t

V_{CC} = Supply voltage in volts

R = Charging path resistance (R_{BKCHG}) in Ω

C = Value of supercap on the V_{RTCcap} pin in farads

5.2.7 Example 3

A fully discharged capacitor of value 1.0 F is connected to the V_{RTCcap} pin. When 3.0 V is applied to the nvSRAM V_{CC}, it starts charging the capacitor on V_{RTCcap} to a minimum voltage level of 0.5 V before it starts oscillation in t_{OCS} time.

The typical time nvSRAM takes to charge the capacitor from 0 V to 0.5 V is 118 sec.

Calculation

Equation 17 $0.5 = 3.0\ (1 - e^{-t/(650*1)})$

t (sec) = 118 seconds (approximately 2 minutes)

You can apply this formula to calculate the actual charging time for the RTC capacitor that is connected on the V_{RTCcap} pin of nvSRAM.

Refer to the device datasheet for V_{RTCcap}/V_{RTCbat} (min/max), I_{BAK} (min /max), and R_{BKCHG} (min/max) values.

Note: If a battery is applied to the V_{RTCbat} pin prior to V_{CC}, the chip will draw high I_{BAK} current. This occurs even if the oscillator is disabled. To maximize battery life, V_{CC} must be applied before a battery is applied to the V_{RTCbat} pin.

6 PCB Design Considerations

The RTC crystal oscillator is a low-current circuit with high impedance nodes on the crystal pins. Due to the lower timekeeping current of RTC, the crystal connections are very sensitive to noise on the board. Hence, it is necessary to isolate the RTC circuit from other signals on the board.

It is also critical to minimize the stray capacitance on the PCB board. Stray capacitances add to the overall crystal load capacitance and therefore cause oscillation frequency errors. Proper bypassing and careful layout are required to achieve optimum RTC performance.

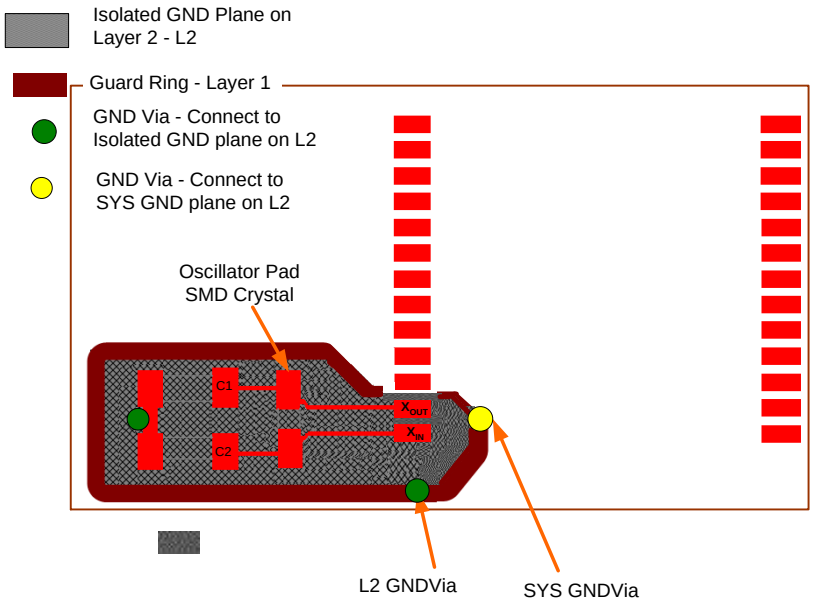
6.1 Signal Routing

The board layout must adhere to (but is not limited to) the following guidelines while routing nvSRAM RTC circuitry. Following these guidelines can help you achieve optimum performance from the nvSRAM RTC design.

- Place the crystal as close as possible to the X_{IN} and X_{OUT} pins. Keep the trace lengths between the crystal and the RTC equal in length and as short as possible to reduce the probability of noise coupling by reducing the length of the antenna.
- Keep the X_{IN} and X_{OUT} trace width less than 8 mils. A wider trace width leads to larger trace capacitance. The larger these bond pads and traces are, the more likely it is that noise can couple from adjacent signals.
- Shield the X_{IN} and X_{OUT} signals by providing a guard ring around the crystal circuitry. This guard ring prevents noise coupling from neighboring signals.
- Take care while routing any other high-speed signal in the vicinity of the RTC traces. The more the crystal is isolated from other signals on the board, the less likely it is that noise is coupled into the crystal. Maintain a minimum 200-mil separation between the X_{IN}, X_{OUT} traces and any other high-speed signal on the board.
- Do not route any signals underneath crystal components on the same PCB layer.
- Create an isolated solid copper plane on the adjacent PCB layer and underneath the crystal circuitry to prevent unwanted noise coupled from traces routed on the other signal layers of the PCB. The local plane should be separated by at least 40 mils from the neighboring plane on the same PCB layer. The solid plane should be in the vicinity of RTC components only, and its perimeter should be kept equal to the guard ring perimeter.

Figure 8 shows the recommended layout for the nvSRAM RTC circuit.

Figure 8. Recommended Layout for nvSRAM RTC



6.2 RTC Clock Calibration

The RTC is driven by a quartz-controlled oscillator with a nominal frequency of 32.768 kHz. The clock accuracy depends on the quality of the crystal, usually ±20 ppm limits at 25 °C. This error could equate to 1.53 minutes per month. The nvSRAM RTC employs a digital calibration circuit, which can improve the accuracy to +1/–2 ppm at 25 °C. The calibration circuit adds or subtracts counts from the oscillator divider circuit. The number of times the pulses are suppressed (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five calibration bits defined in the calibration control register. Adding counts speeds up the clock; subtracting counts slows down the clock. The calibration bits occupy the five lower order bits in the control register. These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a sign bit, where “1” indicates positive calibration and “0” indicates negative calibration. Calibration occurs within a 64-minute cycle.

The first 62 minutes in the cycle may, once per minute, have 1 second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary “1” is loaded into the register, only the first 2 minutes of the 64-minute cycle is modified; if a binary “6” is loaded, the first 12 is affected and so on. Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is, +4.068 or –2.034 ppm of adjustment per calibration step.

To determine the calibration value, set the CAL bit in the flag register to one. This causes the INT pin to toggle at 512-Hz nominal frequency. Any deviation measured from the 512 Hz indicates the degree and direction of the required correction. For example, a reading of 512.01024 Hz indicates a +20-ppm error, requiring a –10 (001010) to be loaded into the calibration register. Note that setting or changing the calibration register does not affect the test output frequency. Refer to AN53313 for more information on nvSRAM RTC clock calibration techniques.

6.3 Troubleshooting Guide for nvSRAM RTC

The Cypress nvSRAM troubleshoot guide KBA94279 addresses common nvSRAM RTC issues that can occur in systems and provides resolution on majority of these.

7 Summary

To get the desired accuracy from the RTC circuit, you must consider various factors that can directly affect RTC performance. These factors are crystal and component selection, layout design rules, and operating conditions. This application note highlights the key design rules that should be followed to get the desired RTC performance from the nvSRAM RTC.

8 Related Documents

Application Note

- AN53313 - Real Time Clock Calibration in Cypress nvSRAM

Datasheets

- CY14B101P: 1-Mbit (128 K × 8) Serial SPI nvSRAM with Real Time Clock
- CY14B512P: 512-Kbit (64 K × 8) Serial (SPI) nvSRAM with Real Time Clock
- CY14B256P: 256-Kbit (32 K x 8) Serial (SPI) nvSRAM with Real Time Clock
- CY14B104K, CY14B104M: 4-Mbit (512 K × 8/256 K × 16) nvSRAM with Real Time Clock
- CY14C064I, CY14B064I, CY14E064I: 64-Kbit (8 K × 8) Serial (I2C) nvSRAM with Real Time Clock
- CY14C064PA, CY14B064PA, CY14E064PA: 64-Kbit (8 K × 8) SPI nvSRAM with Real Time Clock
- CY14C256I, CY14B256I, CY14E256I: 256-Kbit (32 K × 8) Serial (I2C) nvSRAM with Real Time Clock
- CY14C256PA, CY14B256PA, CY14E256PA: 256-Kbit (32 K × 8) SPI nvSRAM with Real Time Clock
- CY14C512I, CY14B512I, CY14E512I: 512-Kbit (64 K × 8) Serial (I2C) nvSRAM with Real Time Clock
- CY14C101I, CY14B101I, CY14E101I: 1-Mbit (128 K × 8) Serial (I2C) nvSRAM with Real Time Clock
- CY14C101PA, CY14B101PA, CY14E101PA: 1-Mbit (128 K × 8) Serial (SPI) nvSRAM with Real Time Clock
- CY14B104K, CY14B104M: 4-Mbit (512 K × 8/256 K × 16) nvSRAM with Real Time Clock
- CY14B108K, CY14B108M: 8-Mbit (1024 K × 8/512 K × 16) nvSRAM with Real Time Clock
- CY14B116K, CY14B116M: 16-Mbit (2048 K × 8/1024 K × 16) nvSRAM with Real Time Clock

Knowledge Base Articles

- Troubleshooting Guide for nvSRAM and FRAM-KBA94279

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Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2930446	ZSK	05/11/2010	New application note.
*A	3283741	ZSK	06/15/2011	Table1 is modified to include a few new nvSRAM RTC parts. Table1 has added a note (Note1) for a few devices which are not recommended for new designs now.
*B	3638383	ZSK	06/08/2012	Added note in Discharge Time for Capacitor. Updated template.
*C	3721292	ZSK	08/23/2012	Added following paragraph in RTC Backup Power Options. "Because Super capacitors with value greater than 1 Farad and voltage rating above 3.6V are not easily available in small foot print package options. If users' application can allow larger capacitor packages, the RTC back up time for more than 30 days can be obtained with capacitor value larger than 1 Farad. Calculation for nvSRAM RTC backup time is shown through Equation 11 $Time = \frac{C\Delta V}{I}$ Where, Time = Total discharge time in seconds C = Value of supercap on VRTCcap pin in farad ΔV = VCC – VRTCcap (min) I = Supercap discharge current in amperes Supercap discharge current (I) comprises nvSRAM RTC backup current (IBAK) and supercap self-leakage current (iL), as shown in Equation 12. Equation 12 $I = IBAK + iL$ Example 1 for capacitor and Example 2 for battery options. These two examples are valid for any rated value of a capacitor or a battery used in applications."
*D	4675902	ZSK	03/04/2015	Update the following in **Table 1**: ▫ Replaced the obsolete part CY14B101K/M with its drop-in-replacement part CY14B101KA/MA ▫ Added 16-Mbit nvSRAM RTC part CY14B116K/M Added Note 2 on battery installation in Equation 16 $Vc(t) = Vcc(1 - e^{-t/RC})$ Where, Vc(t) = Voltage across the capacitor at a time t VCC = Supply voltage in volts R = Charging path resistance (RBKCHG) in Ω C = Value of supercap on the VRTCcap pin in farads Example 3. Added Troubleshooting Guide for nvSRAM RTC section. Added Related Documents section. Updated the entire document with minor changes.

Revision	ECN	Orig. of Change	Submission Date	Description of Change
*E	4717021	ZSK	04/08/2015	Update the application note landing page link: http://www.cypress.com/go/AN61546. Fixed the broken links in the datasheet category, in Related Documents.
*F	4790158	ZSK	06/08/2015	Updated Table 1. Formatted the document as per new template.
*G	5823067	AESATP12	07/20/2017	Updated logo and copyright.

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