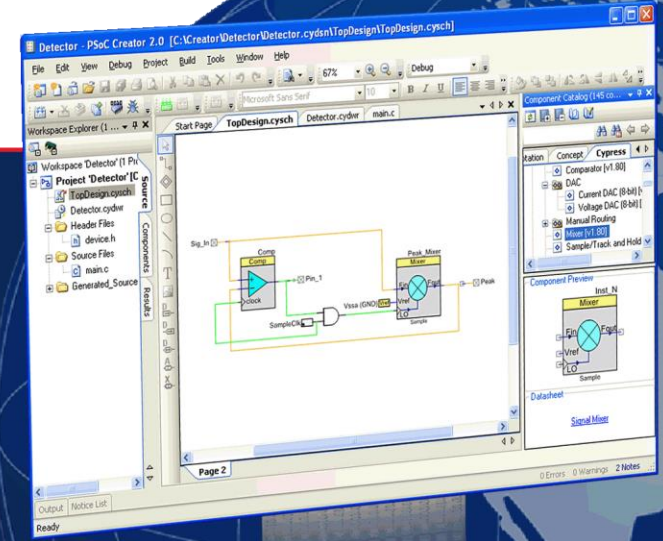




# Quick Presentation: High-Performance 4-PLL Clock Generator



Cypress Delivers Industry-Leading Flexible Timing Solutions for Next-Generation Consumer Devices

# Product Overview

## Applications

Multifunction printers  
 Digital TVs  
 Blu-ray recorders  
 Home gateways  
 Femtocells  
 Routers and switches

## Features

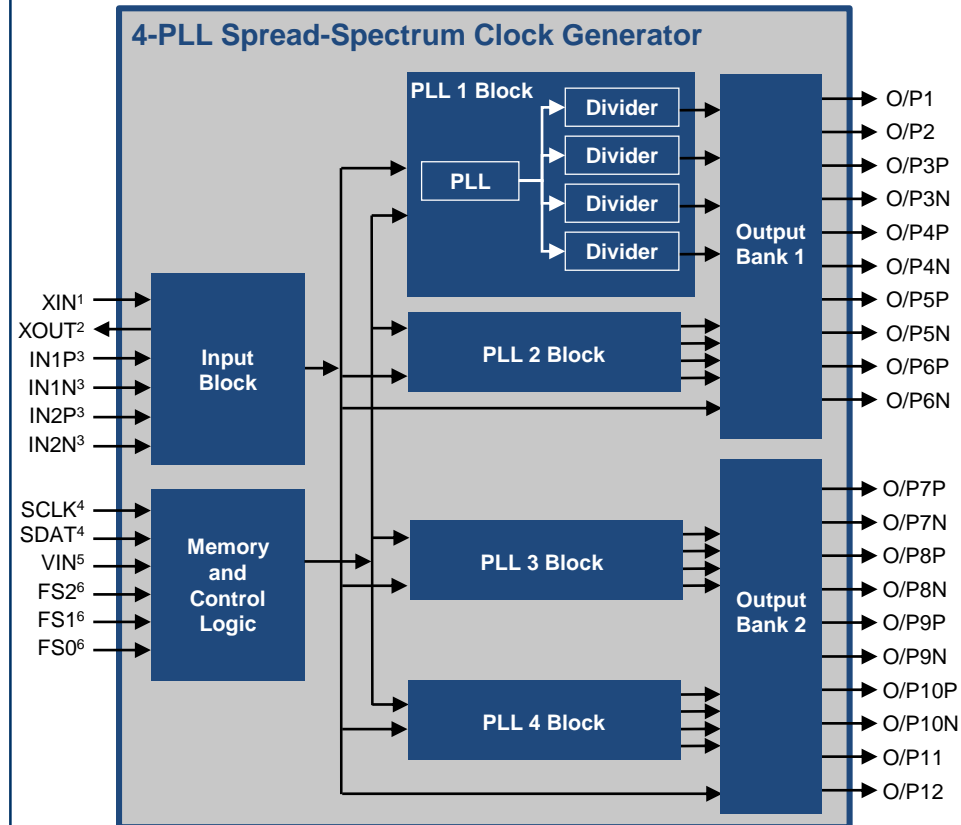
High frequency: 700-MHz differential, 250-MHz single-ended  
 Pin select and I<sup>2</sup>C programming  
 Twelve outputs:  
     Eight configurable as differential or single-ended  
     Four single-ended  
 Reference clock support for PCIe 3.0, SATA 2.0 and 10 GbE  
 RMS Phase Jitter < 0.7 ps (typical)  
 Additional features:  
     Configurable as zero or non-zero delay buffer  
     Glitch-free frequency switching  
     Frequency Select  
     Phase alignment of outputs  
     Early/late phase clocks  
     PLL cascading  
     Voltage Controlled Frequency Synthesis (VCFS)

## Collateral

Datasheet, Application Notes: [CY27410](#)

<sup>1</sup> Crystal input  
<sup>2</sup> Crystal output  
<sup>3</sup> Reference clock inputs

## Block Diagram



## Availability

Sampling: Now  
 Production: Now

<sup>4</sup> Serial port  
<sup>5</sup> Voltage input pin for VCFS  
<sup>6</sup> Frequency select inputs




# Cypress 4-PLL Clock Generator vs. Competition's



<u>Feature</u>	<u>CY274xx</u>	<u>5V49EE902</u>	<u>Si5338</u>
<b>Max. O/P Freq. (single-ended)</b>	<b>250 MHz</b>	200 MHz	200 MHz
<b>Max. O/P Freq. (differential)</b>	<b>700 MHz</b>	500 MHz	<b>700 MHz</b>
<b>Cycle-to-Cycle Jitter</b>	<b>30 ps</b>	200 ps	<b>30 ps</b>
<b>RMS Phase Jitter</b>	<b>0.7 ps</b>	3 ps	<b>0.7 ps</b>
<b>Number of Outputs</b>	<b>12 Single-Ended, 8 Differential</b>	9 Single-Ended, 2 Differential	8 Single-Ended, 4 Differential
<b>Current per PLL</b>	<b>20 mA</b>	22.5 mA	45 mA
<b>Standards</b>	<b>PCIe 3.0</b> , SATA 2.0, 10 GbE, USB 3.0	PCIe 1.0, SATA 2.0, 10 GbE, USB 3.0	<b>PCIe 3.0</b> , SATA 2.0, 10 GbE, USB 3.0
<b>VDD</b>	1.8, 2.5, 3.3 V	3.3 V	1.8, 2.5, 3.3 V
<b>Programmability</b>	I <sup>2</sup> C	No	I <sup>2</sup> C
<b>SS (center)</b>	Center: $\pm 0.225\%$ to $\pm 2.50\%$	Center: $\pm 0.5\%$	<b>Center: <math>\pm 0.2\%</math> to <math>\pm 5\%</math></b>
<b>SS (down)</b>	<b>Down: -0.25% to -5.0%</b>	Down: -0.5%	Down: -0.5%
<b>Temperature Grade</b>	<b>Industrial and AEQ-100 (-40°C to +85°C)</b>	Industrial (-40°C to +85°C)	Industrial (-40°C to +85°C)

# Cypress 4-PLL Clock Generator vs. Competition's



<u>Feature</u>	 <u>CY274xx</u>	 <u>5V49EE902</u>	 <u>Si5338</u>
<b>VCFS</b>	Yes	No	No
<b>Cascading PLL</b>	Yes	No	No
<b>Zero Delay Buffer Mode</b>	Yes	No	Yes
<b>Non-Zero Delay Buffer Mode</b>	Yes	No	No
<b>Early/Late Phase Clock</b>	Yes	No	Yes
<b>Glitch-Free Outputs</b>	Yes	Yes	No
<b>Frequency Select</b>	Yes	Yes	No
<b>On-Board Programming</b>	Yes	No	Yes