AN58815

# Advantages of 65-nm Technology over 90-nm Technology QDR® Family of SRAMs

**Associated Project: No**
**Associated Part Family: CY7C13xxKV18, CY7C14xxKV18 CY7C15xxKV18, CY7C25xxKV18, CY7C16xxKV18, CY7C26xxKV18**
**Software Version: None**
**Related Application Notes: AN42468, AN54908**

The advantages of the 65-nm technology QDR® SRAMs over the 90-nm technology QDR® SRAM devices are outlined in this Application Note.

## Introduction

The 65-nm technology QDR family of devices offers significant advantages over the 90-nm technology family. This application note describes these advantages and provides guidelines to migrate from 90-nm to 65-nm devices.

## Overview

Table 1 highlights the features and differences between the 65-nm and 90-nm QDR device families.

Table 1. Features of 65-nm and 90-nm QDR Family of Devices

| | | QDR II | DDRII | DDRII SIO | QDRII+ | QDRII+ | DDRII+ | DDRII+ | DDRII+ SIO | DDRII+ SIO |
|---|---|---|---|---|---|---|---|---|---|---|
| **Read Latency – 90-nm and 65-nm** | | 1.5 | 1.5 | 1.5 | 2 | 2.5 | 2 | 2.5 | 2 | 2.5 |
| **Write Latency – 90-nm and 65-nm** | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| **Frequency (Burst of 4)** | **65-nm** | 333 MHz | 333 MHz | N/A | 450 MHz | 550 MHz | 450 MHz | 550 MHz | N/A | N/A |
| | **90-nm** | 300 MHz | 300 MHz | N/A | 400 MHz | 450 MHz | 400 MHz | 450 MHz | N/A | N/A |
| **Bandwidth[1] (Burst of 4)** | **65-nm** | 48 Gbps | 24 Gbps | N/A | 64 Gbps | 80 Gbps | 32 Gbps | 40 Gbps | N/A | N/A |
| | **90-nm** | 44 Gbps | 22 Gbps | N/A | 58 Gbps | 64 Gbps | 29 Gbps | 32 Gbps | N/A | N/A |
| **Idd - Active Current [2,4] (Burst of 4)** | **65-nm** | 850 mA | 510 mA | N/A | 1100 mA | 1310 mA | 630 mA | 740 mA | N/A | N/A |
| | **90-nm** | 1040 mA | 900 mA | N/A | 1300 mA | 1475 mA | 950 mA | 1050 mA | N/A | N/A |
| **Iddq - I/O Switching Current [3,4] (Burst of 4)** | **65-nm** | 90 mA | 90 mA | N/A | 120 mA | 150 mA | 120 mA | 150 mA | N/A | N/A |
| | **90-nm** | 80 mA | 80 mA | N/A | 110 mA | 120 mA | 110 mA | 120 mA | N/A | N/A |

| 65-nm | 90-nm | 65-nm and 90-nm |
|---|---|---|

[1] Maximum Bandwidth = Maximum frequency x Data Rate x Maximum Bus Width x Number of Ports

[2] The active currents specified above for comparison are the values for 72M QDRII/DDRII/QDRII+/DDRII+ SRAMs. Refer to the respective product datasheets for active currents (Idd) for other density SRAMs in the link below:
http://www.cypress.com/?id=95

[3] The I/O switching currents specified above for comparison are the values based on 1.5 V Vddq, 5 pF load capacitance, 36 switching I/Os, and mentioned highest frequency assumptions.

[4] To calculate the total power consumed by SRAM, refer the tool in the link below:
http://www.cypress.com/?docID=23984

Table 1. Features of 65-nm and 90-nm QDR Family of Devices

| | | QDR II | DDRII | DDRII SIO | QDRII+ | QDRII+ | DDRII+ | DDRII+ | DDRII+ SIO | DDRII+ SIO |
|---|---|---|---|---|---|---|---|---|---|---|
| **Frequency (Burst of 2 )** | **65-nm** | 333 MHz | 333 MHz | 333 MHz | 333 MHz | 333 MHz | 450 MHz | 550 MHz | 450 MHz | 550 MHz |
| | **90-nm** | 300 MHz | 300 MHz | 300 MHz | 300 MHz | 300 MHz | 400 MHz | 450 MHz | N/A | N/A |
| **Bandwidth[1] (Burst of 2 )** | **65-nm** | 48 Gbps | 24 Gbps | 24 Gbps | 48 Gbps | 48 Gbps | 32 Gbps | 40 Gbps | 64 Gbps | 80 Gbps |
| | **90-nm** | 44 Gbps | 22 Gbps | 22 Gbps | 44 Gbps | 44 Gbps | 29 Gbps | 32 Gbps | N/A | N/A |
| **Idd - Active Current [2,4] (Burst of 2)** | **65-nm** | 990 mA | 640 mA | 640 mA | 990 mA | 990 mA | 820 mA | 970 mA | 820 mA | 970 mA |
| | **90-nm** | 1215 mA | 1020 mA | 980 mA | N/A | 1150 mA | 1420 mA | 1420 mA | N/A | N/A |
| **Iddq - I/O Switching Current [3,4] (Burst of 2)** | **65-nm** | 90 mA | 90 mA | 90 mA | 90 mA | 90 mA | 120 mA | 150 mA | 120 mA | 150 mA |
| | **90-nm** | 80 mA | 80 mA | 80 mA | N/A | 80 mA | 110 mA | 120 mA | N/A | N/A |
| **Input/Output Capacitance[5]** | **65-nm** | 4 pF/4 pF | 4 pF/4 pF | 4 pF/4 pF | 4 pF/4 pF | 4 pF/4 pF | 4 pF/4 pF | 4 pF/4 pF | 4pF/4 pF | 4 pF/4 pF |
| | **90-nm** | 5.5 pF/6 pF | 5.5 pF/6 pF | 5.5 pF/6 pF | 5 pF/7 pF | 5 pF/7 pF | 5 pF/8 pF | 5 pF/8 pF | N/A | N/A |
| **Input Clocks for Output Data (C,C#) — 90-nm and 65-nm** | | Yes | | | No | | | | | |
| **QVLD (Valid output data indicator) — 90-nm and 65-nm** | | No | | | Yes | | | | | |
| **ODT (On-Die Termination) — Applicable in 65-nm only. Not supported in 90-nm.** | | No | | | Yes | | | | | |
| **Density** | **65-nm** | 18 Mb, 36 Mb, 72 Mb, and 144 Mb | | | | | | | | |
| | **90-nm** | 18 Mb, 36 Mb, 72 Mb | | | | | | | | |
| **Organization (Bus Width) – 90-nm and 65-nm** | | x9, x18, x36 | | | | | | | | |
| **VDD (Core) – 90-nm and 65-nm** | | 1.8 V ± 0.1 V | | | | | | | | |
| **VDDQ (I/O) – 90-nm and 65-nm** | | 1.8 V ± 0.1 V or 1.5 V ± 0.1 V | | | | | | | | |
| **SER (FIT/Mb)[6]** | **Logical Single Bit Upset (LSBU) – 65-nm** | 216 at 85 °C | | | | | | | | |
| | **Logical Single Bit Upset (LSBU) – 90-nm** | 368 at 85 °C | | | | | | | | |
| | **Logical Multi Bit Upset (LMBU) – 90-nm and 65-nm** | 0.01 at 85 °C | | | | | | | | |
| **SEL (FIT/Dev) – 90-nm and 65-nm** | | 0.1 at 85 °C | | | | | | | | |
| **Clock generation and Lock Time** | **Phase-locked loop (PLL) – 65-nm[7]** | Yes (PLL Lock time): 20 µs [8] | | | | | | | | |
| | **Delay locked loop (DLL) – 90-nm** | Yes (DLL lock time): 1024 clock cycles for QDRII/DDRII and 2048 clock cycles for the QDRII+/DDRII+ | | | | | | | | |
| **Echo Clocks (CQ, CQ#)** | | Yes | | | | | | | | |
| **PKG—90-nm and 65-nm** | | 165 Ball FBGA | | | | | | | | |

| 65-nm | 90-nm | 65-nm and 90-nm |
|---|---|---|

[5] The capacitance values specified above for comparison are the values for 72M QDRII/DDRII/QDRII+/DDRII+ SRAMs. Refer to the respective product datasheets for capacitance for other density SRAMs in the link below:
http://www.cypress.com/?id=95

[6] For more details see the Application Note, "AN54908, Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates"

[7] The PLL lock time of 20 µs is a QDR consortium defined specification. Cypress 65-nm QDR family of devices are backward compatible with the 90-nm QDR family devices in that the PLL lock time meets 1024 clock cycle for QDRII or DDRII devices and 2048 clock cycles for the QDRII+ or DDRII+ devices

[8] Number of clock cycles = Frequency x 20 µs

# Advantages of 65-nm Technology Devices

## Faster Operating Frequencies

The 65-nm technology devices are capable of operating at higher operating frequencies of 550 MHz and total data rates up to 80 Gbps[1]. This results in the significant bandwidth improvement (~25 percent) over the 90-nm QDR family of devices that can operate upto a maximum frequency of 450 MHz. This improvement in operating frequency satisfies the higher banwidth requirements in networking application.

## Lower Power Consumption

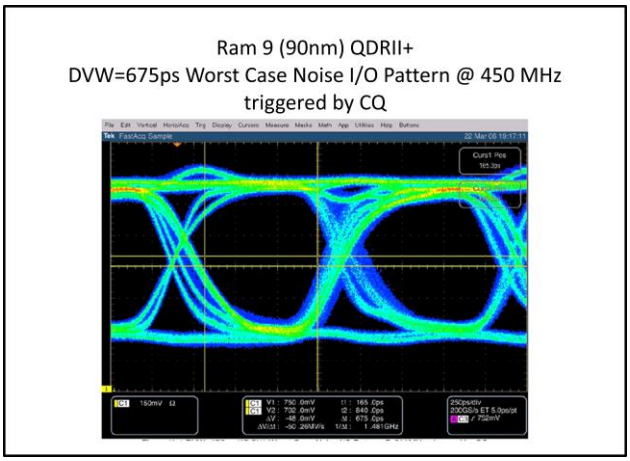
The 65-nm technology QDR devices have lower power consumption than the equivalent 90-nm technology QDR devices. The power saving is ~30 percent at worst case condition.

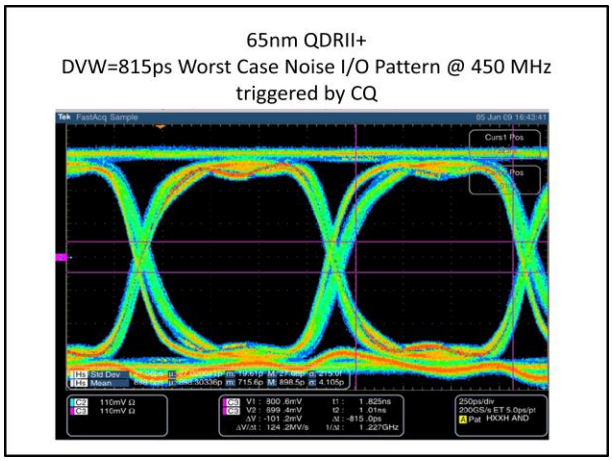
## Improved Data Valid Window

The data valid window for the outputs of 65-nm QDR devices is about 21 percent wider than the 90-nm QDR devices. This improvement is achieved using a low jitter clock generating phase-locked loop (PLL) as opposed to a delay locked loop (DLL) in the 90-nm technology device. The PLL filters the incoming jitter and corrects any duty cycle distortion for the inputs. The improved data valid window helps to achieve better timing margins for the 65-nm technology device.

Figure 1 compares the data valid window of a 90-nm QDRII+ and a 65-nm QDRII+ device at 500 MHz. As shown in the figure, there is a significant improvement (~21 percent) in the data window for the 65-nm QDRII+ devices.

Figure 1. Comparison of Data Valid Window (Taken from Lab)




## Improved Signal Integrity

The 65-nm technology QDRII+ or DDRII+ devices have on-die termination for inputs such as data inputs, byte write signals, and input clocks (K/Kb). This feature is not present in the 90-nm technology QDRII+ or DDRII+ devices. On-die termination improves signal integrity because It eliminates the need for external termination resistors thereby simplifies board routing, reduces the cost, board area and power consumed by external resistors. For more details on on-die termination, see the application note AN42468, *On-Die Termination for QDRII+/DDRII+ SRAMs.*

## Lower Input and Output Capacitances

Compared with the 90-nm predecessors, the 65-nm QDR family of SRAMs has lower input and output capacitance by ~50 percent. This translates to lower return loss and therefore lower reflections or discontinuity at the inputs. A lower capacitance also results in lower AC power consumption at the input.

## Lower Power Consumption and Junction Temperature

### Power Dissipation ($P_d$)

Calculate the power dissipation based on the following equations:

$P_d$ = Core Power + I/O Switching Power

$P_d = V_{DD}\ I_{DD} + \alpha\ f\ C_L\ V_{DDQ}^2\ N$

Where:

$V_{DD}$ = Core voltage

$I_{DD}$ = Active current

α = Activity factor, or the ratio of frequency at which outputs toggle to clock frequency

f = Operating frequency

$C_L$= External load capacitance

$V_{DDQ}$ = I/O voltage

N = Number of I/Os that are switching

Table 2 shows that 65-nm parts have better power ratings than 90-nm parts.

Table 2. Comparison of Power Dissipation between 65-nm and 90-nm QDR-II+ Devices

| **65-nm QDR-II+ SRAM (18 Mb)<br>CY7C1165KV18-400BZC** | **90-nm QDR-II+ SRAM (18 Mb)<br>CY7C1165V18-400BZC** |
|---|---|
| $V_{DD}$ = 1.8 V | $V_{DD}$ = 1.8 V |
| $I_{DD}$ = 850 mA | $I_{DD}$ = 1080 mA |
| α = 1 | α = 1 |
| f = 400 MHz | f = 400 MHz |
| $C_L$= 5 pF | $C_L$= 5 pF |
| $V_{DDQ}$ = 1.5 V | $V_{DDQ}$ = 1.5 V |
| N = 36 | N = 36 |
| Therefore:<br>$P_d = V_{DD}\ I_{DD} + \alpha\ f\ C_L\ V_{DDQ}^2\ N$<br>$P_d$ = 1.8 V x 850 mA + 1 x 400 MHz x 5 pF x (1.5 V) $^2$ x 36 | Therefore:<br>$P_d = V_{DD}\ I_{DD} + \alpha\ f\ C_L\ V_{DDQ}^2\ N$<br>$P_d$ = 1.8 V x 1080 mA + 1 x 400 MHz x 5 pF x (1.5 V)$^2$ x 36 |
| **Total Power Dissipation = 1692 mW** | **Total Power Dissipation = 2106 mW** |

### Junction Temperature ($T_J$)

Calculate the junction temperature based on the following equation:

$T_J = P_d\ \theta_{JA} + T_A$

Where:

$\theta_{JA}$ = Junction-to-ambient thermal resistance

$T_A$ = Ambient temperature

$P_d$ = Power dissipation

Table 3 shows that 65-nm parts have lower junction temperature ratings than 90-nm parts.

Table 3. Comparison of Junction Temperature (TJ) between 65-nm and 90-nm QDR-II+ Devices

| **65-nm QDR-II+ SRAM (18 Mb)<br>CY7C1165KV18-400BZC (165 BGA)** | **90-nm QDR-II+ SRAM (18 Mb)<br>CY7C1165V18-400BZC (165 BGA)** |
|---|---|
| $\theta_{JA}$ = 18.96 °C/W | $\theta_{JA}$ = 17.2 °C/W |
| $T_A$ = 60 °C | $T_A$ = 60 °C |
| $P_d$ = 1692 mW | $P_d$ = 2106 mW |
| Therefore:<br>$T_J = P_d\ \theta_{JA} + T_A$<br>$T_J$ = (1692m x 18.96) + 60<br>**Junction Temperature = 92.08 °C** | Therefore:<br>$T_J = P_d\ \theta_{JA} + T_A$<br>$T_J$ = (2106m x 17.2) + 60<br>**Junction Temperature = 96.22 °C** |

## Summary

The 65-nm technology QDR family of devices provides the ability to achieve high performance and bandwidth with few changes to existing boards. Compared to the 90-nm technology, it has less power consumption, lower input and output capacitances, improved data valid window and better signal integrity with On-die termination devices.

## Document History

Document Title: AN58815 – Advantages of 65-nm Technology over 90-nm Technology QDR® Family of SRAMs

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| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| ** | 2847143 | NJY | 01/13/2010 | New application note. |
| *A | 2867379 | SHEA | 01/27/2010 | Minor ECN to correct document number in the footer. |
| *B | 3339199 | NJY | 08/10/2011 | Added part numbers (CY7C16xxKV18, CY7C26xxKV18) to the Associated Part Family in page 1.<br>Added AN42468 to the Associated Application Notes in page 1.<br>Updated Overview:<br>Updated Table 1:<br>Added footnote 7 and referred the same note in “Phase-locked loop (PLL) – 65 nm”.<br>Updated Design Changes to Migrate from 90 nm to 65 nm Family:<br>Updated Host Controller Changes:<br>Updated description.<br>Updated Pinout Changes:<br>Updated description. |
| *C | 3704481 | PRIT | 08/07/2012 | Updated Overview:<br>Updated Table 1:<br>Updated almost entire table.<br>Added footnote 1, 2, 3, 4, 5, 8 and referred them in respective places in the table.<br>Removed “Design Changes to Migrate from 90-nm to 65-nm Family”. |
| *D | 3865941 | PRIT | 01/11/2013 | No technical updates.<br>Completing Sunset Review. |
| *E | 4652688 | PRIT | 02/09/2015 | Updated Advantages of 65-nm Technology Devices:<br>Added Lower Power Consumption and Junction Temperature. |
| *F | 5849999 | HARA | 08/16/2017 | Updated logo and copyright. |
| *G | 6042545 | NILE | 01/23/2018 | Updated to new template.<br>Completing Sunset Review. |

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