AN220973

Traveo Family MCUs: Safe System Recovery from a Power Supply Drop Below Vreset

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Associated Part Family: Traveo

Related Application Notes: For a complete list, click here.

Today's Cypress MCUs are used in multi-power systems. There are power shutdowns which sometimes are intended and sometimes unintended, and glitches. Systems use external monitors as well as internal low-voltage detection (LVD) features of the MCU to detect power glitches and recover safely. In this app note, scenarios where a power supply falls below the LVD threshold and then recovers safely are covered.

1 Introduction

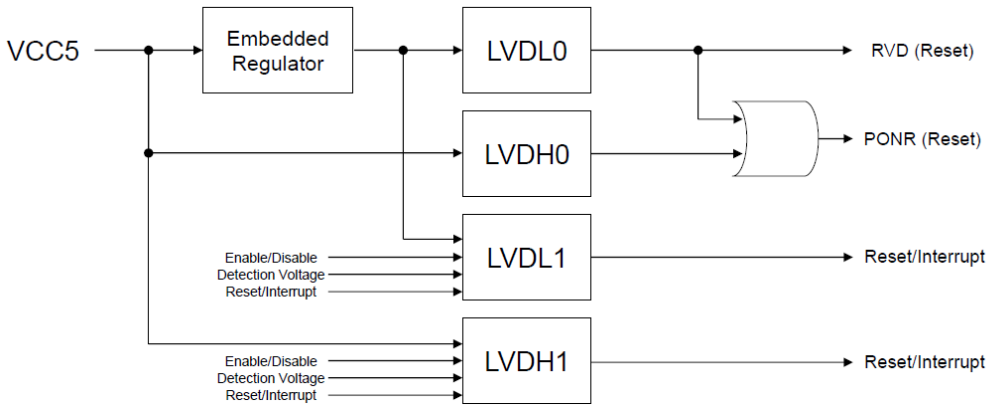
This application note describes the general requirements for achieving a valid Power On Reset (POR) and recovering the system in the best possible way. Designs that implement these requirements makes the system robust to handle unintended power glitches that the system may face. There are multiple power lines required and monitored by Cypress MCUs, but POR is generated by a subset of the supplies (Main 5V supply and core supply). In the next section, all the scenarios to achieve a POR are described.

2 Power Drop Below Vreset and Methods to Recover Safely

There are three scenarios where the device achieves a POR if the power supply (VCC5) drops below Vreset (Vreset is called LVDH0 in the case of the Traveo I MCU series). These scenarios involve conditions on ramp rate and on the time spent below VCC_{low} (for example, 0.2 V for Traveo MCU series) and Vreset. Figure 1 shows the internal hardware structure of the LVD for VCC5 for Traveo devices, even though a similar concept applies for other Traveo devices. For more details on the internal architecture, refer to the device TRM.

The Vreset level is set by the hardware and cannot be modified by the user. An important requirement for the power sequence to note here is that VCC5 must always be greater than or equal to other supplies. This requirement applies at any given point and in any given state.

Figure 1. VCC5 LVD internal structure in Traveo I MCU Series

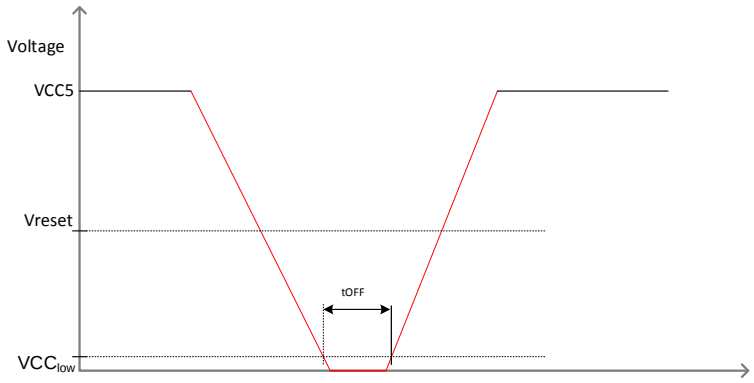


Each scenario listed above is shown graphically in the figures below. Meeting any any of the three requirementsresults in a POR.

2.1 Scenario 1

t_{OFF} greater than the device specification (check device datasheet). Figure 2 illustrates scenario 1.

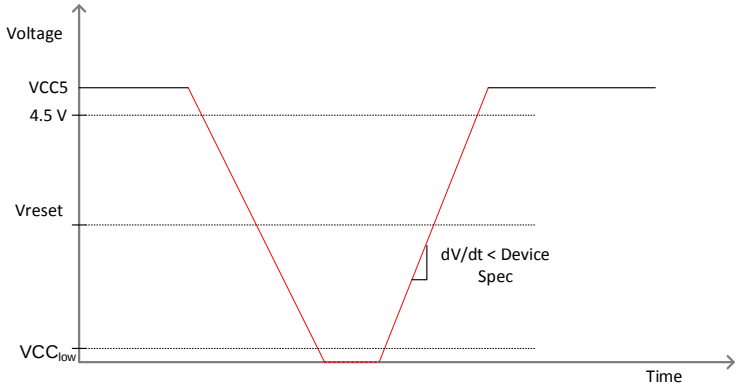
Figure 2. Supply Stays Below VCClow for At Least t_{OFF}



2.2 Scenario 2

Keeping the ramp up rate of VCC5 slower than the device specification during the period from VCC_{low} to Vreset as Figure 3 shows. Specifications on the ramp up rate can be found in the device datasheet.

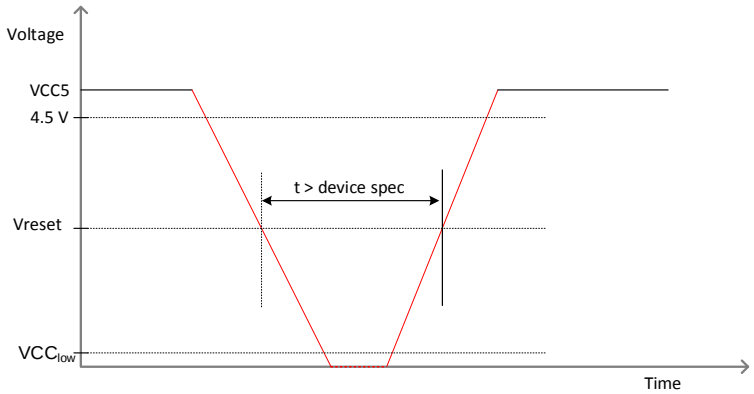
Figure 3. Ramp Rate Kept Below Device Specification to Achieve POR



2.3 Scenario 3

VCC5 stays below Vreset for a minimum of 't' seconds to ensure that the internal LVD detects the glitch.

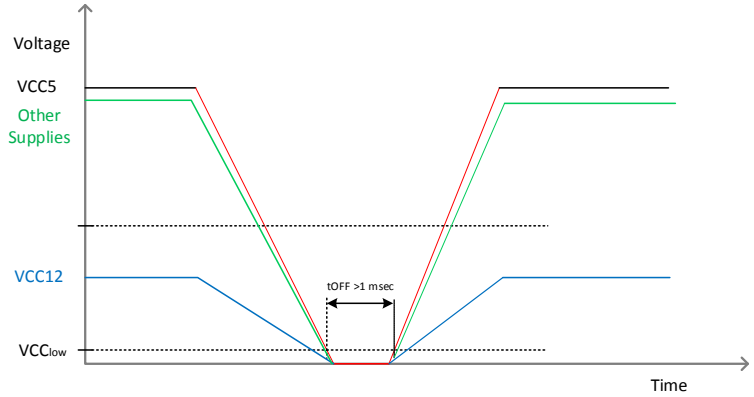
Figure 4. Power Supply Stays Below Vreset for At Least the Time Specified in Device Datasheet



3 Device Power Supply General Requirement

All Traveo devices must have all other supplies as equal to or less than the main power line (VCC5) as shown in Figure 5. To achieve this requirement, the VCC12 (core voltage) must be discharged quickly when a power glitch occurs such that it is never greater than VCC5. The discharge rate is temperature-dependent; it slows down with decreasing temperature.

Figure 5. Power Supply Requirement: VCC5 Must Always Be Greater Than Other Supplies



4 Safe Recovery from Power Supply Drop

4.1 Quick Discharge of Core Voltage (VCC12) and Main Power supply (VCC5)

When a power drop occurs, VCC5 may drop quickly but VCC12 may still hold a residual voltage (VCC12 > VCC5). Powering up from this state violates the general power supply requirement explained in the previous section.

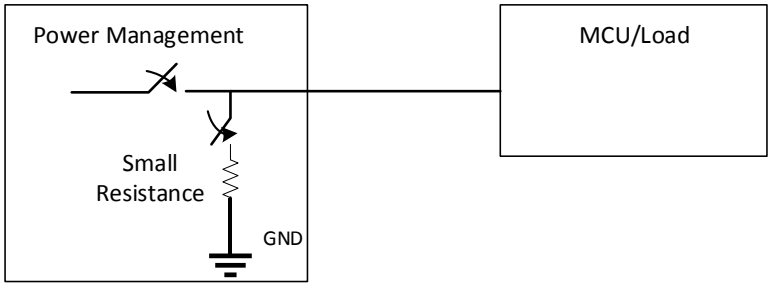
The root cause for this residual voltage on VCC12 is that the MCU goes to the reset state when VCC5 is below Vreset. VCC12 is the core-only power supply and there is no load if the core is in the reset state; therefore, only the leakage current discharges the line, which is slow and temperature-dependent.

A solution to this problem is to discharge the VCC12 and VCC5 lines as quickly as possible. Also, discharging VCC5 quickly ensures that it goes below Vreset for every power drop. There can be several ways to discharge the power rails quickly, two of the simplest being:

1) Use an external regulator featuring an active discharge option.
2) Add a bleeder resistor in parallel to the power rail. (This is a cheaper solution but may increase the current draw during operation).

Figure 6 shows a simple block diagram to explain active discharging. The small resistance is needed to reduce the discharge time and keep the line from floating. Active discharging also ensures that there is no floating voltage on the power line and it is always in a defined power state.

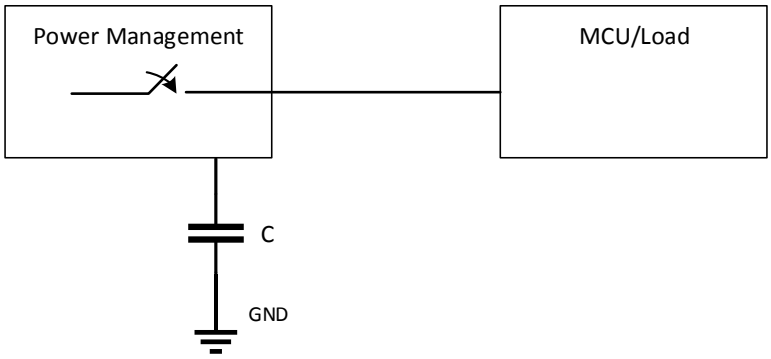
Figure 6. Basic Active Discharging



4.2 Controlled Ramp Rate of VCC5

A feasible way to achieve a valid POR is to have the VCC5 ramp-up rate within the device spec. (refer to the datasheet). Keeping the ramp rate controlled when the supply is below Vreset ensures that the device powers up with a valid POR. You must still make sure that all other supplies are less than or equal to VCC5 at all times. There are certain PMICs available that offer programmable ramp rates for the supply. Figure 7 depicts the basic concept behind ramp rate control.

Figure 7. Control Ramp Rate by Using Appropriate Capacitor Value



5 Conclusion

A power interruption can happen at any time. Achieving a valid POR is of crucial importance when the supply voltage falls below Vreset. This document describes possible scenarios and how to ensure that the device receives a valid POR to recover proper system operation. Discharging the supply line quickly and controlling the power supply ramp rate are two simple measures to satisfy the POR requirement.

6 Definitions, Acronyms, and Abbreviations

C	Capacitor
GND	Ground
MCU	Microcontroller
POR	Power-On Reset
t_{OFF}	VCC OFF time
Vreset	Voltage level of VCC where a POR is issued
VCC_{low}	Voltage level below which VCC is considered OFF
VCC5	Main 5V Power Supply
VCC12	1.2V core supply (external)

7 Related Documents

- S6J3310/S6J3320/S6J3330/S6J3340 Series 32-bit Microcontroller Traveo Family Datasheet
- S6J3200 Series 32-bit Microcontroller Traveo™ Family Datasheet
- AN220402 – Traveo Family MCUs: Power Supply Drop Below Minimum Supply Voltage Level But Above Vreset
- AN220401 – Traveo Family MCUs: Power Supply Drop Above VCCmin and Supply Monitor Detection Level
- AN220338 – Traveo Family MCUs: Intended Power Cycles
- AN220339 – Traveo Family MCUs: Unintended Power Cycles

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