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CE216048 – FM0+ Base Timer PPG

This application uses a programmable pulse generator, implemented in a Base Timer, to drive an LED.

Overview

This example uses the Base Timer (BT) in PPG mode. The PPG peripheral generates a duty cycle by counting down from two 16-bit values: one for the low signal, and the second for the high signal. When the low count reaches zero the signal changes to high. The timer then counts down from the high value. When that count expires, the signal changes to low, the underflow interrupt occurs, and the process repeats. The output pin for the BT_PPG is connected to the blue LED. The LED brightness varies with the PPG duty cycle.

In this application the high pulse (LED off) has a fixed duration and the low pulse duration is varied from 0 to 20% of the high pulse, creating a breathing LED effect.

Requirements

Tool: PSoC Creator 4.0

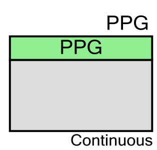
Programming Language: C (GCC 4.9.3)

Associated Parts: All S6E1A and S6E1C parts

Related Hardware: FM0-V48-S6E1A1 and FM0-64L-S6E1C3

Design

The schematic includes the PPG Timer Component, which is the Base Timer configured as a PPG.



The firmware performs following functions:

1. Route the TIOA signal from the Base Timer to the LED pin
2. Initialize the PPG component
3. Set the initial low and high pulse durations
4. Enable counting
5. Trigger the PPG (start)
6. The interrupt modifies the low width duration periodically

Design Considerations

Underflow Interrupt

You set the low and high pulse widths with the Bt_Ppg_WriteLowWidthVal() and Bt_Ppg_WriteHighWidthVal() functions respectively. The actual timer count for each value (low and high) is the value passed to the function plus 1. For example, if you pass 0 as a value, the actual pulse width is equal to one count clock cycle.

The underflow interrupt occurs when the signal level changes from high to low. It does not occur when the signal level changes from low to high. As a result it occurs once per duty cycle.

PDL Installation

The project assumes that you have installed the PDL in the location specified in the **Project Management** panel of the **Tools** > **Options** dialog. If that location is incorrect you will see the build error "The given PDL path is invalid. Unable to find required PDSC file." To correct this problem in a newly-created project open the **Project** > **Properties** dialog and enter the correct path to the PDL. To avoid the problem in projects you create in the future, make sure you put the correct path in the **Tools** > **Options** dialog.

Hardware Setup

Table 1 lists the pin connections required to use this code example on FM0+ kits.

Note that the PPG drives the TIOA signal, which is routed to a pin in firmware. On the FM0-64L-S6E1C3 kit this signal is routed directly to the blue LED on the board. On the FM0-V48-S6E1A1 kit the TIOA signal cannot be routed to a pin with an LED. As a result it is necessary to use alternative means of viewing the output, for example, by connecting up an LED on a breadboard. On the FM0-V48-S6E1A1 kit, P3F is available on header CN5.11.

Table 1. List of Pins

Pin	FM0-V48-S6E1A1	FM0-64L-S6E1C3
PPG:TIOA	P3F	P3F

Components

Table 2 lists the PSoC Creator Components used in this example, as well as the hardware resources used by each.

Table 2. List of PSoC Creator Components

Component	Version	Hardware Resources
PDL_BT as a PPG	1.0	BT block, 1 GPIO pin

Parameter Settings

The PPG Component uses default parameter settings, with these exceptions.

Table 3: Component Settings

Tab	Setting	Value
Basic	BTConfig	PPG
	ConnectTIOA	True
Interrupts	bPpgUnderflowIrq	True
	pfnPpgUnderflowIrqCb	PpgUnderflowIrqCb
	bTouchNvic	True

The ConnectTIOA parameter controls the visibility of PPG:TIOA in the Pin editor. If you are not driving the PPG output off-chip, leave this parameter as false so that the pin can be used for another function.

Operation

Program the kit and observe the blue LED change from dim to bright, and back, as the PPG duty cycle changes over the course of a few seconds.

On the FM0-V48-S6E1A1 kit you will need to connect up an LED on a breadboard as described in Hardware Setup, above.

Related Documents

Table 4 lists relevant application notes, code examples, knowledge base articles, device datasheets, and Component datasheets.

Table 4. Related Documents

PSoC Creator Component Datasheets	
PDL_BT	Supports PWM, PPG, PWC, and RT modes, with interrupts appropriate to the mode of operation. Right-click the Component to access.
Device Documentation	
S6E1A	FM0+ S6E1A-Series 5V Robust ARM® Cortex®-M0+ Microcontroller (MCU) Family
S6E1C	FM0+ S6E1C-Series Ultra Low Power ARM® Cortex®-M0+ Microcontroller (MCU) Family
Development Kit (DVK) Documentation	
FM0-V48-S6E1A1	ARM® Cortex®-M0+ FM0+ MCU Evaluation Board
FM0-64L-S6E1C3	ARM® Cortex®-M0+ MCU Starter Kit with USB and Digital Audio Interface

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5373076	YFS	09/22/13	New Code Example.
*A	5775270	YFS	6/15/17	Added search keyword so that user can quickly find Code Examples from the component instance popup menu. Updated logo and copyright date.
*B	5987626	YFS	12/7/17	Removed S6E1B support.

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