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Cypress Semiconductor
Product Qualification Report

QTP# 044403
July 2013

72 Meg Synchronous SRAM Family Technology R9T-3R, Fab4	
CY7C1470V25/BV25 CY7C1472V25/BV25 CY7C1474V25/BV25	72-Mbit (2M x 36/4M x 18/1M x 72) 2.25V Pipelined SRAM with NoBL™ Architecture
CY7C1471V25/BV25 CY7C1473V25/BV25 CY7C1475V25/BV25	72-Mbit (2M x 36/4M x 18/1M x 72) 2.25V Flow-Through SRAM with NoBL™ Architecture
CY7C1480V25/BV25 CY7C1482V25/BV25 CY7C1486V25/BV25	72-Mbit (2M x 36/4M x 18/1M x 72) 2.25V Pipelined Sync SRAM
CY7C1481V25/BV25 CY7C1483V25/BV25	72-Mbit (2M x 36/4M x 18/1M x 72) 2.25V Flow-Through SRAM
CY7C1484V25/BV25 CY7C1485V25/BV25	72-Mbit (2M x 36/4M x 18) 2.25V Pipelined DCD Sync SRAM
CY7C1470V33/BV33 CY7C1472V33/BV33 CY7C1474V33/BV33	72-Mbit (2M x 36/4M x 18/1M x 72) 3.3V Pipelined SRAM with NoBL™ Architecture
CY7C1471V33/BV33 CY7C1473V33/BV33 CY7C1475V33/BV33	72-Mbit (2M x 36/4M x 18/1M x 72) 3.3V Flow-Through SRAM with NoBL™ Architecture
CY7C1480V33/BV33 CY7C1482V33/BV33 CY7C1486V33/BV33	72-Mbit (2M x 36/4M x 18/1M x 72) 3.3V Pipelined Sync RAM
CY7C1481V33/BV33 CY7C1483V33/BV33	72-Mbit (2M x 36/4M x 18/1M x 72) 3.3V Flow-Through SRAM
CY7C1484V33/BV33 CY7C1485V33/BV33	72-Mbit (2M x 36/4M x 18) 3.3V Pipelined DCD Sync SRAM

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

Zhaomin Ji
Principal Reliability Engineer
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Mira Ben-Tzur
Quality Engineering Director
(408) 943-2675

PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
033302	New Technology R9T-3R, Fab 4, and New Device CY7C137*/138*E (18Meg) Synchronous Product Family	Sept 04
044403	New Device CY7C147*/7C148* AC (72Meg) Device Family, R9T-3R Technology @ Fab4	Nov 04
071001	New Mask change to fix Single Event Latch-up on 72Meg Device Family, R9T-3R @Fab4	Jun 07

Cypress products are manufactured using qualified processes. The technology qualification for this product is referenced above and must be considered to get a complete and thorough evaluation of the reliability of the product.

PRODUCT DESCRIPTION (for qualification)	
Qualification Purpose:	Qualify CY7C147*E/148*A Synchronous product family in qualified technology R9T-3R, Fab 4
Marketing Part #:	CY7C1470/2/4BV25, CY7C1471/3/4BV25, CY7C1481/3BV25, CY7C1484/5BV25, CY7C1480/2/6BV25, CY7C1470/2/4BV33, CY7C1471/3/4BV33, CY7C1480/2/6BV33, CY7C1481/3BV33, CY7C1484/5BV33
Device Description:	2.5V, 3.3V, Commercial
Cypress Division:	Cypress Semiconductor Corporation –Memory & Image Division (MID)

TECHNOLOGY/FAB PROCESS DESCRIPTION – R9T-3R			
Number of Metal Layers:	3	Metal Composition:	Metal 1: 150Å Ti /3200Å Al / 300Å TiW Metal 2: 150Å Ti /6000 Å Al / 300Å TiW Metal 3: 150Å Ti / 8,000Å Al / 300Å TiW
Passivation Type and Materials:		1000Å Oxide TEOS / 9000Å Nitride	
Generic Process Technology/Design Rule (□-drawn):		CMOS, Triple Metal, 90 nm	
Gate Oxide Material/Thickness (MOS):		Nitridized SiO_2, Thin GOX 20A, Thick GOX, 58A	
Name/Location of Die Fab (prime) Facility:		Cypress Semiconductor -- Bloomington, MN	
Die Fab Line ID/Wafer Process ID:		Fab4/R9T-3R	

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
100-Lead TQFP	**CML-RA, JT-CHINA,**
165/209-Ball FBGA	**TAIWAN-G**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	A100
Package Outline, Type, or Name:	100-Lead Thin Quad Flat Pack (TQFP)
Mold Compound Name/Manufacturer:	Hitachi CEL 9200HF9-U (V80)
Mold Compound Flammability Rating:	N/A
Oxygen Rating Index:	N/A
Lead Frame Material:	Copper Alloy 194
Lead Finish, Composition / Thickness:	Ni-40um, Pd-0.8um, Au-0.1 to 0.6um
Die Backside Preparation Method/Metallization:	Grinding
Die Separation Method:	Step-Cut
Die Attach Supplier:	Dexter
Die Attach Material:	QMI 509 Snap Cure
Die Attach Method:	Silver Epoxy
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0 mil
Thermal Resistance Theta JA °C/W:	16.8°C/W
Package Cross Section Yes/No:	N/A
Name/Location of Assembly (prime) facility:	Cypress Philippines (CML-R)
MSL Level	3
Reflow Profile	260C

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	CML-R, GO-TAIWAN, KY-TAIWAN

Note: Please contact a Cypress Representative for other packages availability

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max (Core) = 2.2V, 150°C Dynamic Operating Condition, Vcc Max (Core) = 2.25V, 150°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max (Core)=2.25V, 150°C	P
High Temperature Steady State Life	Static Operating Condition, Vcc Max= 2.25V, 150°C	P
Low Temperature Operating Life	Dynamic Operating Condition, Vcc = 6.50V, -30°C	P
High Accelerated Saturation Test (HAST)	130°C, 3.63V, 85%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow, **260°C**+0, -5°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow, **260°C**+0, -5°C	P
Pressure Cooker	121°C, 100%RH, 15 Psig Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow**, 260°C**+0, -5°C	P
High Temperature Storage	150□C ± 5°C, no bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V JEDEC EIA/JESD22-A114-B	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V JESD22-C101C	P
Current Density	Meets the Technology Device Level Reliability Specifications	P
Age Bond Strength	200°C, 4HRS MIL-STD-883, Method 883-2011	P
Acoustic Microscopy	J-STD-020	P
Dynamic Latch up	In accordance with JESD78	P
Static Latch up	125C, ± 200/300mA In accordance with JESD78	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate	1,391 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	594,000 DHRs	0	0.7	170	9 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 033302

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC-MSL3							
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	COMP	15	0	
CY7C1470V33 (7C1470A)	4321389	*610417280*	CML-R	COMP	15	0	
CY7C1470V33 (7C1470A)	4323794	*610348235*	TAIWN-G	COMP	15	0	
STRESS: AGE BOND STRENGTH							
CY7C1370DV33 (7C1370E)	4421235	*610447674*	CML-R	COMP	5	0	
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	COMP	5	0	
CY7C1370DV33 (7C1370E)	4410258	*610437891*	CML-R	COMP	5	0	
STRESS: BALL SHEAR							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	10	0	
STRESS: BOND PULL							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	10	0	
STRESS: DYNAMIC LATCH-UP							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	3	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	3	0	
CY7C1370DV33 (7C1370E)	4345377	*610417723*	CML-R	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	9	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	9	0	
CY7C1370DV33 (7C1370E)	4421235	*610446833*	CML-R	COMP	9	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	9	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	9	0	
CY7C1370DV33 (7C1370E)	4345377	*610417723*	CML-R	COMP	9	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C, no bias							
CY7C1470V33 (7C1470A)	4323794	*610348234*	TAIWN-G	500	47	0	
CY7C1470V33 (7C1470A)	4323794	*610348234*	TAIWN-G	1000	47	0	

Reliability Test Data

QTP #: 033302

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 2.25V, Vcc Max (Core)							
CY7C1370DV33 (7C1370E)	4345377	*610424939*	CML-R	48	193	0	
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	48	951	0	
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	48	1246	0	
CY7C1370DV33 (7C1370E)	4410258	*610437891*	CML-R	48	1382	1	Non-Visual
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 2.25V, Vcc Max (Core)							
CY7C1370DV33 (7C1370E)	4345377	*610424939*	CML-R	500	170	0	
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	500	400	0	
CY7C1370DV33 (7C1370E)	4410258	*610437891*	CML-R	500	400	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 2.25V, Vcc Max							
CY7C1470V33 (7C1470A)	4405088	*610418824*	TAIWN-G	80	85	0	
CY7C1470V33 (7C1470A)	4405088	*610418824*	TAIWN-G	168	85	0	
STRESS: INTERNAL VISUAL							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	5	0	
STRESS: LOW TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, -30C, 6.50V, Vcc							
CY7C1470V33 (7C1470A)	4333765	*610349455*	CML-R	500	45	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	168	50	0	
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	168	50	0	
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	168	43	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 3.63V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	128	50	0	
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	128	47	0	
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	128	44	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 7.5V, +/300mA							
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	3	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	3	0	
CY7C1370DV33 (7C1370E)	4345377	*610417723*	CML-R	COMP	3	0	

Reliability Test Data

QTP #: 033302

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	300	50	0	
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	500	49	0	
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	1000	49	0	
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	300	43	0	
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	500	43	0	
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	1000	42	0	
CY7C1470V33 (7C1470A)	4321389	*610417280*	CML-R	300	34	0	
CY7C1470V33 (7C1470A)	4321389	*610417280*	CML-R	500	33	0	
CY7C1470V33 (7C1470A)	4321389	*610417280*	CML-R	1000	33	0	
STRESS: THERMAL SHOCK							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	100	46	0	
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	200	46	0	
STRESS: X-RAY							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	15	0	

Reliability Test Data

QTP #: 044403

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC- MSL3							
CY7C1470V33 (7C1470A)	4323794	*610348323*	TAIWN-G	COMP	15	0	
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	15	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	15	0	
STRESS: AGE BOND STRENGTH							
CY7C1370DV33 (7C1370E)	4410258	*610437891*	CML-R	COMP	5	0	
CY7C1470V33 (7C1470A)	4321389	*610354349*	TAIWN-G	COMP	3	0	
CY7C1470V33 (7C1470A)	4323794	*610348235*	TAIWN-G	COMP	3	0	
STRESS: DYNAMIC LATCH-UP							
CY7C1470V33 (7C1470A)	4323794	*610348323*	TAIWN-G	COMP	3	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1470V33 (7C1470A)	4333765	*610349455*	TAIWN-G	COMP	9	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	9	0	
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY7C1470V33 (7C1470A)	4333765	*610349455*	TAIWN-G	COMP	3	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	3	0	
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY7C1470V33 (7C1470A)	4333765	*610349455*	TAIWN-G	COMP	9	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	9	0	
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	9	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 2.25V, Vcc Max (Core)							
CY7C1470V33 (7C1470A)	4423022	*610453316*	TAIWN-G	48	447	0	
CY7C1470V33 (7C1470A)	4425478	*610451858*	TAIWN-G	48	833	0	
CY7C1470V33 (7C1470A)	4425554	*610453022*	TAIWN-G	48	560	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 2.25V, Vcc Max (Core)							
CY7C1470V33 (7C1470A)	4423022	*610453316*	TAIWN-G	500	397	0	
CY7C1470V33 (7C1470A)	4425478	*610451858*	TAIWN-G	500	397	0	
CY7C1470V33 (7C1470A)	4425554	*610453022*	TAIWN-G	500	394	0	

Reliability Test Data

QTP #: 044403

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 2.25V, Vcc Max							
CY7C1470V33 (7C1470A)	4405088	*610418824*	TAIWN-G	80	85	0	
CY7C1470V33 (7C1470A)	4405088	*610418824*	TAIWN-G	168	85	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 3.63V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1470V33 (7C1470A)	4321389	*610417278*	TAIWN-G	128	47	0	
CY7C1470V33 (7C1470A)	4414234	*610446423*	TAIWN-G	128	49	0	
CY7C1470V33 (7C1470A)	4414234	*610446424*	TAIWN-G	128	46	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY7C1470V33 (7C1470A)	4323794	*610348234*	TAIWN-G	500	47	0	
CY7C1470V33 (7C1470A)	4323794	*610348234*	TAIWN-G	1000	47	0	
STRESS: LOW TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, -30C, 6.50V, Vcc							
CY7C1470V33 (7C1470A)	4323794	*610348323*	TAIWN-G	500	45	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1470V33 (7C1470A)	4321389	*610417278*	TAIWN-G	168	43	0	
CY7C1470V33 (7C1470A)	4414234	*610446423*	TAIWN-G	168	50	0	
CY7C1470V33 (7C1470A)	4414234	*610446424*	TAIWN-G	168	51	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 7V, +/300mA							
CY7C1470V33 (7C1470A)	4333765	*610349455*	TAIWN-G	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 7.5V, +/300mA							
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	3	0	
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	3	0	
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1470V33 (7C1470A)	4323794	*610348323*	TAIWN-G	300	48	0	
CY7C1470V33 (7C1470A)	4323794	*610348323*	TAIWN-G	500	48	0	
CY7C1470V33 (7C1470A)	4323794	*610348323*	TAIWN-G	1000	48	0	
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	300	50	0	
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	500	50	0	
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	1000	50	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	300	50	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	500	50	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	1000	50	0	

Reliability Test Data

***QTP #:* 071001**

Device	*Fab Lot #*	*Assy Lot #*	*Assy Loc*	*Duration*	*Samp*	*Rej*	*Failure Mechanism*
STRESS: ACOUSTIC- MSL3							
CY7C1471BV25 (7C14712B)	4708823	*610720982*	CML-R	COMP	15	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1471BV25 (7C14712B)	4708823	*610720982*	CML-R	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY7C1471BV25 (7C14712B)	4708823	*610720982*	CML-R	COMP	8	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 2.2V, Vcc Max							
CY7C1471BV25 (7C14712B)	4708823	*610720982*	CML-R	48	1391	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 4.2V, +/200mA							
CY7C1471BV25 (7C14712B)	4708823	*610720982*	CML-R	COMP	3	0	

History Page

Document Title: QTP#044403: 72 MEG SYNCHRONOUS SRAM FAMILY (CY7C147*/148*) TECHNOLOGY R9T-3R, FAB4
Document Number: 001-62484

Rev.	ECN No.	Orig. of Change	Description of Change
**	2959485	HGA	Initial spec release
*A	4050749	NSR	Added QTP# in the spec title Removed VERSION 5.2 in the title page. Updated Electrical Test Location Removed Obsolete Bond Diagram Spec 10-04921 and Assembly process flow spec 11-21009. Removed reference Cypress specs in the reliability tests performed table.
*B	5373248	JYF DCON	Sunset: No Change Updated Cypress logo with the new tagline, and removed Distribution: WEB and Posting: None in the document history page.