

Hardware Design Guidelines for EZ-PD CCG3PA in Power Adapter Applications

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Associated Part Family: CYPD3174, CYPD3175

Related Application Notes: [AN218179](#), [AN210403](#), [AN200210](#)

AN218238 provides an overview of USB Type-C power adapter applications that EZ-PD™ CCG3PA USB Type-C controllers can support and provides hardware design guidelines. The application note primarily covers the capabilities of EZ-PD CCG3PA USB Type-C controllers and the associated hardware design guidelines for typical power adapter applications like notebook power adapters and mobile power adapters.

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1 Introduction

EZ-PD CCG3PA belongs to Cypress' family of USB Type-C controllers that comply with the latest USB Type-C and Power Delivery (PD) standards. In addition, built-in overvoltage protection (OVP) and overcurrent protection (OCP) help to reduce the need for additional components and the overall cost of a Type-C ecosystem. Typical applications using CCG3PA include mobile power adapters, PC power adapters, power banks, and car chargers.

1.1 EZ-PD CCG3PA Features

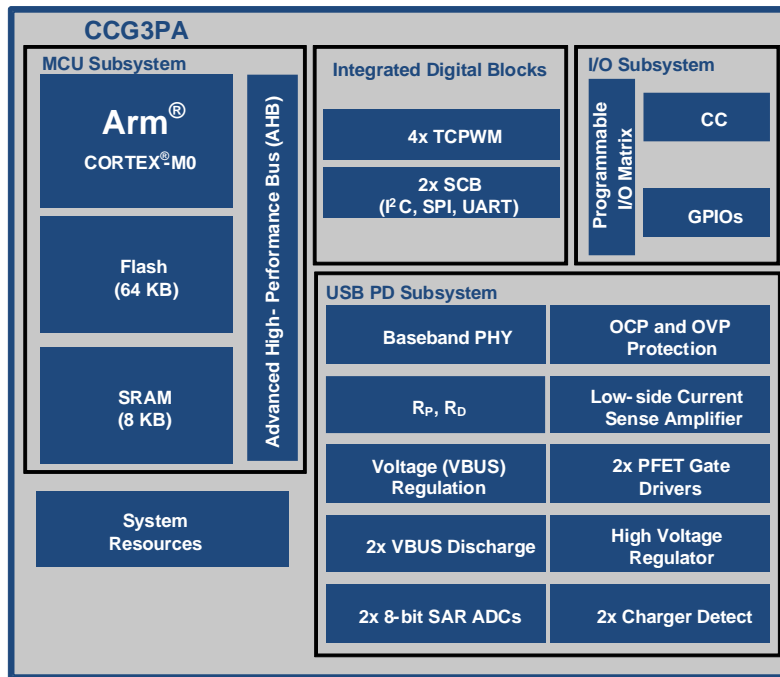
- Type-C Support and USB-PD Support
 - Supports USB PD 3.0 spec including Programmable Power Supply (PPS) Mode
 - Configurable resistors R_P and R_D
 - Supports one USB Type-C port and one Type-A port
- 2x Legacy/Proprietary Charging Blocks
 - Supports Quick Charge (QC) 4.0, Apple Charging 2.4A, Adaptive Fast Charging (AFC), Battery Charging (BC) 1.2
 - Integrates all required termination on DP/DM lines
- System-Level Fault Protection
 - On-chip OVP, OCP, Undervoltage Protection (UVP), and Short Circuit Protection (SCP)
 - Supports Over Temperature Protection (OTP) through an integrated ADC circuit
- 32-bit MCU Subsystem
 - Arm® Cortex®-M0 CPU
 - 64 KB Flash
 - 8 KB SRAM

- Clocks and Oscillators
 - Integrated oscillator eliminating the need for external clock
- Power
 - 3.0 V to 24.5 V operation (30 V tolerant)
- System-Level ESD Protection
 - On Configuration Channel (CC), VBUS, and DP/DM pins
 - ± 8 kV Contact Discharge and ± 15 kV Air Gap Discharge based on IEC61000-4-2 level 4C
- Packages
 - 24-pin QFN and 16-pin SOIC
 - Supports extended industrial temperature range (-40° C to +105° C)

1.2 CCG3PA Block Diagram

Figure 1 shows a block diagram of the CCG3PA architecture. For more details, see the [CCG3PA datasheet](#).

Figure 1. CCG3PA Architecture Block Diagram



1.3 CCG3PA Resources

For Type-C customers who are new to Cypress' existing hardware and software platforms, [Table 1](#) lists the resources that will help in getting started with CCG3PA in their upcoming designs.

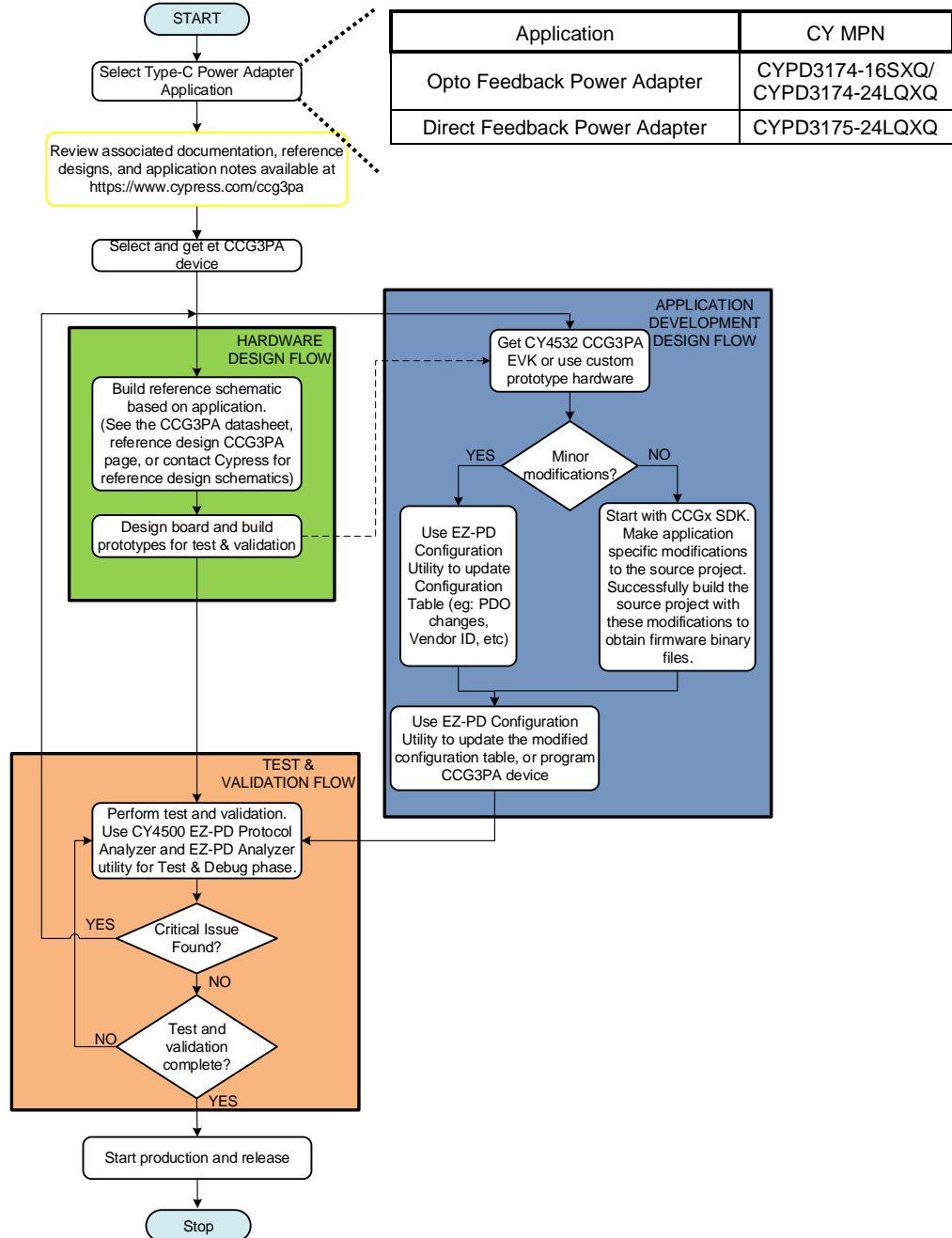
Table 1. CCG3PA Design Resources

Category	Available Resources
Datasheet	CCG3PA datasheet
Hardware	CY4532 CCG3PA EVK – Contains documentation and design files
Programming Specifications Document	CYPD3xxx Programming specifications – Provides guidelines on how to program the flash memory of CCG3PA devices
Host PC Software	EZ-PD CCGx SDK
Host PC Software Debugging Tools	EZ-PD Configuration Utility 1.1 or later (GUI-based Windows application that helps in configuring CCGx controllers)
	PSoC Creator™ 4.1 or later (firmware development tool)
	PSoC Programmer 3.26 or later (firmware programming tool)
	CY4500 EZ-PD™ Protocol Analyzer – Includes EZ-PD Analyzer Utility and documentation
Videos	USB Type-C Essentials , USB Type-C 101 Video Training Series
Other Collateral	CCG3PA specific Knowledge Base Articles
Reference Designs	CCG3PA Reference Designs

1.4 CCG3PA Design Flow

This section describes a typical design flow that you would go through during the Type-C application design from concept to manufacturing using CCG3PA devices. This section also covers how the hardware, software, and firmware resources described in this application note are used in the design flow. Figure 2 shows a typical design flow using CCG3PA devices.

Figure 2. CCG3PA Design Flow



After you determine the CCG3PA-based Type-C application and review the reference designers, you can start the application development phase in parallel.

Hardware development includes building reference schematics based on the end application and designing boards to get a few prototypes ready for the next phase. These reference schematics can be based on the reference designs available on Cypress' CCG3PA [webpage](#).

Application development can begin with the [CY4532 EZ-PD CCG3PA Evaluation Kit \(EVK\)](#), so that it can proceed in parallel with hardware development. You can use the [EZ-PD Configuration Utility](#) to update the configuration table of the CCG3PA device (for example, changing PDOs and Vendor IDs). For making application-specific modifications, you can use the custom CCG3PA FW Package in the [EZ-PD CCGx Software Development Kit \(SDK\)](#).

Once hardware and application development are completed, the existing system design is ready for the test and validation cycle. You can use the [CY4500 EZ-PD Protocol Analyzer](#) for testing, firmware debugging, and performance analysis. Mass production and manufacturing can start once test and validation is complete and the system design is final.

2 Constant Voltage and Constant Current loops

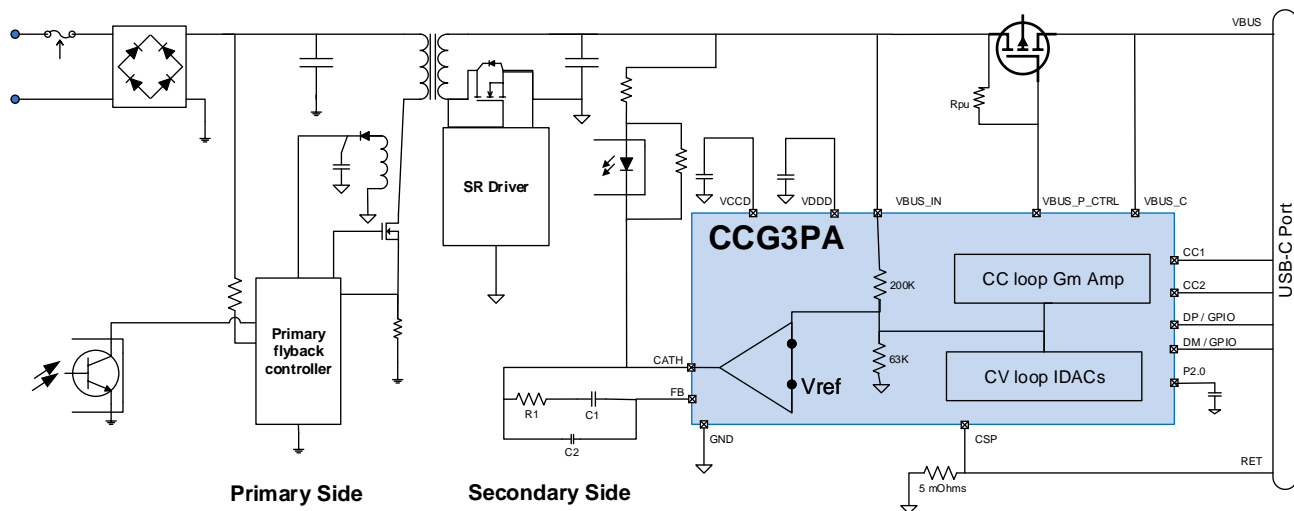
CCG3PA is targeted towards power adapters, car chargers and power bank applications. In these systems, CCG3PA regulates VBUS by providing an appropriate feedback to the upstream AC-DC or DC-DC converter. CCG3PA regulates VBUS in two distinct modes – Constant Voltage (CV) and Constant Current (CC). In CV mode, CCG3PA modulates the feedback to keep the load voltage constant. In CC mode, CCG3PA modulates the feedback to keep the load current constant.

The feedback architecture varies depending on the type of the upstream power converter. Opto feedback and direct feedback are two of the most common feedback systems.

2.1 Opto Feedback System

In most power adapter applications, feedback from the secondary side to the primary fly-back controller is through an opto isolator. In these systems, CCG3PA regulates VBUS by controlling the current drawn through the cathode (CATH) node.

Figure 3. CCG3PA Application Diagram Using Opto Feedback System



- CCG3PA is designed to regulate VBUS in the 3.3 V–20 V range, with a 20-mV step size as needed by the Programmable Power Supply (PPS) specification.
- Default 5 V VBUS is dictated by the reference voltage V_{ref} and the internal resistor divider of 200 k Ω and 63 k Ω .
- The CV loop IDACs can sink up to 102.3 μ A of current and can source up to 12.7 μ A of current.
- Both the IDAC source and sink have a step size of 100 nA. A step change of 100 nA in IDAC current results in a VBUS change of 20 mV.
- The maximum current that can be drawn through the CATH pin is 10 mA.

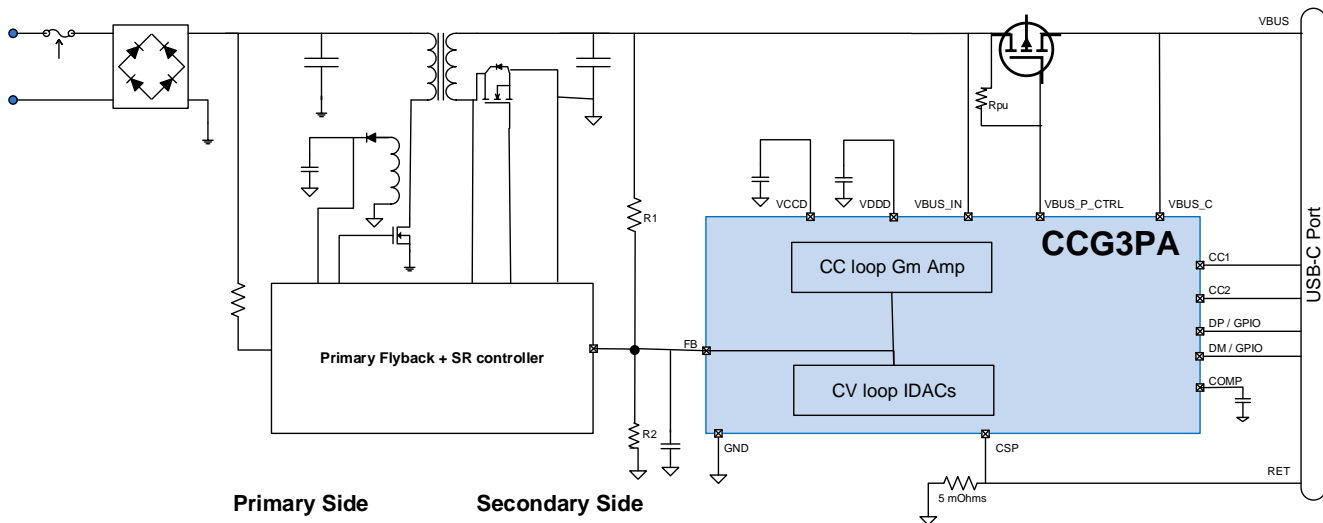
As shown in Figure 3, an external compensation network and a compensation capacitor are needed for CV and CC mode operations respectively. The CV loop compensation network must be designed in conjunction with the rest of the power circuit. The type of compensation network and component values are dependent on the complete power topology; these design choices and trade-offs are beyond the scope of this application note. The compensation network shown in Figure 3 is from the example reference design [CCG3PA USB-C Mobile Power Adapter Solution using Diodes](#); refer to the design schematics for component values.

The CC loop compensation capacitor can be placed on any free GPIO; P2.0 is the recommended pin. P2.0 is the recommended pin for the simple reason that this aligns with the SDK firmware and the reference design hardware. Again, the value of the compensation capacitor varies from design to design. A compensation capacitor of 330 nF is a good starting point for most designs.

2.2 Direct Feedback System

The second most common feedback architecture is a direct feedback system. In these systems, CCG3PA provides feedback to the upstream power converter by modulating the current drawn on the Feedback (FB) pin. CCG3PA sources current on the FB pin to decrease VBUS and sinks current on the FB pin to increase VBUS.

Figure 4. CCG3PA Application Diagram Using Direct Feedback System



- The default VBUS voltage is dictated by external resistor dividers. External resistors R1 and R2 must be chosen such that at 5-V VBUS, without CCG3PA sourcing or sinking any current on the FB pin, the voltage at the feedback node shall be the default feedback voltage expected by the power converter.
- The CV loop IDACs can sink up to 102.3 μA of current and can source up to 12.7 μA of current.
- Both the IDAC source and sink have a step size of 100 nA.
- Depending on the overall power converter design requirements, it is optional to have a filter capacitor at the FB node.

Equation 1 and Equation 2 show the relationship between VBUS, feedback voltage, and resistor dividers:

When CCG3PA is sourcing current to reduce VBUS:

Equation 1

$$V_{FB} = [(V_{BUS} + (I_{src} * R1)) * R2] / (R1 + R2)$$

When CCG3PA is sinking current to increase VBUS:

Equation 2

$$V_{FB} = [(V_{BUS} - (I_{snk} * R1)) * R2] / (R1 + R2)$$

Derived from equations 1 and 2, Equation 3 arrives at the relationship between change in VBUS for a given change in IDAC current:

Equation 3

$$\text{Change in VBUS} = \text{Change in IDAC current} * R1$$

From Equation 3, knowing the default feedback voltage, you can calculate external resistor divider values for a given system. For example, consider a power adapter design with the following requirements:

- VBUS output range is 3.3 V–20 V.
- Default feedback voltage expected by the upstream converter is 1.265 V.
- Should support Programmable Power Supply mode. This means that the system should support a 20 mV step change in voltage across the 3.3 V–20 V range.

With these requirements, let us go through the steps to calculate the required feedback resistors R1 and R2:

1. First, choose the top resistor R1 such that a delta current change of 100 nA produces a proportional 20 mV delta change in VBUS. From Equation 3:

$$R1 = 20 \text{ mV} / 100 \text{ nA} = 200 \text{ k}\Omega$$

2. Knowing R1 and the default feedback voltage as 1.265 V, you can calculate R2. The requirement is that at 5-V default VBUS, voltage at the feedback node must be 1.265 V. Solving the following equation gives R2 = 68 k Ω .

$$1.265 \text{ V} = (5 \text{ V} * R2) / (R1 + R2)$$

3. As the last step, make sure that with the chosen R1, VBUS can be regulated in the required output voltage range with the available IDAC source and sink currents.

From Equation 3, with R1 200 k Ω , to increase VBUS from 5 V to 20 V, the required IDAC current sink is $15 \text{ V} / 200 \text{ k}\Omega = 75 \mu\text{A}$. Similarly, to reduce VBUS from 5 V to 3.3 V, the required IDAC current source is $1.7 \text{ V} / 200 \text{ k}\Omega = 8.5 \mu\text{A}$. Both the requirements are well within the available IDAC range.

Along with external resistor dividers, this design also needs a CC loop compensation capacitor. Place the compensation capacitor on the dedicated pin COMP. As discussed earlier, the value of the compensation capacitor varies from design to design. A compensation capacitor of 100 nF is a good starting point for most designs. See [CCG3PA USB-C Mobile Power Adapter Solution using Power Integrations](#) for an example reference design.

2.3 PWM Feedback and Other Systems

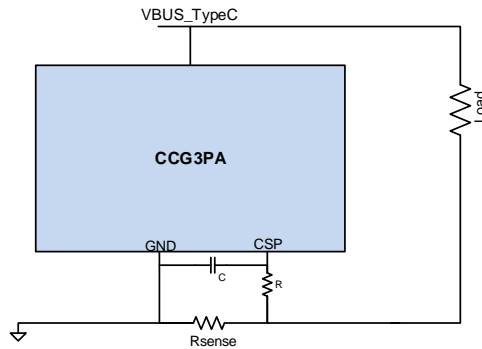
In addition to opto and direct feedback systems, there are other power converters that regulate VBUS based on a PWM input or a serial communication interface. CCG3PA can also work with these converters. There are no specific design considerations here and it is not pursued further in this application note. See [CY4532 EZ-PD™ CCG3PA Evaluation Kit](#) for an example reference design.

3 PCB Layout Guideline – Current Sense Path

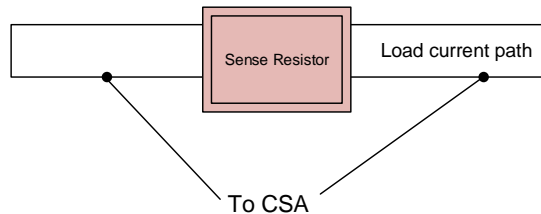
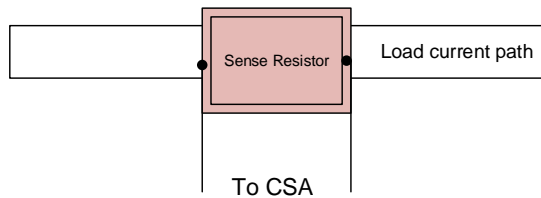
CCG3PA integrates a Low Side Current Sense Amplifier (LSCSA), which plays a key role in the Constant Current mode of operation and the overcurrent fault detection. This section covers the design recommendations for the current sense path.

- Suggested value for Rsense is 5 m Ω .
- It is recommended to place a low-pass filter at the current sense input. Note that the RC filter is a requirement only if the current sense path is noisy and needs to be filtered out. It is a good idea to have this filter during the prototype phase of the hardware design. Depending on test results and hardware optimization, you can choose to remove the RC filter in the final hardware design.

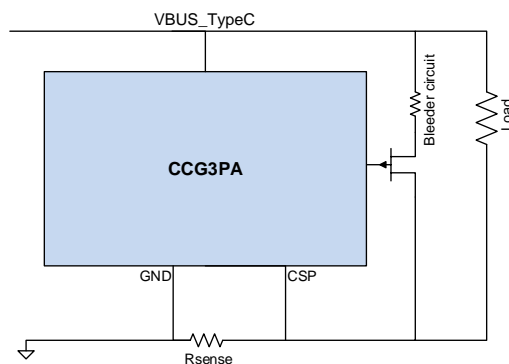
Figure 5. Current Sense RC Filter



- Use Kelvin sense lines for wiring R_{sense} . Sense lines should connect directly to sense resistor terminals; traces should be symmetrical and have the same length and thickness. See [Figure 6](#) to [Figure 9](#) as a reference for correct and incorrect R_{sense} wiring.

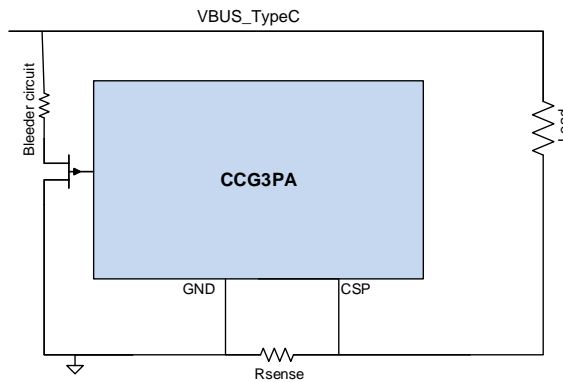
 Figure 6. R_{sense} Not Following Kelvin Connection

 Figure 7. R_{sense} Following Kelvin Connection


- During the schematic and layout phase, ensure that the only current flowing through the sense resistor is the load current and there are no parallel current paths. For example, consider that the design needs a bleeder circuit from the secondary output under certain operating conditions. Hooking up the bleeder circuit as shown in [Figure 8](#) leads to inaccurate CC mode operation as the current through the bleeder circuit inadvertently offsets the target load current.

 Figure 8. Incorrect R_{sense} Wiring


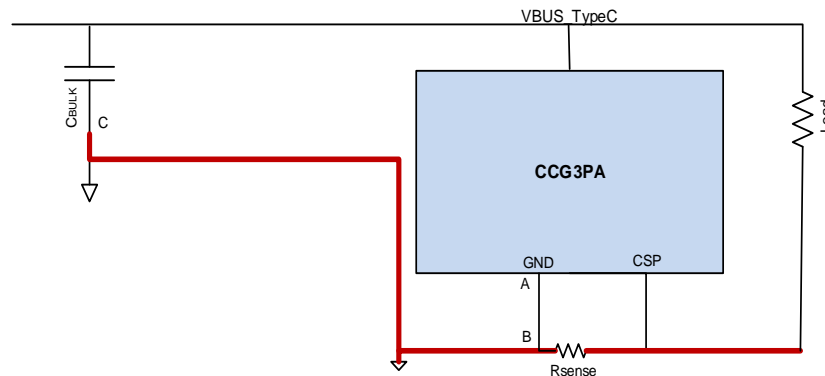
See [Figure 9](#) for the suggested way to hook up the same circuit without it impacting the CC mode accuracy.

Figure 9. Correct Rsense Wiring



- Ensure that the load current path and ground connections follow the necessary layout routing guidelines as shown in [Figure 10](#). The trace highlighted in red should be kept as short and wide as feasible. Also, ensure that all CCG3PA bypass capacitors are ground referenced to point A.

Figure 10. CSA Layout Routing



4 VBUS Discharge

CCG3PA supports VBUS discharge capability on both VBUS_IN and VBUS_TypeC ends (before and after the provider FET respectively). VBUS_IN discharge is via the VBUS_IN_DISCHARGE pin, while VBUS_TypeC discharge is via the VBUS_C_MON_DISCHARGE pin. The discharge FET and resistors are internal to CCG3PA and no external components are needed for either discharge path. See application block diagrams [Figure 3](#) and [Figure 4](#) for discharge path connections.

Discharge drive strength is configurable in both the VBUS_IN and VBUS_TypeC discharge paths. The internal discharge resistor can be set in the range of 31.25 Ω to 2000 Ω .

5 CC and D+/D- Terminations

CCG3PA supports termination needed on the CC line for Type-C power delivery. The only external component needed is a 390-pF capacitor on each of the CC lines (CC1 and CC2). CCG3PA also has the required termination on the D+/D- lines to support legacy charging protocols such as BC1.2, Samsung AFC, Apple Charging, and Qualcomm Charging. CCG3PA supports two pairs of D+/D- lines, which can be useful in dual port charging systems.

For more information on the legacy protocols supported, see the [CCG3PA datasheet](#).

6 PFET Gate Drivers

CCG3PA integrates two PFET gate drivers – one each for VBUS provider and consumer paths. VBUS_P_CTRL and VBUS_C_CTRL are the two PFET gate driver pins. An external pull-up resistor is needed for each gate driver circuit. This is shown as R_{PU} in [Figure 3](#) and [Figure 4](#). Because [Figure 3](#) and [Figure 4](#) are for power adapter applications only, the VBUS_C_CTRL pin (if available) is left unconnected. VBUS_C_CTRL is a simple pull-down switch where it pulls the line LOW to turn ON the PFET and stays at High-Z to turn OFF the PFET.

VBUS_P_CTRL is similar to VBUS_C_CTRL, but with two additional features:

- You can programmatically control the FET turn-on rate. This feature is intended to limit the in-rush current.
- It also has an internal pull-up resistor, which can be useful to support faster FET turn-off.

7 Generic Guidelines

- Place all the bypass capacitors as close as possible to CCG3PA.
- Ensure CCG3PA is not placed to high frequency switching components in the circuit.

Document History

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**	5969811	MKKU	12/12/2017	New application note.
*A	6227443	MKKU	07/18/2018	Added more design details in section 'Constant Voltage and Constant Current loops Added new section 'PCB Layout Guideline – Current Sense Path Minor edits in other section Updated document title
*B	6519280	MKKU	03/23/2019	Corrected equations 1 and 2. Added additional layout guidelines in Section 3. Added Section 7

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