



EZ-PD™ Dock Reference Design 1.1

Release Notes

Version 1.1.0, June 18, 2018

Thank you for your interest in the EZ-PD™ Dock Reference Design version 1.1. This version of the EZ-PD Dock Reference Design supports Upstream Type-C port supporting DisplayPort sink, power source, and USB device over a USB SuperSpeed hub and Downstream Type-C port supporting DisplayPort source, power source, and USB hub downstream ports.

Introduction

EZ-PD Dock Reference Design is a self-powered dock capable of providing power to both upstream and downstream ports while providing display and USB 3.1 Gen 1 functionality.

EZ-PD Dock Reference Design supports the following:

- Upstream Type-C port capable of providing power up to 60 W at 20 V (extendable to 100 W at 20 V with minor hardware and firmware-configuration changes), USB 3.1 Gen 1 (5 Gbps) data sink, and DisplayPort sink capability to HDMI
- Downstream Type-C port capable of providing power up to 15 W at 5 V, USB 3.1 Gen 1 (5 Gbps) data source, and DisplayPort source capability
- HDMI port for Display output
- Three USB 3.1 Gen 1 legacy Type-A connectors
- Two USB Hi-Speed downstream ports (Legacy Type-A connector)
- RJ45 port to provide Ethernet connectivity
- Billboard support to indicate alternate mode status
- Firmware download support

The reference design also provides a set of firmware resources that allows you to build customized dock/monitor applications using the CCG4 family of Type-C port controllers and Dock Management Controller (DMC) for the firmware update of various dock components.

CCG4 firmware is based on a CCGx firmware stack, which is tested and proven to be fully compliant with the USB Type-C and USB-PD specifications, and provides programming hooks and interfaces for customers to implement their own policy and system management schemes.

The key application-level features for the CCG4 firmware stack are as follows:

- USB Type-C Revision 1.2 and USB-PD Revision 3.0 specification compliant PD stack
- Docking Application support with one USB-PD port on the dock upstream and one USB-PD port on the dock downstream, with independent functionality.
- Drivers for various hardware blocks on the CCGx controllers.
- Implementation of a Host Processor Interface (HPI) that allows an external Embedded Controller (EC) to monitor and control the CCGx device operation.
- Implementation of the DisplayPort Alternate Mode that allows transfer of video signals over the Type-C data lanes.



- Allow manufacturing-level customization of device parameters such as power profiles, default port behavior, Over Voltage Protection, and so on, without changing the firmware.
- Map firmware to system hardware design changes without any impact on the core firmware modules.
- Facilitate source-level debugging so that new customers can get familiarized with the stack.

DMC firmware is based on a DMC firmware stack and provides APIs, interfaces, and sample code for customers to implement their own update logic for the custom devices.

The key application-level features for DMC firmware stack are as follows:

- USB device stack that is compliant with the USB 2.0 specification
- Billboard device class support (compliant with the USB Billboard Specification Revision 1.21)
- Implementation of firmware update interface in other components of the dock
- Comprehensive dock status query support
- Implementation of crypto block with support for Secure Hash Algorithm (SHA-256)
- Drivers for various hardware blocks on DMC

The EZ-PD Dock Reference Design 1.1 can support Signed Firmware update (firmware authentication using digital signatures) for all Cypress components supporting firmware update (DMC, CCG4, HX3s).

For more details on the signed firmware capability, contact Cypress (www.cypress.com/support).

Release Package Contents

Figure 1 provides an overview of the EZ-PD Dock *Reference Design* installation.

Figure 1. EZ-PD Dock Reference Design Installation Directory Structure

EZ-PD DOCK REFERENCE DESIGN	
+---Documentation	Documentation: User guide, API guide etc.
+---Firmware	
+---CCG4	CCG4 USB-PD Controller Firmware
+---binaries	CCG4 Firmware binaries with configuration information
+---lib	PD stack libraries
+---projects	CCG4 Reference Project
\---CYPD4236-40LQXI_dock	CCG4 project for CYPD4236-40LQXIT part
\---src	Firmware Stack Sources
+---app	Application layer
+---hpiss	HPI protocol headers
+---pd_common	PD stack headers
+---pd_hal	PD block low level drivers
+---scb	Serial communication block driver
\---system	Low level drivers, firmware update, timer
+---DMC	Dock Management Controller (DMC) Firmware
+---binaries	DMC Firmware binaries with configuration information
+---lib	DMC stack libraries
+---projects	DMC Reference Project
\---CY7C65219-40LQXIT_dmc	DMC project for CY7C65219-40LQXIT part
\---src	Firmware Stack Sources
+---crypto	Low Level Hardware driver for the crypto hardware
+---dmc	Billboard and firmware update implementation for the DMC device, I2C master and HPI master module
+---system	Low level drivers, timer, flash access functions
\---usb	USB drivers
+---HX3_Tier1	Tier 1 HX3 Firmware
\---binaries	Tier 1 HX3 Firmware binaries with settings
\---HX3_Tier2	Tier 2 HX3 Firmware
\---binaries	Tier 2 HX3 Firmware binaries with settings
+---Hardware	EZ-PD Dock Reference Design Hardware files
+---License	EZ-PD Dock Reference Design License Files
+---Software Tools	EZ-PD Dock Tools for firmware update
\---Updater	



EZ-PD Dock Reference Design installation contains the following folders:

- **Documentation:** This folder contains the EZ-PD Dock Reference Design documentation, which includes release notes, dock reference design guide, firmware user guide, and API reference guides.
- **Firmware:** This folder contains the firmware stack sources, pre-compiled libraries, and reference projects for various dock components in the EZ-PD Dock Reference Design.
 - **CCG4** directory contains the firmware for the CCG4 controller to be used in EZ-PD Dock Reference Design
 - **binaries:** This folder contains the pre-built firmware binary for reference design.
 - **lib:** This folder contains the USB-PD stack and HPI module in pre-compiled library format.

Note: The *lib* folder is made available for reference. A copy of the relevant libraries used by the project are added locally to the Reference project.

- **projects:** This folder contains the sources and PSoC Creator™ workspace for the USB-PD controller design based on CYPD4236-40LQXI.
- **src:** This folder contains the sources for the CCGx firmware stack organized by the firmware module.

Note: The *src* folder is made available for reference. A copy of the *src* folder used by the project is added locally to the Reference project.

The *src* folder has the following sub-folders:

- **app:** The *app* folder contains the top-level application layer functionality that implements the required USB-PD controller functions. This includes functionality such as PDO evaluation and contract negotiation, VDM handling for both DFP and UFP roles, handling of control messages such as role swap; and alternate mode discovery and negotiation. The alternate mode specific implementation is in the *app/alt_mode* directory. The *app* folder also includes handlers for legacy charger detection and Type-A port controller detection.
- **hpiss:** This folder contains the header file for the HPI, which is an I2C-based software protocol that allows an external EC to monitor and control the CCGx device operation. HPI provides a register-based interface through which the EC can manage the power contracts, send and receive VDMs, and perform flash read/write operations. Contact Cypress for more details on HPI and its capabilities
- **pd_common:** This folder contains the headers for the core Type-C and USB-PD stack for the CCGx device. This includes the HAL, the Type-C port manager, the USB-PD protocol layer, the USB-PD policy engine, and the Device Policy Manager.
- **pd_hal:** This folder contains the low-level driver header and source files for the USB-PD hardware block.
- **scb:** This folder contains the driver code for I2C slave mode operation using the Serial Controller Blocks (SCB) on the CCGx device. Since I2C slave mode is the most commonly-used interface for CCGx, a specially optimized driver is provided for the same.
- **system:** This folder contains header and source files relating to the CCGx device hardware and registers, bootloader and flash access functions, low-level drivers for the GPIO blocks on the CCGx device, and a soft timer implementation used by the firmware stack.

Note: CYPD4236-40LQXI_dock is intended to work on the CCG4 Dock Reference Design board and is targeted for CYPD4236-40LQXI silicon part.

- *DMC* directory contains the firmware for the Dock Management Controller.
 - *binaries*: This folder contains the pre-built firmware binary for reference design.
 - *lib*: This folder contains the firmware update state machine, HPI master module, HX3 firmware update support, and CCGX firmware update support in pre-compiled library format.
Note: The *lib* folder is made available for reference. A copy of the relevant libraries used by the project are added locally to the Reference project.
 - *projects*: This folder contains the sources and PSoC Creator workspace for DMC.
 - *src*: This folder contains the sources for DMC firmware stack organized by the firmware module.
Note: The *src* folder is made available for reference. A copy of the *src* folder used by the project is added locally to the Reference project.
The *src* folder has the following sub-folders:
 - *crypto*: This folder contains the Hardware Abstraction Layer (HAL) or the low-level hardware driver for the crypto hardware in DMC. The driver functionality includes crypto block initialization, SHA-256 calculation code, crypto block de-initialization
 - *dmc*: This folder contains the Billboard and firmware update implementation for DMC. This also includes the wrapper for SHA-256 module. In addition, the folder provides I2C master module for providing driver level access to multiple SCB components and HPI master to communicate with CCGx controllers.
 - *system*: This folder contains header and source files relating to DMC device hardware and registers, flash access functions, low level drivers for the GPIO blocks on DMC, and soft timer implementation.
 - *usb*: This folder contains header and source files relating to the hardware and registers of USB-FS PHY present within DMC. The folder also contains handler for reading and writing to EP0 and non-EP0 endpoints.

Note: The CY7C65219-40LQXIT_dmc project is intended to work on the CCG4 Dock Reference Design board and is targeted for the CY7C65219-40LQXIT silicon part.

- *Hardware* directory includes reference schematic, BOM, and layout files.
- *License* directory includes the Cypress Software and End User License Agreements.
- *Software Tools* directory includes the following tools:
 - EZ-PD Dock DMC Configuration Generation Tool, Version 1.0.0.13: This tool (ezpd_dockconfiguredmc.exe) can be used to create DMC images with modified configuration information.
 - EZ-PD Dock Image Creation Tool, Version 1.0.3.2: This tool (ezpd_dockcreateimage.exe) is used to create a single combined firmware image file, referred to as the composite dock image (.bin) from firmware files of components present in the dock.
 - EZ-PD Dock Firmware Update Tool, Version 1.0.3.7: This tool (ezpd_dockupdatefw.exe) is a WinUSB-based application that runs on Windows systems. This tool updates firmware for devices in the dock and reports the final consolidated status. This tool takes the files generated using the EZ-PD Dock Image Creation Tool as input and initiates a firmware update.

The EZ-PD Dock Reference Design installer also includes the following additional tools for configuring CCG4 and HX3 firmware images shipped as part of this design:

- CCG4 Configuration: EZ-PD Configuration Utility with support for CYPD4236-40LQXI part
- HX3 Configuration: HX3 Blaster Plus utility



For additional details on firmware, tools, and usage instructions, see the *EZ-PD Dock Reference Design Guide*.

Limitations and Known Issues with Software Tools

Maximum number of devices that can be added to the dock topology is limited to seven (against eight that is supported by the firmware) due to a limitation in EZ-PD Dock Firmware Update Tool, Version 1.0.3.7. This issue will be fixed in the future releases of the tool.

Other Limitations and Known Issues

When firmware upgrade is attempted from a Thunderbolt™ 3 host, the EZ-PD Dock may not enumerate after completing the firmware upgrade successfully. EZ-PD Dock needs to be disconnected from the host and reconnected to recover.

Note: EZ-PD Dock firmware update mechanism causes a self-reset of all dock components after completing the firmware update to enable the newly downloaded firmware to take effect. This results in disconnection and reconnection of the EZ-PD Dock with the host and the host needs to enumerate the dock again. It was found that the above-mentioned issue observed with Thunderbolt hosts can be eliminated by introducing a delay of 30 seconds in the EZ-PD dock firmware between the disconnection and reconnection events so that the Thunderbolt host can reload the driver properly. The EZ-PD Dock CCG4 firmware provides a compile time option to introduce a configurable delay which can be used to eliminate this issue. See the `ENABLE_HPI_SOFTRESET_DELAY` macro in the *EZ-PD Dock Firmware User Guide* for more details.

Note: Enabling the macro and introducing the delay in the EZ-PD dock CCG4 firmware will cause DMC to re-enumerate after the configured delay. This would require the EZ-PD Dock Firmware Update Tool re-enumeration timeout also to be set to a value equal to the delay (at the least) set in the CCG4 firmware. See the tool context help for more details on the re-enumeration timeout parameter.



CYPD4236-40LQXI Firmware Release Notes

This section describes the CYPD4236-40LQXI firmware, which is part of the EZ-PD Dock Reference Design version 1.1 release. This section also describes key updates and known issues.

Introduction

EZ-PD CCG4 is a dual USB Type-C controller that complies with the latest USB Type-C and PD standards. EZ-PD CCG4 provides a complete dual USB Type-C and USB-Power Delivery port control solution for notebooks, power adapters, and docking stations. It can also be used in dual role and downstream facing port applications. EZ-PD CCG4 uses Cypress' proprietary M0S8 technology with a 32-bit, 48-MHz Arm[®] Cortex[®]-M0 processor with 128 KB flash and integrates two complete Type-C Transceivers including the Type-C termination resistors RP and RD.

The CYPD4236-40LQXI device is a dual port version of CCG4, which supports all other device feature enhancements over previous versions of Cypress Type-C controllers. This device supports USB-PD protocol revision 3.0 specification.

Here are some key application-level requirements:

- Integrated dual-port USB-PD controller as per PD 3.0 specification.
- Integrated Rp, Rd resistor on CC1/2 pins.
- Integrated system level ESD protection for exposed pins.
- Integrated boot loader to support firmware update over I2C.
- Integrated VCONN FETS to provide power to EMCA cables.
- Support for USB-PD extended messages.

Firmware Features (version 3.2.1.1652 md.1.0.3)

This version of the CYPD4236-40LQXI firmware supports the following key application-level features:

- USB-PD Protocol as per PD 3.0 specification.
- Two USB-PD ports.
- Docking Application support with one USB-PD port on the dock upstream and one USB-PD port on the dock downstream, with independent functionalities.
- USB-PD power contract negotiation as provider or consumer for upstream port and as provider for downstream port.
- Support for VBUS Over-Voltage protection on both PD ports.
- Support for VBUS Over-Current protection based on external current limited load switch.
- Support for DisplayPort alternate mode sink with PS8742B MUX for data path switching between USB-SS and DisplayPort on the upstream port.
- Support for DisplayPort alternate mode source with PI3USB30532ZLE MUX for data path switching between USB-SS and DisplayPort on the downstream port.
- I2C-based interface for status reporting and configuration updates from an EC in the system.
- Capability of in-system firmware upgrade through the I2C interface from EC.
- Capability to update USB-PD profiles and change operating conditions through the I2C interface from EC.
- USBPD extended messages support.

Default Device Configuration

Table 1. Configuration Settings

Port	Parameter	Supported Settings
Upstream	Source PDOs	5 V @ 3.0 A, 9 V @ 3.0 A, 15 V @ 3.0 A, 20 V @ 3.0 A
	Sink PDOs	5 V @ 0 A
Downstream	Source PDOs	5 V @ 3.0 A
	Sink PDOs	-

Default SVDM Response

When the CYPD4236-40LQXI device functions as a UFP device, it will provide the following responses for the structured vendor defined message (SVDM) requests.

DISCOVER_ID Response

Upstream Port: 0xFF008041, 0x6C0004B4, 0x00000000, 0xF6D10000, 0x00000001

Downstream Port: 0xFF008041, 0x820004B4, 0x00000000, 0xF6D20000

Table 2. DISCOVER_ID Response Details

Bits	Description	Upstream Port	Downstream Port
VDM Header			
B31..16	Standard or Vendor ID (SVID)	0xFF00	0xFF00
B15	VDM Type	1b	1b
B14..13	Structured VDM Version	00b	00b
B12..11	Reserved	00b	00b
B10..8	Object Position	000b	000b
B7..6	Command Type	01b	01b
B5	Reserved	0b	0b
B4..0	Command	00001b	00001b
ID Header			
B31	Data Capable as USB Host	0b	1b
B30	Data Capable as a USB Device	1b	0b
B29..27	Product Type (UFP)	101b	000b
B26	Modal Operation Supported	1b	0b
B25..23	Product Type (DFP)	000b	100b
B22..16	Reserved. Shall be set to zero.	0x0	0x0
B15..0	16-bit USB Vendor ID	0x04B4	0x04B4



Bits	Description	Upstream Port	Downstream Port
Cert Stat VDO			
B31..20	Reserved, shall be set to zero.	0	0
B19..0	20-bit unsigned integer	0	0
Product VDO			
B31..16	USB Product ID	0xF6D1	0xF6D2
B15..0	bcdDevice	0x0000	0x0000

DISCOVER_SVID Response

Upstream Port: 0xFF008042, 0xFF010000

DISCOVER_MODES Response

Upstream Port: 0xFF018043, 0x001C0045

Limitations and Known Problems of CCG4 Firmware

None



CY7C65219-40LQXI Firmware Release Notes

This section describes the CY7C65219-40LQXI Dock Management Controller (DMC) firmware, which is part of the EZ-PD Dock Reference Design 1.1 release. This section also describes key features and known issues.

Introduction

The CY7C65219-40LQXI DMC is a USB Controller that is specifically designed for managing dock and monitor solutions. DMC provides USB full-speed capability to support latest USB Billboard device class and supports signed and unsigned firmware download over USB to other controllers on the dock or monitor solution. DMC is implemented on Cypress' proprietary M0S8 platform integrating a 32-bit, 48-MHz CM0 processor, dual 64 KB flash, and integrates SHA2 capability in a 40-pin QFN package. DMC meets all key requirements; low manufacturing cost, small package, integration of key features, and 128 KB flash.

The CY7C65219-40LQXI device is a new addition to the USB product family which supports USB Billboard and signed and unsigned firmware download functionalities. By "signed firmware download" it is implied that the controller verifies the authenticity of any firmware downloaded to the dock components and prevents malicious firmware or configuration information from being downloaded into any of the dock components over USB. This device supports USB Billboard class revision 1.21 specification.

Here are some key application-level requirements:

- Integrated full-speed USB controller as per USB 2.0 specification.
- Integrated USB Billboard controller as per USB Billboard v1.21 specification.
- Firmware download functionality to Cypress dock components such as CCG4, HX3, and DMC.

Firmware Features (version 3.1.1.1424 dm.1.1.0)

This version of the CY7C65219-40LQXI firmware supports the following key application-level features:

- USB Billboard specification support as per Billboard 1.21 specification.
- Unsigned firmware download support for CCG4, HX3, and DMC
- Comprehensive dock status querying and version reporting for components of dock such as CCG4, HX3, and DMC.
- Recovery of HX3 firmware in case of update failure or corrupted firmware update.

Prerequisites

At manufacturing, the HX3 needs to have a valid firmware programmed into the EEPROM and be capable of enumeration to allow DMC to enumerate before firmware updates can be done over USB.

Valid DMC firmware (including an updated dock topology table which reflects the customer design) should be programmed to DMC before attempting to flash any of the other dock components using DMC.

Limitations and Known Problems of DMC Firmware

None



CYUSB3314-88LTXC Firmware Release Notes

This section describes the details of the HX3 firmware images, which are part of the EZ-PD™ Dock Reference Design version 1.1 release. The section also describes the key features and known issues.

Introduction

HX3 is a family of USB 3.0 hub controllers compliant with the USB 3.0 specification revision 1.0. HX3 supports SuperSpeed (SS), Hi-Speed (HS), Full-Speed (FS), and Low-Speed (LS) on all ports. HX3 has integrated termination, pull-up, and pull-down resistors, and supports configuration options through pin-straps to reduce the overall BOM of the system.

Firmware Features Version

The HX3 hub firmware images for this reference design are stored on external I2C EEPROM devices connected to each of the HX3. The EEPROM devices should be 32 KB in size to support dual firmware images for each HX3.

Tier-1 HX3 Hub, Firmware Version 0.1.1.183

The Tier-1 HX3 hub in the EZ-PD Dock Reference Design supports the following:

- Upstream Port connected to Dock Upstream Type-C Port.
- One Downstream USB 3.0 port on a Type-C receptacle.
- One Downstream USB 3.0 port on a Type-A receptacle.
- One Downstream port connected to the Upstream port of the Tier-2 HX3 hub.
- One Downstream port connected to the CY7C65219-40LQXI Dock Management Controller.

Figure 2 shows the HX3 Blaster Plus snapshot of the configuration settings enabled for this firmware image.



Table 3. Tier-1 Hub Device Settings

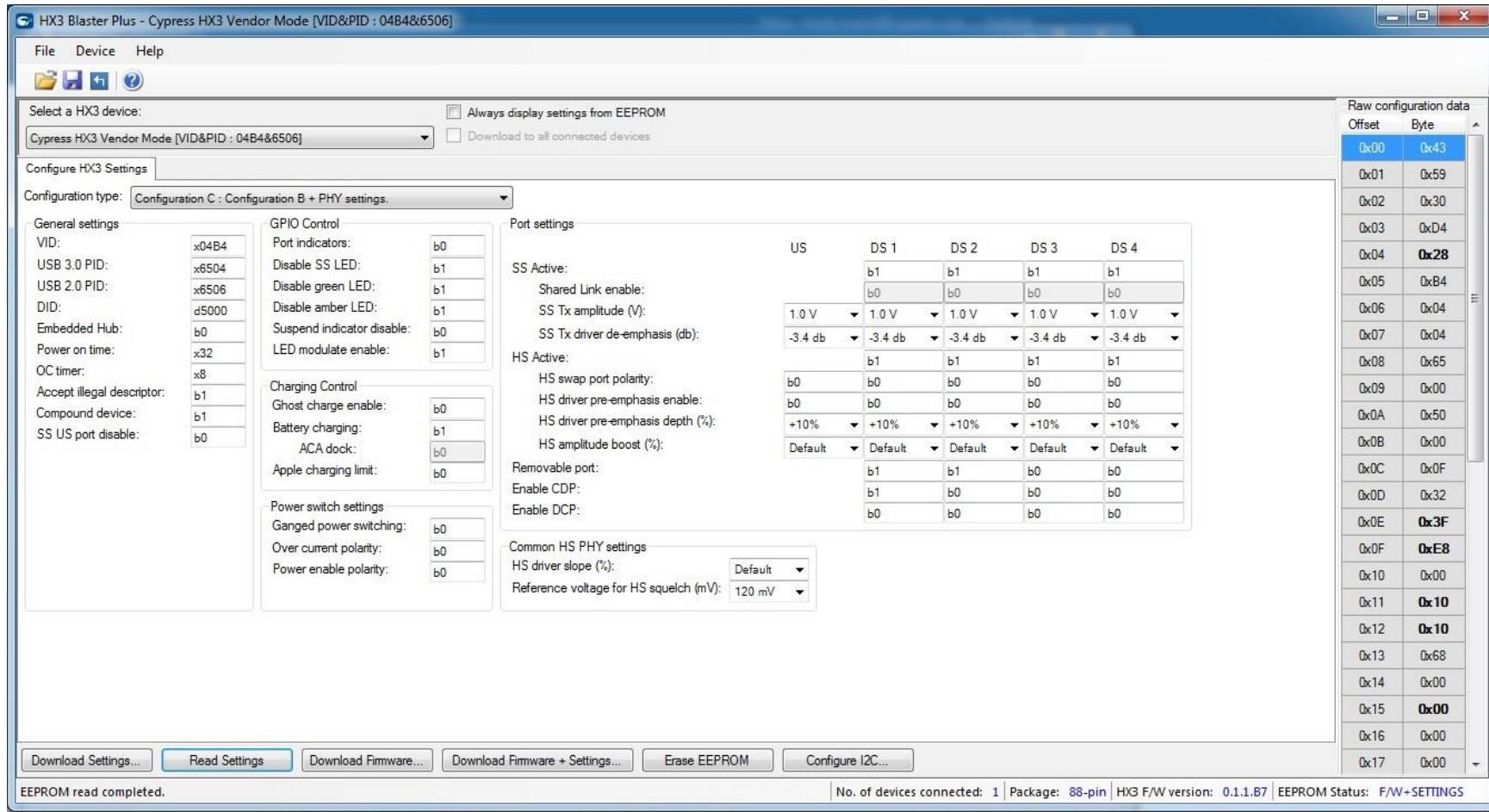
Setting	Value
Vendor ID (VID)	0x04B4 ¹
USB 3.0 Product ID (PID)	0x6504
USB 2.0 Product ID (PID)	0x6506
Device ID (DID)	5000
Embedded Hub	0
Ghost Charging Enabled	0
Battery Charging	1
Ganged Power Switching	0
Over Current Polarity	0

Note: ¹0x04B4 is the Cypress USB Vendor ID (VID) and is used on the EZ-PD Dock reference design for demonstration purposes only. Production dock releases, based on this design, are required to use VID of the manufacturer/OEM instead of the Cypress VID. USB VIDs are assigned and maintained by USB Implementers Forum, Inc. (USB-IF). The USB-IF recommends that each manufacturer/OEM set up a coordinated allocation scheme for Product IDs (PIDs), so that different teams do not inadvertently choose the same PID for different products of the same manufacturer/ OEM. For more information on USB-IF membership and on how to obtain a VID, visit www.usb.org. Contact [Cypress customer support](#) for any further clarifications.

Table 4. Tier-1 Hub Downstream Ports

	Port 1	Port 2	Port 3	Port 4
Function	USB 3.0 Type-A Port	USB 3.0 Type-C Port	DMC Controller	Tier-2 HX3 USB 3.0 Hub
Removable	1	1	0	0

Figure 2. Tier-1 Hub Configuration Settings



HX3 Blaster Plus - Cypress HX3 Vendor Mode [VID&PID : 04B4&6506]

Select a HX3 device: Cypress HX3 Vendor Mode [VID&PID : 04B4&6506]

Configure HX3 Settings

Configuration type: Configuration C : Configuration B + PHY settings.

General settings

VID: x04B4
 USB 3.0 PID: x6504
 USB 2.0 PID: x6506
 DID: d5000
 Embedded Hub: b0
 Power on time: x32
 OC timer: x8
 Accept illegal descriptor: b1
 Compound device: b1
 SS US port disable: b0

GPIO Control

Port indicators: b0
 Disable SS LED: b1
 Disable green LED: b1
 Disable amber LED: b1
 Suspend indicator disable: b0
 LED modulate enable: b1

Charging Control

Ghost charge enable: b0
 Battery charging: b1
 ACA dock: b0
 Apple charging limit: b0

Power switch settings

Ganged power switching: b0
 Over current polarity: b0
 Power enable polarity: b0

Port settings

SS Active:
 Shared Link enable: b0
 SS Tx amplitude (V): 1.0 V
 SS Tx driver de-emphasis (db): -3.4 db

HS Active:
 HS swap port polarity: b0
 HS driver pre-emphasis enable: b0
 HS driver pre-emphasis depth (%): +10%
 HS amplitude boost (%): Default

	US	DS 1	DS 2	DS 3	DS 4
Shared Link enable:	b0	b0	b0	b0	b0
SS Tx amplitude (V):	1.0 V	1.0 V	1.0 V	1.0 V	1.0 V
SS Tx driver de-emphasis (db):	-3.4 db	-3.4 db	-3.4 db	-3.4 db	-3.4 db
HS Active:	b1	b1	b1	b1	b1
HS swap port polarity:	b0	b0	b0	b0	b0
HS driver pre-emphasis enable:	b0	b0	b0	b0	b0
HS driver pre-emphasis depth (%):	+10%	+10%	+10%	+10%	+10%
HS amplitude boost (%):	Default	Default	Default	Default	Default
Removable port:	b1	b1	b1	b1	b1
Enable CDP:	b1	b0	b0	b0	b0
Enable DCP:	b0	b0	b0	b0	b0

Common HS PHY settings

HS driver slope (%): Default
 Reference voltage for HS squelch (mV): 120 mV

Raw configuration data

Offset	Byte
0x00	0x43
0x01	0x59
0x02	0x30
0x03	0xD4
0x04	0x28
0x05	0xB4
0x06	0x04
0x07	0x04
0x08	0x65
0x09	0x00
0x0A	0x50
0x0B	0x00
0x0C	0x0F
0x0D	0x32
0x0E	0x3F
0x0F	0xE8
0x10	0x00
0x11	0x10
0x12	0x10
0x13	0x68
0x14	0x00
0x15	0x00
0x16	0x00
0x17	0x00

EEPROM read completed. No. of devices connected: 1 | Package: 88-pin | HX3 F/W version: 0.1.1.B7 | EEPROM Status: F/W+SETTINGS



Tier-2 HX3 Hub, Firmware Version 0.1.2.183

The Tier-2 HX3 hub in the EZ-PD Dock Reference Design supports the following:

- Upstream Port connected to Downstream port of Tier-1 hub.
- Two Downstream USB 3.0 ports on Type-A receptacles.
- One Downstream port connected to the Upstream port of the Tier-3 HX2VL hub.
- One Downstream port connected to the CYUSB3610 GX3 USB 3.0 To Ethernet Controller.

Figure 3 shows the HX3 Blaster Plus snapshot of the configuration settings enabled for this firmware image.

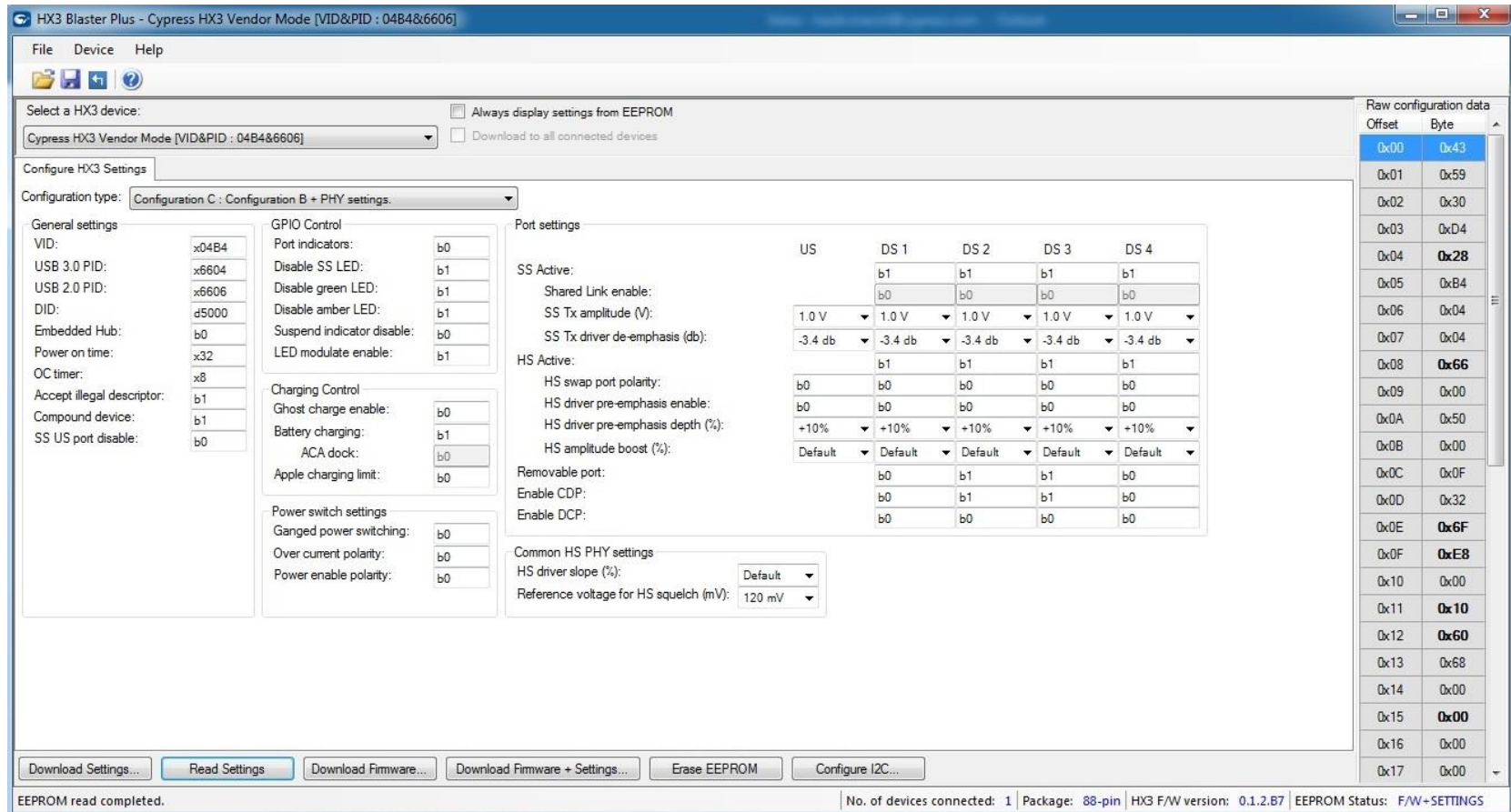
Table 5. Tier-2 Hub Device Settings

Setting	Value
Vendor ID (VID)	0x04B4
USB 3.0 Product ID (PID)	0x6604
USB 2.0 Product ID (PID)	0x6606
Device ID (DID)	5000
Embedded Hub	0
Ghost Charging Enabled	0
Battery Charging	1
Ganged Power Switching	0
Over Current Polarity	0
Power Enable Polarity	0
Compound Device	1

Table 6. Tier-2 Hub Downstream Ports

	Port 1	Port 2	Port 3	Port 4
Function	Tier-3 HX2VL USB 2.0 Hub	USB 3.0 Type- A Port	USB 3.0 Type- A Port	CYUSB3610 GX3 USB 3.0 To Ethernet
Removable	0	1	1	0

Figure 3. Tier-2 Hub Configuration Settings



The screenshot shows the HX3 Blaster Plus software interface. The main window title is "HX3 Blaster Plus - Cypress HX3 Vendor Mode [VID&PID : 04B4&6606]". The interface includes a menu bar (File, Device, Help), a toolbar, and a main configuration area. The configuration area is divided into several sections:

- Select a HX3 device:** Cypress HX3 Vendor Mode [VID&PID : 04B4&6606].
- Configure HX3 Settings:** Configuration type: Configuration C : Configuration B + PHY settings.
- General settings:** VID: x04B4, USB 3.0 PID: x6604, USB 2.0 PID: x6606, DID: d5000, Embedded Hub: b0, Power on time: x32, OC timer: x8, Accept illegal descriptor: b1, Compound device: b1, SS US port disable: b0.
- GPIO Control:** Port indicators: b0, Disable SS LED: b1, Disable green LED: b1, Disable amber LED: b1, Suspend indicator disable: b0, LED modulate enable: b1.
- Charging Control:** Ghost charge enable: b0, Battery charging: b1, ACA dock: b0, Apple charging limit: b0.
- Power switch settings:** Ganged power switching: b0, Over current polarity: b0, Power enable polarity: b0.
- Port settings:** SS Active: Shared Link enable: b0, SS Tx amplitude (V): 1.0 V, SS Tx driver de-emphasis (db): -3.4 db, HS Active: HS swap port polarity: b0, HS driver pre-emphasis enable: b0, HS driver pre-emphasis depth (%): +10%, HS amplitude boost (%): Default, Removable port: Enable CDP: b0, Enable DCP: b0.
- Common HS PHY settings:** HS driver slope (%): Default, Reference voltage for HS squelch (mV): 120 mV.

At the bottom of the window, there are buttons for "Download Settings...", "Read Settings", "Download Firmware...", "Download Firmware + Settings...", "Erase EEPROM", and "Configure I2C...". The status bar at the bottom indicates "EEPROM read completed.", "No. of devices connected: 1", "Package: 88-pin", "HX3 F/W version: 0.1.2.B7", and "EEPROM Status: F/W+SETTINGS".

Raw configuration data table:

Offset	Byte
0x00	0x43
0x01	0x59
0x02	0x30
0x03	0xD4
0x04	0x28
0x05	0xB4
0x06	0x04
0x07	0x04
0x08	0x66
0x09	0x00
0x0A	0x50
0x0B	0x00
0x0C	0x0F
0x0D	0x32
0x0E	0x6F
0x0F	0xE8
0x10	0x00
0x11	0x10
0x12	0x60
0x13	0x68
0x14	0x00
0x15	0x00
0x16	0x00
0x17	0x00



Limitations and Known Problems of HX3 Firmware

The Hub compliance tools from compliance test vendors are currently designed for single-level hubs. As this design has a multi-level hub design (Tier-1 and Tier-2 HX3 and Tier 3 HX2VL) there might be failures reported during the compliance tests for ports on Tier-2 and Tier-3 hubs. Contact Cypress technical support for any clarifications.

Tool Requirements

This version of EZ-PD Dock Reference Design (DMC and CCG Firmware) projects require PSoC Creator 4.2 for compilation.

Download the latest PSoC Creator version from:

www.cypress.com/products/psoc-creator-integrated-design-environment-ide

Technical Support

For further assistance, go to www.cypress.com/support.

Additional Information

For more information about the CCG4 Type-C controller, visit the webpage:

www.cypress.com/products/ez-pd-ccg4-two-port-usb-type-c-controller-power-delivery

For more information about the CCG4 Dock Reference Design from Cypress, visit the webpage:

www.cypress.com/documentation/reference-designs/ez-pd-ccg4-usb-type-c-monitordock-solution

For more information about the Cypress Type-C controller family, visit the webpage:

www.cypress.com/products/usb-type-c-and-power-delivery



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