Cypress Semiconductor
Reliability Qualification Report

QTP# Q100811 Version *A

S72XS256RE0AH

Qualification of: S72XS256RE0AH, Stacked Flash and SDRAM-256 Megabit MirrorBit 1.8 Volt-only Simultaneous Read/Write, Burst Mode Multiplexed Flash Memory and 256 Megabit Burst Mode SDRAM in RSC133 (8 x 8 x 1mm) 133 Ball, Multi-Chip Fine Pitch Ball Grid Array Package (MCP)

FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT
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I. Product and Package Information

Product Description: S72XS256RE0AH **Cypress Division:** Memory Product Division

Stacked Flash and SDRAM-256 Megabit MirrorBit 1.8 Volt-only Simultaneous Read/Write, Burst Mode Multiplexed Flash Memory and 256 Megabit Burst Mode SDRAM

Package:	RSC133	**QTP:**	Q100811		
Description:	(8 x 8 x 1mm) 133 Ball, Multi-Chip Fine Pitch Ball Grid Array Package (MCP)			**Flammability:**	**O2 Index:**
Assembly:	Cypress Thailand	**Molding Compound:**	ShinEtsu KMC 3580LVA	UL-V0	>28
Electrical Test:	Cypress Thailand	**Theta Ja / Psi Jt:**	35 °C/W / 9.5 °C/W		
Substrate/Leadframe:	Laminate Substrate	**Die Attachment:**	QMI 546 (Die 1), FH 4026T (Die 2)		
Lead Finish:	98.5Sn1.0Ag0.5Cu Spheres	**Bond Wire:**	Gold		
Comments:					

Est. Field Temperature:	55 °C	**Life Test Temperature:**	150 °C
Est. DC Field Current:	40 mA	**Life Test Dynamic Current:**	12 mA
Est. Field Voltage:	1.8 V	**Life Test Voltage:**	1.95 V
Est. Field Power Dissipation:	72 mWatts	**Est. Stress Power Dissipation:**	23.4 mWatts
Est. Field Tj:	57.5 °C	**Est. Stress Tj:**	150.8 °C

Die #1:	**Die:**	98214B	**Die Size:**	5.00 x 4.77 mm	**Number of Dies:**
(Bottom)	**Process:**	CS239L (65nm)	**Fab:**	Cypress Fab25	2
	Type:	MirrorBit	**Density:**	256M	
Die #2:	**Die:**	EMD56164PCI	**Die Size:**	3.92 x 2.45 mm	
	Process:	45nm	**Fab:**	JSC	
	Type:	DDR SDRAM	**Density:**	256M	

II. CS239/L Life Test Failure Rate Calculation

HTOL Stress Temperature - 125 °C

Failure Mechanism	Read Points / Test Results			Modeling Parameters @ 55°C					Avg. Failure Rate FITS @ 55°C, 60% Conf.	
	24 hrs	168 hrs	1000 hrs	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life	Inherent Life
PLASTIC										
Sample Size	3930	3926	700							
Zero fails, Process ave. Ea	0 *	0	0	0.66	41	1	41		58	18
Totals	**0**	**0**	**0**					**6342**	**58**	**18**

* Contributes to early life FITS

Data Retention Bake - 150 °C

Reliability Stress	Number of Rejects	Sample Size	Failure Rate %	Failure Mechanism
500 hrs	0	1050	0.00	No Failures
1000 hrs	0	1039	0.00	No Failures

III. Summary of Stress Test Results

Stress Test	Stress Condition	Package Type	Sample Size	Num. of Lots	Num. of Fails	Failure Rate %	Comments
Data From Qualification Q100811:							
ESD CDM	N/A	RSC133 [1]	15	1	Passed 1.0kV		
Preconditioning	(PC9/260°C, +0°C/-5°C)	RSC133 [1]	231	1	Passed Jedec L3 / Jeita Rank E		
Precon+Temp Cycle	(PC9/260°C, -55°C/125°C)	RSC133 [1]	77	1	0	0.00	1000 cycles
Precon+HAST	(PC9/260°C, Biased, 110°C/85% RH)	RSC133 [1]	77	1	0	0.00	264 hours
Precon+uHAST	(PC9/260°C, Unbiased, 130°C/85% RH)	RSC133 [1]	77	1	0	0.00	96 hours
Construction Analysis	N/A	RSC133 [1]	30	1	Passed		
Generic Reference Data:							
Latch Up	(125°C, +/- 100mA)	VDJ044 [4]	6	1	Passed		
Preconditioning	(PC9/260°C, +0°C/-5°C)	RSC133 [2]	154	1	Passed Jedec L3 / Jeita Rank E		
	(PC1/260°C, +0°C/-5°C)	RSD056 [3]	462	3	Passed Jedec L3 / Jeita Rank E		
Precon+Temp Cycle	(PC9/260°C, -55°C/125°C)	RSC133 [2]	77	1	0	0.00	1000 cycles
	(PC1/260°C, -55°C/125°C)	RSD056 [3]	231	3	0	0.00	500 cycles
Precon+uHAST	(PC9/260°C, Unbiased, 130°C/85% RH)	RSC133 [2]	77	1	0	0.00	96 hours
	(PC1/260°C, Unbiased, 130°C/85% RH)	RSD056 [3]	231	3	0	0.00	96 hours

Notes / Justification:
1) Results from Qual Q100811, S72XS256RE0AH, CS239L (65nm) MirrorBit + 45nm DDR SDRAM in 133 Ball MCP (8 x 8 x 1mm)
2) Results from Qual Q100017, S72VS256RE0A in 133 Ball MCP (8 x 8 x 1mm) - Same Package and Flash Device
3) Results from Qual Q99689, S71NS256RD0AHKKL in 56 Ball MCP (7.7 x 6.2 x 1mm) - Same MCP Package Type and Same Flash Technology Device
4) Results from Qual Q99243, S29VS256R in 44 Ball vFBGA (7.7 x 6.2 x 1mm) - Same Flash from different Fab Location

Preconditioning Flows: PC1 (Exceeds JEDEC L3 and JEITA Rank E): Bake 125°C, 24hr => Soak @ 30°C/70%RH, 216hr => 3x Reflow
PC9 (Accelerated JEDEC L3 / JEITA Rank E): Bake 125°C, 24hr => Soak @ 60°C/70%RH, 72hr => 3x Reflow

Reliability Tests Performed per Specification Requirements

Stress	Condition	Specification Reference
Construction Analysis	N/A	Internal Specifications
ESD CDM	N/A	JS002 / AEC-Q100-011
Latch Up	(125°C, +/- 100mA)	JESD78 / AEC Q100-004
Precon+HAST	(PC9/260°C, Biased, 110°C/85% RH)	JESD22-A110
Precon+Temp Cycle	(PC1/260°C, -55°C/125°C)	JESD22-A104
Precon+Temp Cycle	(PC9/260°C, -55°C/125°C)	JESD22-A104
Precon+uHAST	(PC1/260°C, Unbiased, 130°C/85% RH)	JESD22-A118
Precon+uHAST	(PC9/260°C, Unbiased, 130°C/85% RH)	JESD22-A118
Preconditioning	(PC1/260°C, +0°C/-5°C)	J-STD-020 / EIAJ ED-4701-100 Method 104
Preconditioning	(PC9/260°C, +0°C/-5°C)	J-STD-020 / EIAJ ED-4701-100 Method 104

IV. Revision History

Document Number: 002-20407

Document Title: Q100811: Qualification of S72XS256RE0AH in RSC133 Package

Rev.	Issue Date	ECN#	Originator	Description
**	7/18/2017	5822398	EKNG	Initial Release.
*A	9/28/2017	5899072	EKNG	Included LU data