AN4017

Understanding Temperature Specifications: An Introduction

Associated Part Family: Sync SRAMs
Associated Project: No
Software Version: NA
Related Application Notes: AN42468

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AN4017 gives a basic understanding of the temperature specifications found in Cypress's product datasheets. There are many factors that affect the thermal operation of a device. This application note also gives you an understanding of the thermal parameters and temperature specifications of the device.

1 Introduction

Power is required to operate integrated circuits (ICs). This power is provided to the IC in the form of voltage and current through power supply pins. The consumption of power creates heat and results in junction temperatures different from the surrounding ambient temperature. There are several factors that affect the junction temperature:

- Heat from neighboring ICs
- Airflow
- IC packaging material
- IC packaging technique (example flip chip versus wire bond)
- Number of leads on the IC package
- Printed circuit board (PCB) materials
- Ambient temperature

The air temperature (T_A) dictates the minimum temperature at which the device operates. No matter how much heat sinking or airflow is supplied, the device will not get colder than the surrounding air. Once the IC begins to dissipate power the junction temperature (T_J) increases above the ambient temperature. You can reduce the junction temperature by adding airflow or heat sinks, but as long as the power is dissipated, the junction rises to a temperature above T_A.

Thermal resistance is the ability for a given device to dissipate the internally generated heat, expressed in units of °C/W. Basically, the thermal resistance is derived to show how much the T_J increases based on the power dissipated by the device.

2 Definitions

The following are some important definitions that pertain to the operating condition of the devices.

T_A = **Ambient temperature**. This is the temperature of the environment, still air.

T_C = **Case temperature**. This is the temperature of the case of the semiconductor device.

T_J = **Operating Junction temperature**. This is the temperature of the device circuit itself under given operating conditions. T_J must be calculated or inferred from the case and/or ambient temperature.

T_{Jmax} = **Maximum Junction temperature**. This is the maximum temperature that the device tolerates to guarantee reliable operation. The system designer needs to ensure that $T_J < T_{Jmax}$ to guarantee reliability.

Table 1. Maximum Junction Temperature

SRAM Type	T_{Jmax}
Sync SRAMs	125 °C
nvSRAM	150 °C
Async SRAM	150 °C
Dual port RAMs and FIFOs	125 °C
F-RAM	125 °C

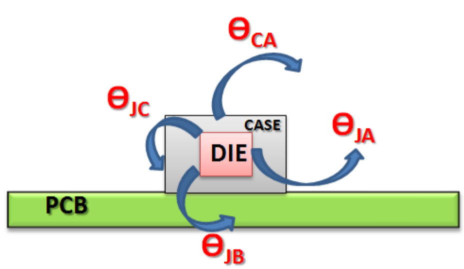
Max junction temperature is listed in Table 1 for various Cypress memory devices.

Power Dissipation (P_d) = This is the power consumed while the device is in operation and this power consumption creates heat. It is typically expressed in Watts.

Airflow = The movement of air over and around a device that is used to remove heat from the system.

Thermal Resistance = An empirically derived set of constants that describe the heat flow characteristics of a given system, expressed in °C/W. Thermal resistance is a measure of the ability of a package to transfer the heat generated by the device inside a package to the ambient. Some factors that affect thermal resistance include: (1) the die size of the IC chip, (2) the mold compound, and (3) lead frame / substrate design. θ_{JA} (junction-to-ambient thermal resistance), θ_{JC} (junction-to-case thermal resistance), θ_{CA} (case-to-ambient thermal resistance), and θ_{JB} (junction to board) are the thermal parameters generally used to characterize a package.

Figure 1. Types of Thermal Resistance



θ_{JA} is the junction-to-ambient thermal resistance. θ_{JA} represents the ability of the package to conduct heat from the IC chip inside the package to the environment. θ_{JA} is defined as the difference between the junction temperature and the ambient temperature when the device is dissipating 1 W of power. θ_{JA} (expressed in °C/W) = $(T_J - T_A)/Pd$. For a given package and lead frame, some factors that affect θ_{JA} are: (1) the die size of the IC chip, (2) the length of the printed circuit board traces attached to the IC package on the system board, and (3) the amount of airflow across the package. θ_{JA} value is available in the datasheet of the device.

θ_{JC} is the junction-to-case thermal resistance. θ_{JC} is defined as the temperature difference between the junction and a reference point on the package when the device is dissipating 1 W of power. θ_{JC} (expressed in °C / W) = $(T_J - T_C)/Pd$. It is mainly a function of the thermal properties of the materials constituting the package. θ_{JC} value is available in the datasheet of the device.

θ_{JB} is the junction-to-board thermal resistance. θ_{JB} is defined as the temperature difference between the junction and the board when the device is dissipating 1 W of power. θ_{JB} (expressed in °C/W) = $(T_J - T_B)/P_d$. T_B is the temperature of the PCB board taken at a predefined location near the die. θ_{JB} can be provided upon request.

θ_{CA} is the case-to-ambient thermal resistance. θ_{CA} is defined as the temperature difference between a reference point on the package and the ambient temperature when the device is dissipating 1 W of power. θ_{CA} (expressed in °C/W) = $(T_C - T_A)/P_d$. θ_{CA} is mainly dependent on the surface area available for convection and radiation and the ambient conditions, among other factors. This can be controlled by using heat-sinks, providing greater surface area and better conduction path, or by air or liquid cooling.

The junction-to-ambient thermal resistance is the sum of the thermal resistances of junction-to-case and case-to-ambient. In other words, the relationship between the thermal parameters can be expressed as: $\theta_{JA} = \theta_{JC} + \theta_{CA}$

3 Calculating the Junction Temperature

When the junction-to-ambient thermal resistance (θ_{JA}) and the ambient temperature are given, you can calculate the junction temperature of the chip after calculating the power dissipated by the device, as follows:

$T_J = P_d\, \theta_{JA} + T_A$

Where,

θ_{JA} = Junction-to-ambient thermal resistance

T_A = Ambient temperature

P_d = Core power + I/O switching power + ODT Power

Core power = $V_{DD(max.)} \times I_{DD}$ and

I/O switching power = $\alpha \times f \times C_L \times V^2$ x (number of I/Os that are switching),

where:

α is the activity factor, or the ratio of frequency at which outputs toggle to the clock frequency

= 0.5 for single data rate devices like Std Sync, NoBL™- SRAMs;

= 1 for double data rate devices (such as DDR/QDR™ SRAMs)

f = operating frequency

C_L = external load capacitance

V is output voltage swing,

For example,

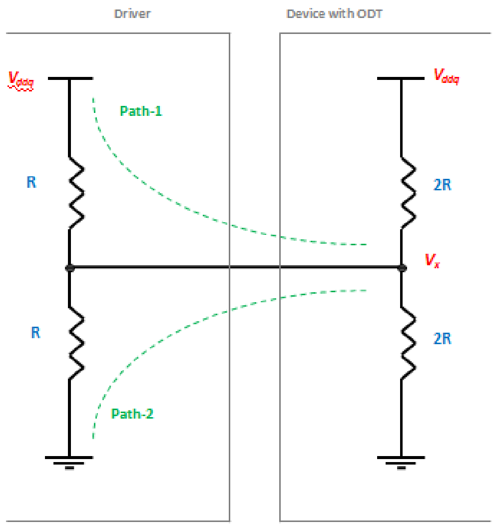
= V_{ddq} for unterminated load

= $V_{ddq}/2$ for a terminated load with pull-up termination

ODT Power is the power dissipated in the input on die termination resistors. For Non-ODT parts this power is zero. See Figure 2 for a description of ODT Power consumption.

If the driver source impedance is R, the input on die termination resistors are 2R as shown below.

Figure 2. ODT Power Consumption



Depending on whether the source is driving a “1” or “0” either Path-1 or Path-2 is active. In either case the Power dissipated in the ODT resistors is

ODT Power = (5/16) × $(V_{ddq})^2$ × (1/R) × (number of inputs with ODT resistors), where:

= V_{ddq} is I/O voltage

= 2R is the termination resistor, used for pull-up and pull-down termination

See AN42468 for derivation of the ODT Power Equations.

4 SRAM Example

Let us look at an example using the 100-lead SRAM TQFP device (specifically, part number CY7C1381D). The thermal resistance is 28.66 °C/W for a 4-layer board with 0 ft/s of airflow. Assuming the device is running at 100 MHz with a 40-pF capacitive load and all I/Os switching, the power dissipated is calculated as follows:

P_d = Core power + I/O switching power + ODT power

Core power = $V_{DD(max.)} \times I_{DD} = 3.6 \times 175 \times 10^{-3} = 0.63$ W

I/O switching power = $\alpha \times f \times C_L \times V^2$ x (number of I/Os that are switching) = $0.5 \times 100 \times 10^6 \times 40 \times 10^{-12} \times (3.6)^2 \times 36$ = 0.93 W

ODT power = 0, as there are no input ODT resistors.

Therefore total power dissipated, P_d = 1.56 W

The junction temperature increase is then calculated using the thermal resistance value:

$T_J = T_A$ + (Thermal resistance × Power)

$= T_A + (\theta_{JA} \times P_d)$

$= T_A$ + (28.66 °C/W × 1.56 W)

$= T_A$ + 44.71 °C

Note: θ_{JA} used is a referenced value and will vary by device.

If the application is rated for commercial temperature range, we can have an ambient temperature from 0 °C to 70 °C. Assume a typical environment within the system is 30 °C, the resulting junction temperature is:

T_J = 30 °C + 44.71 °C

= 74.71 °C

If the same system had airflow, the junction temperature would be lower.

In a worse-case scenario, we can have T_A = 70 °C:

T_J = 70 °C + 44.71 °C = 114.71 °C

However, note that a typical application will have boards with more layers and better heat sinking characteristics. We see that the temperature at the junction will be much higher than the temperature of the air around it, and that airflow and board construction have a large impact on the junction temperature.

For more information, see the online tool for calculating the junction temperature for Synchronous SRAM products.

5 Temperature Specifications

The thermal parameters exhibit worst-case values when there is no airflow. Also, with higher temperatures the thermal performance becomes even more critical. Because of this, as we move from commercial temperature ranges to industrial or automotive temperature ranges, temperature specifications become much higher.

To ensure good thermal management, it is essential that the junction temperature remains well below the maximum rated value $\mathbf{T_{Jmax}}$. This is because an increase in junction temperature (T_J) can adversely affect the long-term operating life of a device.

6 System Considerations

The major part of the heat travels through the PCB only. There are essentially four paths for heat to transfer out of the chip into the PCB:

1. The small amount of heat transfer from case to ambient through the air around the device.
2. Heat transfer into the PCB through the top layer.
3. Heat transfer to the internal dielectric material and copper layers though via array.
4. Finally, the heat that travels through via array below the chip and into the PCB's bottom-most copper layer.

The manner in which an IC package is mounted and positioned in its surrounding environment has significant effects on operating junction temperatures. These conditions are controlled by the system designer and are worthy of serious consideration in the PC board layout and system ventilation and airflow features.

Forced air cooling significantly reduces thermal resistance. Airflow parallel to the long dimension of the package is generally a little more effective than airflow perpendicular to the long dimension of the package.

External heat sink applied to an IC package can improve thermal resistance by increasing heat flow to the surrounding environment. Heat sink performance will vary by size, material, design, and system airflow. In general, they can provide a substantial improvement.

Package mounting can affect thermal resistance. For example, surface mount packages dissipate significant amounts of heat through the leads that attach to the traces.

The metal (copper traces) on PC boards conduct heat away from the package and dissipate heat to the ambient; thus the larger the trace area the lower the thermal resistance.

The dielectric material used in the PCB with higher thermal conductivity can also help to get the lower thermal resistances. For example, the thermal resistance from junction to board (θ_{JB}) is about 10% lower in the case of RT/duroid 6035HTC (Rogers) than FR-4[1].

[1] Based on Cypress' 72M QDR-II+ and JEDEC standard PCB board thermal resistance measurement simulation results.

The other most effective conduction path is vias. The more the number of vias under the chip, the lower the thermal resistances; as a result, the junction temperature of the chip will be reduced. Optimized conduction paths from vias to copper layers and dielectric material through accurate design of the via array provides the most efficient paths in the design for removing heat from the chip.

Also, as package sizes shrink and more devices are mounted on the board the thermal characteristics become a major concern.

7 Measurement of T_J

Measurement of junction temperature to confirm whether it is well below the specification is a possible but difficult procedure.

A practical and easier method is to measure the case temperature. The measurement can be done through a direct measurement — such as a thermocouple or resistance temperature detector (RTD) placed in contact with the device under test — or with a noninvasive method, such as an infrared heat detector. Once T_C is known, T_J can then be calculated using the junction-to-case thermal resistance and the power as mentioned in the previous example.

See JEDEC Specification JESD51 - Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device) for details.

In general, the case temperature will be within a few degrees of the junction temperature so the calculation will not be necessary. Therefore it is advisable to measure the case temperature, and ensure it is below the maximum rated junction temperature. If it is higher than the maximum specified junction temperature, the junction will be even hotter and the application will be running outside of specification.

8 Summary

The thermal characteristics of a device have been and will continue to be a major concern for board designers. It is crucial that the thermal parameters, especially junction temperature, are well below the specified limit. This is because an increase in junction temperature can adversely affect the long term operating life of a device. As it is impractical to measure junction temperature directly, it is better to measure the case temperature of the device and then calculate the junction temperature. Some factors affecting T_J are controlled by the IC manufacturer and others are controlled by the system designer. Also, temperature specifications as well as thermal management become a major concern to board designers as package sizes shrink and board density increases.

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1051123	SFV	05/15/2007	New Application Note.
*A	1736124	VIDB	11/29/2007	No technical updates. Updated to new template (To enable google search functionality).
*B	3111380	VIDB	12/15/2010	No technical updates.
*C	3187210	NJY	03/03/2011	Updated Abstract.
*D	3339187	NJY	08/10/2011	Changed the “Technical note” to “Application note” in the Abstract section. Included link to online tool for calculating Junction temperature in page 2.
*E	3557468	AVIA	03/21/2012	Updated Definitions: Added Table 1. Defined T_{jmax}, and explained the condition $T_j < T_{jmax}$. Added Figure 1. Updated Calculating the Junction Temperature: Updated the equations for power dissipation with ODT Power included. Added Figure 2. Added a reference to application note AN42468. Updated Measurement of T_J: Added reference to JEDEC JESD-51 for calculating thermal parameters. Fixed all the grammatical errors across the document. Converted application note from FrameMaker to Word template.
*F	3606064	PRIT	05/02/2012	Updated Definitions: Updated Table 1: Changed value of T_{jmax} of NVSRAM from 125 °C to 150 °C.
*G	4235003	PRIT	01/02/2014	Updated to new template. Completing Sunset Review.
*H	4537562	PRIT	10/14/2014	Updated System Considerations.
*I	4831299	PRIT	07/14/2015	Updated Definitions: Updated Table 1: Added F-RAM and its corresponding maximum junction temperature. Updated to new template.
*J	5703509	AESATMP9	04/20/2017	Updated logo and copyright.

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