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AN42468

On-Die Termination for QDR® II+/DDR II+ SRAMs

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Associated Part Family: QDR/DDR–II+/II+Xtreme
Related Application Notes: AN4065

AN42468 discusses on-die termination (ODT) scheme, implementation, advantages and power calculation for the QDR™II+ and DDRII+ family of Synchronous SRAMs on the 65-nm technology devices.

1. Introduction

High frequency signals are susceptible to losses along transmission lines thereby causing signal distortion at the receiver. This will impact the receiver's ability to interpret information correctly. In order for a transmission line to minimize distortion of the signal, the impedance of every location on the transmission line should be uniform throughout its length. If there is any place in the line where the impedance is not uniform for some reason (open circuit, impedance discontinuity, different material) the signal gets modified by reflection at the impedance change point which results in distortion, ringing and so forth.

When the signal path has impedance discontinuity, in other words an impedance mismatch, then termination impedance with the equivalent amount of impedance is placed at the point of line discontinuity.

There are different methods of termination.

- Using external resistors – Attach an external resistor with a suitable resistance value at the end of the transmission line.
- On-die termination (ODT) – Embed the termination resistors within the die.

In this application note, we will discuss On-die termination.

ODT has the following advantages:

- Improves signal integrity by having termination closer to the device inputs
- Simplifies board routing
- Saves board space by eliminating external resistors
- Reduces cost involved in using external termination resistors

1.1 ODT Offering on QDRII+ and DDRII+ SRAMs

Cypress offers ODT on the HSTL input signals (Data inputs, K/Kb clocks and BWSb) for the QDRII+ and DDRII+ SRAM family of devices in the 65-nm technology node. Two types of QDRII+ and DDRII+ SRAMs are available:

- Devices without ODT
- ODT enabled devices – The ODT function cannot be disabled for ODT-enabled device option

For ODT-enabled QDRII+ and DDRII+ SRAMs, ODT is offered on the following input signals:

- Input clocks (K and Kb clocks)
- Data input signals
- Control signals (Byte Write Select signals)

1.2 ODT Implementation on QDRII+ and DDRII+ SRAMs

In ODT-enabled devices, the pin R6 in the 165-ball BGA package is used for ODT range selection. The ODT range selection is made during power up initialization of the SRAM.

The ODT termination value tracks the value of the external resistor RQ tied to the ZQ pin, which sets the output impedance.

The allowable range of RQ that guarantees an impedance tolerance of ±15% is between 175 Ω and 350 Ω.

There are two range settings for ODT:

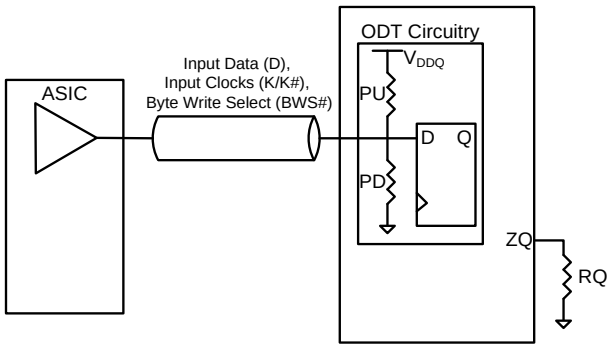
- Low range – Set by tying the ODT pin (pin R6) Low. The impedance range is between 52.5 Ω and 105 Ω (Thévenin equivalent) that follows RQ/3.33 for 175 Ω ≤ RQ ≤ 350 Ω.
- High range – Set by tying the ODT pin (pin R6) High. The impedance range is between 105 Ω and 150 Ω (Thévenin equivalent) that follows RQ/1.66 for 175 Ω ≤ RQ ≤ 250 Ω. For RQ values greater than 250 Ω, the tolerance for the impedance values is not guaranteed.

If the ODT pin is left floating, it defaults to high range.

In DDRII+ SRAMs with a common IO bus, ODT is automatically enabled when the SRAM is used as input and disabled when the SRAM outputs data. See AN4065 for termination techniques for the QDR-II, QDR-II+, DDR-II, and DDR-II+ SRAM devices.

Figure 1 shows the ODT implementation on the HSTL input signals for the QDRII+ and DDRII+ SRAMs.

Figure 1. ODT Implementation in QDRII+/DDRII+ SRAMs



Notes

1. There is no difference in the AC timing parameters between the ODT-enabled QDRII+ and DDRII+ SRAMs, and the QDRII+ and DDRII+ SRAMs without ODT.
2. There is no increase in the Idd (current consumption from the core voltage supply) with ODT enabled. This is because the ODT circuitry is powered by the I/O supply voltage (Vddq) and not the core voltage (Vdd).
3. The ODT is enabled for the QDRII+ SRAMs even when the I/Os are not switching.
4. There is a ~50-percent increase in the Iddq (current consumption from the I/O voltage supply) with ODT enabled.
5. Cypress recommends some method of cooling method like airflow or heatsink in the system for ODT-enabled parts as these parts have higher power dissipation compared to devices without ODT.
6. You cannot disable ODT in a device with ODT capability.
7. In DDRII+ SRAMs with that have common I/O architecture, the ODT is automatically enabled when the SRAM inputs data and disabled when the SRAM outputs data. In DDRII+ SRAMs that have separate I/O architecture, the ODT is always enabled.

2 Power Calculation

The formula for calculating the total power dissipation for an ODT enabled device is given as follows.

Total Power Dissipation = Core Power + I/O Switching Power + ODT Power Equation 1

The section below describes how to calculate the ODT Power.

See Figure 2 for the HSTL Input Termination circuit used to derive ODT power consumption.

Figure 2. Input Termination Circuit

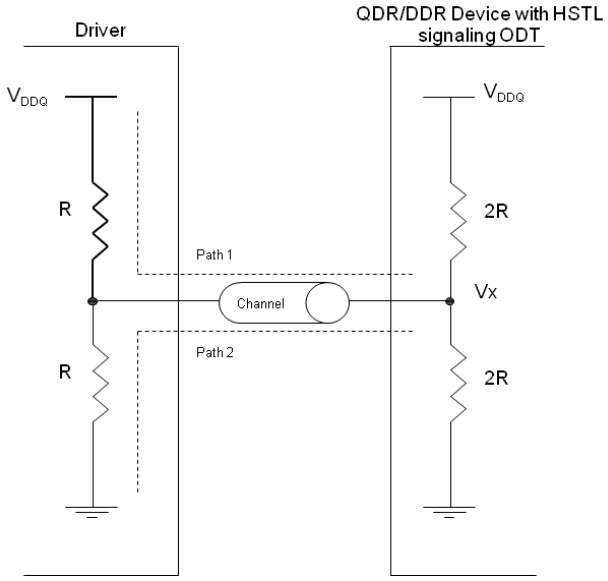


Figure 2 shows a Driver sourcing a device with ODT.

The driver source impedance is represented by "R" .The input ODT resistance is "2R" .This represents an impedance matched circuit.

Depending on whether the source is driving a "1" or a "0" either Path-1 or Path-2 is active. In either case, the power consumption is identical.

Consider Path-1. The Voltage Vx is derived as follows:

Vx = 2R x Vddq / (2R + (R || 2R))

= 2R x Vddq / (2R + 2R/3)

= (3/4) Vddq Equation 2

Power Consumption in the pull-up and pull-down resistors is:

ODT Power = { (Vddq - Vx)^2 / 2R} + {(Vx)^2 / 2R}

= 1/(32R) x (Vddq)^2 + (9/32R) x (Vddq)^2

= 5/(16R) x Vddq^2 Equation 3

Hence,

ODT Power = 5/(16R) x Vddq^2 x (number of inputs with ODT resistors)

For more information, see the online tool for calculating the power consumption and junction temperature for Synchronous SRAM products.

3 Summary

The ODT feature in the QDRII+ and DDRII+ family of devices improves the signal quality at high frequencies (greater than 300 MHz). This feature also helps reduce board space by eliminating external termination resistors on the board and the cost associated with these external resistors.

Document History

Document Title: AN42468 - On-Die Termination for QDR® II+/DDR II+ SRAMs

Document Number: 001-42468

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1797166	VIDB	12/10/2007	New application note
*A	3112628	VIDB	12/16/2010	No change in content. Added Document History heading.
*B	3339295	NJY	08/10/2011	Removed the part number CY7C15xxKV18 and added parts CY7C21xxKV18, CY7C22xxKV18 and CY7C26xxKV18 to the Associated Part Family. Added bullet that ODT function cannot be disabled for ODT enabled device option on page 1. Added clarification to Note 2 on page 2. Clarified Note 4 on page 2. Added I/O power calculation section in page 2 Corrected low range impedance value from 52 Ω to 52.5 Ω. Changed Byte Write Signal to Byte Write Select signals on page 1.
*C	3381851	PRIT	09/21/2011	Associated Application Notes Modified Power Calculation section Included link to online tool for calculating Power consumption and Junction temperature in page 2. Updated template
*D	3558860	PRIT/AVIA	03/27/2012	Added derivation for ODT Power dissipation. Updated template.
*E	3732214	NJY	09/04/2012	Modified Abstract and Introduction. Updated Figure 1.
*F	4235003	PRIT	01/02/2014	Updated in new template. Completing Sunset Review.
*G	4346132	PRIT	04/14/2014	Updated product family to QDR/DDR–II+/II+Xtreme Updated Figure 1 and Figure 2.
*H	5585611	DEVM	01/13/2017	Updated template
*I	5826090	AESATMP9	07/21/2017	Updated logo and copyright.

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