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Section A: Overview

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- Introduction chapter on page 18
- Getting Started chapter on page 24
- Document Construction chapter on page 25

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1. Introduction

The PSoC® MCU is a scalable and reconfigurable platform architecture that supports a family of programmable embedded system controllers with Arm® Cortex® CPUs (single and multi-core). The PSoC 63 with BLE product family is a combination of a microcontroller with a Bluetooth Low Energy (Bluetooth Smart) subsystem in a single package. It incorporates integrated low-power flash technology, digital programmable logic, high-performance analog-to-digital and digital-to-analog conversion, low-power comparators, touch sensing, serial memory interface with encryption, and standard communication and timing peripherals.

1.1 Features

PSoC 6 MCUs have these characteristics:

- 32-bit dual core (Arm Cortex-M4 and Arm Cortex M0+) CPU subsystem
- Integrated (on-chip) flash memory
- Bluetooth Smart BT 4.2 subsystem
- Audio subsystem with I²S interface and two PDM channels
- Serial memory interface with on-the-fly encryption and decryption
- Low-power modes
- Configurable digital peripherals
- Programmable digital logic
- High-performance analog system
- Flexible and programmable interconnect
- Capacitive touch sensing (CapSense®)
- Programmable GPIOs

This document describes each function block of the PSoC 63 with BLE in detail. In this document, PSoC 6 MCU refers to PSoC 63 with BLE unless explicitly mentioned otherwise.
1.2 Architecture

Figure 1-1 shows the major components of the PSoC 6 MCU architecture. There are five major subsystems: the CPU subsystem, BLE subsystem, system resources, peripheral blocks, and I/O subsystem.

The block diagram shows the device subsystems and gives a simplified view of their interconnections. The color-code shows the lowest power mode where the particular block is still functional (for example, LP comparator is functional in Deep Sleep and Hibernate modes).
1.3 CPU Subsystem (CPUSS)

1.3.1 CPU

The CPU subsystem in PSoC 6 MCUs consists of two Arm Cortex cores and their associated buses and memories: M4 with floating-point unit (FPU) and memory protection unit (MPU), and M0+ with an MPU. The Cortex M0+ provides a secure, uninterruptible boot function. This guarantees that post-boot, system integrity is checked and privileges enforced. Shared resources can be accessed through the normal Arm multi-layer bus arbitration. Exclusive accesses are supported by an inter-processor communication (IPC) scheme, which implements hardware semaphores and protection.

1.3.2 DMA Controllers

PSoC 6 MCUs have DMA controllers that support independent access to peripherals using the multilayer advanced high-performance bus (AHB).

1.3.3 Flash

PSoC 6 MCUs have a flash module with one block that can be used for EEPROM emulation for longer retention. It also has a block of flash that can be securely locked and is accessible only via a key lock that cannot be changed (one-time programmable). The flash block supports Read-While-Write (RWW) operation so that flash updates may be performed while the CPU is active.

1.3.4 SRAM

PSoC 6 MCUs have an SRAM module that can be retained in Deep Sleep mode either fully or in increments of user-designated blocks.

1.3.5 SROM

PSoC 6 MCUs have a supervisory ROM that contains boot and configuration routines. This ROM guarantees secure boot if authentication of user flash is required.

1.3.6 OTP eFuse

The OTP memory can provide a unique and unalterable identifier on a per-chip basis. This unalterable key can be used to access the secured flash.

1.3.7 Program and Debug

PSoC 6 MCUs have extensive support for programming, testing, debugging, and tracing both hardware and firmware. Complete debug-on-chip functionality enables full device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug. The PSoC Creator integrated development environment (IDE) provides fully-integrated programming and debug support for PSoC 6 MCUs. The SWJ (SWD and JTAG) interface is fully compatible with industry-standard third-party probes. With the ability to disable debug features, with robust flash protection, and by allowing customer-proprietary functionality to be implemented in on-chip programmable blocks, the PSoC 6 MCU family provides a high level of security. Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled.

1.4 System Resources Subsystem (SRSS)

1.4.1 Power System

The power system confirms that voltage levels meet the requirements for the respective mode and will either delay mode entry (on power-on reset, for example) until voltage levels meet requirements or generate resets (brownout detect) when the power supply drops below specified levels. The design guarantees safe chip operation between power supply voltage dropping below specified levels and the reset. The VDD power supply feeds an on-chip LDO, which produces the core logic supply. In addition, the device includes an on-chip buck regulator that can be used to power the core.

1.4.2 Clocking System

The PSoC 6 MCU clock system provides clocks to subsystems that require clocks and switches between different clock sources without glitches. In addition, the clock system ensures that no metastable conditions occur. The clock system for PSoC 6 MCU consists of the internal main oscillator (IMO), the internal low-speed oscillator (ILO), the precision internal low-speed oscillator (PILO), the external crystal oscillator, and the watch crystal oscillator (WCO). One phase-locked loop (PLL) and one frequency-locked loop (FLL) are used to generate high-speed clocks from either the IMO or the crystal oscillator or from an external clock supplied from a pin. The PLL and FLL enable independent clock frequencies for peripherals.

1.4.2.1 IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 6 MCU. It is trimmed during testing to achieve the specified accuracy.
1.4.2.2  ILO Clock Source
The ILO is a very low-power oscillator, which may be used to generate clocks for peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

1.4.2.3  Watchdog Timer
A watchdog timer is implemented in the clock block running from the ILO. This allows watchdog operation during Deep Sleep and Hibernate modes, and generates a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

1.4.2.4  Clock Dividers
Integer and fractional clock dividers are provided for peripheral use and timing purposes. The clock dividers are 16 and 24 bits in length to allow very fine clock control.

1.4.2.5  Reset
PSoC 6 MCUs can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which allows the software to determine the cause of the reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration.

1.4.3  GPIO
The GPIO pins are organized in logical entities called ports, which are eight bits in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix (HSIOM) is used to multiplex between various signals that may connect to an I/O pin. Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it. Four GPIO pins are capable of overvoltage tolerant (OVT) operation where the input voltage may be higher than VDD (these may be used for I²C functionality to allow powering the chip off while maintaining physical connection to an operating I²C bus without affecting its functionality).

1.5  Analog Subsystem

1.5.1  12-bit SAR ADC
PSoC 6 MCUs have a 12-bit SAR ADC. The SAR is connected to a fixed set of pins through an eight-input sequencer. The sequencer cycles through the selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth remains the same whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware-driven switching. The sequencer supports the buffering of each channel to reduce CPU interrupt-service requirements. To accommodate signals with varying source impedances and frequencies, different sample times can be programmed for each channel. Also, the signal range specification through a pair of range registers (low- and high-range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is able to digitize the output of the on-chip temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes because it requires a high-speed clock.

1.5.2  Temperature Sensor
The PSoC 6 MCU has an on-chip temperature sensor. This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value by using a Cypress-supplied software that includes calibration and linearization.

1.5.3  12-bit Digital-to-Analog Converter
The PSoC 6 MCU has a 12-bit voltage mode DAC, which may be driven by the DMA controllers to generate user-defined waveforms. The DAC output from the chip can either be the resistive ladder output (highly linear near ground) or a buffered output.
1.5.4 Continuous Time Block (CTBm)

This block consists of two opamps, which have their inputs and outputs connected to fixed pins and have three power modes and a comparator mode. The outputs of these opamps can be used as buffers for the SAR inputs. The non-inverting inputs of these opamps can be connected to either of two pins, thus allowing independent sensors to be used at different times. The pin selection can be made via firmware. The opamps can be set to one of the four power levels; the lowest level allowing operation in Deep Sleep mode to preserve low performance continuous-time functionality in Deep Sleep mode. The DAC output can be buffered through an opamp.

1.5.5 Low-Power Comparators

PSoC 6 MCUs have a pair of low-power comparators, which can operate in Deep Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels in Deep Sleep and Hibernate modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator-switch event.

1.5.6 CapSense

The CapSense system, used primarily for touch sensing, can measure the self-capacitance of an electrode or the mutual capacitance between a pair of electrodes. CapSense provides industry’s best-in-class signal-to-noise ratio (SNR), high touch sensitivity, low-power operation, and superior EMI performance. CapSense touch sensing also supports liquid-tolerant operation using a driven shield signal. Any analog-capable GPIO can be used as a sensor or shield electrode.

In addition to capacitive sensing, the CapSense system can function as an ADC to measure voltage on any GPIO pin that supports the CapSense functionality. Moreover, if the CapSense block is not used for touch sensing or ADC functionality, a CapSense comparator and the two 8-bit IDACs can be used as general-purpose analog blocks. See the PSoC 4 and PSoC 6 MCU CapSense Design Guide for more details.

1.6 Programmable Digital

1.6.1 Smart I/O

The PSoC 6 MCU has two smart I/O blocks, which allow Boolean operations on signals going to the GPIO pins from the device subsystems or on signals coming into the device. Operation can be synchronous or asynchronous and the blocks operate in low-power modes, such as Deep Sleep and Hibernate. This allows, for example, detection of logic conditions that can indicate that the CPU should wake up instead of waking up on general I/O interrupts, which consume more power and can generate spurious wakeups.

1.6.2 Universal Digital Blocks (UDBs) and Port Interfaces

The PSoC 6 MCU supports custom programmable digital functions using UDBs, which also provide a switched digital system interconnect (DSI) fabric that allows signals from peripherals and ports to be routed to and through the UDBs for communication and control.

1.7 Digital Subsystem

1.7.1 Timer/Counter/PWM Block

The timer/counter/PWM block consists of counters with user-programmable period length. It has a capture register, which records the count value of an event (such as an I/O event), a period register, which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals, which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow the use as deadband programmable complementary PWM outputs. It also has a kill input to force outputs to a predetermined state; for example, this is used in motor-drive systems when an overcurrent state is indicated and the PWMs driving the FETs must be shut off immediately with no time for software intervention.

1.7.2 Serial Communication Blocks (SCB)

PSoC 6 MCU SCBs can implement communication interfaces such as I2C, UART, or SPI.

1.7.2.1 I2C Mode

The hardware I2C block implements a full multimaster and slave interface (it is capable of multimaster arbitration). This block has flexible buffering options to reduce the interrupt overhead and latency for the CPU. It also supports EzI2C, which creates a mailbox address range in the PSoC 6 MCU memory and effectively reduces the I2C communication to reading from and writing to an array in the memory. In addition, the block supports a 256-byte FIFO for receive and transmit, which, by increasing the time given for the CPU to read the data, reduces the need for clock stretching caused by the CPU not having read the data on time. The FIFO mode is available in all channels and is useful in the absence of DMA.
The I\textsuperscript{2}C peripheral is compatible with I\textsuperscript{2}C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I\textsuperscript{2}C-bus specification and user manual (UM10204). The I\textsuperscript{2}C bus I/O is implemented with GPIO in open-drain modes.

**1.7.2.2 UART Mode**
This is a full-feature UART that supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the multiprocessor mode that allows the addressing of peripherals connected over common Rx and Tx lines. Common UART functions such as parity error, break detect, and frame error are supported. A 256-byte FIFO tolerates much greater CPU service latencies.

**1.7.2.3 SPI Mode**
The SPI mode supports full Motorola SPI, TI Secure Simple Pairing (SSP) (essentially adds a start pulse that is used to synchronize SPI codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO and supports an EzSPI mode in which the data interchange is reduced to reading and writing an array in memory.

**1.7.3 Serial Memory Interface (SMIF)**
A serial memory interface has selectable 1-, 2-, or 4-bit widths. This block also supports on-the-fly encryption and decryption to support Execute-In-Place operation.

**1.7.4 Audio Subsystem**
This subsystem consists of an I\textsuperscript{2}S block and two PDM channels. The PDM channels interface to a PDM microphone’s bit-stream output.

**1.8 BLE Subsystem (BLESS)**
The PSoC 6 MCU incorporates a Bluetooth Smart subsystem that contains the Physical Layer (PHY) and Link Layer (LL) engines with an embedded security engine. The physical layer consists of the digital PHY and the RF transceiver that transmits and receives Gaussian frequency shift keying (GFSK) packets over a 2.4-GHz ISM band, which is compliant with Bluetooth Smart Bluetooth Specification 4.2. The baseband controller is a composite hardware and firmware implementation that supports both master and slave modes. Key protocol elements, such as human computer interface (HCI) and link control, are implemented in firmware. Time-critical functional blocks, such as encryption, CRC, data whitening, and access code correlation, are implemented in hardware (in the LL engine).

The RF transceiver contains an integrated balun, which provides a single-ended RF port pin to drive a 50-\textohm antenna via a matching/filtering network. In the receive direction, this block converts the RF signal from the antenna to a digital bit stream after performing GFSK demodulation. In the transmit direction, this block performs GFSK modulation and then converts a digital baseband signal to a radio frequency before transmitting it to air through the antenna.

Key features of BLESS are as follows:
- Master and slave single-mode protocol stack with logical link control and adaptation protocol (L2CAP), attribute (ATT), and security manager (SM) protocols
- API access to generic attribute profile (GATT), generic access profile (GAP), and L2CAP
- L2CAP connection-oriented channel (Bluetooth 4.1 feature)
- Broadcaster, Observer, Peripheral, and Central roles
- User-defined advertising data
- Multiple bond support
- GATT client and server
- Supports GATT sub-procedures
- 32-bit universally unique identifier (UUID) (Bluetooth 4.1 feature)
- Supports all SIG-adopted BLE profiles
- Security Manager (SM)
  - Pairing methods: Just works, Passkey Entry, and Out of Band
  - LE Secure Connection Pairing model
  - Authenticated man-in-the-middle (MITM) protection and data signing
2. Getting Started

2.1 PSoC 6 MCU Resources

This chapter provides the complete list of PSoC 6 MCU resources that helps you get started with the device and design your applications with them. If you are new to PSoC, Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device and quickly and effectively integrate it into your design.

The following is an abbreviated list of PSoC 6 MCU resources:

- **Overview**: PSoC Portfolio, PSoC Roadmap, PSoC 6 MCU webpage
- **Product Selectors**: See the PSoC 6 MCU Product Selector Guide to choose a part that suits your application. In addition, PSoC Creator includes a similar device selection tool to select devices for PSoC Creator projects.
- **Datasheets** describe and provide electrical specifications for each device family.
- **Application Notes** and **Code Examples** cover a broad range of topics, from basic to advanced level. Many of the application notes include code examples, which can be opened from PSoC Creator.
- **Technical Reference Manuals (TRMs)** provide detailed descriptions of the architecture and registers in each device family.
- **CapSense Design Guide**: Learn how to design capacitive touch-sensing applications with PSoC devices.
- **Development Tools**
  - **PSoC Creator** is a free integrated design environment (IDE). It enables you to design hardware and firmware systems concurrently with PSoC devices.
  - **CY8CKIT-062-BLE PSoC 6 Pioneer Kit** is an easy-to-use and inexpensive development platform for PSoC 63 MCU with BLE. This kit includes connectors for Arduino™-compatible shields and Digilent® Pmod™ daughter cards.
  - **CY8CKIT-062 WiFi-BT Pioneer Kit** is a low-cost hardware platform that enables design and debug of the MCU and the Murata LBEESKL1DX Module (CYW4343W WiFi + Bluetooth Combo Chip). This kit includes connectors for Arduino-compatible shields and Digilent Pmod daughter cards.
  - **CySmart BLE Host Emulation Tool** for Windows, iOS, and Android is an easy-to-use app that enables you to test and debug your BLE Peripheral applications.
- **Additional Resources**: Visit the PSoC 6 MCU webpage for additional resources such as IBIS, BSDL models, CAD Library Files, and Programming Specifications.
- **Training Videos**: Visit www.cypress.com/training for a wide variety of video training resources on PSoC devices and PSoC Creator, such as:
  - Introduction to PSoC 6 BLE
  - Getting to know PSoC Creator
  - PSoC 6 BLE Pioneer Kit
  - Introduction to BLE
  - Configuring your first BLE design
  - Writing firmware for your first BLE design
- **Technical Support**
  - **Forum**: See if your question is already answered by fellow developers of the PSoC 6 community.
  - Cypress support: Visit our support page and create a technical support case or contact a local sales representative. If you are in the United States, you can talk to our technical support team by calling our toll-free number: +1-800-541-4736. Select option 8 at the prompt.
3. Document Construction

This document includes the following sections:

- Section B: CPU Subsystem on page 29
- Section C: System Resources Subsystem (SRSS) on page 118
- Section D: Digital Subsystem on page 208
- Section E: Analog Subsystem on page 415
- Section F: BLE Subsystem (BLESS) on page 467

3.1 Major Sections

For ease of use, information is organized into sections and chapters that are divided according to device functionality.

- Section – Presents the top-level architecture, how to get started, and conventions and overview information of the product.
- Chapter – Presents the chapters specific to an individual aspect of the section topic. These are the detailed implementation and use information for some aspect of the integrated circuit.
- Glossary – Defines the specialized terminology used in this technical reference manual (TRM). Glossary terms are presented in bold, italic font throughout.
- Registers Technical Reference Manual – Supplies all device register details summarized in the technical reference manual. This is an additional document.

3.2 Documentation Conventions

This document uses only four distinguishing font types, besides those found in the headings.

- The first is the use of *italics* when referencing a document title or file name.
- The second is the use of **bold italics** when referencing a term described in the Glossary of this document.
- The third is the use of Times New Roman font, distinguishing equation examples.
- The fourth is the use of Courier New font, distinguishing code examples.

3.2.1 Register Conventions

Register conventions are detailed in the *PSOC 63 with BLE Registers TRM*.

3.2.2 Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or 3Ah) and hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b or 01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimal.
3.2.3 Units of Measure

This table lists the units of measure used in this document.

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Unit of Measure</th>
</tr>
</thead>
<tbody>
<tr>
<td>bps</td>
<td>bits per second</td>
</tr>
<tr>
<td>°C</td>
<td>degrees Celsius</td>
</tr>
<tr>
<td>dB</td>
<td>decibels</td>
</tr>
<tr>
<td>dBm</td>
<td>decibels-milliwatts</td>
</tr>
<tr>
<td>fF</td>
<td>femtofarads</td>
</tr>
<tr>
<td>G</td>
<td>Giga</td>
</tr>
<tr>
<td>Hz</td>
<td>Hertz</td>
</tr>
<tr>
<td>k</td>
<td>kilo, 1000</td>
</tr>
<tr>
<td>K</td>
<td>kilo, $2^{10}$</td>
</tr>
<tr>
<td>KB</td>
<td>1024 bytes, or approximately one thousand bytes</td>
</tr>
<tr>
<td>Kbit</td>
<td>1024 bits</td>
</tr>
<tr>
<td>kHz</td>
<td>kilohertz (32.000)</td>
</tr>
<tr>
<td>kΩ</td>
<td>kilohms</td>
</tr>
<tr>
<td>MHz</td>
<td>megahertz</td>
</tr>
<tr>
<td>MΩ</td>
<td>megaohms</td>
</tr>
<tr>
<td>μA</td>
<td>microamperes</td>
</tr>
<tr>
<td>μF</td>
<td>microfarads</td>
</tr>
<tr>
<td>μs</td>
<td>microseconds</td>
</tr>
<tr>
<td>μV</td>
<td>microvolts</td>
</tr>
<tr>
<td>μVrms</td>
<td>microvolts root-mean-square</td>
</tr>
<tr>
<td>mA</td>
<td>milliamperes</td>
</tr>
<tr>
<td>ms</td>
<td>milliseconds</td>
</tr>
<tr>
<td>mV</td>
<td>millivolts</td>
</tr>
<tr>
<td>nA</td>
<td>nanoamperes</td>
</tr>
<tr>
<td>ns</td>
<td>nanoseconds</td>
</tr>
<tr>
<td>nV</td>
<td>nanovolts</td>
</tr>
<tr>
<td>Ω</td>
<td>ohms</td>
</tr>
<tr>
<td>pF</td>
<td>picofarads</td>
</tr>
<tr>
<td>pp</td>
<td>peak-to-peak</td>
</tr>
<tr>
<td>ppm</td>
<td>parts per million</td>
</tr>
<tr>
<td>SPS</td>
<td>samples per second</td>
</tr>
<tr>
<td>σ</td>
<td>sigma: one standard deviation</td>
</tr>
<tr>
<td>V</td>
<td>volts</td>
</tr>
</tbody>
</table>

3.2.4 Acronyms and Initializations

This table lists the acronyms and initializations used in this document.

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABUS</td>
<td>analog output bus</td>
</tr>
<tr>
<td>AC</td>
<td>alternating current</td>
</tr>
<tr>
<td>ADC</td>
<td>analog-to-digital converter</td>
</tr>
<tr>
<td>ADV</td>
<td>advertising</td>
</tr>
<tr>
<td>AES</td>
<td>Advanced Encryption Standard</td>
</tr>
<tr>
<td>AHB</td>
<td>AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm data transfer bus</td>
</tr>
<tr>
<td>API</td>
<td>application programming interface</td>
</tr>
<tr>
<td>APOR</td>
<td>analog power-on reset</td>
</tr>
<tr>
<td>BC</td>
<td>broadcast clock</td>
</tr>
<tr>
<td>BCD</td>
<td>binary coded decimal</td>
</tr>
<tr>
<td>BESL</td>
<td>best effort service latency</td>
</tr>
<tr>
<td>BLE</td>
<td>Bluetooth Low Energy (Bluetooth Smart)</td>
</tr>
<tr>
<td>BLESS</td>
<td>BLE subsystem</td>
</tr>
<tr>
<td>BOD</td>
<td>brownout detect</td>
</tr>
<tr>
<td>BOM</td>
<td>bill of materials</td>
</tr>
<tr>
<td>BR</td>
<td>bit rate</td>
</tr>
<tr>
<td>BRA</td>
<td>bus request acknowledge</td>
</tr>
<tr>
<td>BRQ</td>
<td>bus request</td>
</tr>
<tr>
<td>CAN</td>
<td>controller area network</td>
</tr>
<tr>
<td>CI</td>
<td>carry in</td>
</tr>
<tr>
<td>CIC</td>
<td>cascaded integrator comb</td>
</tr>
<tr>
<td>CMAC</td>
<td>cipher-based message authentication code</td>
</tr>
<tr>
<td>CMP</td>
<td>compare</td>
</tr>
<tr>
<td>CO</td>
<td>carry out</td>
</tr>
<tr>
<td>COM</td>
<td>LCD common signal</td>
</tr>
<tr>
<td>CPHA</td>
<td>clock phase</td>
</tr>
<tr>
<td>CPOL</td>
<td>clock polarity</td>
</tr>
<tr>
<td>CPU</td>
<td>central processing unit</td>
</tr>
<tr>
<td>CPUSS</td>
<td>CPU subsystem</td>
</tr>
<tr>
<td>CRC</td>
<td>cyclic redundancy check</td>
</tr>
<tr>
<td>CSD</td>
<td>CapSense sigma delta</td>
</tr>
<tr>
<td>CSX</td>
<td>CapSense cross-point</td>
</tr>
<tr>
<td>CT</td>
<td>cipher text</td>
</tr>
<tr>
<td>CTB</td>
<td>continuous time block</td>
</tr>
<tr>
<td>CTBm</td>
<td>continuous time block mini</td>
</tr>
<tr>
<td>CTI</td>
<td>cross triggering interface</td>
</tr>
<tr>
<td>CTM</td>
<td>cross triggering matrix</td>
</tr>
<tr>
<td>ESR</td>
<td>equivalent series resistance</td>
</tr>
<tr>
<td>DAC</td>
<td>digital-to-analog converter</td>
</tr>
</tbody>
</table>
**Table 3-2. Acronyms and Initializations (continued)**

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAP</td>
<td>debug access port</td>
</tr>
<tr>
<td>DC</td>
<td>direct current</td>
</tr>
<tr>
<td>DES</td>
<td>Data Encryption Standard</td>
</tr>
<tr>
<td>DFF</td>
<td>D flip-flop</td>
</tr>
<tr>
<td>DI</td>
<td>digital or data input</td>
</tr>
<tr>
<td>DL</td>
<td>drive level</td>
</tr>
<tr>
<td>DMA</td>
<td>direct memory access</td>
</tr>
<tr>
<td>DMIPS</td>
<td>Dhrystone million instructions per second</td>
</tr>
<tr>
<td>DNL</td>
<td>differential nonlinearity</td>
</tr>
<tr>
<td>DO</td>
<td>digital or data output</td>
</tr>
<tr>
<td>DSI</td>
<td>digital system interconnect</td>
</tr>
<tr>
<td>DSP</td>
<td>digital signal processing</td>
</tr>
<tr>
<td>DSM</td>
<td>Deep Sleep mode</td>
</tr>
<tr>
<td>DU</td>
<td>data unit</td>
</tr>
<tr>
<td>DW</td>
<td>data wire</td>
</tr>
<tr>
<td>ECO</td>
<td>external crystal oscillator</td>
</tr>
<tr>
<td>EEPROM</td>
<td>electrically erasable programmable read only memory</td>
</tr>
<tr>
<td>EMIF</td>
<td>external memory interface</td>
</tr>
<tr>
<td>ETM</td>
<td>embedded trace macrocell</td>
</tr>
<tr>
<td>FB</td>
<td>feedback</td>
</tr>
<tr>
<td>FIFO</td>
<td>first in first out</td>
</tr>
<tr>
<td>FPU</td>
<td>floating point unit</td>
</tr>
<tr>
<td>FSR</td>
<td>full scale range</td>
</tr>
<tr>
<td>GAP</td>
<td>generic access profile</td>
</tr>
<tr>
<td>GATT</td>
<td>generic attribute profile</td>
</tr>
<tr>
<td>GFSK</td>
<td>Gaussian frequency-shift keying</td>
</tr>
<tr>
<td>GPIO</td>
<td>general-purpose I/O</td>
</tr>
<tr>
<td>HCI</td>
<td>host-controller interface (BLE stack)</td>
</tr>
<tr>
<td>HFCLK</td>
<td>high-frequency clock</td>
</tr>
<tr>
<td>HMAC</td>
<td>hashed message authentication code</td>
</tr>
<tr>
<td>HPF</td>
<td>high-pass filter</td>
</tr>
<tr>
<td>HSIOM</td>
<td>high-speed I/O matrix</td>
</tr>
<tr>
<td>I²C</td>
<td>inter-integrated circuit</td>
</tr>
<tr>
<td>I²S</td>
<td>inter-IC sound</td>
</tr>
<tr>
<td>IDE</td>
<td>integrated development environment</td>
</tr>
<tr>
<td>ILO</td>
<td>internal low-speed oscillator</td>
</tr>
<tr>
<td>ITO</td>
<td>indium tin oxide</td>
</tr>
<tr>
<td>IMO</td>
<td>internal main oscillator</td>
</tr>
<tr>
<td>INL</td>
<td>integral nonlinearity</td>
</tr>
<tr>
<td>I/O</td>
<td>input/output</td>
</tr>
<tr>
<td>IOR</td>
<td>I/O read</td>
</tr>
<tr>
<td>IOW</td>
<td>I/O write</td>
</tr>
</tbody>
</table>

**Table 3-2. Acronyms and Initializations (continued)**

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPC</td>
<td>inter-processor communication</td>
</tr>
<tr>
<td>IPTAT</td>
<td>proportional to absolute temperature</td>
</tr>
<tr>
<td>IRES</td>
<td>initial power on reset</td>
</tr>
<tr>
<td>IRA</td>
<td>interrupt request acknowledge</td>
</tr>
<tr>
<td>IRK</td>
<td>identity resolution key</td>
</tr>
<tr>
<td>IRQ</td>
<td>interrupt request</td>
</tr>
<tr>
<td>ISA</td>
<td>instruction set architecture</td>
</tr>
<tr>
<td>ISR</td>
<td>interrupt service routine</td>
</tr>
<tr>
<td>ITM</td>
<td>instrumentation trace macrocell</td>
</tr>
<tr>
<td>IVR</td>
<td>interrupt vector read</td>
</tr>
<tr>
<td>IZTAT</td>
<td>zero dependency to absolute temperature</td>
</tr>
<tr>
<td>JTAG</td>
<td>Joint Test Action Group</td>
</tr>
<tr>
<td>L2CAP</td>
<td>logical link control and adaptation protocol</td>
</tr>
<tr>
<td>LCD</td>
<td>liquid crystal display</td>
</tr>
<tr>
<td>LFCLK</td>
<td>low-frequency clock</td>
</tr>
<tr>
<td>LFSR</td>
<td>linear feedback shift register</td>
</tr>
<tr>
<td>LIN</td>
<td>local interconnect network</td>
</tr>
<tr>
<td>LJ</td>
<td>left justified</td>
</tr>
<tr>
<td>LL</td>
<td>link layer</td>
</tr>
<tr>
<td>LNA</td>
<td>low-noise amplifier</td>
</tr>
<tr>
<td>LPCOMP</td>
<td>low-power comparator</td>
</tr>
<tr>
<td>LPM</td>
<td>link power management</td>
</tr>
<tr>
<td>LR</td>
<td>link register</td>
</tr>
<tr>
<td>LRb</td>
<td>last received bit</td>
</tr>
<tr>
<td>LRB</td>
<td>last received byte</td>
</tr>
<tr>
<td>LSb</td>
<td>least significant bit</td>
</tr>
<tr>
<td>LSB</td>
<td>least significant byte</td>
</tr>
<tr>
<td>LUT</td>
<td>lookup table</td>
</tr>
<tr>
<td>MAC</td>
<td>message authentication code</td>
</tr>
<tr>
<td>MISO</td>
<td>master-in-slave-out</td>
</tr>
<tr>
<td>MMIO</td>
<td>memory mapped input/output</td>
</tr>
<tr>
<td>MOSI</td>
<td>master-out-slave-in</td>
</tr>
<tr>
<td>MPU</td>
<td>memory protection unit</td>
</tr>
<tr>
<td>MSb</td>
<td>most significant bit</td>
</tr>
<tr>
<td>MSB</td>
<td>most significant byte</td>
</tr>
<tr>
<td>MSP</td>
<td>main stack pointer</td>
</tr>
<tr>
<td>MTB</td>
<td>micro trace buffer</td>
</tr>
<tr>
<td>NI</td>
<td>next instant</td>
</tr>
<tr>
<td>NMI</td>
<td>non-maskable interrupt</td>
</tr>
<tr>
<td>NVIC</td>
<td>nested vectored interrupt controller</td>
</tr>
<tr>
<td>OE</td>
<td>output enable</td>
</tr>
<tr>
<td>OSR</td>
<td>over-sampling ratio</td>
</tr>
<tr>
<td>OVP</td>
<td>over-voltage protection</td>
</tr>
</tbody>
</table>
Table 3-2. Acronyms and Initializations (continued)

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>PA</td>
<td>power amplifier</td>
</tr>
<tr>
<td>PC</td>
<td>program counter</td>
</tr>
<tr>
<td>PCB</td>
<td>printed circuit board</td>
</tr>
<tr>
<td>PCH</td>
<td>program counter high</td>
</tr>
<tr>
<td>PCL</td>
<td>program counter low</td>
</tr>
<tr>
<td>PD</td>
<td>power down</td>
</tr>
<tr>
<td>PDU</td>
<td>protocol data unit</td>
</tr>
<tr>
<td>PGA</td>
<td>programmable gain amplifier</td>
</tr>
<tr>
<td>PHY</td>
<td>physical layer</td>
</tr>
<tr>
<td>PLD</td>
<td>programmable logic device</td>
</tr>
<tr>
<td>PM</td>
<td>power management</td>
</tr>
<tr>
<td>PMA</td>
<td>PSoC memory arbiter</td>
</tr>
<tr>
<td>POR</td>
<td>power-on reset</td>
</tr>
<tr>
<td>PPOR</td>
<td>precision power-on reset</td>
</tr>
<tr>
<td>PPU</td>
<td>peripheral protection units</td>
</tr>
<tr>
<td>PRNG</td>
<td>pseudo random number generator</td>
</tr>
<tr>
<td>PRS</td>
<td>pseudo random sequence</td>
</tr>
<tr>
<td>PSoC</td>
<td>Programmable System-on-Chip</td>
</tr>
<tr>
<td>PSP</td>
<td>process stack pointer</td>
</tr>
<tr>
<td>PSR</td>
<td>program status register</td>
</tr>
<tr>
<td>PSRR</td>
<td>power supply rejection ratio</td>
</tr>
<tr>
<td>PSSDC</td>
<td>power system sleep duty cycle</td>
</tr>
<tr>
<td>PWM</td>
<td>pulse width modulator</td>
</tr>
<tr>
<td>RAM</td>
<td>random-access memory</td>
</tr>
<tr>
<td>RETI</td>
<td>return from interrupt</td>
</tr>
<tr>
<td>RF</td>
<td>radio frequency</td>
</tr>
<tr>
<td>RNG</td>
<td>random number generator</td>
</tr>
<tr>
<td>ROM</td>
<td>read only memory</td>
</tr>
<tr>
<td>RPA</td>
<td>resolvable private address</td>
</tr>
<tr>
<td>RMS</td>
<td>root mean square</td>
</tr>
<tr>
<td>RW</td>
<td>read/write</td>
</tr>
<tr>
<td>SAR</td>
<td>successive approximation register</td>
</tr>
<tr>
<td>SARSEQ</td>
<td>SAR sequencer</td>
</tr>
<tr>
<td>SEG</td>
<td>LCD segment signal</td>
</tr>
<tr>
<td>SE0</td>
<td>single-ended zero</td>
</tr>
<tr>
<td>SC</td>
<td>switched capacitor</td>
</tr>
<tr>
<td>SCB</td>
<td>serial communication block</td>
</tr>
<tr>
<td>SIE</td>
<td>serial interface engine</td>
</tr>
<tr>
<td>SIMO</td>
<td>single input multiple output</td>
</tr>
<tr>
<td>SIO</td>
<td>special I/O</td>
</tr>
<tr>
<td>SNR</td>
<td>signal-to-noise ratio</td>
</tr>
<tr>
<td>SMPU</td>
<td>shared-noise ratio</td>
</tr>
<tr>
<td>SOF</td>
<td>start of frame</td>
</tr>
<tr>
<td>SOI</td>
<td>start of instruction</td>
</tr>
<tr>
<td>SP</td>
<td>stack pointer</td>
</tr>
<tr>
<td>SPD</td>
<td>sequential phase detector</td>
</tr>
<tr>
<td>SPI</td>
<td>serial peripheral interconnect</td>
</tr>
<tr>
<td>SPIIM</td>
<td>serial peripheral interconnect master</td>
</tr>
<tr>
<td>SPIIS</td>
<td>serial peripheral interconnect slave</td>
</tr>
<tr>
<td>SRAM</td>
<td>static random-access memory</td>
</tr>
<tr>
<td>SRROM</td>
<td>supervisory read only memory</td>
</tr>
<tr>
<td>SRSS</td>
<td>system resources subsystem</td>
</tr>
<tr>
<td>SSADC</td>
<td>single slope ADC</td>
</tr>
<tr>
<td>SSC</td>
<td>supervisor system call</td>
</tr>
<tr>
<td>SVCall</td>
<td>supervisor call</td>
</tr>
<tr>
<td>SYSCLK</td>
<td>system clock</td>
</tr>
<tr>
<td>SWD</td>
<td>single wire debug</td>
</tr>
<tr>
<td>SWV</td>
<td>serial wire viewer</td>
</tr>
<tr>
<td>TAR</td>
<td>turn-around time</td>
</tr>
<tr>
<td>TC</td>
<td>terminal count</td>
</tr>
<tr>
<td>TCPWM</td>
<td>timer, counter, PWM</td>
</tr>
<tr>
<td>TD</td>
<td>transaction descriptors</td>
</tr>
<tr>
<td>TDM</td>
<td>time division multiplexed</td>
</tr>
<tr>
<td>TFF</td>
<td>toggle flip-flop</td>
</tr>
<tr>
<td>TIA</td>
<td>trans-impedance amplifier</td>
</tr>
<tr>
<td>TPIU</td>
<td>trace port interface unit</td>
</tr>
<tr>
<td>TRM</td>
<td>technical reference manual</td>
</tr>
<tr>
<td>TRNG</td>
<td>True random number generator</td>
</tr>
<tr>
<td>UART</td>
<td>universal asynchronous receiver/transmitter</td>
</tr>
<tr>
<td>UDB</td>
<td>universal digital block</td>
</tr>
<tr>
<td>USB</td>
<td>universal serial bus</td>
</tr>
<tr>
<td>USBIO</td>
<td>USB I/O</td>
</tr>
<tr>
<td>VTOR</td>
<td>vector table offset register</td>
</tr>
<tr>
<td>WCO</td>
<td>watch crystal oscillator</td>
</tr>
<tr>
<td>WDT</td>
<td>watchdog timer</td>
</tr>
<tr>
<td>WDR</td>
<td>watchdog reset</td>
</tr>
<tr>
<td>WIC</td>
<td>wakeup interrupt controller</td>
</tr>
<tr>
<td>XRES</td>
<td>external reset</td>
</tr>
<tr>
<td>XRES_N</td>
<td>external reset, active low</td>
</tr>
</tbody>
</table>
Section B: CPU Subsystem

This section encompasses the following chapters:

- CPU Subsystem (CPUSS) chapter on page 30
- Inter-Processor Communication chapter on page 36
- Fault Monitoring chapter on page 40
- Interrupts chapter on page 47
- Protection Units chapter on page 62
- DMA Controller chapter on page 72
- Cryptographic Function Block (Crypto) chapter on page 81
- Program and Debug Interface chapter on page 85
- Nonvolatile Memory Programming chapter on page 94
- eFuse Memory chapter on page 112
- Chip Operational Modes chapter on page 113
- Device Security chapter on page 115

Top Level Architecture

CPU System Block Diagram
The CPU subsystem is based on dual 32-bit Arm Cortex CPUs, as Figure 4-1 shows. The Cortex-M4 is the main CPU. It is designed for short interrupt response time, high code density, and high 32-bit throughput while maintaining a strict cost and power consumption budget. A secondary Cortex-M0+ CPU implements security, safety, and protection features.

This section provides only an overview of the Arm Cortex CPUs in PSoC 6 MCUs. For details, see the Arm documentation sets for Cortex-M4 and Cortex-M0+.

Some PSoC 6 MCU parts have only one CPU. See the device datasheet for details.

4.1 Features

The PSoC 6 MCU Arm Cortex CPUs have the following features:

- **Cortex-M4** has a floating-point unit (FPU) that supports single-cycle digital signal processing (DSP) instructions, and a memory protection unit (MPU). Cortex-M0+ has an MPU.
- Both CPUs have 8-KB instruction caches with four-way set associativity.
- Maximum clock frequency of 150 MHz for the Cortex-M4 and 100 MHz for the Cortex-M0+.
- The Cortex-M4 implements a version of the Thumb instruction set based on Thumb-2 technology (defined in the *Armv7-M Architecture Reference Manual*). The Cortex-M0+ supports the Armv6-M Thumb instruction set (defined in the *Armv6-M Architecture Reference Manual*). See “Instruction Set” on page 35.
- Both CPUs have nested vectored interrupt controllers (NVIC) for rapid and deterministic interrupt response. For details, see the Interrupts chapter on page 47.
- Both CPUs have extensive debug support. For details, see the Program and Debug Interface chapter on page 85.
  - SWJ: combined serial wire debug (SWD) and Joint Test Action Group (JTAG) ports
  - Serial wire viewer (SWV): provides real-time trace information through the serial wire output (SWO) interface
  - Breakpoints
  - Watchpoints
  - Trace: Cortex-M4: embedded trace macrocell (ETM). Cortex-M0+: 4-KB micro trace buffer (MTB)
- Inter-processor communication (IPC) hardware – see the Inter-Processor Communication chapter on page 36.

4.2 Architecture
Each CPU is a 32-bit processor with its own 32-bit datapath and a 32-bit memory interface. Each CPU has its own set of 32-bit registers. They support a wide variety of instructions in the Thumb instruction set. They support two operating modes (see “Operating Modes and Privilege Levels” on page 34).

The Cortex-M4 instruction set includes:
- Signed and unsigned, 32×32 → 32-bit and 32×32 → 64-bit, multiply and multiply-accumulate, all single-cycle
- Signed and unsigned 32-bit divides that take two to 12 cycles
- DSP instructions
- Complex memory-load and store access
- Complex bit manipulation; see the bitfield instructions in Table 4-6

The Cortex-M4 FPU has its own set of registers and instructions. It is compliant with the ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic.

The Cortex-M0+ has a single cycle 32x32 → 32-bit signed multiplication instruction.

4.2.1 Address and Memory Maps

Both CPUs have a fixed address map, with shared access to memory and peripherals. The 32-bit (4 GB) address space is divided into the regions shown in Table 4-1. Note that code can be executed from the code and SRAM regions.

<table>
<thead>
<tr>
<th>Address Range</th>
<th>Name</th>
<th>Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00000000 – 0x1FFFFFFF</td>
<td>Code</td>
<td>Program code region. You can also put data here. It includes the exception vector table, which starts at address 0.</td>
</tr>
<tr>
<td>0x20000000 – 0x3FFFFFFF</td>
<td>SRAM</td>
<td>Data region. You can also execute code from this region. Note that Cortex-M4 bit-band in this region is not supported.</td>
</tr>
<tr>
<td>0x40000000 – 0x5FFFFFFF</td>
<td>Peripheral</td>
<td>All peripheral registers. Code cannot be executed from this region. Note that Cortex-M4 bit-band in this region is not supported.</td>
</tr>
<tr>
<td>0x60000000 – 0x9FFFFFFF</td>
<td>External RAM</td>
<td>SMIF (see the Serial Memory Interface (SMIF) chapter on page 257). You can execute code from this region.</td>
</tr>
<tr>
<td>0xA0000000 – 0xDFFFFFFF</td>
<td>External device</td>
<td>Not used</td>
</tr>
<tr>
<td>0xE0000000 – 0xE00FFFFF</td>
<td>Private peripheral bus (PPB)</td>
<td>Provides access to peripheral registers within the CPU core.</td>
</tr>
<tr>
<td>0xE0100000 – 0xFFFFFFFF</td>
<td>Device</td>
<td>Device-specific system registers.</td>
</tr>
</tbody>
</table>

The device memory map shown in Table 4-2 applies to both CPUs. That is, the CPUs share access to all PSoC 6 MCU memory and peripheral registers.

<table>
<thead>
<tr>
<th>Address Range</th>
<th>Name</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00000000 – 0x00020000</td>
<td>SROM</td>
<td>128 Kbytes. See section 1.3.5 SROM</td>
</tr>
<tr>
<td>0x08000000 – 0x08048400</td>
<td>SRAM</td>
<td>Up to 288 Kbytes. See section 1.3.4 SRAM</td>
</tr>
<tr>
<td>0x10000000 – 0x10100000</td>
<td>User Flash</td>
<td>Up to 1 Mbyte. See section 1.3.3 Flash</td>
</tr>
<tr>
<td>0x14000000 – 0x14008000</td>
<td>Working Flash</td>
<td>32K for EEPROM emulation</td>
</tr>
<tr>
<td>0x16000000 – 0x16008000</td>
<td>Supervisory Flash</td>
<td>32K for secure access</td>
</tr>
</tbody>
</table>

Note that SRAM is located in the Code region for both CPUs (see Table 4-1). This facilitates executing code out of SRAM. There is no physical memory located in the CPUs’ SRAM region.
4.3 Registers

Both CPUs have sixteen 32-bit registers, as Table 4-3 shows. See the Arm documentation for details.

- R0 to R12 – General-purpose registers. R0 to R7 can be accessed by all instructions; the other registers can be accessed by a subset of the instructions.
- R13 – Stack pointer (SP). There are two stack pointers, with only one available at a time. In thread mode, the CONTROL register indicates the stack pointer to use – Main Stack Pointer (MSP) or Process Stack Pointer (PSP).
- R14 – Link register. Stores the return program counter during function calls.
- R15 – Program counter. This register can be written to control program flow.

<table>
<thead>
<tr>
<th>Name</th>
<th>Typea</th>
<th>Reset Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>R0 – R12</td>
<td>RW</td>
<td>Undefined</td>
<td>R0–R12 are 32-bit general-purpose registers for data operations.</td>
</tr>
<tr>
<td>MSP (R13)</td>
<td>RW</td>
<td>[0x00000000]</td>
<td>The stack pointer (SP) is register R13. In thread mode, bit[1] of the CONTROL register indicates the stack pointer to use: 0 = Main stack pointer (MSP). This is the reset value. 1 = Process stack pointer (PSP). On reset, the processor loads the MSP with the value from address 0x00000000.</td>
</tr>
<tr>
<td>PSP (R13)</td>
<td>RW</td>
<td>[0x00000000]</td>
<td>The stack pointer (SP) is register R13. In thread mode, bit[1] of the CONTROL register indicates the stack pointer to use: 0 = Main stack pointer (MSP). This is the reset value. 1 = Process stack pointer (PSP). On reset, the processor loads the MSP with the value from address 0x00000000.</td>
</tr>
<tr>
<td>LR (R14)</td>
<td>RW</td>
<td>See noteb</td>
<td>The link register (LR) is register R14. It stores the return information for subroutines, function calls, and exceptions.</td>
</tr>
<tr>
<td>PC (R15)</td>
<td>RW</td>
<td>[0x00000004]</td>
<td>The program counter (PC) is register R15. It contains the current program address. On reset, the processor loads the PC with the value from address 0x00000004. Bit[0] of the value is loaded into the EPSR T-bit (see Table 4-4) at reset; it must always be 1.</td>
</tr>
<tr>
<td>PSR</td>
<td>RW</td>
<td>Undefined</td>
<td>The program status register (PSR) combines: Application Program Status Register (APSR). Execution Program Status Register (EPSR). Interrupt Program Status Register (IPSR).</td>
</tr>
<tr>
<td>APSR</td>
<td>RW</td>
<td>Undefined</td>
<td>The APSR contains the current state of the condition flags from previous instruction executions.</td>
</tr>
<tr>
<td>EPSR</td>
<td>RO</td>
<td>0x01000000</td>
<td>On reset, the EPSR Thumb state bit is loaded with the value bit[0] of the register [0x00000004]. It must always be 1. In Cortex-M4, other bits in this register control the state of interrupt-continuable instructions and the if-then (IT) instruction.</td>
</tr>
<tr>
<td>IPSR</td>
<td>RO</td>
<td>0</td>
<td>The IPSR contains the current exception number.</td>
</tr>
<tr>
<td>PRIMASK</td>
<td>RW</td>
<td>0</td>
<td>The PRIMASK register prevents activation of all exceptions with configurable priority.</td>
</tr>
<tr>
<td>CONTROL</td>
<td>RW</td>
<td>0</td>
<td>The CONTROL register controls: - The privilege level in Thread mode; see 4.4 Operating Modes and Privilege Levels. - The currently active stack pointer, MSP or PSP. - Cortex-M4 only: whether to preserve the floating-point state when processing an exception.</td>
</tr>
<tr>
<td>FAULTMASK</td>
<td>RW</td>
<td>0</td>
<td>Cortex-M4 only. Bit 0 = 1 prevents the activation of all exceptions except NMI.</td>
</tr>
<tr>
<td>BASEPRI</td>
<td>RW</td>
<td>0</td>
<td>Cortex-M4 only. When set to a nonzero value, prevents processing any exception with a priority greater than or equal to the value.</td>
</tr>
</tbody>
</table>

a. Describes access type during program execution in thread mode and handler mode. Debug access can differ.

b. LR reset value is 0xFFFFFFFF in Cortex-M4, undefined in Cortex-M0+. 
The Cortex-M4 floating-point unit (FPU) also has the following registers:

- Thirty-two 32-bit single-precision registers, S0 to S31. These registers can also be addressed as sixteen 64-bit double-precision registers, D0 to D15.

- Five FPU control and status registers:
  - CPACR – Coprocessor Access Control Register
  - FPCCR – Floating-point Context Control Register
  - FPCAR – Floating-point Context Address Register
  - FPSCR – Floating-point Status Control Register
  - FPDSCR – Floating-point Default Status Control Register

For more information on how these registers are used, see the Arm Cortex-M4 documentation.

Use the MSR and MRS instructions to access the PSR, PRIMASK, CONTROL, FAULTMASK, and BASEPRI registers. Table 4-4 and Table 4-5 show how the PSR bits are assigned.

Table 4-4. Cortex-M4 PSR Bit Assignments

<table>
<thead>
<tr>
<th>Bit</th>
<th>PSR Register</th>
<th>Name</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>APSR</td>
<td>N</td>
<td>Negative flag</td>
</tr>
<tr>
<td>30</td>
<td>APSR</td>
<td>Z</td>
<td>Zero flag</td>
</tr>
<tr>
<td>29</td>
<td>APSR</td>
<td>C</td>
<td>Carry or borrow flag</td>
</tr>
<tr>
<td>28</td>
<td>APSR</td>
<td>V</td>
<td>Overflow flag</td>
</tr>
<tr>
<td>27</td>
<td>APSR</td>
<td>Q</td>
<td>DSP overflow and saturation flag</td>
</tr>
<tr>
<td>26 – 25</td>
<td>EPSR</td>
<td>IC/IT</td>
<td>Control interrupt-continuable and IT instructions</td>
</tr>
<tr>
<td>24</td>
<td>EPSR</td>
<td>T</td>
<td>Thumb state bit. Must always be 1. Attempting to execute instructions when the T bit is 0 results in a HardFault exception.</td>
</tr>
<tr>
<td>23 – 20</td>
<td>–</td>
<td>–</td>
<td>Reserved</td>
</tr>
<tr>
<td>19 – 16</td>
<td>APSR</td>
<td>GE</td>
<td>Greater than or equal flags, for the SEL instruction</td>
</tr>
<tr>
<td>15 – 10</td>
<td>EPSR</td>
<td>IC/TI</td>
<td>Control interrupt-continuable and IT instructions</td>
</tr>
<tr>
<td>9</td>
<td>–</td>
<td>–</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| 8 – 0 | IPSR | ISR_NUMBER | Exception number of current ISR:  
0 = thread mode  
1 = reserved  
2 = NMI  
3 = HardFault  
4 = MemManage  
5 = BusFault  
6 = UsageFault  
7 – 10 = reserved  
11 = SVC  
12 = reserved for debug  
13 = reserved  
14 = PendSV  
15 = SysTick (see “System Tick (SysTick) Exception” on page 53)  
16 = IRQ0  
…  
255 = IRQ240 |
4.4 Operating Modes and Privilege Levels

Both CPUs support two operating modes and two privilege levels:

- **Operating Modes:**
  - Thread Mode – used to execute application software. The processor enters Thread mode when it comes out of reset.
  - Handler Mode – used to handle exceptions. The processor returns to Thread mode when it has finished all exception processing.

- **Privilege Levels:**
  - Unprivileged – the software has limited access to the MSR and MRS instructions, and cannot use the CPSID and CPSIE instructions. It cannot access the system timer, NVIC, or system control block. It may have restricted access to memory or peripherals.
  - Privileged – the software can use all the instructions and has access to all resources.

In Thread mode, the CONTROL register controls whether software execution is privileged or unprivileged. In Handler mode, software execution is always privileged.

Only privileged software can write to the CONTROL register to change the privilege level. Unprivileged software can use the SVC instruction to transfer control to privileged software.

In Handler mode, the MSP is always used. The exception entry and return mechanisms automatically update the CONTROL register, which may change whether MSP/PSP is used.

In Thread mode, use the MSR instruction to set the stack pointer bit in the CONTROL register. When changing the stack pointer, use an ISB instruction immediately after the MSR instruction. This ensures that instructions after the ISB execute using the new stack pointer.

### Table 4-5. Cortex-M0+ PSR Bit Assignments

<table>
<thead>
<tr>
<th>Bit</th>
<th>PSR Register</th>
<th>Name</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>APSR</td>
<td>N</td>
<td>Negative flag</td>
</tr>
<tr>
<td>30</td>
<td>APSR</td>
<td>Z</td>
<td>Zero flag</td>
</tr>
<tr>
<td>29</td>
<td>APSR</td>
<td>C</td>
<td>Carry or borrow flag</td>
</tr>
<tr>
<td>28</td>
<td>APSR</td>
<td>V</td>
<td>Overflow flag</td>
</tr>
<tr>
<td>27 – 25</td>
<td>–</td>
<td>–</td>
<td>Reserved</td>
</tr>
<tr>
<td>24</td>
<td>EPSR</td>
<td>T</td>
<td>Thumb state bit. Must always be 1. Attempting to execute instructions when the T bit is 0 results in a HardFault exception.</td>
</tr>
<tr>
<td>23 – 6</td>
<td>–</td>
<td>–</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>5 – 0</th>
<th>IPSR</th>
<th>Exception Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 – 0</td>
<td>–</td>
<td>Exception number of current ISR:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = thread mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2 = NMI</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3 = HardFault</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4 – 10 = reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11 = SVCall</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12, 13 = reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td>14 = PendSV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>15 = SysTick</td>
</tr>
<tr>
<td></td>
<td></td>
<td>16 = IRQ0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>…</td>
</tr>
<tr>
<td></td>
<td></td>
<td>47 = IRQ31</td>
</tr>
</tbody>
</table>
4.5 Instruction Set

Both CPUs implement subsets of the Thumb instruction set, as Table 4-6 shows. The table does not show the large number of variants and conditions of the instructions. For details, see one of the Arm Cortex Generic User Guides or Technical Reference Manuals.

An instruction operand can be a register, a constant, or another instruction-specific parameter. Instructions act on the operands and often store the result in a destination register. Many instructions have restrictions on using the PC or SP for the operands or destination register. See the Arm documentation for details.

Table 4-6. Instruction Set Summary – Cortex-M4 and Cortex-M0+

<table>
<thead>
<tr>
<th>Functional Group</th>
<th>Cortex-M4</th>
<th>Cortex-M0+</th>
<th>Brief List of Instruction Mnemonics</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory access</td>
<td>✔</td>
<td>✔</td>
<td>LDR, STR, ADR, PUSH, POP</td>
</tr>
<tr>
<td>General data processing</td>
<td>✔</td>
<td>✔</td>
<td>Cortex-M0+: ADD, ADC, AND, ASR, BICS, CMN, CMP, EOR, LSL, LSR, MOV, MVNS, ORR, REV, ROR, SBC, SUB, SXT, UXT, TST</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Cortex-M4 has all of the above plus: CLZ, ORN, RRX, SADD, SAS, SSA, SSUB, TEQ, UADD, UAS, USA, USUB</td>
</tr>
<tr>
<td>Multiply and divide</td>
<td>✔</td>
<td>MUL only</td>
<td>MLA, MLS, MUL, SDIV, SMLA, SMLS, SMMLA, SMMLS, SMU, SMA, SMU, SMUS, UDIV, UMAAL, UMLAL, UMLLA, UMULL</td>
</tr>
<tr>
<td>Saturating</td>
<td>✔</td>
<td>–</td>
<td>SSAT, USAT, QADD, QSUB, QASX, QSAX, QDADD, QDSUB, UQADD, UQASX, UQSUB</td>
</tr>
<tr>
<td>Packing and unpacking</td>
<td>✔</td>
<td>–</td>
<td>PKH, SXT, SXTA, UXT, UXTA</td>
</tr>
<tr>
<td>Bitfield</td>
<td>✔</td>
<td>–</td>
<td>BFC, BFI, SBFX, UBFX</td>
</tr>
<tr>
<td>Branch and control</td>
<td>✔</td>
<td>✔</td>
<td>Cortex-M0+: B(cc), BL, BLX, BX</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Cortex-M4 has all of the above plus: CBNZ, CBZ, IT, TB</td>
</tr>
<tr>
<td>Miscellaneous</td>
<td>✔</td>
<td>✔</td>
<td>CPSID, CPSIE, DMB, DSB, ISB, MRS, MSR, NOP, SEV, SVC, WFE, WFI</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Cortex-M4 has all of the above plus BKPT</td>
</tr>
<tr>
<td>Floating-point</td>
<td>✔</td>
<td>–</td>
<td>VABS, VADD, VCMP, VCVT, VDIV, VFMA, VFNMA, VFMS, VFNMS, VLD, VLMA, VLM, VMOV, VMRS, VMSR, VMUL, VNEG, VNMLA, VNMLS, VNMUL, VPOP, VPUSH, VSQRT, VST, VSUB</td>
</tr>
</tbody>
</table>
5. Inter-Processor Communication

Inter-processor communication (IPC) provides the functionality for multiple processors to communicate and synchronize their activities. IPC hardware is implemented using two register structures.

- IPC Channel: Communication and synchronization between processors is achieved using this structure.
- IPC Interrupt: Each interrupt structure configures an interrupt line, which can be triggered by a ‘notify’ or ‘release’ event of any IPC channel.

5.1 Features

The features of IPC are as follows:

- Implements locks for mutual exclusion between processors
- Allows sending messages between processors
- Supports up to 16 channels for communication
- Supports up to 16 interrupts, which can be triggered using notify or release events from the channels

5.2 Architecture

5.2.1 IPC Channel

An IPC channel is implemented as five hardware registers, as shown in Figure 5-1. The IPC channel registers are accessible to all the processors in the system.

- IPC_ACQUIRE: This register determines the lock feature of the IPC. The IPC channel is acquired by reading this register. If the SUCCESS field returns a ‘1’, the read acquired the lock. If the SUCCESS field returns a ‘0’, the read did not acquire the lock.
  Note that a single read access performs two functions:
  - The attempt to acquire a lock.
  - Return the result of the acquisition attempt (SUCCESS field).
  The atomicity of these two functions is essential in a CPU with multiple tasks that can preempt each other.
  The register also has bitfields that provide information about the processor that acquired it. When acquired, this register is released by writing any value into the IPC_RELEASE register. If the register was already in an acquired state another attempt to read the register will not be able to acquire it.
- IPC_NOTIFY: This register is used to generate an IPC notify event. Each bit in this register corresponds to an IPC interrupt structure. The notify event generated from an IPC channel can trigger any or multiple interrupt structures.
- IPC_RELEASE: Any write to this register will release the IPC channel. This register also has a bit that corresponds to each IPC interrupt structure. The release event generated from an IPC channel can trigger any or multiple interrupt structures. To only release the IPC channel and not generate an interrupt, you can write a zero into the IPC release register.
- IPC_DATA: This is a 32-bit register meant to hold data. It can be considered as the shared data memory for the channel. Typically, this register will hold messages that need to be communicated between processors. If the messages are larger than the 32-bit size, place a pointer in the IPC_DATA register.
- IPC_LOCK_STATUS: This register provides the instantaneous lock status for the IPC channel. The register provides details if the channel is acquired. If acquired, it provides the processor’s ID, protection context, and other details. The
reading of lock status provides only an instantaneous status, which can be changed in the next cycle based on the activity of other processors on the channel.

![IPC Channel Structure](image)

### 5.2.2 IPC Interrupt

Each IPC interrupt line in the system has a corresponding IPC interrupt structure. An IPC interrupt can be triggered by a notify or a release event from any of the IPC channels in the system. You can choose to mask any of the sources of these events using the IPC interrupt registers. Figure 5-2 shows the registers in an IPC Interrupt structure.

**IPC_INTR:** This register provides the instantaneous status of the interrupt sources. Note that there are 16 notify and 16 release event bits in this register. These are the notify and release events corresponding to the 16 IPC channels. When a notify event is triggered in the IPC channel 0, the corresponding Notify0 bit is activated in the interrupt registers. A write of ‘1’ to a bit will clear the interrupt.

**IPC_INTR_MASK:** The bit in this register masks the interrupt sources. Only the interrupt sources with their masks enabled can trigger the interrupt.

**IPC_INTR_SET:** A write of ‘1’ into this register will set the interrupt.

**IPC_INTR_MASKED:** This register provides the instantaneous value of the interrupts after they are masked. The value in this register is (IPC_INTR AND IPC_INTR_MASK).

![IPC Interrupt Structure](image)

### 5.2.3 IPC Channels and Interrupts

The IPC block has a set of IPC interrupts associated with it. Each IPC interrupt register structure corresponds to an IPC interrupt line. This interrupt can trigger an interrupt on any of the processors in the system. The interrupt routing for processors are dependent on the device architecture.

Each IPC channel has a release and notify register, which can drive events on any of the IPC interrupts. An illustration of this relation between the IPC channels and the IPC interrupt structure is shown in Figure 5-3.
5.3 Implementing Locks

The IPC channels can be used to implement locks. Locks are typically used in multi-core systems to implement some form of mutually exclusive access to a shared resource. When multiple processors share a resource, the processors are capable of acquiring and releasing the IPC channel. So the processor can assume an IPC channel as a lock. The semantics of this code is that access to the shared resource is gated by the processor's ownership of the channel. So the processors will need to acquire the IPC channel before they access the shared resource.

A failure to acquire the IPC channel signifies a lock on the shared resource because another processor has control of it. Note that the IPC channel will not enforce which processor acquires or releases the channel. All processors can acquire or release the IPC channel and the semantics of the code must make sure that the processor that acquires the channel is the one that releases it.

5.4 Message Passing

IPC channels can be used to communicate messages between processors. In this use case, the channel is used in conjunction with the interrupt structures. The IPC channel is used to lock the access to the Data register. The IPC channel is acquired by the sender and used to populate the message. The receiver reads the message and then releases the channel. Thus, between the sender putting data into the channel and receiver reading it, the channel is locked for all other task access. The sender uses a notify event on the receiver's IPC interrupt to denote a send operation. The receiver acts on this interrupt and reads the data from the data register. After the reception is complete, the receiver releases the channel and can also generate a release event to the sender's IPC interrupt. Note that the action of locking the channel does not, in hardware, restrict access to the data register. This is a semantic that should be enforced by software.

Figure 5-4 portrays an example of a sender (Processor A) sending data to a receiver (Processor B). IPC interrupt A is
Inter-Processor Communication

configured to interrupt Processor A. IPC interrupt B is configured to interrupt Processor B.

1. The sender will attempt to acquire the IPC channel by reading the IPC_ACQUIRE register. If the channel was acquired, the sender has ownership of the channel for data transmission. If the channel was not acquired, the processor should wait until the channel is free for acquisition. This can be done by polling the IPC channel’s IPC_LOCK_STATUS register.

2. After the IPC channel is acquired, the sender has control of the channel for communication and places the 32-bit message data in the IPC_DATA register.

3. Now that the message is placed in the IPC channel, the sender generates a notify event on the receiver’s interrupt line. It does this by setting the corresponding bit in the IPC channel’s IPC_NOTIFY register. This event creates a notify event at IPC interrupt B. If the IPC channel’s notify event was enabled by setting the mask bit in the IPC interrupt B, this will generate an interrupt in the receiver.

4. When it receives IPC interrupt B, the receiver can poll the IPC_INTR_MASKED register to understand which IPC channel had triggered the notify event. Based on this, the receiver identifies the channel to read and reads from the IPC channel’s IPC_DATA register. The receiver has now received the data sent by the sender. It needs to release the channel so that other processors/processes can use it.

5. The receiver releases the channel. It also optionally generates a release event on the sender’s IPC interrupt A. This will generate a release event interrupt on the sender if the corresponding channel release event was masked.

On receiving the release interrupt, the sender can act on the event based on the application requirement. It can either try to reacquire the channel for further transmission or go on to other tasks because the transmission is complete.

In the previous example, the size of the data being transmitted was just 32 bits. Larger messages can be sent as pointers. The sender can allocate a larger message structure in memory and pass the pointer in the 32-bit data register. Figure 5-5 shows the usage. Note that the user code must implement the synchronization of the message read process.

- The implementation can stall the channel until the receiver has used up all the data in the message packet and the message packet can be rewritten. This is wasteful because it will stall other inter-process communications as the number of IPC channels is limited.

- The receiver can release the channel as soon as it receives the pointer to the message packet. It implements the synchronization logic in the message packet as a flag, which the sender sets on write complete and receiver clears on a read complete.

![Figure 5-4. Sending Messages using IPC](image)

![Figure 5-5. Communicating Larger Messages](image)
6. Fault Monitoring

Fault monitoring allows you to monitor various faults generated within the device and take actions based on the fault reported. The fault structures present in the PSoC 6 MCU monitor access violation faults at protection units (MPU, SMPU, or PPU) and flash controller bus error/fault. In addition to reporting faults, the fault structures in PSoC 6 MCUs provide mechanism to log data from the fault sources and optionally perform soft reset.

The PSoC 6 MCU family supports two centralized fault report/monitoring structures that monitor faults generated within the device. Each fault report structure can monitor and report faults from up to 96 sources.

6.1 Features

Each PSoC 6 MCU fault report structure supports:
- Monitoring protection unit access violation faults and flash controller bus errors
- Four 32-bit data registers to record fault information
- Soft reset on fault detection while retaining the fault information
- Interrupt on fault detection
- Trigger output to DMA for fault data transfer
- Fault detected output to a pin for external fault handling

6.2 Architecture

![Fault Report Structure Diagram]

Fault source 0 to Fault source 95

Fault Data

Pending faults

Fault report Structure[x]

Fault report Structure [0]

Fault Data

Fault Data

Interrupt fault[x]

Fault_out[x]

Fault_reset_req[x]

Retained during soft reset

Single structure used by all fault report structures
Fault Monitoring

The PSoC 6 MCU family uses centralized fault report structures. This centralized nature allows for a system wide handling of faults simplifying firmware development. Only a single fault interrupt handler is required to monitor multiple faults. The fault report structure provides the fault source and additional fault specific information through a single set of registers; no iterative search for the fault source and fault information is required.

The fault structure can be configured to capture one or more faults as listed in Table 6-2. When the configured fault is triggered, the structure captures the fault along with the fault information provided by the source. The fault is initially recorded and only if a fault structure is configured to capture the fault and free (does not contain an already captured fault), the fault request is acknowledged and fault data is captured in the fault structure registers. In addition, a successful capture can trigger an interrupt and be processed by either Cortex-M4 or Cortex-M0+ depending on the application requirement.

It should be noted that each fault structure is capable of capturing only one fault at a time and as long as that fault is not serviced, subsequent faults will not be captured by the fault structure. In addition to capturing faults, the fault structure can optionally perform a soft reset while retaining the fault information. This reset results in RESET_ACT_FAULT reset cause in the SRSS_RES_CAUSE register.

6.2.1 Fault Report

The PSoC 6 MCU family supports two fault report structures. Each fault report structure has a dedicated set of control and status registers. Each fault report structure captures a single fault. The captured fault information includes:

- Fault validity bit that indicates a fault is captured (VALID bit [31] of the CPUSS_FAULTx_STATUS register). This bit is set whenever a fault is captured. The bit should be cleared after processing the fault information. New faults are captured only when this bit is ‘0’.
- Fault index, as shown in Table 6-2, identifies the fault source (IDX bits [6:0] of CPUSS_FAULTx_STATUS)
- Additional fault information describing fault specifics (CPUSS_FAULTx_DATA0 through CPUSS_FAULTx_DATA3 registers). This additional information is fault source specific. For example, an MPU protection violation provides information on the violating bus address, the bus master identifier, and bus access control information in only two FAULT_DATA registers. The details of the fault information for various faults is explained in Table 6-1.
<table>
<thead>
<tr>
<th>Fault Source</th>
<th>Fault Information</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPU/SMPU violation</td>
<td>DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31]: '0': MPU violation; '1': SMPU violation.</td>
</tr>
<tr>
<td>Flash controller bus error</td>
<td>FAULT_DATA0[31:0]: Violating address. FAULT_DATA1[31]: '0': FLASH macro interface bus error; '1': memory hole. FAULT_DATA1[15:12]: Protection context identifier. FAULT_DATA1[11:8]: Master identifier.</td>
</tr>
</tbody>
</table>
6.2.2 Signaling Interface

In addition to captured fault information, each fault report structure supports a signaling interface to notify the system about the captured fault. The interface of fault report structure 'x' supports the following:

- A fault interrupt (interrupt_fault[x]). Use the CPUSS_FAULTx_INTR, CPUSS_FAULTx_INTR_SET, CPUSS_FAULTx_INTR_MASK and CPUSS_FAULTx_INTR_MASKED registers to monitor, set, and mask the Fault_STRUCTURE[x]'s interrupt. Only a single interrupt cause is available, which indicates that a fault is detected. The fault report registers be read in the interrupt handler to deduce the fault. The FAULT bit [0] of the CPUSS_FAULTx_INTR_MASK register provides a mask/enable for the interrupt. The FAULT bit [0] of the CPUSS_FAULTx_INTR register is set to '1' when a fault is captured. Setting this bit in firmware clears the interrupt.

- A DMA trigger (tr_fault[x]). The fault structure generates a DMA trigger when VALID bit [31] of the CPUSS_FAULTx_STATUS register is set. To enable the trigger, set the TR_EN bit [0] of the CPUSS_FAULTx_CTL register. The trigger can be connected to a DMA controller, which can transfer captured fault information from the fault report structure to memory and can clear the VALID bit [31] of the CPUSS_FAULTx_STATUS register.

- A chip output signal (fault_out[x]). The fault structure generates an output signal, which is set when VALID bit [31] of the CPUSS_FAULTx_STATUS register is set. This signal can be routed out of the device through the HSIOM (refer to the device datasheet). The output signal is enabled by setting the OUT_EN bit [1] of the CPUSS_FAULTx_CTL register. The output signal can be used to communicate non-recoverable faults to off-chip components (possibly resulting in a reset of the chip).

- A fault reset request signal (fault_reset_req[x]). The fault structure generates a soft reset when VALID bit [31] of the CPUSS_FAULTx_STATUS register is set. The reset capability is enabled by setting RESET_REQ_EN bit [2] of CPUSS_FAULTx_CTL. The reset request performs a soft reset. This reset request performs a soft reset. The fault information in CPUSS_FAULTx_STATUS and CPUSS_FAULTx_DATA registers is retained through this reset.

Because the device has a single fault_reset_req signal, the individual fault_reset_req[x] signals from the fault structures are combined into a single fault_reset_req signal as shown in Figure 6-2.

![Figure 6-2. Fault Reset Request](image)

6.2.3 Monitoring

A central structure, which is shared by all fault report structures, keeps track of all pending faults in the system. The CPUSS_FAULTx_PENDING0, CPUSS_FAULTx_PENDING1, CPUSS_FAULTx_PENDING2 registers reflect what fault sources are pending. The registers provide a single pending bit for up to 96 fault sources. The CPUSS_FAULTx_PENDING registers are mirrored in all the fault report structures – the registers read the same value in all fault structures. The bit indexing in the registers follow the fault index captured in Table 6-2. For instance, bit [0] of CPUSS_FAULTx_PENDING0 captures a CM0+ MPU/SMPU violation and bit [1] of CPUSS_FAULTx_PENDING1 captures a peripheral group#1 PPU violation.

The pending faults are faults that are not yet captured by a fault structure. When a pending fault is captured by a fault structure, the associated pending bit is cleared to '0'.

Each fault report structure is selective in the faults it captures. The CPUSS_FAULTx_MASK0, CPUSS_FAULTx_MASK1, CPUSS_FAULTx_MASK2 registers of a fault structure decide the pending faults that it captures. These faults are referred to as "enabled" faults. The CPUSS_FAULTx_MASK registers are unique to each fault structure. This allows for the following:

- One fault report structure is used to capture recoverable faults and one fault report structure is used to capture non-recoverable faults. The former can be used to generate a fault interrupt and the latter can be used to activate a chip output signal and/or activate a reset request.

- Two fault report structures are used to capture the same faults. The first fault is captured by the structure with the lower index (for example, fault structure 0) and the second fault is captured by the structure with the higher index (for example, fault structure 1). Note that both structures cannot capture the same fault at the same time. As soon as a fault is captured, the pending bit is cleared and the other structure will not be aware of the fault. Fault structure 0 has precedence over fault structure 1.
The fault structure captures “enabled” faults only when VALID bit [31] of CPUSS_FAULTx_STATUS register is ‘0’. When a fault is captured, hardware sets the VALID bit [31] of the CPUSS_FAULTx_STATUS register. In addition, hardware clears the associated pending bit to ‘0’. When a fault structure is processed, firmware or a DMA transfer should clear the VALID bit [31] of the CPUSS_FAULTx_STATUS register. Note that fault capturing does not consider FAULT bit [0] of CPUSS_FAULTx_INTR register and firmware should clear the bit after servicing the interrupt, if the interrupt is enabled.

### 6.2.4 Low-power Mode Operation

The fault report structure functionality is available in Active and Sleep (and their LP counterparts) power modes only. The interfaces between the fault sources and the fault report structures is reset in Deep Sleep power mode. Because the fault report structure is an active functionality, pending faults (in the CPUSS_FAULTx_PENDING registers) are not retained when transitioning to Deep Sleep power mode. The fault structure’s registers can be partitioned based on the reset domain and their retention capability as follows:

- **Active reset domain:** CPUSS_FAULTx_PENDING, CPUSS_FAULTx_INTR, CPUSS_FAULTx_INTR_SET, and CPUSS_FAULTx_INTR_MASKED registers. These registers are not retained in Deep Sleep power mode.
- **Deep Sleep reset domain:** CPUSS_FAULTx_CTL, CPUSS_FAULTx_MASK, and CPUSS_FAULTx_INTR_MASK registers. These registers are retained in Deep Sleep power mode but any system reset will reset these registers to the default state.
- **Hard reset domain:** CPUSS_FAULTx_STATUS and CPUSS_FAULTx_DATA registers. These registers are retained through soft resets (detectable in SRSS_RES_CAUSE registers). However, hard resets such as XRES/POR/BOD will reset the registers.

### 6.2.5 Using a Fault Structure

Follow these steps to configure and use a fault structure:

1. Identify the faults from Table 6-2 to be monitored in the system.
2. For firmware fault handling through interrupts
   a. Set the FAULT bit [0] of the CPUSS_FAULTx_INTR_MASK register.
   b. Set the FAULT bit [0] of the CPUSS_FAULTx_INTR register to clear any pending interrupt.
   c. Enable the CPUSS_FAULTx interrupt to the CPU by configuring the appropriate ISER register. Refer to the Interrupt chapter on page 47.
3. For fault handling through DMA
   a. Set the TR_EN bit [0] of the CPUSS_FAULTx_CTL register.

   b. Route the tr_fault[x] signal to the trigger input DMA controller. Refer to the Trigger Multiplexer Block chapter on page 197.
   c. Configure and enable the DMA controller to transfer CPUSS_FAULTx_STATUS and CPUSS_FAULTx_DATA registers to memory and write back ‘0’ to CPUSS_FAULTx_STATUS register after the transfer is complete. Refer to the DMA Controller chapter on page 72.

4. For fault handling outside the device
   b. Route the fault_out[x] signal to a pin through HSIOM. Refer to the device datasheet.
   c. Use the signal externally for processing the fault – generate external reset, power cycle, or log fault information.

5. Set the RESET_REQ_EN bit [2] of the CPUSS_FAULTx_CTL register, if a soft reset is required on any fault detection in the structure.


7. Set the fault index bits in the CPUSS_FAULTx_MASK registers for faults that need to be captured by the fault structure as explained in 6.2.3 Monitoring.

### 6.2.6 CPU Exceptions Versus Fault Monitoring

Some faults captured in Table 6-2 also result in bus errors or CPU exceptions (Cortex-M4 Bus/Usage/Memory/Hard faults). The faults can be communicated in two ways:

- As a bus error to the master of the faulting bus transfer. This will result in Bus, Usage, Memory, or Hard fault exceptions in the CPU.
- As a fault in a fault report structure. This fault can be communicated as a fault interrupt to any processor in the system. This allows fault handling on a processor that is not the master of the faulting bus transfer. It is useful for faults that cause the master of the faulting transfer to become unresponsive or unreliable.
### 6.3 Fault Sources

The fault sources can vary between device families. Table 6-2 provides the list of fault sources available in PSoC 6 MCUs.

<table>
<thead>
<tr>
<th>Fault Index</th>
<th>Source</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>cpuss.mpu_vio[0]</td>
<td>CM0+ MPU/SMPU violation</td>
</tr>
<tr>
<td>1</td>
<td>cpuss.mpu_vio[1]</td>
<td>CRYPTO MPU/SMPU violation</td>
</tr>
<tr>
<td>2</td>
<td>cpuss.mpu_vio[2]</td>
<td>DW0 MPU/SMPU violation</td>
</tr>
<tr>
<td>3</td>
<td>cpuss.mpu_vio[3]</td>
<td>DW1 MPU/SMPU violation</td>
</tr>
<tr>
<td>4 to 13</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>cpuss.mpu_vio[14]</td>
<td>CM4 MPU/SMPU violation (I/D bus)</td>
</tr>
<tr>
<td>15</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>cpuss.mpu_vio[16]</td>
<td>CM4 MPU/SMPU violation (system bus)</td>
</tr>
<tr>
<td>17 to 27</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>peri.ms_vio[0]</td>
<td>CM0+ peripheral master interface PPU violation</td>
</tr>
<tr>
<td>29</td>
<td>peri.ms_vio[1]</td>
<td>CM4 peripheral master interface PPU violation</td>
</tr>
<tr>
<td>30</td>
<td>peri.ms_vio[2]</td>
<td>DW0 peripheral master interface PPU violation</td>
</tr>
<tr>
<td>31</td>
<td>peri.ms_vio[3]</td>
<td>DW1 peripheral master interface PPU violation</td>
</tr>
<tr>
<td>32</td>
<td>peri.group_vio[0]</td>
<td>Peripheral group #0 (peripheral clock dividers, trigger mux and so on) PPU violation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Register address range: 0x40000000 to 0x40000000</td>
</tr>
<tr>
<td>33</td>
<td>peri.group_vio[1]</td>
<td>Peripheral group #1 (Crypto block) PPU violation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Register address range: 0x40100000 to 0x40100000</td>
</tr>
<tr>
<td>34</td>
<td>peri.group_vio[2]</td>
<td>Peripheral group #2 (CPUSS, SRSS, eFuse, and energy profiler) PPU violation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Register address range: 0x40200000 to 0x40200000</td>
</tr>
<tr>
<td>35</td>
<td>peri.group_vio[3]</td>
<td>Peripheral group #3 (IOSS, UDB, LPCOMP, CSD, TCPWM, LCD, BLE) PPU violation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Register address range: 0x40300000 to 0x40300000</td>
</tr>
<tr>
<td>36</td>
<td>peri.group_vio[4]</td>
<td>Peripheral group #4 (SMIF) PPU violation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Register address range: 0x40400000 to 0x40400000</td>
</tr>
<tr>
<td>37</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>38</td>
<td>peri.group_vio[6]</td>
<td>Peripheral group #6 (SCB) PPU violation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Register address range: 0x40600000 to 0x40600000</td>
</tr>
<tr>
<td>39</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>41</td>
<td>peri.group_vio[9]</td>
<td>Peripheral group #9 (PASS) PPU violation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Register address range: 0x41000000 to 0x41000000</td>
</tr>
<tr>
<td>42</td>
<td>peri.group_vio[10]</td>
<td>Peripheral group #10 (audio subsystem) PPU violation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Register address range: 0x42000000 to 0x42000000</td>
</tr>
<tr>
<td>43 to 49</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>50</td>
<td>cpuss.flashc_main_bus_err</td>
<td>Flash controller bus error</td>
</tr>
<tr>
<td>51 to 95</td>
<td>Reserved</td>
<td></td>
</tr>
</tbody>
</table>
## 6.4 Register List

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPUSS_FAULTx_CTL</td>
<td>Fault control register for enabling DMA trigger, fault output, and fault reset signals</td>
</tr>
<tr>
<td>CPUSS_FAULTx_STATUS</td>
<td>Fault status register that stores the validity and fault index of the currently captured fault</td>
</tr>
<tr>
<td>CPUSS_FAULTx_DATA0</td>
<td>Fault data register 0 that stores fault information associated with the currently captured fault</td>
</tr>
<tr>
<td>CPUSS_FAULTx_DATA1</td>
<td>Fault data register 1 that stores fault information associated with the currently captured fault</td>
</tr>
<tr>
<td>CPUSS_FAULTx_DATA2</td>
<td>Fault data register 2 that stores fault information associated with the currently captured fault</td>
</tr>
<tr>
<td>CPUSS_FAULTx_DATA3</td>
<td>Fault data register 3 that stores fault information associated with the currently captured fault</td>
</tr>
<tr>
<td>CPUSS_FAULTx_PENDING0</td>
<td>Fault pending register 0 that stores pending (not captured) faults with fault index from 0 to 31</td>
</tr>
<tr>
<td>CPUSS_FAULTx_PENDING1</td>
<td>Fault pending register 1 that stores pending (not captured) faults with fault index from 32 to 63</td>
</tr>
<tr>
<td>CPUSS_FAULTx_PENDING2</td>
<td>Fault pending register 2 that stores pending (not captured) faults with fault index from 64 to 95</td>
</tr>
<tr>
<td>CPUSS_FAULTx_MASK0</td>
<td>Fault mask register 0 that enables the capture of pending faults with fault index from 0 to 31 by the fault structure</td>
</tr>
<tr>
<td>CPUSS_FAULTx_MASK1</td>
<td>Fault mask register 1 that enables the capture of pending faults with fault index from 32 to 63 by the fault structure</td>
</tr>
<tr>
<td>CPUSS_FAULTx_MASK2</td>
<td>Fault mask register 2 that enables the capture of pending faults with fault index from 64 to 95 by the fault structure</td>
</tr>
<tr>
<td>CPUSS_FAULTx_INTR</td>
<td>Fault interrupt register that stores the unmasked status of the fault structure's interrupt</td>
</tr>
<tr>
<td>CPUSS_FAULTx_INTR_SET</td>
<td>Fault interrupt set register used to set the fault structure's interrupt through firmware</td>
</tr>
<tr>
<td>CPUSS_FAULTx_INTR_MASK</td>
<td>Fault interrupt mask register that masks fault interrupt</td>
</tr>
<tr>
<td>CPUSS_FAULTx_INTR_MASKED</td>
<td>Fault interrupt register that stores the masked status of the fault structure's interrupt</td>
</tr>
</tbody>
</table>
7. Interrupts

The PSoC 6 MCU family supports interrupts and system exceptions on both Cortex-M4 and Cortex-M0+ cores. Any condition that halts normal execution of instructions is treated as an exception by the CPU. Thus an interrupt request is treated as an exception. However, in the context of this chapter, interrupts refer to those events generated by peripherals external to the CPU such as timers, serial communication block, and port pin signals; exceptions refer to those events that are generated by the CPU such as memory access faults and internal system timer events. Both interrupts and exceptions result in the current program flow being stopped and the exception handler or interrupt service routine (ISR) being executed by the CPU. Both Cortex-M4 and Cortex-M0+ cores provide their own unified exception vector table for both interrupt handlers/ISR and exception handlers.

7.1 Features

The PSoC 6 MCU supports the following interrupt features:

- Supports 147 system interrupts
  - Up to 147 Cortex-M4 interrupts
  - Up to 32 Cortex-M0+ interrupts
  - Up to 41 interrupt sources capable of waking the device from Deep Sleep power mode
- Nested vectored interrupt controller (NVIC) integrated with each CPU core, yielding low interrupt latency
- Wakeup interrupt controller (WIC) enabling interrupt detection (CPU wakeup) in Deep Sleep power mode
- Vector table may be placed in either flash or SRAM
- Configurable priority levels (eight levels for Cortex-M4 and four levels for Cortex-M0+) for each interrupt
- Level-triggered and pulse-triggered interrupt signals
7.2 Architecture

Figure 7-1. PSoC 6 MCU Interrupts Block Diagram

PSoC 6 Interrupt Architecture

- M0+ Interrupt multiplexers 240:1
- M0+ processor
- NVIC
- Cortex M0+
- Cortex M4
- M0+ Wakeup
- M4 Wakeup
- System Wakeup

Interrupt sources (Peripherals)

- INT Source 0
- INT Source 1
- INT Source 2
- INT Source 146

- IRQ0 – IRQ7
- IRQ0 – IRQ40
- IRQ0 – IRQ146

- IRQn can be connected to any one of the 147 (max 240) interrupt sources
- IRQn is connected to INT source n

- Available in Deep Sleep
- Register control

- M0+ interrupt settings
  - Enable / Disable Interrupt
  - Set Priority
  - Mask Interrupt
  - Set NMI source
  - Software trigger

- M4 interrupt settings
  - Enable / Disable Interrupt
  - Set Priority
  - Mask Interrupt
  - Set NMI source
  - Software Trigger
Figure 7-1 shows the PSoC 6 MCU interrupt architecture. The PSoC 6 MCU has 147 system and peripheral interrupts. These interrupt signals are processed by the NVIC of the individual core. In the Cortex-M4 core, the system interrupt source ‘n’ is directly connected to IRQn. For Cortex-M0+, which has only 32 IRQs, the interrupt source connected to a particular IRQn is configurable and any of the 147 system interrupts can be connected to any of the IRQn. The NVIC takes care of enabling/disabling individual interrupt IRQs, priority resolution, and communication with the CPU core. The other exceptions such as NMI and hard faults are not shown in Figure 7-1 because they are part of CPU core generated events, unlike interrupts, which are generated by peripherals external to the CPU.

In addition to the NVIC, the PSoC 6 MCU supports wakeup interrupt controllers (WIC) and multiple synchronization blocks. The WIC provides detection of Deep Sleep interrupts in the Deep Sleep CPU power mode. Each CPU can individually be in Deep Sleep mode; the device is said to be in Deep Sleep mode only when both the CPUs are in Deep Sleep mode. Refer to the Device Power Modes chapter on page 128 for details. The Cortex-M4 WIC block supports up to 41 interrupts that can wake up the CPU from Deep Sleep power mode. The Cortex-M0+ WIC block supports up to eight interrupts. The device exits Deep Sleep mode (System Wakeup signal in Figure 7-1) as soon as one CPU wakes up. The synchronization blocks synchronize the interrupts to the CPU clock frequency as the peripheral interrupts can be asynchronous to the CPU clock frequency.

7.3 Interrupts and Exceptions - Operation

7.3.1 Interrupt/Exception Handling

The following sequence of events occurs when an interrupt or exception event is triggered:

1. Assuming that all the interrupt and exception signals are initially low (idle or inactive state) and the processor is executing the main code, a rising edge on any one of the signals is registered by the NVIC, if the interrupt or exception is enabled to be serviced by the CPU. The signal is now in a pending state waiting to be serviced by the CPU. The NVIC takes care of enabling/disabling individual interrupt IRQs, priority resolution, and communication with the CPU core.

2. On detecting the signal from the NVIC, the CPU stores its current context by pushing the contents of the CPU registers onto the stack.

3. The CPU also receives the exception number of the triggered interrupt from the NVIC. All interrupts and exceptions have a unique exception number, as given in Table 7-1. By using this exception number, the CPU fetches the address of the specific exception handler from the vector table.

4. The CPU then branches to this address and executes the exception handler that follows.

5. Upon completion of the exception handler, the CPU registers are restored to their original state using stack pop operations; the CPU resumes the main code execution.

Figure 7-2. Interrupt Handling When Triggered

When the NVIC receives an interrupt request while another interrupt is being serviced or receives multiple interrupt requests at the same time, it evaluates the priority of all these interrupts, sending the exception number of the highest priority interrupt to the CPU. Thus, a higher priority interrupt can block the execution of a lower priority ISR at any time.

Exceptions are handled in the same way that interrupts are handled. Each exception event has a unique exception number, which is used by the CPU to execute the appropriate exception handler.

7.3.2 Level and Pulse Interrupts

Both CM0+ and CM4 NVICs support level and pulse signals on the interrupt lines (IRQn). The classification of an interrupt as level or pulse is based on the interrupt source.

Figure 7-3. Level Interrupts
Interrupts

Figure 7-3 and Figure 7-4 show the working of level and pulse interrupts, respectively. Assuming the interrupt signal is initially inactive (logic low), the following sequence of events explains the handling of level and pulse interrupts:

1. On a rising edge event of the interrupt signal, the NVIC registers the interrupt request. The interrupt is now in the pending state, which means the interrupt requests have not yet been serviced by the CPU.

2. The NVIC then sends the exception number along with the interrupt request signal to the CPU. When the CPU starts executing the ISR, the pending state of the interrupt is cleared.

3. For pulse interrupts, when the ISR is being executed by the CPU, one or more rising edges of the interrupt signal are logged as a single pending request. The pending interrupt is serviced again after the current ISR execution is complete (see Figure 7-4 for pulse interrupts).

4. For level interrupts, if the interrupt signal is still high after completing the ISR, it will be pending and the ISR is executed again. Figure 7-3 illustrates this for level triggered interrupts, where the ISR is executed as long as the interrupt signal is high.

7.3.3 Exception Vector Table

The exception vector tables (Table 7-1 and Table 7-2) store the entry point addresses for all exception handlers in Cortex-M0+ and Cortex-M4 cores. The CPU fetches the appropriate address based on the exception number.

Table 7-1. M0+ Exception Vector Table

<table>
<thead>
<tr>
<th>Exception Number</th>
<th>Exception Priority</th>
<th>Vector Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>–</td>
<td>Initial Stack Pointer Value</td>
<td>Not applicable (NA)</td>
</tr>
<tr>
<td>1</td>
<td>Reset</td>
<td>–3, the highest priority</td>
</tr>
<tr>
<td>2</td>
<td>Non Maskable Interrupt (NMI)</td>
<td>–2</td>
</tr>
<tr>
<td>3</td>
<td>HardFault</td>
<td>–1</td>
</tr>
<tr>
<td>4-10</td>
<td>Reserved</td>
<td>NA</td>
</tr>
<tr>
<td>11</td>
<td>Supervisory Call (SVCall)</td>
<td>Configurable (0 – 3)</td>
</tr>
<tr>
<td>12-13</td>
<td>Reserved</td>
<td>NA</td>
</tr>
<tr>
<td>14</td>
<td>PendSupervisory (PendSV)</td>
<td>Configurable (0 – 3)</td>
</tr>
<tr>
<td>15</td>
<td>System Timer (SysTick)</td>
<td>Configurable (0 – 3)</td>
</tr>
<tr>
<td>16</td>
<td>External Interrupt (IRQ0)</td>
<td>Configurable (0 – 3)</td>
</tr>
<tr>
<td>…</td>
<td>…</td>
<td>Configurable (0 – 3)</td>
</tr>
<tr>
<td>47</td>
<td>External Interrupt (IRQ31)</td>
<td>Configurable (0 – 3)</td>
</tr>
</tbody>
</table>

<sup>a</sup> Start Address = 0x0000 on reset and is later modified by user code by updating the CM0P_SCS_VTOR register.

Table 7-2. Cortex-M4 Exception Vector Table

<table>
<thead>
<tr>
<th>Exception Number</th>
<th>Exception Priority</th>
<th>Vector Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>–</td>
<td>Initial stack pointer value</td>
<td>–</td>
</tr>
<tr>
<td>1</td>
<td>Reset</td>
<td>–3, highest priority</td>
</tr>
<tr>
<td>2</td>
<td>Non Maskable Interrupt (NMI)</td>
<td>–2</td>
</tr>
<tr>
<td>3</td>
<td>Hard fault</td>
<td>–1</td>
</tr>
<tr>
<td>4</td>
<td>Memory management fault</td>
<td>Configurable (0 – 7)</td>
</tr>
<tr>
<td>5</td>
<td>Bus fault</td>
<td>Configurable (0 – 7)</td>
</tr>
<tr>
<td>6</td>
<td>Usage fault</td>
<td>Configurable (0 – 7)</td>
</tr>
<tr>
<td>7–10</td>
<td>Reserved</td>
<td>–</td>
</tr>
<tr>
<td>11</td>
<td>Supervisory call (SVCall)</td>
<td>Configurable (0 – 7)</td>
</tr>
<tr>
<td>12-13</td>
<td>Reserved</td>
<td>–</td>
</tr>
<tr>
<td>14</td>
<td>Pend Supervisory (PendSV)</td>
<td>Configurable (0 – 7)</td>
</tr>
<tr>
<td>15</td>
<td>System Tick timer (SysTick)</td>
<td>Configurable (0 – 7)</td>
</tr>
</tbody>
</table>
### 7.4 Exception Sources

This section explains the different exception sources listed in Table 7-1 and Table 7-2 (exception numbers 1 to 15).

#### 7.4.1 Reset Exception

Device reset is treated as an exception in PSoC 6 MCUs. Reset exception is always enabled with a fixed priority of –3, the highest priority exception in both the cores. When the device boots up, only the Cortex-M0+ core is available. The CM0+ core executes the ROM boot code and can enable Cortex-M4 core from the application code. The reset exception of the CM0+ core is tied to the device reset or startup. When the Cortex-M0+ core releases the Cortex-M4 reset, the M4 reset exception is executed. A device reset can occur due to multiple reasons, such as power-on-reset (POR), external reset signal on XRES pin, or watchdog reset. When the device is reset, the initial boot code for configuring the device is executed by the Cortex-M0+ out of supervisory read-only memory (SROM). The boot code and other data in SRAM memory are programmed by Cypress, and are not read/write accessible to external users. After completing the SRAM boot sequence, the Cortex-M0+ code execution jumps to flash memory. Flash memory address 0x100000004 (Exception#1 in Table 7-1) stores the location of the startup code in flash memory. The CPU starts executing code out of this address. Note that the reset exception address in the SRAM vector table will never be used because the device comes out of reset with the flash vector table selected. The register configuration to select the SRAM vector table can be done only as part of the startup code in flash after the reset is de-asserted. Note that the reset exception flow for Cortex-M4 is the same as Cortex-M0+. However, Cortex-M4 execution begins only after CM0+ core de-asserts the M4 reset.

#### 7.4.2 Non-Maskable Interrupt Exception

Non-maskable interrupt (NMI) is the highest priority exception next to reset. It is always enabled with a fixed priority of –2. Both the cores have their own NMI exception. There are three ways to trigger an NMI exception in a CPU core:

- **NMI exception from a system interrupt**: Both Cortex-M0+ and Cortex-M4 provide an option to trigger an NMI exception using one of the 147 system interrupts. The NMI exception triggered due to the interrupt will execute the NMI handler pointed to by the active vector table. The CPUSS_CMx_NMI_CTL register selects the interrupt source that triggers the NMI from hardware.

- **NMI exception by setting NMIPENDSET bit (user NMI exception)**: An NMI exception can be triggered in software by setting the NMIPENDSET bit in the interrupt control state registers (CM0P_SCS_ICSR and CM4_SCS_ICSR). Setting this bit will execute the NMI handler pointed to by the active vector table in the respective CPU cores.

- **System Call NMI exception**: This exception is used for nonvolatile programming and other system call operations such as flash write operation and flash checksum operation. Inter processor communication

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### Table 7-2. Cortex-M4 Exception Vector Table (continued)

<table>
<thead>
<tr>
<th>Exception Number</th>
<th>Exception Description</th>
<th>Exception Priority</th>
<th>Vector Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>External interrupt (IRQ0)</td>
<td>Configurable (0 – 7)</td>
<td>Start_Address + 0x0040</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>159</td>
<td>External interrupt (IRQ143)</td>
<td>Configurable (0 – 7)</td>
<td>Start_Address + 0x0280</td>
</tr>
<tr>
<td>160</td>
<td>External interrupt (IRQ144)</td>
<td>Configurable (0 – 7)</td>
<td>Start_Address + 0x0284</td>
</tr>
<tr>
<td>161</td>
<td>External interrupt (IRQ145)</td>
<td>Configurable (0 – 7)</td>
<td>Start_Address + 0x0288</td>
</tr>
<tr>
<td>162</td>
<td>External interrupt (IRQ146)</td>
<td>Configurable (0 – 7)</td>
<td>Start_Address + 0x028C</td>
</tr>
</tbody>
</table>

* a. Start Address = 0x0000 on reset and is later modified by user code by updating CM4_SCS_VTOR register.

In Table 7-1 and Table 7-2, the first word (4 bytes) is not marked as exception number zero. This is because the first word in the exception table is used to initialize the main stack pointer (MSP) value on device reset; it is not considered as an exception. In the PSoC 6 MCU, both the vector tables can be configured to be located either in flash memory or SRAM. The vector table offset register (VTOR) present as part of Cortex-M0+ and Cortex-M4 system control space registers configures the vector table offset from the base address (0x0000). The CM0P_SCS_VTOR register sets the vector offset address for the CM0+ core and CM4_SCS_VTOR sets the offset for the M4 core. The VTOR value determines whether the vector table is in flash memory (0x10000000 to 0x10100000) or SRAM (0x08000000 to 0x08048000). Note that the VTOR registers can be updated only in privilege CPU mode, refer to the Chip Operational Modes chapter on page 113 for details. The advantage of moving the vector table to SRAM is that the exception handler addresses can be dynamically changed by modifying the SRAM vector table contents. However, the nonvolatile flash memory vector table must be modified by a flash memory write.

The exception sources (exception numbers 1 to 15) are explained in 7.4 Exception Sources. The exceptions marked as Reserved in Table 7-1 are not used, although they have addresses reserved for them in the vector table. The interrupt sources (exception numbers 16 to 162) are explained in 7.5 Interrupt Sources.
Interrupts

7.4.3 HardFault Exception
Both CM0+ and CM4 cores support HardFault exception. HardFault is an always-enabled exception that occurs because of an error during normal or exception processing. HardFault has a fixed priority of –1, meaning it has higher priority than any exception with configurable priority. A HardFault exception is a catch-all exception for different types of fault conditions, which include executing an undefined instruction and accessing an invalid memory addresses. The CPU does not provide fault status information to the HardFault exception handler, but it does permit the handler to perform an exception return and continue execution in cases where software has the ability to recover from the fault situation.

7.4.4 Memory Management Fault Exception
A memory management fault is an exception that occurs because of a memory protection-related fault. The fixed memory protection constraints determine this fault, for both instruction and data memory transactions. This fault is always used to abort instruction accesses to Execute Never (XN) memory regions. The memory management fault is only supported by the M4 core. The priority of the exception is configurable from 0 (highest) to 7 (lowest).

7.4.5 Bus Fault Exception
A Bus Fault is an exception that occurs because of a memory-related fault for an instruction or data memory transaction. This might be from an error detected on a bus in the memory system. The bus fault is supported only by the M4 core. The priority of the exception is configurable from 0 (highest) to 7 (lowest).

7.4.6 Usage Fault Exception
A Usage Fault is an exception that occurs because of a fault related to instruction execution. This includes:
- an undefined instruction
- an illegal unaligned access
- invalid state on instruction execution
- an error on exception return

The following can cause a usage fault when the core is configured to report them:
- an unaligned address on word and halfword memory access
- division by zero

The usage fault is supported only by the M4 core. The priority of the exception is configurable from 0 (highest) to 7 (lowest).

7.4.7 Supervisor Call (SVCall) Exception
Both CM0+ and CM4 cores support SVCall exception. Supervisor Call (SVCall) is an always-enabled exception caused when the CPU executes the SVC instruction as part of the application code. Application software uses the SVC instruction to make a call to an underlying operating system and provide a service. This is known as a supervisor call. The SVC instruction enables the application to issue an SVCall that requires privileged access to the system.

The priority of an SVCall exception can be configured to a value between 0 and 3 for CM0+ and 0 to 7 for CM4 core by writing to the bitfields PRI_11 of the System Handler Priority Register 2 (CM0P_SCS_SHPR2 and CM4_SCS_SHPR2). When the SVC instruction is executed, the SVCall exception enters the pending state and waits to be serviced by the CPU. The SVCALLPENDED bit in the System Handler Control and State Register (CM0P_SCS_SHCSR and CM4_SCS_SHCSR) can be used to check or modify the pending status of the SVCall exception.

7.4.8 PendSupervisory (PendSV) Exception
Both CM0+ and CM4 cores support PendSV exception. PendSV is another supervisor call related exception similar to SVCall, normally being software-generated. PendSV is always enabled and its priority is configurable similar to SVCall. The PendSV exception is triggered by setting the PENDSVSET bit in the Interrupt Control State Register (CM0P_SCS_ICSR and CM4_SCS_ICSR). On setting this bit, the PendSV exception enters the pending state, and waits to be serviced by the CPU. The pending state of a PendSV exception can be cleared by setting the PENDSVCLR bit in the Interrupt Control State Register. The
priority of a PendSV exception can be configured to a value between 0 and 3 for CM0+ and 0 to 7 for M4 by writing to the bitfields PRI_14 of the System Handler Priority Register 3. See the Armv6-M Architecture Reference Manual for more details.

### 7.4.9 System Tick (SysTick) Exception

Both CM0+ and CM4 cores in PSoC 6 MCUs support a system timer, referred to as SysTick, as part of their internal architecture. SysTick provides a simple, 24-bit decrementing counter for various timekeeping purposes such as an RTOS tick timer, high-speed alarm timer, or simple counter. The SysTick timer can be configured to generate an interrupt when its count value reaches zero, which is referred to as a SysTick exception. The exception is enabled by setting the TICKINT bit in the SysTick Control and Status Register (CM0P_SCS_SYST_CSR and CM4_SCS_SYST_CSR). The priority of a SysTick exception can be configured to a value between 0 and 3 for CM0+ and 0 to 7 for M4 by writing to the bitfields PRI_15 of the System Handler Priority Register 3 (SHPR3). The SysTick exception can always be generated in software at any instant by writing a one to the PENDSTSET bit in the Interrupt Control State Register. Similarly, the pending state of the SysTick exception can be cleared by writing a one to the PENDSTCLR bit in the Interrupt Control State Register.

### 7.5 Interrupt Sources

The PSoC 6 MCU supports 147 interrupts from peripherals. The source of each interrupt is listed in Table 7-3. These system interrupts are mapped directly to Cortex-M4 core (IRQ0 to IRQ146 or exception 16 to 162). For Cortex-M0+ core, any of the 147 interrupts can be routed to the available 32 interrupts (IRQ0 to IRQ31 or exception 16 to 47). The CPUSS_CM0_INT_CTLx registers are used to make this interrupt selection in CM0+.

The interrupts include standard interrupts from the on-chip peripherals such as TCPWM, serial communication block, CSD block, watchdog, ADC, and so on. The interrupt generated is usually the logical OR of the different peripheral states. The peripheral interrupt status register should be read in the ISR to detect which condition generated the interrupt. These interrupts are usually level interrupts. The appropriate interrupt registers should be cleared in the ISR to deassert the interrupt. Usually a write ‘1’ is required to clear the registers. If the interrupt register is not cleared in the ISR, the interrupt will remain asserted and the ISR will be executed continuously. See the I/O System chapter on page 164 for details on GPIO interrupts. Note that CM0+ core supports 32 IRQ lines and each IRQ line can connect to any of the available 147 interrupt sources.

As seen from Table 7-3, 41 interrupts (IRQ0 to IRQ40) are capable of waking up the device from Deep Sleep power mode. For Cortex-M4, IRQ0 to IRQ40 directly map to these sources. However, in the Cortex-M0+, only the first eight IRQ lines support Deep Sleep wakeup. This means the 41 Deep Sleep wakeup-capable interrupts can be connected to the first eight IRQ lines of Cortex-M0+, if such a wakeup is desired. Therefore, reserve and use the first eight IRQ lines of Cortex-M0+ for Deep Sleep wakeup-capable sources.

Table 7-3. List of PSoC 6 MCU Interrupt Sources

<table>
<thead>
<tr>
<th>Interrupt</th>
<th>Cortex M4 Exception Number</th>
<th>Power Mode</th>
<th>Interrupt source</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMI</td>
<td>2</td>
<td>Active</td>
<td>Any of the below 147 IRQ source</td>
</tr>
<tr>
<td>IRQ0</td>
<td>16</td>
<td>Deep Sleep</td>
<td>GPIO Interrupt - Port 0</td>
</tr>
<tr>
<td>IRQ1</td>
<td>17</td>
<td>Deep Sleep</td>
<td>GPIO Interrupt - Port 1</td>
</tr>
<tr>
<td>IRQ2</td>
<td>18</td>
<td>Deep Sleep</td>
<td>GPIO Interrupt - Port 2</td>
</tr>
<tr>
<td>IRQ3</td>
<td>19</td>
<td>Deep Sleep</td>
<td>GPIO Interrupt - Port 3</td>
</tr>
<tr>
<td>IRQ4</td>
<td>20</td>
<td>Deep Sleep</td>
<td>GPIO Interrupt - Port 4</td>
</tr>
<tr>
<td>IRQ5</td>
<td>21</td>
<td>Deep Sleep</td>
<td>GPIO Interrupt - Port 5</td>
</tr>
<tr>
<td>IRQ6</td>
<td>22</td>
<td>Deep Sleep</td>
<td>GPIO Interrupt - Port 6</td>
</tr>
<tr>
<td>IRQ7</td>
<td>23</td>
<td>Deep Sleep</td>
<td>GPIO Interrupt - Port 7</td>
</tr>
<tr>
<td>IRQ8</td>
<td>24</td>
<td>Deep Sleep</td>
<td>GPIO Interrupt - Port 8</td>
</tr>
<tr>
<td>IRQ9</td>
<td>25</td>
<td>Deep Sleep</td>
<td>GPIO Interrupt - Port 9</td>
</tr>
<tr>
<td>IRQ10</td>
<td>26</td>
<td>Deep Sleep</td>
<td>GPIO Interrupt - Port 10</td>
</tr>
<tr>
<td>IRQ11</td>
<td>27</td>
<td>Deep Sleep</td>
<td>GPIO Interrupt - Port 11</td>
</tr>
<tr>
<td>IRQ12</td>
<td>28</td>
<td>Deep Sleep</td>
<td>GPIO Interrupt - Port 12</td>
</tr>
<tr>
<td>IRQ13</td>
<td>29</td>
<td>Deep Sleep</td>
<td>GPIO Interrupt - Port 13</td>
</tr>
<tr>
<td>IRQ14</td>
<td>30</td>
<td>Deep Sleep</td>
<td>GPIO Interrupt - Port 14</td>
</tr>
</tbody>
</table>
# Table 7-3. List of PSoC 6 MCU Interrupt Sources (continued)

<table>
<thead>
<tr>
<th>Interrupt</th>
<th>Cortex M4 Exception Number</th>
<th>Power Mode</th>
<th>Interrupt source</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRQ15</td>
<td>31</td>
<td>Deep Sleep</td>
<td>GPIO All Ports</td>
</tr>
<tr>
<td>IRQ16</td>
<td>32</td>
<td>Deep Sleep</td>
<td>GPIO Supply Detect Interrupt</td>
</tr>
<tr>
<td>IRQ17</td>
<td>33</td>
<td>Deep Sleep</td>
<td>Low-Power Comparator Interrupt</td>
</tr>
<tr>
<td>IRQ18</td>
<td>34</td>
<td>Deep Sleep</td>
<td>Serial Communication Block #8 Interrupt</td>
</tr>
<tr>
<td>IRQ19</td>
<td>35</td>
<td>Deep Sleep</td>
<td>Multi-Counter Watchdog Timer (MCWDT0) Interrupt</td>
</tr>
<tr>
<td>IRQ20</td>
<td>36</td>
<td>Deep Sleep</td>
<td>Multi-Counter Watchdog Timer (MCWDT1) Interrupt</td>
</tr>
<tr>
<td>IRQ21</td>
<td>37</td>
<td>Deep Sleep</td>
<td>Real-Time-Clock (Backup domain) Interrupt</td>
</tr>
<tr>
<td>IRQ22</td>
<td>38</td>
<td>Deep Sleep</td>
<td>LVD and WDT Interrupt</td>
</tr>
<tr>
<td>IRQ23</td>
<td>39</td>
<td>Deep Sleep</td>
<td>Continuous Time block (CTBm) Interrupt</td>
</tr>
<tr>
<td>IRQ24</td>
<td>40</td>
<td>Deep Sleep</td>
<td>Bluetooth Radio Interrupt</td>
</tr>
<tr>
<td>IRQ25</td>
<td>41</td>
<td>Deep Sleep</td>
<td>CPUSS Inter Process Communication Interrupt #0</td>
</tr>
<tr>
<td>IRQ26</td>
<td>42</td>
<td>Deep Sleep</td>
<td>CPUSS Inter Process Communication Interrupt #1</td>
</tr>
<tr>
<td>IRQ27</td>
<td>43</td>
<td>Deep Sleep</td>
<td>CPUSS Inter Process Communication Interrupt #2</td>
</tr>
<tr>
<td>IRQ28</td>
<td>44</td>
<td>Deep Sleep</td>
<td>CPUSS Inter Process Communication Interrupt #3</td>
</tr>
<tr>
<td>IRQ29</td>
<td>45</td>
<td>Deep Sleep</td>
<td>CPUSS Inter Process Communication Interrupt #4</td>
</tr>
<tr>
<td>IRQ30</td>
<td>46</td>
<td>Deep Sleep</td>
<td>CPUSS Inter Process Communication Interrupt #5</td>
</tr>
<tr>
<td>IRQ31</td>
<td>47</td>
<td>Deep Sleep</td>
<td>CPUSS Inter Process Communication Interrupt #6</td>
</tr>
<tr>
<td>IRQ32</td>
<td>47</td>
<td>Deep Sleep</td>
<td>CPUSS Inter Process Communication Interrupt #7</td>
</tr>
<tr>
<td>IRQ33</td>
<td>49</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IRQ34</td>
<td>50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IRQ35</td>
<td>51</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IRQ36</td>
<td>52</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IRQ37</td>
<td>53</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IRQ38</td>
<td>54</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IRQ39</td>
<td>55</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IRQ40</td>
<td>56</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IRQ41</td>
<td>57</td>
<td>Active</td>
<td>Serial Communication Block #0</td>
</tr>
<tr>
<td>IRQ42</td>
<td>58</td>
<td>Active</td>
<td>Serial Communication Block #1</td>
</tr>
<tr>
<td>IRQ43</td>
<td>59</td>
<td>Active</td>
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<td>IRQ49</td>
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<td>CapSense Interrupt</td>
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<td>IRQ57</td>
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### Table 7-3. List of PSoC 6 MCU Interrupt Sources (continued)

<table>
<thead>
<tr>
<th>Interrupt</th>
<th>Cortex M4 Exception Number</th>
<th>Power Mode</th>
<th>Interrupt source</th>
</tr>
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<tbody>
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<td>CPUSS DataWire #1, Channel #0</td>
</tr>
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<td>IRQ67</td>
<td>83</td>
<td>Active</td>
<td>CPUSS DataWire #1, Channel #1</td>
</tr>
<tr>
<td>IRQ68</td>
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<td>Active</td>
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<td>IRQ77</td>
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<td>Active</td>
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<td>IRQ82</td>
<td>98</td>
<td>Active</td>
<td>CPUSS Fault Structure Interrupt #0</td>
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<td>CPUSS Fault Structure Interrupt #1</td>
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<td>Active</td>
<td>Crypto Accelerator Interrupt</td>
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<td>IRQ85</td>
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<td>Flash Macro Interrupt</td>
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<td>Cortex-M0+ CTI #0</td>
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<td>IRQ90</td>
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<td>TCPWM #0 (32-bit), Counter #0</td>
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<td>TCPWM #0 (32-bit), Counter #1</td>
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<td>IRQ92</td>
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<td>Active</td>
<td>TCPWM #0 (32-bit), Counter #4</td>
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<td>Active</td>
<td>TCPWM #0 (32-bit), Counter #5</td>
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<td>IRQ96</td>
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<td>Active</td>
<td>TCPWM #0 (32-bit), Counter #6</td>
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<td>IRQ97</td>
<td>113</td>
<td>Active</td>
<td>TCPWM #0 (32-bit), Counter #7</td>
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<td>IRQ98</td>
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<tr>
<td>IRQ99</td>
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<td>IRQ100</td>
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## Table 7-3. List of PSoC 6 MCU Interrupt Sources (continued)

<table>
<thead>
<tr>
<th>Interrupt</th>
<th>Cortex M4 Exception Number</th>
<th>Power Mode</th>
<th>Interrupt source</th>
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<tr>
<td>IRQ101</td>
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<td>TCPWM #1 (16-bit), Counter #4</td>
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<td>IRQ103</td>
<td>119</td>
<td>Active</td>
<td>TCPWM #1 (16-bit), Counter #5</td>
</tr>
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<td>IRQ104</td>
<td>120</td>
<td>Active</td>
<td>TCPWM #1 (16-bit), Counter #6</td>
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<td>Active</td>
<td>TCPWM #1 (16-bit), Counter #7</td>
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<td>TCPWM #1 (16-bit), Counter #8</td>
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<td>TCPWM #1 (16-bit), Counter #9</td>
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<td>IRQ108</td>
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<td>IRQ109</td>
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<td>IRQ110</td>
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<td>TCPWM #1 (16-bit), Counter #12</td>
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<td>IRQ111</td>
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<td>TCPWM #1 (16-bit), Counter #13</td>
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<td>IRQ112</td>
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<td>Active</td>
<td>TCPWM #1 (16-bit), Counter #15</td>
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<td>TCPWM #1 (16-bit), Counter #16</td>
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<td>IRQ115</td>
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<td>TCPWM #1 (16-bit), Counter #23</td>
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<td>UDB Interrupt #1</td>
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<td>IRQ124</td>
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<td>UDB Interrupt #2</td>
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<td>Active</td>
<td>UDB Interrupt #3</td>
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<td>IRQ126</td>
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<td>Active</td>
<td>UDB Interrupt #4</td>
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<td>IRQ127</td>
<td>143</td>
<td>Active</td>
<td>UDB Interrupt #5</td>
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<td>144</td>
<td>Active</td>
<td>UDB Interrupt #6</td>
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<td>IRQ129</td>
<td>145</td>
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<td>146</td>
<td>Active</td>
<td>UDB Interrupt #8</td>
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<td>IRQ131</td>
<td>147</td>
<td>Active</td>
<td>UDB Interrupt #9</td>
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<td>IRQ132</td>
<td>148</td>
<td>Active</td>
<td>UDB Interrupt #10</td>
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<tr>
<td>IRQ133</td>
<td>149</td>
<td>Active</td>
<td>UDB Interrupt #11</td>
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<tr>
<td>IRQ134</td>
<td>150</td>
<td>Active</td>
<td>UDB Interrupt #12</td>
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<td>IRQ135</td>
<td>151</td>
<td>Active</td>
<td>UDB Interrupt #13</td>
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<td>IRQ136</td>
<td>152</td>
<td>Active</td>
<td>UDB Interrupt #14</td>
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<td>IRQ137</td>
<td>153</td>
<td>Active</td>
<td>UDB Interrupt #15</td>
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<td>IRQ138</td>
<td>154</td>
<td>Active</td>
<td>SAR ADC Interrupt</td>
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<td>IRQ139</td>
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<td>Active</td>
<td>I²S Audio Interrupt</td>
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<td>IRQ140</td>
<td>156</td>
<td>Active</td>
<td>PDM/PCM Audio Interrupt</td>
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<td>IRQ141</td>
<td>157</td>
<td>Active</td>
<td>Energy Profiler Interrupt</td>
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<tr>
<td>IRQ142</td>
<td>158</td>
<td>Active</td>
<td>Serial Memory Interface Interrupt</td>
</tr>
</tbody>
</table>
7.6 Interrupt/Exception Priority

Exception priority is useful for exception arbitration when there are multiple exceptions that need to be serviced by the CPU. Both M4 and M0+ cores in PSoC 6 MCUs provide flexibility in choosing priority values for different exceptions. All exceptions other than Reset, NMI, and HardFault can be assigned a configurable priority level. The Reset, NMI, and HardFault exceptions have a fixed priority of –3, –2, and –1, respectively. In PSoC 6 MCUs, lower priority numbers represent higher priorities. This means that the Reset, NMI, and HardFault exceptions have the highest priorities. The other exceptions can be assigned a configurable priority level between 0 and 3 for Cortex-M0+ and 0 to 7 for Cortex-M4.

Both M0+ and M4 support nested exceptions in which a higher priority exception can obstruct (interrupt) the currently active exception handler. This pre-emption does not happen if the incoming exception priority is the same as or lower than the active exception. The CPU resumes execution of the lower priority exception handler after servicing the higher priority exception. The CM0+ core in the PSoC 6 MCU allows nesting of up to four exceptions; the CM4 core allows up to eight exceptions. When the CPU receives two or more exceptions requests of the same priority, the lowest exception number is serviced first.

The registers to configure the priority of exception numbers 1 to 15 are explained in Exception Sources on page 51.

The priority of the 32 CM0+ and 147 CM4 interrupts can be configured by writing to the respective Interrupt Priority registers (CM0P_SCS_IPR and CM4_SCS_IPR). This is a group of eight (CM0+) and 60 (CM4) 32-bit registers with each register storing the priority values of four interrupts, as given in Table 7-4 and Table 7-5.

7.7 Enabling and Disabling Interrupts

The NVICs of both CM0+ and CM4 core provide registers to individually enable and disable the interrupts in software. If an interrupt is not enabled, the NVIC will not process the interrupt requests on that interrupt line. The Interrupt Set-Enable Register (CM0P_SCS_ISER and CM4_SCS_ISER) and the Interrupt Clear-Enable Register (CM0P_SCS_ICER and CM4_SCS_ICER) are used to enable and disable the interrupts respectively. These registers are 32-bit wide and each bit corresponds to the same numbered interrupt in CM0+. For CM4 core, there are eight ISER/ICER registers. These registers can also be read in software to get the enable status of the interrupts. Table 7-6 shows the register access properties for these two registers. Note that writing zero to these registers has no effect.

The ISER and ICER registers are applicable only for the interrupts. These registers cannot be used to enable or disable the exception numbers 1 to 15. The 15 exceptions have their own support for enabling and disabling, as explained in Exception Sources on page 51.
The PRIMASK register in the CPUs (both CM0+ and CM4) can be used as a global exception enable register to mask all the configurable priority exceptions irrespective of whether they are enabled. Configurable priority exceptions include all the exceptions except Reset, NMI, and HardFault listed in Table 7-1. When the PM bit (bit 0) in the PRIMASK register is set, none of the configurable priority exceptions can be serviced by the CPU, though they can be in the pending state waiting to be serviced by the CPU after the PM bit is cleared.

### 7.8 Interrupt/Exception States

Each exception can be in one of the following states.

Table 7-7. Exception States

<table>
<thead>
<tr>
<th>Exception State</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inactive</td>
<td>The exception is not active and not pending. Either the exception is disabled or the enabled exception has not been triggered.</td>
</tr>
<tr>
<td>Pending</td>
<td>The exception request has been received by the CPU/NVIC and the exception is waiting to be serviced by the CPU.</td>
</tr>
<tr>
<td>Active</td>
<td>An exception that is being serviced by the CPU but whose exception handler execution is not yet complete. A high-priority exception can interrupt the execution of lower priority exception. In this case, both the exceptions are in the active state.</td>
</tr>
<tr>
<td>Active and Pending</td>
<td>The exception is being serviced by the processor and there is a pending request from the same source during its exception handler execution.</td>
</tr>
</tbody>
</table>

The Interrupt Control State Register (CM0P_SCS_ICSR and CM4_SCS_ICSR) contains status bits describing the various exceptions states.

- The VECTACTIVE bits ([8:0]) in the ICSR store the exception number for the current executing exception. This value is zero if the CPU does not execute any exception handler (CPU is in thread mode). Note that the value in VECTACTIVE bitfields is the same as the value in bits [8:0] of the Interrupt Program Status Register (IPSR), which is also used to store the active exception number.
- The VECTPENDING bits ([20:12]) in the ICSR store the exception number of the highest priority pending exception. This value is zero if there are no pending exceptions.
- The ISRPENDING bit (bit 22) in the ICSR indicates if a NVIC generated interrupt is in a pending state.

#### 7.8.1 Pending Interrupts/Exceptions

When a peripheral generates an interrupt request signal to the NVIC or an exception event occurs, the corresponding exception enters the pending state. When the CPU starts executing the corresponding exception handler routine, the exception is changed from the pending state to the active state. The NVIC allows software pending of the 32 (CM0+) or 147 (CM4) interrupt lines by providing separate register bits for setting and clearing the pending states of the interrupts. The Interrupt Set-Pending register (CM0P_SCS_ISPR and CM4_SCS_ISPR) and the Interrupt Clear-Pending register (CM0P_SCS_ICPR and CM4_SCS_ICPR) are used to set and clear the pending status of the interrupt lines. These registers are 32 bits wide, and each bit corresponds to the same numbered interrupt. In the case of CM4, there are eight sets of such registers to accommodate all 147 interrupts. Table 7-8 shows the register access properties for these two registers. Note that writing zero to these registers has no effect.

Table 7-8. Interrupt Set Pending/Clear Pending Registers

<table>
<thead>
<tr>
<th>Register</th>
<th>Operation</th>
<th>Bit Value</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interrupt Set-Pending</td>
<td>Write</td>
<td>1</td>
<td>To put an interrupt to pending state</td>
</tr>
<tr>
<td>Register (ISPR)</td>
<td>Read</td>
<td>1</td>
<td>Interrupt is pending</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>Interrupt is not pending</td>
</tr>
<tr>
<td>Interrupt Clear-Pending</td>
<td>Write</td>
<td>1</td>
<td>To clear a pending interrupt</td>
</tr>
<tr>
<td>Register (ICPR)</td>
<td>Read</td>
<td>1</td>
<td>Interrupt is pending</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>Interrupt is not pending</td>
</tr>
</tbody>
</table>
Setting the pending bit when the same bit is already set results in only one execution of the ISR. The pending bit can be updated regardless of whether the corresponding interrupt is enabled. If the interrupt is not enabled, the interrupt line will not move to the pending state until it is enabled by writing to the ISER register.

Note that the ISPR and ICPR registers are used only for the peripheral interrupts. These registers cannot be used for pending the exception numbers 1 to 15. These 15 exceptions have their own support for pending, as explained in Exception Sources on page 51.

### 7.9 Stack Usage for Interrupts/Exceptions

When the CPU executes the main code (in thread mode) and an exception request occurs, the CPU stores the state of its general-purpose registers in the stack. It then starts executing the corresponding exception handler (in handler mode). The CPU pushes the contents of the eight 32-bit internal registers into the stack. These registers are the Program and Status Register (PSR), ReturnAddress, Link Register (LR or R14), R12, R3, R2, R1, and R0. Both Cortex-M4 and Cortex-M0+ have two stack pointers - MSP and PSP. Only one of the stack pointers can be active at a time. When in thread mode, the Active Stack Pointer bit in the Control register is used to define the current active stack pointer. When in handler mode, the MSP is always used as the stack pointer. The stack pointer always grows downwards and points to the address that has the last pushed data.

When the CPU is in thread mode and an exception request comes, the CPU uses the stack pointer defined in the control register to store the general-purpose register contents. After the stack push operations, the CPU enters handler mode to execute the exception handler. When another higher priority exception occurs while executing the current exception, the MSP is used for stack push/pop operations, because the CPU is already in handler mode. See the CPU Subsystem (CPUSS) chapter on page 30 for details.

### 7.10 Interrupts and Low-Power Modes

The PSoC 6 MCU family allows device (CPU) wakeup from low-power modes when certain peripheral interrupt requests are generated. The Wakeup Interrupt Controller (WIC) block generates a wakeup signal that causes the CPU to enter Active mode when one or more wakeup sources generate an interrupt signal. After entering Active mode, the ISR of the peripheral interrupt is executed.

The Wait For Interrupt (WFI) or Wait For Event (WFE) instruction, executed by the CPU, triggers the transition into Sleep, and Deep Sleep modes. Both the WFI and WFE instructions are capable of waking up on interrupts. However, the WFE requires the interrupts to be unmasked in the CPU’s Priority Mask register. Refer to the PRIMASK register definition on the Arm website. In addition, the WFE instruction puts the CPU to sleep based on the status of an event bit and wakes up from an event signal, typically sent by the other CPU. WFI does not require PRIMASK unmasking and can wake up the CPU from any pending interrupt masked to the NVIC or WIC. However, WFI cannot wake up the CPU from event signals from other CPUs. The sequence of entering the different low-power modes is detailed in the Device Power Modes chapter on page 128. Chip low-power modes have two categories of interrupt sources:

- Interrupt sources that are available in the Active, Sleep, and Deep Sleep modes (watchdog timer interrupt, RTC, GPIO interrupts, and low-power comparators)
- Interrupt sources that are available only in the Active and Sleep modes

When using the WFE instruction in CM4, make sure to call the WFE instruction twice to properly enter and exit Sleep/Deep Sleep modes. This behavior comes from the event register implementation in Arm v7 architecture used in Cortex-M4. According to the ARM V7 architecture reference manual (Section B1.5.18 Wait For Event and Send Event):

- A reset clears the event register.
- Any WFE wakeup event, or the execution of an exception return instruction, sets the event register.
- A WFE instruction clears the event register.
- Software cannot read or write the value of the event register directly.

Therefore, the first WFE instruction puts CM4 to sleep and second WFE clears the event register after a WFE wakeup, which sets the event register. So the next WFE will put the core to sleep.

Note that this behavior is not present in Arm v6 architecture used in Cortex-M0+. Therefore, in CM0+ only one WFE instruction is sufficient to successfully enter or exit Sleep and Deep Sleep modes.

### 7.11 Interrupt/Exception – Initialization/Configuration

This section covers the different steps involved in initializing and configuring exceptions in the PSoC 6 MCU.

1. Configuring the Exception Vector Table Location: The first step in using exceptions is to configure the vector table location as required - either in flash memory or SRAM. This configuration is done as described in Exception Vector Table on page 50.

The vector table should be available in SRAM if the application must change the vector addresses.
dynamically. If the table is located in flash, then a flash write operation is required to modify the vector table contents. The PSoC Creator IDE uses the vector table in SRAM by default.

2. Configuring Individual Exceptions: The next step is to configure individual exceptions required in an application, as explained in earlier sections.
   a. Configure the exception or interrupt source; this includes setting up the interrupt generation conditions. The register configuration depends on the specific exception required. Refer to the respective peripheral chapter to know more about the interrupt configuration supported by them.
   b. Define the exception handler function and write the address of the function to the exception vector table. Table 7-1 gives the exception vector table format; the exception handler address should be written to the appropriate exception number entry in the table.
   c. Set up the exception priority, as explained in Interrupt/Exception Priority on page 57.
   d. Enable the exception, as explained in Enabling and Disabling Interrupts on page 57.
## 7.12 Register List

Table 7-9. Register List

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPUSS_CM0_NMI_CTL</td>
<td>Cortex-M0+ NMI control</td>
</tr>
<tr>
<td>CPUSS_CM0_INT_CTL0</td>
<td>Cortex-M0+ interrupt control 0</td>
</tr>
<tr>
<td>CPUSS_CM0_INT_CTL1</td>
<td>Cortex-M0+ interrupt control 1</td>
</tr>
<tr>
<td>CPUSS_CM0_INT_CTL2</td>
<td>Cortex-M0+ interrupt control 2</td>
</tr>
<tr>
<td>CPUSS_CM0_INT_CTL3</td>
<td>Cortex-M0+ interrupt control 3</td>
</tr>
<tr>
<td>CPUSS_CM0_INT_CTL4</td>
<td>Cortex-M0+ interrupt control 4</td>
</tr>
<tr>
<td>CPUSS_CM0_INT_CTL5</td>
<td>Cortex-M0+ interrupt control 5</td>
</tr>
<tr>
<td>CPUSS_CM0_INT_CTL6</td>
<td>Cortex-M0+ interrupt control 6</td>
</tr>
<tr>
<td>CPUSS_CM0_INT_CTL7</td>
<td>Cortex-M0+ interrupt control 7</td>
</tr>
<tr>
<td>CPUSS_CM4_NMI_CTL</td>
<td>Cortex-M4 NMI control</td>
</tr>
<tr>
<td>SYSTEM_CM0P_SCS_ISER</td>
<td>Cortex-M0+ interrupt set-enable register</td>
</tr>
<tr>
<td>SYSTEM_CM0P_SCS_ICER</td>
<td>Cortex-M0+ interrupt clear enable register</td>
</tr>
<tr>
<td>SYSTEM_CM0P_SCS_ISPR</td>
<td>Cortex-M0+ interrupt set-pending register</td>
</tr>
<tr>
<td>SYSTEM_CM0P_SCS_ICPR</td>
<td>Cortex-M0+ interrupt clear-pending register</td>
</tr>
<tr>
<td>SYSTEM_CM0P_SCS_IPR</td>
<td>Cortex-M0+ interrupt priority register</td>
</tr>
<tr>
<td>SYSTEM_CM0P_SCS_ICSR</td>
<td>Cortex-M0+ interrupt control state register</td>
</tr>
<tr>
<td>SYSTEM_CM0P_SCS_VTOR</td>
<td>Cortex-M0+ vector table offset register</td>
</tr>
<tr>
<td>SYSTEM_CM0P_SCS_AIRCR</td>
<td>Cortex-M0+ application interrupt and reset control register</td>
</tr>
<tr>
<td>SYSTEM_CM0P_SCS_SHPR2</td>
<td>Cortex-M0+ system handler priority register 2</td>
</tr>
<tr>
<td>SYSTEM_CM0P_SCS_SHPR3</td>
<td>Cortex-M0+ system handler priority register 3</td>
</tr>
<tr>
<td>SYSTEM_CM0P_SCS_SHCSR</td>
<td>Cortex-M0+ system handler control and state register</td>
</tr>
<tr>
<td>SYSTEM_CM4_SCS_ISER</td>
<td>Cortex-M4 interrupt set-enable register</td>
</tr>
<tr>
<td>SYSTEM_CM4_SCS_ICER</td>
<td>Cortex-M4 interrupt clear enable register</td>
</tr>
<tr>
<td>SYSTEM_CM4_SCS_ISPR</td>
<td>Cortex-M4 interrupt set-pending register</td>
</tr>
<tr>
<td>SYSTEM_CM4_SCS_ICPR</td>
<td>Cortex-M4 interrupt clear-pending register</td>
</tr>
<tr>
<td>SYSTEM_CM4_SCS_JPR</td>
<td>Cortex-M4 interrupt priority registers</td>
</tr>
<tr>
<td>SYSTEM_CM4_SCS_VTOR</td>
<td>Cortex-M4 vector table offset register</td>
</tr>
<tr>
<td>SYSTEM_CM4_SCS_AIRCR</td>
<td>Cortex-M4 application interrupt and reset control register</td>
</tr>
<tr>
<td>SYSTEM_CM4_SCS_SHPR2</td>
<td>Cortex-M4 system handler priority register 2</td>
</tr>
<tr>
<td>SYSTEM_CM4_SCS_SHPR3</td>
<td>Cortex-M4 system handler priority register 3</td>
</tr>
<tr>
<td>SYSTEM_CM4_SCS_SHCSR</td>
<td>Cortex-M4 system handler control and state register</td>
</tr>
</tbody>
</table>
8. Protection Units

Protection units are implemented in the PSoC 6 MCU to enforce security based on different operations. A protection unit allows or restricts bus transfers on the bus infrastructure. The rules are enforced based on specific properties of a transfer.

8.1 Features

- An address range that is accessed by the transfer
- Access attributes such as:
  - Read/write attribute
  - Execute attribute to distinguish a code access from a data access
  - User/privilege attribute to distinguish access; for example, OS/kernel access from a task/thread access
  - Secure/non-secure attribute to distinguish a “secure” access from a “non-secure” access.
  - A protection context attribute to distinguish accesses from different protection contexts

8.2 Architecture

A protection structure is a register structure that defines this rule. Each protection structure defines a rule, which includes an address range and the access attributes.

In addition, each bus master has its own access attributes, which define the bus master’s access privileges. Some of these attributes, such as secure/non-secure, are set for a master. Other attributes such as protection context and user/privilege attribute are dynamic attributes, which change based on bus master’s context and state.

Thus protection units secure bus transfer address range either in memory locations (SRAM/flash) or peripheral registers. From an architectural perspective, there is no difference between memory protection and peripheral protection. However, from an implementation perspective, separate memory protection and peripheral protection are provided.

- Two types of protection units, MPU and SMPU, are provided in the CPU subsystem (CPUSS) to protect memory locations:
  - MPUs are intended to distinguish user and privileged accesses from a single bus master
  - SMPUs are intended to distinguish between different protection contexts and to distinguish secure from non-secure accesses
- PPUs are protection units provided in the PERI register space for peripheral protection. Refer to the PSoC 63 with BLE Registers TRM for details. The PPUs are intended to distinguish between different protection contexts and to distinguish secure from non-secure accesses and user mode accesses from privileged mode accesses.

A bus master may have a dedicated MPU. In a CPU bus master, the MPU is typically implemented as part of the CPU and under control of the OS/kernel. In a non-CPU bus master, the MPU is typically implemented as part of the bus infrastructure and under control of the OS/kernel of the CPU that “owns or uses” the bus master. If a CPU switches tasks or if a non-CPU switches ownership, the MPU settings are typically updated by OS/kernel software. The different MPU types are:

- An MPU that is implemented as part of the CPU. This type is found in the Arm CM0+ and CM4 CPUs.
- An MPU that is implemented as part of the bus infrastructure. This type is found in bus masters such as crypto and test controller. The definition of this MPU type follows the Arm MPU definition (in terms of memory region and access attribute definition) to ensure a consistent software interface.

The platform’s DMA controller does not have an MPU. Instead, a DMA controller channel inherits the access control attributes of the bus transfer that programmed the channel.
The definition of SMPU and PPU follows the MPU definition and adds the capability to distinguish accesses from different protection contexts (the MPU does not include support for a protection context). If security is required, the SMPU and possibly PPUs MMIO registers must be controlled by a secure CPU that enforces system-wide protection.

Figure 8-1 gives an overview of the location of MPUs, SMPUs, and PPUs in the system. Note that a peripheral group PPU needs to provide access control only to the peripherals within a peripheral group (group of peripherals with a shared bus infrastructure).

As mentioned, the MPU, SMPU, and PPU protection functionality follows the Arm MPU definition:

- Multiple protection structures are supported.
- Each structure specifies an address range in the unified memory architecture and access attributes. An address range can be as small as 32 bytes.

A protection violation is caused by a mismatch between a bus transfer’s address region and access attributes and the protection structure address range and access attributes. A protection structure address range is 32 bytes, multiple cycles are required for matching – one cycle per 32-byte region.

Protection violations are captured in the fault report structure to allow for failure analysis. The fault report structures can generate an interrupt to indicate the occurrence of a fault. This is useful if the violating bus master cannot resolve the bus error by itself, but requires another CPU bus master to resolve the bus error on its behalf.

A protection violation results in a bus error and the bus transfer will not reach its target. An MPU or SMPU violation that targets a peripheral will not reach the associated PPU. In other words, MPU and SMPU have a higher priority over PPU.

Protection unit addresses the following:

- Security requirements. This includes prevention of malicious attacks to access secure memory or peripherals. For example, a non-secure master should not be able to access key information in a secure memory region.

- Safety requirements. This includes detection of accidental (non-malicious) software errors and random hardware errors. Enabling failure analysis is important.
so the root cause of a safety violation can be investigated. For example, analyzing a flash memory failure on a device that is returned from the field should be possible.

To address security requirements, the Cortex M0+ is used as a ‘secure CPU’. This CPU is considered a trusted entity.

8.3 Bus Master Attributes

The protection structures set up the rules for different memory regions and their access attributes. The bus master’s own access attributes are used by the protection units to regulate access, based on rules set by the protection structures. Not all masters provide all access attributes that are associated with a bus transfer. Some examples are:

- None of the bus masters has a native protection context attribute. This must be set dynamically based on the task being executed by the bus master.
- The Arm Cortex M4 and Arm Cortex M0+ CPUs provide a user/privilege attribute, but do not provide a secure/non-secure attribute natively. This must be set at a system level.

To ensure system-wide restricted access, missing attributes are provided by register fields. These fields may be set during the boot process or by the secure CPU.

- The SMPU MS_CTL.PC_MASK[15:0] and MPU MS_CTL.PC[3:0] register fields provide protection context functionality.
- The SMPU MS_CTL.P register field provides the user/privileged attribute for those masters that do not provide their own attribute.
- The SMPU MS_CTL.NS register provides the secure/non-secure attribute for those masters that do not provide their own attribute.
- Masters that do not provide an execute attribute have the execute attribute set to ‘0’.

The DMA controller channels inherit the access control attributes of the bus transfers that configured the DMA channel.

- All the bus masters in the system have SMPU and MPU MS_CTL registers associated with them.
- The MPU MS_CTL.PC_SAVED field (and associated protection context 0 functionality, which is discussed later in the chapter) is only present for the CM0+ master.
- The SMPU MS_CTL.P, MS_CTL.NS, and MS_CTL.PC_MASK fields are not present for the DMA. The bus transfer attributes are provided through “inheritance”: the bus transfer attributes are from the master that owns the DMA channel that initiated the bus transfer.

- The MPU MS_CTL register is not present for the DMA masters. The protection context (PC) bus transfer attribute is provided through inheritance.

8.4 Protection Context

Each bus master has a MPU MS_CTL.PC[3:0] protection context field. This protection context is used as the protection context attribute for all bus transfers that are initiated by the master. The SMPUs and PPUs allow or restrict bus transfers based on the protection context attribute.

Multiple masters can share a protection context. For example, a CPU and a crypto controlled by the CPU may share a protection context (the CPU and crypto PC[] fields are the same). Therefore, the CPU and crypto share the SMPU and PPU access restrictions.

A bus master protection context is changed by reprogramming the master’s PC[] field. Changing a protection context is required for CPU bus masters that may transition between multiple tasks, each catering to different protection contexts. As the protection context allows or restricts bus transfers, changes to the protection context should be controlled and should not compromise security. Furthermore, changes to the protection context should incur limited CPU overhead to allow for frequent protection context changes. Consider a case in which a CPU executes two software stacks with different protection contexts. To this end, each bus master has an SMPU MS_CTL.PC_MASK[15:0] protection context mask field that identifies what protection contexts can be programmed for the bus master:

- The protection context field MS_CTL.PC[3:0]. This register is controlled by the associated bus master and has the same access restrictions as the bus master’s MPU registers.
- The protection context mask field MS_CTL.PC_MASK[15:0]. This register is controlled by the secure CPU and has the same access restrictions as the SMPU registers.

The PC_MASK[] field is a "hot-one" field that specifies whether the PC[] field can be programmed with a specific protection context. Consider an attempt to program PC[] to ‘3’:

- If PC_MASK[3] is ‘1’, PC[] is set to “3”.
- If PC_MASK[3] is ‘0’, PC[] is not changed.

8.5 Protection Context 0

Protection context 0 has dedicated functionality not available to the user. In a system that requires protection, a “root of trust” must be established. In the PSoC 6 MCU, the Arm CM0+ CPU is intended to be used as the “secure CPU” that executes both Cypress code and customer code.
The Cypress code for the secure CPU, either in ROM or in flash, is considered trustworthy. The Cypress ROM code can be considered as the root of trust, and can be used to authenticate Cypress flash code. Cypress code can be used to provide flash programming, eFuse programming, or other Cypress proprietary functionality.

The customer code for the secure CPU is programmed in flash. Therefore, Cypress has no control over this code. It cannot be assumed that this code is trustworthy and is not compromising Cypress-trusted code.

As both Cypress-trusted code and customer untrusted code are executed on the same CPU, the general protection scheme based on master specific protection contexts, which is completely software-controlled, does not suffice to distinguish the two different types of code. For example, a scheme that relies on separate protection contexts for the two different types of code relies on cooperation, which is something that cannot be relied upon if the customer code is untrusted: nothing prevents customer code from taking the protection context of Cypress code.

Therefore, hardware support is provided to control the secure CPU protection context. This support assigns special meaning to protection context 0. Well-defined entry into Cypress-trusted code in ROM changes the protection context to 0. Protection context 0 provides unlimited (unprotected) access to all memory regions and peripherals. The protection context is changed to 0 under the following two conditions:

- A secure CPU reset. This results in the execution of the reset exception handler. The vector address is provided from ROM address 0x0004:0004. As this is a ROM address, this address can be trusted. If the vector address is also in ROM, the handler’s entry point can be trusted.

  Note that after a secure CPU reset, all interrupts are disabled and CPU execution is deterministic (fully determined by the reset exception handler).

- A secure CPU exception/interrupt handler entry. The handler vector address is provided by the vector table with base address VECTOR_TABLE_BASE. After a secure CPU reset, this VECTOR_TABLE_BASE is 0x0004:0000 and the handler vector address is related to this base. As this is a ROM address, this address can be trusted. However, the CPU can relocate VECTOR_TABLE_BASE to an SRAM address for example, and the handler vector addresses can be programmed to any value. The programmed value may result in customer-provided handler code. As a result, the handler’s entry point cannot be trusted. Fortunately, it is possible to detect whether the vector address from the vector table is different from a specific address. The protection context is only changed to 0 if the secure CPU vector handler address is the same as the specific vector address CM0_PC0_HANDLER. Note that the customer code can relocate the vector table, but a change to protection context 0 requires that the vector address is not modified and still equal to CM0_PC0_HANDLER.

Protection context 0 identifies Cypress-trusted code and provides unlimited access:

- The protection structures are not applied; no protection structure match will “hit” on a protection context 0 address. The user/privileged and secure/non-secure transfer attributes have no protection functionality for protection context 0.

- Hardware changes the protection context to 0 and Cypress-trusted software is responsible for re-establishing the protection context that applied before the Cypress-trusted code is entered. To this end, the secure CPU has two protection context fields in its MS_CTL register (hardware changes both fields):
  - A PC[3:0] field, which specifies the current protection context.
  - A PC_SAVED[3:0] field, which specifies the protection context that applied when the protection context was changed to 0.

The Cypress-trusted exception handler is responsible for updating the MS_PC field when leaving the Cypress-trusted code. For all n, PROT_MPUn_MS_CTL and PROT_MPUn_MS_CTL_PC_SAVED are set to ‘1’. Also for all n, bit 0 of PROT_SMPU_MSn_CTL_PC_MASK is set to ‘1’ to allow PC to have a value of 1.

The Cypress-trusted exception handler is responsible for re-establishing the MS_PC field with the MS_PC_SAVED field when leaving the Cypress-trusted code.

8.6 Protection Structure

The MPU, SMPU, and PPU protection structure definition follows the Arm definition. Each protection structure is defined by:

- An address region
- Access control attributes

A protection structure is always aligned on a 32-byte boundary in the memory space. Two registers define a protection structure: ADDR (address register) and ATT (attribute register). This structure alignment and organization allow for straightforward protection of the protection structures by the protection scheme. This is discussed later in this chapter.

Address region. The address region is defined by:

- The base address of a region as specified by ADDR.ADDR.
- The size of a region as specified by ATT_REGION_SIZE.
- Individual disables for eight subregions within the region, as specified by ADDR.SUBREGION_DISABLE.
The REGION_SIZE field specifies the size of a region. The region size is a power of 2 in the range of [256 B, 4 GB]. The base address ADDR specifies the start of the region, which must be aligned to the region size. A region is partitioned into eight equally sized subregions. The SUBREGION_DISABLE field specifies individual enables for the subregions within a region.

For example, a REGION_SIZE of “8” specifies a region size of 512 bytes. If the start address is 0x1000:5400 (512-byte aligned), the region ranges from 0x1000:5400 to 0x1000:55ff. This region is partitioned into the following eight 64-byte subregions:

- subregion 0 from 0x1000:5400 to 0x1000:543f
- subregion 1 from 0x1000:5440 to 0x1000:547f
- ...
- subregion 7 from 0x1000:55c0 to 0x1000:55ff

If the SUBREGION_DISABLE is 0x82 (bitfields 1 and 7 are ‘1’), subregions 1 and 7 are disabled; subregions 0, 2, 3, 4, 5, and 6 are enabled.

In addition, an ATT.ENABLED field specifies whether the region is enabled. Only enabled regions participate in the protection “matching” process. Matching identifies if a bus transfer address is contained within an enabled subregion (SUBREGION_DISABLE) of an enabled region (ENABLED).

**Access control attributes.** The access attributes specify access control to the region (shared by all subregions within the region). Access control is performed using a transfer’s access attributes. The following access control fields are supported:

- Control for read accesses in user mode (ATT.UR field).
- Control for write accesses in user mode (ATT.UW field).
- Control for execute accesses in user mode (ATT.UX field).
- Control for read accesses in privileged mode (ATT.PR field).
- Control for write accesses in privileged mode (ATT.PW field).
- Control for execute accesses in privileged mode (ATT.PX field).
- Control for secure access (ATT.NS field).
- Control for individual protection contexts (ATT.PC_MASK[15:0], with MASK[0] always constant at ‘1’). This protection context control field is present only for the SMPU and PPU.

The execute and read access control attributes are orthogonal. Execute transfers are typically read transfers. To allow execute and read transfers in user mode, both ATT.UR and ATT.UX must be set to ‘1’. To allow data and read transfers in user mode, only ATT.UR must be set to ‘1’.

In addition, the ATT.PC_MATCH control field is supported, which controls “matching” and “access evaluation” processes. This control field is present only for the SMPU and PPU protection structures.

For example, only protection context 2 can access a specific address range. These accesses are restricted to read and write secure accesses in privileged mode. The access control fields are programmed as follows:

- ATT.UR is ‘0’: read accesses in user mode not allowed.
- ATT.UW is ‘0’: write accesses in user mode not allowed.
- ATT.UX is ‘0’: execute accesses in user mode not allowed.
- ATT.PR is ‘1’: read accesses in privileged mode allowed.
- ATT.PW is ‘1’: write accesses in privileged mode allowed.
- ATT.PX is ‘0’: execute accesses in privileged mode not allowed.
- ATT.NS is ‘0’: secure access required.
- ATT.PC_MASK is “0x0005”: protection context 1 and 3 accesses enabled (all other protection contexts are disabled).
- ATT.PC_MATCH is ‘0’: the PC_MASK field is used for access evaluation.

Three separate access evaluation subprocesses are distinguished:

- A subprocess that evaluates the access based on read/write, execute, and user/privileged access attributes.
- A subprocess that evaluates the access based on the secure/non-secure attribute.
- A subprocess that evaluates the access based on the protection context index (used only by the SMPU and PPU when ATT.PC_MATCH is ‘0’).

If all access evaluations are successful, access is allowed. If any process evaluation is unsuccessful, access is not allowed.

Matching the bus transfer address and access evaluation of the bus transfer (based on access attributes) are two independent processes:

- Matching process. For each protection structure, the process identifies whether a transfer address is contained within the address range. This identifies the “matching” regions.
- Access evaluation process. For each protection structure, the process evaluates the bus transfer access attributes against the access control attributes.

A protection unit typically has multiple protection structures. A protection unit evaluates the protection structures in decreasing order. The first matching structure provides the access control attributes for the evaluation of the transfer’s access attributes. In other words, higher-indexed structures take precedence over lower-indexed structures.
Notes:

- If no protection structure provides a match, the access is allowed.
- If multiple protection structures provide a match, the access control attributes for the access evaluation are provided by the protection structure with the highest index.

An example of using the PC_MATCH feature is as follows:

Two SMPU structures are configured to protect the same address range:

- Case 1:
  SMPU#2: PC = 3, PC_MATCH = 0
  SMPU#1: PC = 2, PC_MATCH = 0
  To access the master of protection context 2, SMPU#2 has highest index and the address match, but attributes do not match; therefore, access is restricted. The SMPU#1 is not evaluated because the PC_MATCH is 0.

- Case 2:
  SMPU#2: PC = 3, PC_MATCH = 1
  SMPU#1: PC = 2, PC_MATCH = 0
  The SMPU#2 address matches but PC does not match, and is skipped because PC_MATCH is 1. SMPU#1 is evaluated and the address and attributes match; therefore, access is allowed.

As mentioned, the protection unit evaluates the protection structures in decreasing order. From a security requirements perspective, this is of importance: a non-secure protection context must not be able to add protection structures that have a higher index than the protection structures that provide secure access. The protection structure with a higher index can be programmed to allow non-secure accesses. Therefore, in a secure system, the higher programmable protection structures are protected to only allow restricted accesses. For more details, see Protection of Protection Structures on page 69).

8.6.1 Protection Violation

If an MPU, SMPU, or PPU detects a not-allowed transfer, the bus transfer results in a bus error. The bus transfer does not reach its target memory location or peripheral register. In addition, information on the violating bus transfer is communicated to the fault report structure.

8.6.2 MPU

The MPUs are situated in the CPUSS and are associated to a single master. An MPU distinguishes user and privileged accesses from a single bus master. However, the capability exists to perform access control on the secure/non-secure attribute.

As an MPU is associated to a single master, the MPU protection structures do not provide protection context control attributes.

![Figure 8-2. MPU Functionality](image-url)
8.6.3 SMPU

The SMPU is situated in the CPUSS and is shared by all bus masters. The SMPU distinguishes between different protection contexts and distinguishes secure from non-secure accesses. However, the capability exists to perform access control on the user/privileged mode attribute.

Figure 8-3. SMPU Functionality

Note that a single set of SMPU region structures provides the same protection information to all SMPUs in the systems.

8.6.4 PPU

The PPUs are situated in the PERI block and are associated with a peripheral group (a group of peripherals with a shared AHB-Lite bus infrastructure). A PPU is shared by all bus masters. The PPU distinguishes between different protection contexts; it also distinguishes secure from non-secure accesses and user mode from privileged mode accesses.

Figure 8-4. PPU Functionality

There are two types of PPU structures: fixed and programmable.

- The fixed-PPU structures protect fixed areas of memory and hence a specific predetermined peripheral region. In other words, the ADDR, SUBREGION_DISABLE, and REGION_SIZE fields are fixed for a specific device. Refer to the PSoC 63 with BLE Registers TRM for definition of fixed PPUs and the address regions they protect. Their protection attributes are configurable. Fixed PPUs protect peripheral regions in three levels. The PPU_GR structures protect at the MMIO level. The PPU_SL structures protect each slave in each MMIO. The PPU_RG structures protect each instance of a block in the slave. For example, IPC channels in IPC are protected by PPU_RG structures while the entire IPC block is protected by PPU_SL register.

- The programmable PPU structures can have configurable protection attributes and address regions. These are similar to SMPU structures but should be used with the peripheral register space. These protection structures are typically used to protect registers in a specific block, which are not covered by the resolution of PPU_RG structures.
8.6.5 Protection of Protection Structures

The MPU, SMPU, and PPU-based protection architecture is consistent and provides the flexibility to implement different system-wide protection schemes. Protection structures can be set once at boot time or can be changed dynamically during device execution. For example, a CPU RTOS can change the CPU’s MPU settings; a secure CPU can change the SMPU and PPUs settings. But such a system will be left insecure if there is no way to protect the protection structures themselves. There must be a way to restrict access to the protection structures.

The protection of protection structures is achieved using another protection structure. For this reason, protection structures are defined in pairs of master and slave. We refer to the slave and master protection structures as a protection pair. Note that the address range of the master protection structure is known, that is, it is constant.

The first (slave) protection structure protects the resource and the second (master) protection structure protects the protection (address range of the second protection structure includes both the master and slave protection structures).

The protection architecture is flexible enough to allow for variations:

- Exclusive peripheral ownership can be shared by more than two protection contexts.
- The ability to change ownership is under control of a single protection context, and exclusive or non-exclusive peripheral ownership is shared by multiple protection contexts.

Note that in secure systems, typically a single secure CPU is used. In these systems, the ability to change ownership is assigned to the secure CPU at boot time and not dynamically changed. Therefore, you must assign the secure CPU its own, dedicated protection context.

Both PPU and SMPU is intended to distinguish between different protection contexts and to distinguish secure from non-secure accesses. Therefore, both PPU and SMPU protection use protection structure pairs. In the SMPU, the slave protection structure provides SMPU protection information and the master protection structure provides PPU protection information (the master and slave protection structures are registers).

8.6.6 Protection Structure Types

Different protection structure types are used because some resources, such as peripheral registers, have a fixed address range. Protection of protection structures requires pairs of neighboring protection structures.

Three types of protection structures with a consistent register interface are described here:

- Programmable protection structures. These are 32-byte protection structures with a programmable address range. These structures are used by the MPUs.
- Fixed protection structure pairs. These are 64-byte master/slave protection structure pairs, consisting of two 32-byte protection structures. These structures are used by the PPUs. Both structures have a fixed, constant address region. The master structure has the UX and PX attributes as constant ‘0’ (execution is never allowed) and the UR and PR attributes as constant ‘1’ (reading is always allowed). The slave structure has the UX and PX attributes as constant ‘1’.
- Programmable protection structure pairs. These are 64-byte master/slave protection structure pairs, consisting of two 32-byte protection structures. These structures are used by the PPU and SMPU. The master structure has the UX and PX attributes as constant ‘0’ (execution is never allowed) and the UR and PR attributes as constant ‘1’ (reading is always allowed). The slave structure has the UX and PX attributes as constant ‘1’.

Note that the master protection structure in a protection structure pair is required only to address security requirements. The distinction between the three protection structure types is an implementation optimization. From an architectural perspective, all PPU protection structures are the same, with the exception that for some protection structures the address range is fixed and not programmable.

As mentioned earlier, a protection unit evaluates the protection regions in decreasing protection structure index order. The protection structures are evaluated in the following order:

- Fixed protection structures for specific peripherals or peripheral register address ranges.
- Programmable protection structures.

In other words, fixed structures take precedence over programmable structures.
Figure 8-5. Fixed Protection Structure Pair

**PPU, fixed protection structure pair**

**Slave structure**

<table>
<thead>
<tr>
<th>ADDR</th>
<th>Constant ADDR[23:0], encompassing peripheral slave MMIO registers</th>
<th>Constant SUBREGION_DISABLE</th>
</tr>
</thead>
</table>

**ATT**

<table>
<thead>
<tr>
<th>ENABLED</th>
<th>PC.MATCH</th>
<th>CONSTANT.SIZE</th>
<th>PC_MASK[15:1]</th>
<th>NS</th>
<th>PX</th>
<th>PW</th>
<th>PR</th>
<th>UX</th>
<th>UW</th>
<th>UR</th>
</tr>
</thead>
</table>

**Master structure**

<table>
<thead>
<tr>
<th>ADDR</th>
<th>Constant ADDR[23:0], encompassing master and slave protection structures</th>
<th>Constant SUBREGION_DISABLE</th>
</tr>
</thead>
</table>

**ATT**

<table>
<thead>
<tr>
<th>ENABLED</th>
<th>PC.MATCH</th>
<th>CONSTANT.SIZE</th>
<th>PC_MASK[15:1]</th>
<th>NS</th>
<th>PX</th>
<th>PW</th>
<th>PR</th>
<th>UX</th>
<th>UW</th>
<th>UR</th>
</tr>
</thead>
</table>
Protection Units

Figure 8-6. Programmable Protection Structure Pair

**PPU, programmable protection structure pair**

**Slave structure**

**Master structure**

**SMPU, programmable protection structure pair**

**Slave structure**

**Master structure**

**SMPU, programmable protection structure pair**
9. DMA Controller

The DMA transfers data to and from memory, peripherals, and registers. These transfers occur independent from the CPU. The DMA can be configured to perform multiple independent data transfers. All data transfers are managed by a channel. There can be up to 32 channels in the DMA. The number of channels in the DMA controller can vary with devices. Refer to the device datasheet for the number of channels supported in the device. A channel has an associated priority; channels are arbitrated according to their priority.

9.1 Features

The DMA controller has the following features:

- Supports up to 32 channels per DMA controller; see the device datasheet for details
- Supports multiple DMA controller instances in a device
- Four levels of priority for each channel
- Descriptors are defined in memory and referenced to the respective channels
- Supports single, 1D, or 2D transfer modes for a descriptor
- Supports transfer of up to 65536 data elements per descriptor
- Configurable source and destination address increments
- Supports 8-bit, 16-bit, and 32-bit data widths at both source and destination
- Configurable input trigger behavior for each descriptor
- Configurable interrupt generation in each descriptor
- Configurable output trigger generation for each descriptor
- Descriptors can be chained to other descriptors in memory
A data transfer is initiated by an input trigger. This trigger may originate from the source peripheral of the transfer, the destination peripheral of the transfer, CPU software, or from another peripheral. Triggers provide Active/Sleep functionality and are not available in Deep Sleep and Hibernate power modes.

The data transfer details are specified by a descriptor. Among other things, this descriptor specifies:

- The source and destination address locations and the size of the transfer.
- The actions of a channel; for example, generation of output triggers and interrupts. See the Interrupts chapter on page 47 for more details.
- Data transfer types can be single, 1D, or 2D as defined in the descriptor structure. These types define the address sequences generated for source and destination. 1D and 2D transfers are used for “scatter gather” and other useful transfer operations.

### 9.3 Channels

The DMA controller supports multiple independent data transfers that are managed by a channel. Each channel connects to a specific system trigger through a trigger multiplexer that is outside the DMA controller.

**Channel priority:** A channel is assigned a priority (CHi_CTL.PRIO) between 0 and 3, with 0 being the highest priority and 3 being the lowest priority. Channels with the same priority constitute a priority group. Priority decoding determines the highest priority pending channel, which is determined as follows.

- The highest priority group with pending channels is identified first.
- Within this priority group, round-robin arbitration is applied. Round-robin arbitration within a priority group gives the highest priority to the lower channel indices in the priority group.

**Channel state:** At any given time, one channel actively performs a data transfer. This channel is called the active channel. A channel can be in one of four channel states.

<table>
<thead>
<tr>
<th>Channel State</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disabled</td>
<td>The channel is disabled by setting CHi_CTL.ENABLED to '0'. The channel trigger is ignored in this state.</td>
</tr>
<tr>
<td>Blocked</td>
<td>The channel is enabled and is waiting for a trigger to initiate a data transfer.</td>
</tr>
<tr>
<td>Pending</td>
<td>The channel is enabled and has received an active trigger. In this state, the channel is ready to initiate a data transfer but waiting for it to be scheduled.</td>
</tr>
<tr>
<td>Active</td>
<td>The channel is enabled, has received an active trigger and has been scheduled. It is actively performing data transfers. If there are multiple channels pending, the highest priority pending channel is scheduled.</td>
</tr>
</tbody>
</table>
The data transfer associated with a trigger is made up of one or more ‘atomic transfers’ or ‘single transfers’; see Table 9-2 for a better understanding. A single trigger could be configured to transfer multiple “single transfers”. A channel can be marked preemptable (CHi_CTL.PREEMPTABLE). If preemptable, and there is a higher priority pending channel, then that higher priority channel can preempt the current channel between single transfers.

A channel has two access control attributes that are used by the shared memory protection units (SMPUs) and peripheral protection units (PPUs) for access control. These fields are typically inherited from the master that modified the channel’s control register.

- The Privileged Mode (CHi_CTL.P) attribute can be set to privileged or user.
- The Non-secure (CHi_CTL.NS) attribute can be set to secure or non-secure.

A descriptor associated with each channel describes the data transfer. The descriptor is stored in memory and CHi_CURR_PTR provides the descriptor address associated with channel “i” and Chi_IDX provides the current X and Y indices into the descriptor.

A channel’s descriptor state is encoded as part of the channel’s register state. The following registers provide a channel’s descriptor state:

- CH_CTL. This register provides generic channel control information.
- CH_CURR_PTR. This register provides the address of the memory location where the current descriptor is located. The user firmware must initialize this register. If the descriptors are chained, the DMA hardware automatically sets this register to the next descriptor pointer.
- CH_IDX. This register provides the current X and Y indices of the channel into the current descriptor. User firmware must initialize this register. DMA hardware sets the X and Y indices to 0, when advancing from the current descriptor to the next descriptor in a descriptor list.

Note that channel state is retained in Deep Sleep power mode.
9.4 Descriptors

The data transfer between a source and destination in a channel is configured using a descriptor. Descriptors are stored in memory. The descriptor pointer is specified in the DMA channel registers. The DMA controller does not modify the descriptor and treats it as read only. A descriptor is a set of up to six 32-bit registers that contain the configuration for the transfer in the associated channel. There are three types of descriptors.

<table>
<thead>
<tr>
<th>Descriptor Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single transfer</td>
<td>Transfers a single data element</td>
</tr>
<tr>
<td>1D transfer</td>
<td>Performs a one-dimensional “for loop”. This transfer is made up of X number of single transfers</td>
</tr>
<tr>
<td>2D transfer</td>
<td>Performs a two-dimensional “for loop”. This transfer is made up of Y number of 1D transfers</td>
</tr>
</tbody>
</table>

Table 9-2. Descriptor Types

**Single Transfer:**

The following pseudo code illustrates a single transfer.

```c
// DST_ADDR is a pointer to an object of type defined by DST_TRANSFER_SIZE
// SRC_ADDR is a pointer to an object of type defined by SRC_TRANSFER_SIZE
// t_DATA_SIZE is the type associated with the DATA_SIZE
DST_ADDR[0] = (t_DATA_SIZE) SRC_ADDR[0];
```

**1D Transfer:**

The following pseudo code illustrates a 1D transfer. Note that the 1D transfer is represented by a loop with each iteration executing a single transfer.

```c
// DST_ADDR is a pointer to an object of type defined by DST_TRANSFER_SIZE
// SRC_ADDR is a pointer to an object of type defined by SRC_TRANSFER_SIZE
// t_DATA_SIZE is the type associated with the DATA_SIZE
```
for (X_IDX = 0; X_IDX <= X_COUNT; X_IDX++) {
    DST_ADDR[X_IDX * DST_X_INCR] = 
        (t_DATA_SIZE) SRC_ADDR[X_IDX * SRC_X_INCR];
}

2D Transfer:

The following pseudo code illustrates a 2D transfer. Note that the 2D transfer is represented by a loop with each iteration executing an inner loop, which is the 1D transfer.

// DST_ADDR is a pointer to an object of type defined by DST_TRANSFER_SIZE
// SRC_ADDR is a pointer to an object of type defined by SRC_TRANSFER_SIZE
// t_DATA_SIZE is the type associated with the DATA_SIZE
for (Y_IDX = 0; Y_IDX <= Y_COUNT; Y_IDX++) {
    for (X_IDX = 0; X_IDX <= X_COUNT; X_IDX++) {
        DST_ADDR[X_IDX * DST_X_INCR + Y_IDX * DST_Y_INCR ] = 
            (t_DATA_SIZE) SRC_ADDR[X_IDX * SRC_X_INCR + Y_IDX * SRC_Y_INCR];
    }
}

The parameters in the descriptor help configure the different aspects of the transfers explained.

Figure 9-3 shows the structure of a descriptor.

### 9.4.1 Address Configuration

**Source and Destination Address:** The source and destination addresses are set in the respective registers in the descriptor. These set the base addresses for the source and destination location for the transfer. In case the descriptor is configured to transfer a single element, this field holds the source/destination address of the data element. If the descriptor is configured to transfer multiple elements with source address or destination address or both in an incremental mode, this field will hold the address of the first element that is transferred.

**DESCR_TYPE:** This field configures whether the descriptor has a single, 1D, or 2D type.

**Trigger input type, TR_IN_TYPE:** This field determines how the DMA engine responds to input trigger signal. This field can be configured for one of the following modes:

- **Type 0:** A trigger results in execution of a single transfer. Regardless of the DESCR_TYPE setting, a trigger input will trigger only a single element transfer. For example, in a 1D transfer, the DMA will transfer only one data element in every trigger.
- **Type 1:** A trigger results in the execution of a single 1D transfer. If the DESCR_TYPE was set to single transfer, the trigger signal will trigger the single transfer specified by the descriptor. For a DESCR_TYPE set to 1D transfer, the trigger signal will trigger the entire 1D transfer configured in the descriptor. For a 2D transfer,
the trigger signal will trigger only a single iteration of the Y loop transfer.

- **Type 2**: A trigger results in execution of the current descriptor. Regardless of DESCR_TYPE, the trigger will execute the entire descriptor. If there was a next descriptor configured for the current descriptor, this trigger setting will not automatically trigger the next descriptor.

- **Type 3**: A trigger results in execution of the current descriptor and also triggering the next descriptor. The execution of the next descriptor from this point will be determined by the TR_IN_TYPE setting of the next descriptor.

**Trigger out type, TR_OUT_TYPE**: This field determines what completion event will generate the output trigger signal. This field can be configured to one of the following modes:

- **Type 0**: Generates a trigger output for completion of every single element transfer.
- **Type 1**: Generates a trigger output for completion of a 1D transfer.
- **Type 2**: Generates a trigger output for completion of the current descriptor. This trigger output is generated independent of the state of the DESCR_NEXT_PTR.
- **Type 3**: Generates a trigger output on completion of the current descriptor, when the current descriptor is the last descriptor in the descriptor chain. This means a trigger is generated when the descriptor execution is complete and the DESCR_NEXT_PTR is '0'.

**Interrupt Type, INTR_TYPE**: This field determines which completion event will generate the output interrupt signal. This field can be configured to one of the following modes:

- **Type 0**: Generates an interrupt output for completion of every single element transfer.
- **Type 1**: Generates an interrupt output for completion of a 1-D transfer.
- **Type 2**: Generates an interrupt output for completion of the current descriptor. This interrupt output is generated independent of the state of the DESCR_NEXT_PTR.
- **Type 3**: Generates an interrupt output on completion of the current descriptor, when the current descriptor is the last descriptor in the descriptor chain. This means an interrupt is generated when the descriptor execution is complete and the DESCR_NEXT_PTR is '0'.

**WAIT_FOR_DEACT**: When the DMA transfer based on the TR_IN_TYPE is completed, the data transfer engine checks the state of trigger deactivation. The data transfer on the second trigger is initiated only after deactivation of the first. The WAIT_FOR_DEACT parameter will determine when the trigger signal is considered deactivated. The first DMA transfer is activated when the trigger is activated, but the transfer is not considered complete until the trigger is deactivated. This field is used to synchronize the controller's data transfers with the agent that generated the trigger. This field has four settings:

- **0 – Pulse Trigger**: Do not wait for deactivation.
- **1 – Level-sensitive**: waits four or 16 SYSCLK cycles: The DMA trigger is deactivated after the level trigger signal is detected for four cycles.
- **2 – Level-sensitive**: waits 16 SYSCLK cycles: The DMA transfer is initiated if the input trigger is seen to be activated after 16 clock cycles.
- **3 – Pulse trigger**: waits indefinitely for deactivation. The DMA trigger is initiated after the trigger signal deactivates. The next transfer is initiated only if the trigger goes low and then high again.

**X Count**: This field determines the number of single element transfers present in the X loop (inner loop). This field is valid when the DESCR_TYPE is set to 1D or 2D transfer.

**Source Address Increment (X loop) (SCR_X_INCR)**: This field configures the index by which the source address is to be incremented for every iteration in an X loop. The field is expressed in multiples of SRC_TRANSFER_SIZE. This field is a signed number and hence may be decrementing or incrementing. If the source address does not need to be incremented, you can set this parameter to zero.

**Destination Address Increment (X loop) (DST_X_INCR)**: This field configures the index by which the destination address is to be incremented, for every iteration in an X loop. The field is expressed in multiples of DST_TRANSFER_SIZE. This field is a signed number and hence may be decrementing or incrementing. If the destination address does not need to be incremented, you can set this parameter to zero.

**Y Count**: This field determines the number of 1-D transfers present in the Y loop (outer loop). This field is valid when the DESCR_TYPE is set to 2-D transfer.

**Source Address Increment (Y loop) (SCR_Y_INCR)**: This field configures the index by which the source address is to be incremented, for every iteration in a Y loop. The field is expressed in multiples of SRC_TRANSFER_SIZE. This field is a signed number and hence may be decrementing or incrementing. If the source address does not need to be incremented, you can set this parameter to zero.

**Destination Address Increment (Y loop) (DST_Y_INCR)**: This field configures the index by which the destination address is to be incremented, for every iteration in a Y loop. The field is expressed in multiples of DST_TRANSFER_SIZE. This field is a signed number and hence may be decrementing or incrementing. If the destination address does not need to be incremented, you can set this parameter to zero.

**Channel Disable (CH_DISABLE)**: This field specifies whether the channel is disabled or not after completion of the current descriptor (independent of the value of the
9.4.2 Transfer Size

The word width for a transfer can be configured using the transfer/data size parameter in the descriptor. The settings are diversified into source transfer size, destination transfer size, and data size. The data size parameter (DATA_SIZE) sets the width of the bus for the transfer. The source and destination transfer sizes set by SCR_TRANSFER_SIZE and DST_TRANSFER_SIZE can have a value either the DATA_SIZE or 32 bit. DATA_SIZE can have a 32-bit, 16-bit, or 8-bit setting.

The source and destination transfer size for the DMA must match the addressable width of the source and destination, regardless of the width of data that must be moved. The DATA_SIZE parameter will correspond to the width of the actual data. For example, if a 16-bit PWM is used as a destination for DMA data, the DST_TRANSFER_SIZE must be set to 32 bit to match the width of the PWM register, because the peripheral register width for the TCPWM block (and most PSoC 6 MCU peripherals) is always 32-bit wide. However, in this example the DATA_SIZE for the destination may still be set to 16 bit because the 16-bit PWM only uses two bytes of data. SRAM and Flash are 8-bit, 16-bit, or 32-bit addressable and can use any source and destination transfer sizes to match the needs of the application.

Table 9-3 summarizes the possible combinations of the transfer size settings and its description.

Table 9-3. Transfer Size Settings

<table>
<thead>
<tr>
<th>DATA_SIZE</th>
<th>SCR_TRANSFER_SIZE</th>
<th>DST_TRANSFER_SIZE</th>
<th>Typical Usage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-bit</td>
<td>8-bit</td>
<td>8-bit</td>
<td>Memory to Memory</td>
<td>No data manipulation</td>
</tr>
<tr>
<td>8-bit</td>
<td>32-bit</td>
<td>8-bit</td>
<td>Peripheral to Memory</td>
<td>Higher 24 bits from the source dropped</td>
</tr>
<tr>
<td>8-bit</td>
<td>8-bit</td>
<td>32-bit</td>
<td>Memory to Peripheral</td>
<td>Higher 24 bits zero padded at destination</td>
</tr>
<tr>
<td>8-bit</td>
<td>32-bit</td>
<td>32-bit</td>
<td>Peripheral to Peripheral</td>
<td>Higher 24 bits from the source dropped and higher 24 bits zero padded at destination</td>
</tr>
<tr>
<td>16-bit</td>
<td>16-bit</td>
<td>16-bit</td>
<td>Memory to Memory</td>
<td>No data manipulation</td>
</tr>
<tr>
<td>16-bit</td>
<td>32-bit</td>
<td>16-bit</td>
<td>Peripheral to Memory</td>
<td>Higher 16 bits from the source dropped</td>
</tr>
<tr>
<td>16-bit</td>
<td>16-bit</td>
<td>32-bit</td>
<td>Memory to Peripheral</td>
<td>Higher 16 bits zero padded at destination</td>
</tr>
<tr>
<td>16-bit</td>
<td>32-bit</td>
<td>32-bit</td>
<td>Peripheral to Peripheral</td>
<td>Higher 16 bits from the source dropped and higher 16-bit zero padded at destination</td>
</tr>
<tr>
<td>32-bit</td>
<td>32-bit</td>
<td>32-bit</td>
<td>Peripheral to Peripheral</td>
<td>No data manipulation</td>
</tr>
</tbody>
</table>

9.4.3 Descriptor Chaining

Descriptors can be chained together. The DESCR_NEXT_PTR field contains a pointer to the next descriptor in the chain. A channel executes the next descriptor in the chain when it completes executing the current descriptor. The last descriptor in the chain has DESCR_NEXT_PTR set to ‘0’ (NULL pointer). A descriptor chain is also referred to as a descriptor list. It is possible to have a circular list; in a circular list, the execution continues indefinitely until there is an error or the channel or the controller is disabled by user code.
9.5 DMA Controller

9.5.1 Trigger Selection
Trigger signals can be generated from different sections of the chips. A trigger multiplexer block helps route these trigger signals to the destination. The DMA is one such destination of triggers. The trigger multiplexer block is outside the DMA block and is discussed in the Trigger Multiplexer Block chapter on page 197.

9.5.2 Pending Triggers
Pending triggers keep track of activated triggers by locally storing them in pending bits. This is essential because multiple channel triggers may be activated simultaneously, whereas only one channel can be served by the data transfer engine at a time. This component enables the use of both level-sensitive (high/‘1’) and pulse-sensitive (two high/‘1’ clk_slow cycles) triggers.

- Level-sensitive triggers are associated with a certain state, for example, a FIFO being full. These triggers remain active as long as the state is maintained. It is not required to track pending level-sensitive triggers in the DMA controller because the triggers are maintained outside the controller.
- Pulse-sensitive triggers are associated with a certain event, for example, an ADC sample has becomes available. It is essential to track these triggers in the DMA controller because the trigger pulse may disappear before it is served by the data transfer engine. Pulse triggers should be high/‘1’ for two clk_slow cycles.

The priority decoder determines the highest priority pending channel.

The data transfer engine is responsible for the data transfer from a source location to a destination location. When idle, the data transfer engine is ready to accept the highest priority activated channel. It is also responsible for reading the channel descriptor from memory.

Master I/F is an AHB-Lite bus master that allows the DMA controller to initiate AHB-Lite data transfers to the source and destination locations as well as to read the descriptor from memory.

Slave I/F is an AHB-Lite bus slave that allows the main CPU to access DMA controller control/status registers.

9.5.3 Output Triggers
Each channel has an output trigger. This trigger is high for two slow clock cycles. The trigger is generated on the completion of a data transfer. At the system level, these output triggers can be connected to the trigger multiplexer component. This connection allows a DMA controller output trigger to be connected to a DMA controller input trigger. In other words, the completion of a transfer in one channel can activate another channel or even reactivate the same channel.

Note that the DMA output triggers also connect to digital system interconnects (DSI) and some DSI signals connect to the trigger multiplexer inputs. Trigger outputs routing to other DMA channels or other peripheral trigger inputs is achieved using the trigger multiplexer. Refer to the Trigger Multiplexer Block chapter on page 197.

9.5.4 Interrupts
Every DMA channel has an interrupt line associated with it. INTR_TYPE parameter in the descriptor determines what event will trigger the interrupt for the channel. In addition each DMA channel has INTR, INTR_SET, INTR_MASK, and INTR_MASKED registers to control their respective interrupt lines. INTR_MASK can be used to mask the interrupt from
the DMA channel. The INTR and INTR_SET can be used to clear and set the interrupt, respectively, for debug purposes.

### 9.5.5 DMA Performance

The DMA block works on the clk_slow domain and hence all clocks described in this section are in clk_slow units.

Every time a DMA channel is triggered the DMA hardware goes through the following steps:

- Trigger synchronization
- Detection, priority decoding, and making channel pending
- Start state machine and load channel configuration
- Load DMA descriptor
- Load next DMA descriptor pointer
- Moving first element of data from source to destination.

Each of these steps involve multiple cycles for completion. Table 9-4 shows the number of cycles needed for each step.

#### Table 9-4. DMA Steps and Performance

<table>
<thead>
<tr>
<th>Operation</th>
<th>Cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>Trigger Synchronization</td>
<td>2</td>
</tr>
<tr>
<td>Detection, priority decoding and making channel pending</td>
<td>1</td>
</tr>
<tr>
<td>Start state machine and load channel config</td>
<td>3</td>
</tr>
<tr>
<td>Load descriptors</td>
<td>4 for single transfer</td>
</tr>
<tr>
<td></td>
<td>5 for 1-D transfer</td>
</tr>
<tr>
<td></td>
<td>6 for 2-D transfer</td>
</tr>
<tr>
<td>Load next pointer</td>
<td>1</td>
</tr>
<tr>
<td>Moving data from source to destination</td>
<td>3</td>
</tr>
<tr>
<td>Total</td>
<td>14 for single transfer</td>
</tr>
</tbody>
</table>

For subsequent transfers on a preloaded descriptor, cycles are needed only to move the data from source to destination. Therefore, transfers such as 1-D and 2-D, which are not preempted, incur all the cycles only for the first transfer; subsequent transfers will cost three cycles.

Based on the configuration of TRIG_IN_TYPE, the trigger synchronization cycles may be incurred for each single element transfer or for each 1-D transfer.

The descriptor is four words long for a single transfer type, five words for 1-D transfer, and six words for a 2-D transfer. Hence, the number of cycles needed to fetch a descriptor will vary based on its type.

Another factor to note is the latency in data or descriptor fetch due to wait states or bus latency.

The DMA performance for different types of transfers can be summarized as follows.

- **Single transfer**
  - 14 cycles per transfer + latency due to wait states or bus latency

- **1D transfer**
  - To transfer n data elements
    - Number of cycles = \(12 + n \times 3 + m\)
    
    m is the total number of wait states seen by DMA while loading or storing descriptors or data. An additional cycle is required for the first transfer, to load the X-Loop configuration register.

- **2D transfer**
  - If the 2 D transfer is transferring n elements then
    - Number of cycles = \(13 + n \times 3 + m\)
    
    m is total number of wait states seen by DMA while loading or storing descriptors or data. Two additional cycles are required for the first transfer, to load the X-loop and Y-Loop configuration register.

If a DMA channel is pre-empted, then it incurs the extra cycles to reinitialize the channel when resuming.

**Note:** Descriptors in memory and memory wait states will also affect the descriptor load delay.
10. Cryptographic Function Block (Crypto)

The Cryptographic block (Crypto) provides hardware implementation and acceleration of cryptographic functions. Implementation in hardware takes less time and energy than the equivalent firmware implementation. In addition, the block provides True Random Number generation functionality in silicon, which is not available in firmware.

10.1 Features
- Symmetric key encryption and decryption
- Hashing
- Message authentication
- Random number generation (pseudo and true)
- Cyclic redundancy checking
- Utility functions such as enable/disable, interrupt settings, and flags

10.2 Architecture

The Crypto block is implemented as a secure block and access to it is through inter-processor calls (IPC); direct access at a register level is not permitted for security reasons. A client-server model is used to access Crypto functions. User tasks (clients) run on either the M4 or M0+; the function calls will effectively call a proxy server, which will call the security server (providing Crypto functions) running on the M0+.

The IPC (see the Inter-Processor Communication chapter on page 36) mechanism will be used to implement a remote procedure call (RPC) model that will be used to make calls to the security server code. Conceptually, the scheme is as follows.

Figure 10-1. Crypto Block Architecture
This model provides security for Crypto tasks that may otherwise expose or compromise key material. An API, as documented in the Crypto Component datasheet, will provide access to Crypto functions for general user code.

10.3 Definitions of Terms

The following terms are used in the description of this block:

- **Plaintext:** An unencrypted message
- **Ciphertext:** An encrypted message
- **Block cipher:** An encryption function for fixed-size blocks of data. This function takes a fixed-size key and a block of plaintext data from the message and encrypts it to generate ciphertext. Block ciphers are reversible, the function performed on a block of encrypted data will decrypt it.
- **Block cipher mode:** A mode of encrypting a message using block ciphers for messages of arbitrary length. The message is padded so that its length is an integer multiple of the block size. Electronic Code Book (ECB), Cipher Block Chaining (CBC), and Cipher Feedback (CFB) are all modes of using block ciphers to create an encrypted message of arbitrary length.
- **Data Encryption Standard (DES):** A block cipher that is now obsolete but supported for legacy reasons. It uses a 56-bit key and a 64-bit message block size.
- **3DES (or TDES):** Triple DES uses the DES operation and three DES encryptions in sequence-encrypt with DES with one 56-bit key, decrypt with a second 56-bit key, and then encrypt again either with the first key or a third 56-bit key. The block size is 64-bits.
- **Advanced Encryption Standard (AES):** This block cipher was designed to replace DES and 3DES. It is the block cipher standard used currently. It uses keys that can be 128, 192, or 256 bits in length and the message block size is 128 bits. This is the U.S. government standard. AES is also used for message authentication.
- **Secure Hash Algorithm (SHA):** This function takes a message of arbitrary length and reduces it to a fixed-length residue or message digest after performing a series of mathematically-defined operations, which guarantees that any change in the message will change the hash value. It is used for message authentication by transmitting a message with a hash value appended to it and recalculating the message hash value using the same algorithm at the recipient’s end. If the hashes differ then the message is corrupted.
- **Message Authentication Code (MAC):** MACs are used to verify that a received message has not been altered. This is done by first computing a MAC value at the sender’s end and appending it to the transmitted message. When the message is received, the MAC is computed again and checked against the MAC value transmitted with the message. If they do not match, the message has been altered. Either a hash algorithm (such as SHA) or a block cipher (such as AES) can be used to produce the MAC value. Keyed MAC schemes use a secret key along with the message, thus the key value must be known to be able to compute the MAC value.
- **Hash Message Authentication Code (HMAC):** This method uses a key along with the message to compute the MAC value using a hash algorithm.
- **Cipher-based Message Authentication Code (CMAC):** This method uses a key along with the message to compute the MAC value using the AES block cipher algorithm.
- **Pseudo Random Number Generator (PRNG):** This is based on Linear Feedback Shift Registers, which generate a sequence starting from a non-zero seed.
- **True Random Number Generator (TRNG):** A block that generates a number that is statistically random and based on some physical random variation, cannot be duplicated by running the process again.
- **Symmetric key cryptography:** Refers to using a common known key to encrypt and decrypt messages (a shared secret between sender and receiver). An efficient method used for encrypting and decrypting messages when the authenticity of the other party has been established. DES (now obsolete), 3DES, and AES (currently used) are well-known symmetric cryptography methods.
- **Asymmetric key cryptography:** Also referred to as Public and Private key methods. If you want to receive a message, you must publish a public key (can be up to 4096 bits). Anyone wishing to send a message to the publisher of the public key encrypts the message with the public key; this message can now only be decrypted with the private key (the other prime factor held secret by the recipient). The message is now sent over any channel to the recipient who can decrypt it with the private, secret key. The same process is used to send messages to the sender of the original message. Asymmetric cryptography relies on the mathematical impracticality (usually related to the processing power available at any given time) of factoring the keys. Common, computationally intensive, asymmetric algorithms are RSA and ECC.
10.4 Crypto Block Functions

The following is a list of currently supported (at an API level) functions.

10.4.1 Symmetric Key Functions

Data Encryption Standard (DES): DES is a block cipher, an encryption function that works on fixed-size blocks of data. The DES block size is 64 bits and it uses a 56-bit key. DES is now considered obsolete, but is retained for compatibility with legacy systems. With block ciphers, encryption is considered a forward cipher; block ciphers have a complementary operation called decryption (inverse cipher), which has the same parameters as encryption and uses either the same key or a transform of that key.

DES is described in FIPS 46-3, which is archived at http://csrc.nist.gov/publications/fips/fips46-3/fips46-3.pdf. Note that DES is not recommended for use anymore and support is provided only for legacy and compatibility reasons.

Triple DES: TDES (also known as Triple-DES or 3DES) is the DES algorithm invoked thrice with three different keys; the first pass encrypts with one key, the second pass decrypts with the second, and the third pass encrypts with the third key.


Advanced Encryption Standard (AES): The AES operation works on a 128-bit block size and uses keys of 128, 192, or 256 bits in length. The block cipher modes supported are ECB, CBC, CFB, and CTR.

The ECB mode is invoked by calling a function, which takes the following parameters: a pointer to the key, the function mode (forward/encryption or inverse/decryption), a pointer to the source block, and a pointer to the result block.

The CBC function is more secure than EBC; it relies on an “Exclusive-Or” of each plaintext block with the previous ciphertext block. Thus, block-sized plaintext patterns cannot be used to derive information about cipher characteristics as with EBC. The CBC function is invoked with the same parameters as EBC, with the addition of a pointer to an initial value.


10.4.2 Hash Functions

Secure Hash Algorithm (SHA): The SHA produces a message digest from a message of arbitrary size. It takes as arguments pointers to the message, the size of the message, a pointer to the initial digest value, and the mode. The mode specifies which SHA algorithm to use. Note that SHA does not use a key but starts with a pre-defined hash value. It supports the following message sizes and produces the stated message digest size.

<table>
<thead>
<tr>
<th>Algorithm</th>
<th>Message Size (bits)</th>
<th>Block Size (bits)</th>
<th>Word Size (bits)</th>
<th>Message Digest Size (bits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SHA-1</td>
<td>&lt; 2^64</td>
<td>512</td>
<td>32</td>
<td>160</td>
</tr>
<tr>
<td>SHA-224</td>
<td>&lt; 2^64</td>
<td>512</td>
<td>32</td>
<td>224</td>
</tr>
<tr>
<td>SHA-256</td>
<td>&lt; 2^64</td>
<td>512</td>
<td>32</td>
<td>256</td>
</tr>
<tr>
<td>SHA-384</td>
<td>&lt; 2^128</td>
<td>1024</td>
<td>64</td>
<td>384</td>
</tr>
<tr>
<td>SHA-512</td>
<td>&lt; 2^128</td>
<td>1024</td>
<td>64</td>
<td>512</td>
</tr>
<tr>
<td>SHA-512/224</td>
<td>&lt; 2^128</td>
<td>1024</td>
<td>64</td>
<td>224</td>
</tr>
<tr>
<td>SHA-512/256</td>
<td>&lt; 2^128</td>
<td>1024</td>
<td>64</td>
<td>256</td>
</tr>
</tbody>
</table>

10.4.3 Message Authentication Code (MAC) Functions

Hashed Message Authentication Code (HMAC)
This function produces a message digest from a message of arbitrary size, but also uses a private key so that the hash cannot be calculated without the knowledge of the private key. HMAC is implemented using SHA described earlier; in addition to the parameters described in Table 10-1, it takes two additional parameters: a pointer to the key and the length of the key.


Cipher-based Message Authentication Code (CMAC)
This is a block-based message authentication algorithm that uses the AES block cipher to produce a message digest (analogous to HMAC, which uses a hash function). This function uses a key to encrypt the first block of the message after which the encrypted block produced is XOR-ed with the second message block and encrypted. The result of that operation is XOR-ed with the third message block and so on. The last message block is mixed with sub-keys derived from the encryption key, XOR-ed with the preceding encryption value, and encrypted to produce the authentication output.

The function implementing CMAC using AES is called with a pointer to the key, the key length, and pointers to the message block, a constant used for sub-key generation, and a pointer to temporary storage.


10.4.4 Cyclic Redundancy Code (CRC)
The CRC block generates a CRC remainder with a programmable polynomial of up to 32 bits. The CRC function considers the following as arguments: the polynomial, the initial state of the LFSR, data byte reversal and XOR-ing with a pattern in a register, remainder reversal and XOR-ing with a pattern in a register, the data size, and a pointer to the data block. It returns the CRC remainder value.

10.4.5 Random Number Generator (RNG)
Pseudo Random Number Generator (PRNG): The PRNG generates pseudo random numbers based on three Linear Feedback Shift Registers (LFSRs). The three registers are initialized to non-zero seed values. The function takes as argument the length of the argument to be returned and returns a pseudo-random number.

True Random Number Generator (TRNG): The TRNG generates true random numbers with programmable bit size. It uses up to size polynomial generators with fixed and programmable polynomials. The function takes as argument the length of the argument to be returned and returns a true random number.

10.5 Module Configuration and Initialization
The Crypto module can be enabled or disabled using the Enable and Disable functions that take no arguments. The operational mode of the block is through a command (and parameters as required) FIFO, which is written with a command and parameters as required. Execution of the command invokes the appropriate operation such as DES, TDES, and SHA.

The interrupt model is based on four registers that contain interrupt flags resulting from various causes, bits for masking interrupts, software writable interrupt flags, and interrupt state bits (logical AND of mask and interrupt flag bits).

An initialization function is provided for setting interrupt flags, which must be responded to, to set interrupt flags in software, masking interrupts, and reading interrupt state.

Details of APIs provided are in the Crypto Component datasheet.
11. Program and Debug Interface

The PSoC 6 MCU Program and Debug interface provides a communication gateway for an external device to perform programming or debugging. The external device can be a Cypress-supplied programmer and debugger, or a third-party device that supports programming and debugging. The serial wire debug (SWD) or the JTAG interface can be used as the communication protocol between the external device and PSoC 6 MCUs.

11.1 Features

- Supports programming and debugging through the JTAG or SWD interface.
- CM4 supports 4-bit ETM tracing, serial wire viewer (SWV), and printf() style debugging through the single-wire output (SWO) pin. CM0+ supports Micro Trace Buffer (MTB) with 4 KB dedicated RAM.
- Supports Cross Triggering Interface (CTI) and Cross Triggering Matrix (CTM).
- CM0+ supports four hardware breakpoints and two watchpoints. CM4 supports six hardware breakpoints and four watchpoints.
- Provides read and write access to all memory and registers in the system while debugging, including the Cortex-M4 and Cortex-M0+ register banks when the core is running or halted.

11.2 Architecture

Figure 11-1 shows the block diagram of the program and debug interface in the PSoC 6 MCU. The debug and access port (DAP) acts as the program and debug interface. The external programmer or debugger, also known as the “host”, communicates with the DAP of the PSoC 6 MCU “target” using either the SWD or JTAG interface. The debug physical port pins communicate with the DAP through the high-speed I/O matrix (HSIOM). See the I/O System chapter on page 164 for details on HSIOM.

The debug infrastructure is organized in the following four groups:

- DAP (provides pin interfaces through which the debug host can connect to the chip)
- Cortex-M0+ core debug components
- Cortex-M4 core debug components
- Other debug infrastructure (includes the CM4 tracing, the CTM, and the System ROM table)
The DAP communicates with the Cortex-M0+ CPU using the Arm-specified advanced high-performance bus (AHB) interface. AHB is the systems interconnect protocol used inside the device, which facilitates memory and peripheral register access by the AHB master. The PSoC 6 MCU has six AHB masters – Arm CM4 CPU core, Arm CM0 CPU core, Datawire0, Datawire1, Crypto, and DAP. The external host can effectively take control of the entire device through the DAP to perform programming and debugging operations.

The following are the various debug and trace components:

- **Debug components**
  - JTAG and SWD for debug control and access

- **Trace source components**
  - Micro trace buffer (MTB-M0+) for tracing Cortex-M0+ program execution
  - Embedded trace macrocell (ETM-M4) for tracing Cortex-M4 program execution

- **Trace sink components**
  - Trace port interface unit (TPIU) to drive the trace information out of the chip to an external trace port analyzer

- **Cross-triggering components**
  - Cross-trigger interface (CTI)
  - Cross-trigger matrix (CTM)

- **ROM tables**
11.2.1 Debug Access Port (DAP)

The DAP consists of a combined SWD/JTAG interface (SWJ) that also includes the SWD listener. The SWD listener decides whether the JTAG interface (default) or SWD interface is active. Note that JTAG and SWD are mutually exclusive because they share pins.

The debug port (DP) connects to the DAP bus, which in turn connects to one of three Access Ports (AP), namely:

- The CM0-AP, which connects directly to the AHB debug slave port (SLV) of the CM0+ and gives access to the CM0+ internal debug components. This also allows access to the rest of the system through the CM0+ AHB master interface. This provides the debug host the same view as an application running on the CM0+. This includes access to the MMIO of other debug components of the Cortex M0+ subsystem. These debug components can also be accessed by the CM0+ CPU, but cannot be reached through the other APs or by the CM4 core.

- The CM4-AP located inside the CM4 gives access to the CM4 internal debug components. The CM4-AP also allows access to the rest of the system through the CM4 AHB master interfaces. This provides the debug host the same view as an application running on the CM4 core. Additionally, the CM4-AP provides access to the debug components in the CM4 core through the External Peripheral Bus (EPB). These debug components can also be accessed by the CM4 CPU, but cannot be reached through the other APs or by the CM0+ core.

- The System-AP, which through an AHB mux gives access to the rest of the system. This allows access to the System ROM table, which cannot be reached by any other way. The System ROM table provides the chip ID but is otherwise empty.

11.2.1.1 DAP Security

For security reasons all three APs each can be independently disabled. Each AP disable is controlled by two MMIO bits. One bit, CPUSS_DP_CTL.xxx_DISABLE (where xxx can be CM0 or CM4 or SYS), can be set during boot, before the debugger can connect, based on eFuse settings. After this bit is set it cannot be cleared.

The second bit, CPUSS_DP_CTL.xxx_ENABLE, is a regular read/write bit. This bit also resets to zero and is set to ‘1’ by either the ROM boot code or the flash boot code depending on the life-cycle stage. This feature can be used to block debug access during normal operation, but re-enable some debug access after a successful authentication.

In addition to the above, the System AP is also protected by an MPU. This can be used to give the debugger limited access to the rest of the system. Allow access to the System ROM table for chip identification. If debug access is restored after successful authentication, this MPU must be configured to allow authentication requests.

Note: The debug slave interfaces of both the CPUs bypass the internal CPU MPU.

11.2.1.2 DAP Power Domain

Almost all the debug components are part of the Active power domain. The only exception is the SWD/JTAG-DP, which is part of the Deep Sleep power domain. This allows the debug host to connect during Deep Sleep, while the application is ‘running’ or powered down. This enables in-field debugging for low-power applications in which the chip is mostly in Deep Sleep.

After the debugger is connected to the chip, it must bring the chip to the Active state before any operation. For this, the SWD/JTAG-DP has a register (DP_CTL_STAT) with two power request bits. The two bits are CDBGWRUPREQ and CSYSWPRUPREQ, which request for debug power and system power, respectively. These bits must remain set for the duration of the debug session.

Note that only the two SWD pins (SWCLKTCK and SWDIOTMS) are operational during the Deep Sleep mode – the JTAG pins are operational only in Active mode. The JTAG debug and JTAG boundary scan are not available when the system is in Deep Sleep mode. JTAG functionality is available only after a chip power-on-reset.

11.2.2 ROM Tables

The ROM tables are organized in a tree hierarchy. Each AP has a register that contains a 32-bit address pointer to the base of the root ROM table for that AP. For PSoC 6 MCUs, there are three such root ROM tables.

Each ROM table contains 32-bit entries with an address pointer that either points to the base of the next level ROM table. Each ROM table also contains a set of ID registers that hold JEDEC compliant identifiers to identify the manufacturer, part number, and major and minor revision numbers. For all ROM tables in PSoC 6 MCUs, these IDs are the same. Each ROM table and CoreSight compliant component also contains component identification registers.

11.2.3 Trace

The micro trace buffer (MTB-M0+) component captures the program execution flow from Cortex-M0+ CPU and stores it in a local SRAM memory. This information can be read by an external debug tool through JTAG/SWD interface to construct the program execution flow.

The embedded trace macrocell (ITM), which is inside Cortex-M4, also generates trace output on its ATB interface. These two ATB interfaces
Program and Debug Interface

11.2.4 Embedded Cross Triggering

The Arm CoreSight includes Embedded Cross Triggering (ECT) to communicate events between debug components. These events are particularly useful with tracing and multicore platforms. For example trigger events can be used to:

- Start or stop both CPUs at (almost) the same time
- Start or stop instruction tracing based on trace buffer being full or not or based on other events

CoreSight uses two components to support ECT, namely a CTI and a CTM, both of which are used in PSoC 6 MCUs.

The CTI component interfaces with other debug components, sending triggers back and forth and synchronizing them as needed. The CTM connects several CTIs, thus allowing events to be communicated from one CTI to another.

The PSoC 6 MCU has three CTIs, one for each CPU and one for the trace components in the debug structure. These three CTIs are connected together through the CTM. The CM4 CTI is located in the fast clock domain and the other two CTIs and the CTM are all located in the same slow-frequency clock domain. For more details, refer to the Arm documentation.

11.3 Serial Wire Debug (SWD) Interface

The PSoC 6 MCU supports programming and debugging through the SWD interface. The SWD protocol is a packet-based serial transaction protocol. At the pin level, it uses a single bidirectional data signal (SWDIO) and a unidirectional clock signal (SWDCK). The host programmer always drives the clock line, whereas either the host or the target drives the data line. A complete data transfer (one SWD packet) requires 46 clocks and consists of three phases:

- **Host Packet Request Phase** – The host issues a request to the PSoC 6 MCU target.
- **Target Acknowledge Response Phase** – The PSoC 6 MCU target sends an acknowledgement to the host.
- **Data Transfer Phase** – The host or target writes data to the bus, depending on the direction of the transfer.

When control of the SWDIO line passes from the host to the target, or vice versa, there is a turnaround period (Tm) where neither device drives the line and it floats in a high-impedance (Hi-Z) state. This period is either one-half or one and a half clock cycles, depending on the transition.

Figure 11-2. SWD Write and Read Packet Timing Diagrams

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The sequence to transmit SWD read and write packets are as follows:

1. **Host Packet Request Phase**: SWDIO driven by the host
   - a. The start bit initiates a transfer; it is always logic 1.
   - b. The AP not DP (APnDP) bit determines whether the transfer is an AP access – 1b or a DP access – 0b.
   - c. The Read not Write bit (RnW) controls which direction the data transfer is in. 1b represents a ‘read from’ the target, or 0b for a ‘write to’ the target.
   - d. The Address bits (A[3:2]) are register select bits for AP or DP, depending on the APnDP bit value. **Note**: Address bits are transmitted with the LSb first.
   - e. The parity bit contains the parity of APnDP, RnW, and ADDR bits. It is an even parity bit; this means, when XORed with the other bits, the result will be 0. If the parity bit is not correct, the header is ignored by the PSoC 6 MCU; there is no ACK response (ACK = 111b). The programming operation should be aborted and retried again by following a device reset.
   - f. The stop bit is always logic 0.
   - g. The park bit is always logic 1.

2. **Target Acknowledge Response Phase**: SWDIO driven by the target
   - a. The ACK[2:0] bits represent the target to host response, indicating failure or success, among other results. See Table 11-1 for definitions. **Note**: ACK bits are transmitted with the LSb first.

3. **Data Transfer Phase**: SWDIO driven by either target or host depending on direction
   - a. The data for read or write is written to the bus, LSb first.
   - b. The data parity bit indicates the parity of the data read or written. It is an even parity; this means when XORed with the data bits, the result will be 0. If the parity bit indicates a data error, corrective action should be taken. For a read packet, if the host detects a parity error, it must abort the programming operation and restart. For a write packet, if the target detects a parity error, it generates a FAULT ACK response in the next packet.

According to the SWD protocol, the host can generate any number of SWDCK clock cycles between two packets with SWDIO low. Three or more dummy clock cycles should be generated between two SWD packets if the clock is not free-running or to make the clock free-running in IDLE mode.

The SWD interface can be reset by clocking the SWDCK line for 50 or more cycles with SWDIO high. To return to the idle state, clock the SWDIO low once.

### 11.3.1 SWD Timing Details

The SWDIO line is written to and read at different times depending on the direction of communication. The host drives the SWDIO line during the Host Packet Request phase and, if the host is writing data to the target, during the Data Transfer phase as well. When the host is driving the SWDIO line, each new bit is written by the host on falling SWDCK edges, and read by the target on rising SWDCK edges. The target drives the SWDIO line during the Target Acknowledge Response phase and, if the target is reading out data, during the Data Transfer phase as well. When the target is driving the SWDIO line, each new bit is written by the target on rising SWDCK edges, and read by the host on falling SWDCK edges.

Table 11-1 and Figure 11-2 illustrate the timing of SWDIO bit writes and reads.

#### Table 11-1. SWDIO Bit Write and Read Timing

<table>
<thead>
<tr>
<th>SWD Packet Phase</th>
<th>SWDIO Edge</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Falling</td>
</tr>
<tr>
<td>Host Packet Request</td>
<td>Host Write</td>
</tr>
<tr>
<td>Host Data Transfer</td>
<td>Host Read</td>
</tr>
<tr>
<td>Target Ack Response</td>
<td>Host Read</td>
</tr>
<tr>
<td>Target Data Transfer</td>
<td>Host Read</td>
</tr>
</tbody>
</table>

#### 11.3.2 ACK Details

The acknowledge (ACK) bitfield is used to communicate the status of the previous transfer. OK ACK means that previous packet was successful. A WAIT response requires a data phase. For a FAULT status, the programming operation should be aborted immediately. Table 11-2 shows the ACK bit-field decoding details.

#### Table 11-2. SWD Transfer ACK Response Decoding

<table>
<thead>
<tr>
<th>Response</th>
<th>ACK[2:0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>OK</td>
<td>001b</td>
</tr>
<tr>
<td>WAIT</td>
<td>010b</td>
</tr>
<tr>
<td>FAULT</td>
<td>100b</td>
</tr>
<tr>
<td>NO ACK</td>
<td>111b</td>
</tr>
</tbody>
</table>

Details on WAIT and FAULT response behaviors are as follows:

- For a WAIT response, if the transaction is a read, the host should ignore the data read in the data phase. The target does not drive the line and the host must not check the parity bit as well.
- For a WAIT response, if the transaction is a write, the data phase is ignored by the PSoC 6 MCU. But, the host must still send the data to be written to complete the packet. The parity bit corresponding to the data should also be sent by the host.
- A WAIT response means that the PSoC 6 MCU is processing the previous transaction. The host can try for a maximum of four continuous WAIT responses to see whether an OK response is received. If it fails, then the
For a FAULT response, the programming operation should be aborted and retried again.

11.3.3 Turnaround (Trn) Period Details

There is a turnaround period between the packet request and the ACK phases, as well as between the ACK and the data phases for host write transfers, as shown in Figure 11-2. According to the SWD protocol, the Trn period is used by both the host and target to change the drive modes on their respective SWDIO lines. During the first Trn period after the packet request, the target starts driving the ACK data on the SWDIO line on the rising edge of SWDCK. This action ensures that the host can read the ACK data on the next falling edge. Thus, the first Trn period lasts only one-half cycle. The second Trn period of the SWD packet is one and a half cycles. Neither the host nor the PSoC 6 MCU should drive the SWDIO line during the Trn period.

11.4 JTAG Interface

In response to higher pin densities on ICs, the Joint Test Action Group (JTAG) proposed a method to test circuit boards by controlling the pins on the ICs (and reading their values) via a separate test interface. The solution, later formalized as IEEE Standard 1149.1-2001, is based on the concept of a serial shift register routed across all of the pins of the IC – hence the name “boundary scan.” The circuitry at each pin is supplemented with a multipurpose element called a boundary scan cell. In PSoC 6 MCUs, most GPIO port pins have a boundary scan cell associated with them (see the GPIO block diagrams in the I/O System chapter on page 164). The interface used to control the values in the boundary scan cells is called the Test Access Port (TAP) and is commonly known as the JTAG interface. It consists of three signals: Test Data In (TDI), Test Data Out (TDO), and Test Mode Select (TMS). Also included is a clock signal (TCK) that clocks the other signals. TDI, TMS, and TCK are all inputs to the device and TDO is the output from the device. This interface enables testing multiple ICs on a circuit board, in a daisy-chain fashion, as shown in Figure 11-3.

Figure 11-3. JTAG Interface to Multiple ICs on a Circuit Board

The JTAG interface architecture within each device is shown in Figure 11-4. Data at TDI is shifted in, through one of several available registers, and out to TDO.
The TMS signal controls a state machine in the TAP. The state machine controls which register (including the boundary scan path) is in the TDI-to-TDO shift path, as shown in Figure 11-5. The following terms apply:

- **IR** - the instruction register
- **DR** - one of the other registers (including the boundary scan path), as determined by the contents of the instruction register
- **capture** - transfer the contents of a DR to a shift register, to be shifted out on TDO (read the DR)
- **update** - transfer the contents of a shift register, shifted in from TDI, to a DR (write the DR)
The registers in the TAP are:

- **Instruction** – Typically two to four bits wide, holds the current instruction that defines which data register is placed in the TDI-to-TDO shift path.
- **Bypass** – one bit wide, directly connects TDI with TDO, causing the device to be bypassed for JTAG purposes.
- **ID** – 32 bits wide, used to read the JTAG manufacturer/part number ID of the device.
- **Boundary Scan Path (BSR)** – Width equals the number of I/O pins that have boundary scan cells, used to set or read the states of those I/O pins.

Other registers may be included in accordance with the device manufacturer specifications. The standard set of instructions (values that can be shifted into the instruction register), as specified in IEEE 1149, are:

- **EXTEST** – Causes TDI and TDO to be connected to the BSR. The device is changed from its normal operating mode to a test mode. Then, the device’s pin states can be sampled using the capture dr JTAG state, and new values can be applied to the pins of the device using the update dr state.
- **SAMPLE** – Causes TDI and TDO to be connected to the BSR, but the device remains in its normal operating mode. During this instruction, the BSR can be read by the capture dr JTAG state to take a sample of the functional data entering and leaving the device.
- **PRELOAD** – Causes TDI and TDO to be connected to the BSR, but the device is left in its normal operating mode. The instruction is used to preload test data into the BSR before loading an EXTEST instruction.

Optional, but commonly available, instructions are:

- **IDCODE** – Causes TDI and TDO to be connected to an IDCODE register.
- **INTEST** – Causes TDI and TDO to be connected to the BSR. While the EXTEST instruction allows access to the device pins, INTEST enables similar access to the corelogic signals of a device.

For more information, see the IEEE Standard, available at [www.ieee.org](http://www.ieee.org).
11.5 Programming the PSoC 6 MCU

The PSoC 6 MCU is programmed using the following sequence. Refer to the PSoC 6 MCU Programming Specifications for complete details on the programming algorithm, timing specifications, and hardware configuration required for programming.

1. Acquire the SWD port in the PSoC 6 MCU.
2. Enter the programming mode.
3. Execute the device programming routines such as Silicon ID Check, Flash Programming, Flash Verification, and Checksum Verification.

11.5.1 SWD Port Acquisition

11.5.1.1 SWD Port Acquire Sequence

The first step in device programming is for the host to acquire the target's SWD port. The host first performs a device reset by asserting the external reset (XRES) pin. After removing the XRES signal, the host must send an SWD connect sequence for the device within the acquire window to connect to the SWD interface in the DAP.

The debug access port must be reset using the standard Arm command. The DAP reset command consists of more than 49 SWDCK clock cycles with SWDIO asserted high. The transaction must be completed by sending at least one SWDCK clock cycle with SWDIO asserted low. This sequence synchronizes the programmer and the chip. Read_DAP() refers to the read of the IDCODE register in the debug port. The sequence of line reset and IDCODE read should be repeated until an OK ACK is received for the IDCODE read or a timeout (2 ms) occurs. The SWD port is said to be in the acquired state if an OK ACK is received within the time window and the IDCODE read matches with that of the Cortex-M0+ DAP.

11.5.2 SWD Programming Mode Entry

After the SWD port is acquired, the host must enter the device programming mode within a specific time window. This is done by setting the TEST_MODE bit (bit 31) in the test mode control register (MODE register). The debug port should also be configured before entering the device programming mode. Timing specifications and pseudo code for entering the programming mode are detailed in the PSoC 6 MCU Programming Specifications document.

11.5.3 SWD Programming Routines Executions

When the device is in programming mode, the external programmer can start sending the SWD packet sequence for performing programming operations such as flash erase, flash program, checksum verification, and so on. The programming routines are explained in the Nonvolatile Memory Programming chapter on page 94. The exact sequence of calling the programming routines is given in the PSoC 6 MCU Programming Specifications document.

11.6 Registers

Table 11-3. List of Registers

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CM0P_DWT</td>
<td>Cortex M0+ Data Watchpoint and Trace (DWT) registers</td>
</tr>
<tr>
<td>CM0P_BP</td>
<td>Cortex M0+ BreakPoint (BP) registers</td>
</tr>
<tr>
<td>CM0P_ROM</td>
<td>Cortex M0+ CPU Coresight ROM table</td>
</tr>
<tr>
<td>CM0P_CTI</td>
<td>Cortex M0+ Cross-Trigger Interface (CTI) registers</td>
</tr>
<tr>
<td>CM0P_MTB</td>
<td>Cortex M0+ Micro Trace Buffer (MTB) registers</td>
</tr>
<tr>
<td>CM4_ITM</td>
<td>Cortex M4 Instrumentation Trace Macrocell (ITM) registers</td>
</tr>
<tr>
<td>CM4_DWT</td>
<td>Cortex M4 Data Watchpoint and Trace (DWT) registers</td>
</tr>
<tr>
<td>CM4_FPB</td>
<td>Cortex M4 Flash Patch and Breakpoint (FPB) registers</td>
</tr>
<tr>
<td>CM4_SCS</td>
<td>Cortex M4 System Control Space (SCS) registers</td>
</tr>
<tr>
<td>CM4_ETM</td>
<td>Cortex M4 Embedded Trace Macrocell (ETM) registers</td>
</tr>
<tr>
<td>CM4_CTI</td>
<td>Cortex M4 Cross-Trigger Interface (CTI) registers</td>
</tr>
<tr>
<td>CM4_ROM</td>
<td>Cortex M4 CPU Coresight ROM table</td>
</tr>
<tr>
<td>TRC_TPIU</td>
<td>System Trace Coresight Trace Port Interface Unit (TPIU) registers</td>
</tr>
</tbody>
</table>
12. Nonvolatile Memory Programming

Nonvolatile memory programming refers to the programming of flash memory in the PSoC 6 MCU. This chapter explains the different functions that are part of device programming, such as erase, write, program, and checksum calculation. Cypress-supplied programmers and other third-party programmers can use these functions to program the PSoC 6 MCU with the data in an application hex file. They can also be used to perform bootloader operations where the CPU will update a portion of the flash memory.

12.1 Features

- User flash with row sizes of 512 bytes
- Supports the Read While Write (RWW) feature with a RWW sector size of 512KB
- SROM API library for flash management through system calls such as Program Row, Erase Flash, and Blow eFuse
- System calls can be performed using CM0+, CM4, or DAP

12.2 Architecture

Flash programming operations are implemented as system calls. System calls are executed out of SROM in Protection Context 0. System calls are executed inside CM0+ NMI. The system call interface makes use of IPC to initiate an NMI to CM0+.

System calls can be performed by CM0+, CM4, or DAP. Each of them have a reserved IPC structure (used as a mailbox) through which they can request CM0+ to perform a system call. Each one acquires the specific mailbox, writes the opcode and argument to the data field of the mailbox, and notifies a dedicated IPC interrupt structure. This results in an NMI interrupt in CM0+. The following diagram illustrates the system call interface using IPC.

Figure 12-1. System Call Interface Using IPC
The PSoC 6 MCU’s IPC component carries only a single 32-bit argument. This argument is either a pointer to SRAM or a formatted opcode or argument value that cannot be a valid SRAM address. The encoding used for DAP and the CM4 or CM0+ is slightly different.

**DAP.** If (opcode + argument) is less than or equal to 31 bits, store them in the data field and set the LSB of the data field as ‘1’. Upon completion of the call, a return value is passed in the IPC data register. For calls that need more argument data, the data field is a pointer to a structure in SRAM (aligned on a word boundary) that has the opcode and the argument. So it is a pointer if and only if the LSB is 0.

**CM4 or CM0+.** A pointer is always used to structure SRAM. Commands that are issued as a single word by DAP can still be issued by CM0+ or CM4, but use an SRAM structure instead.

The NMI interrupt handler for system calls works as follows.

- If the ROM boot process code is not initialized in the protection state (PROTECTION is still at its default/reset value UNKOWN), the NMI calls have no effect and the handler returns.
- A jump table is used to point to the code in ROM or flash. This jump table is located in ROM or flash (as configured in SFLASH).

The IPC mechanism is used to return the result of the system call. Two factors must be considered.

- The result is to be passed in SRAM: CM0+ writes the result in SRAM and releases the IPC structure. The requester knows that the result is ready from the RELEASE interrupt.
- The result is scalar (≤ 32 bits) and there is no SRAM to pass the result: in this case, the CM0+ writes the result to the data field of the IPC structure and releases it. The requester can read the data when the IPC structure lock is released. The requester polls the IPC structure to know when it is released.

External programmers program the PSoC 6 MCU flash memory using the JTAG or SWD protocol by sending the commands to the DAP. The programming sequence for PSoC 6 MCUs with an external programmer is given in *PSoC 6 MCU Programming Specifications*. Flash memory can also be programmed by the CM4/CM0+ CPU by accessing the IPC interface. This type of programming is typically used to update a portion of the flash memory as part of a bootload operation, or other application requirement, such as updating a lookup table stored in the flash memory. All write operations to flash memory, whether from the DAP or from the CPU, are done through the CM0+.

### 12.3 System Call Implementation

#### 12.3.1 System Call via CM0+ or CM4

System calls can be made from the CM0+ or CM4 at any point during code execution. CM0+ or CM4 should acquire the IPC_STRUCT reserved for them and provide arguments in either of the methods described above and notify IPC interrupt 0 to trigger a system call.

#### 12.3.2 System Call via DAP

If the device is acquired, then the boot ROM enters “busy-wait loop” and waits for commands issued by the DAP. For a detailed description on acquiring the device see the *PSoC 6 MCU Programming Specifications*.

#### 12.3.3 Exiting from a System Call

When the API operation is complete, CM0+ will release the IPC structure that initiated the system call. If an interrupt is required upon release, then the corresponding mask bit should be set in IPC_INTR_STRUCT.INTR_MASK.RELEASE[i]. The exit code must also restore the CM0+ protection context (MPU.MS_PC_CTL.MS_PC) to the one that was backed up in MPU.MS_PC_CTL.MS_PC_SAVED.
12.4 SROM API Library

SROM has two categories of APIs:
- Flash management APIs – These APIs provide the ability to program, erase, and test the flash macro.
- System management APIs – These APIs provide the ability to perform system tasks such as checksum and blowing eFuse.

Table 12-1 shows a summary of the APIs.

<table>
<thead>
<tr>
<th>System Call</th>
<th>Opcode</th>
<th>Description</th>
<th>API Category</th>
<th>Uses SRAM</th>
<th>Access Allowed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon ID</td>
<td>0x00</td>
<td>Returns die ID, major/minor ID, and protection state</td>
<td>SYS</td>
<td>No</td>
<td>CM0+, CM4, DAP</td>
</tr>
<tr>
<td>Blow eFuse Bit</td>
<td>0x01</td>
<td>Blows the addressed eFuse bit</td>
<td>SYS</td>
<td>No</td>
<td>CM0+, CM4, DAP</td>
</tr>
<tr>
<td>Read eFuse Bit</td>
<td>0x03</td>
<td>Reads addressed eFuse byte</td>
<td>SYS</td>
<td>No</td>
<td>CM0+, CM4, DAP</td>
</tr>
<tr>
<td>Compute Hash</td>
<td>0x02</td>
<td>Computes the hash value of the mentioned flash region</td>
<td>SYS</td>
<td>Yes</td>
<td>CM0+, CM4, DAP</td>
</tr>
<tr>
<td>Soft Reset</td>
<td>0x1B</td>
<td>Provides system reset to either or both cores</td>
<td>SYS</td>
<td>No</td>
<td>CM0+, CM4, DAP</td>
</tr>
<tr>
<td>Write Row</td>
<td>0x05</td>
<td>Pre-program, erase, and program the addressed flash page</td>
<td>FLS</td>
<td>Yes</td>
<td>CM0+, CM4, DAP</td>
</tr>
<tr>
<td>Program Row</td>
<td>0x06</td>
<td>Programs the addressed flash page</td>
<td>FLS</td>
<td>Yes</td>
<td>CM0+, CM4, DAP</td>
</tr>
<tr>
<td>Erase All</td>
<td>0x0A</td>
<td>Erases all flash</td>
<td>FLS</td>
<td>No</td>
<td>CM0+, CM4, DAP</td>
</tr>
<tr>
<td>Checksum</td>
<td>0x0B</td>
<td>Reads either the whole flash or a row of flash, and returns the sum of each byte read</td>
<td>FLS</td>
<td>Yes</td>
<td>CM0+, CM4, DAP</td>
</tr>
<tr>
<td>Erase Sector</td>
<td>0x14</td>
<td>Erases the addressed flash sector</td>
<td>FLS</td>
<td>No</td>
<td>CM0+, CM4, DAP</td>
</tr>
<tr>
<td>Erase Row</td>
<td>0x1C</td>
<td>Erases the addressed flash page</td>
<td>FLS</td>
<td>No</td>
<td>CM0+, CM4, DAP</td>
</tr>
</tbody>
</table>

a: Refer to Chip Operational Modes chapter on page 113.
12.5 System Calls

Table 12-1 lists all the system calls supported in PSoC 6 MCUs along with the function description and availability in device protection modes. See the Device Security chapter on page 115 for more information on the device protection settings. Note that some system calls cannot be called by the CM4, CM0+, or DAP as given in the table. The following sections provide detailed information on each system call.

12.5.1 Silicon ID

This function returns a 12-bit family ID, 16-bit silicon ID, 8-bit revision ID, and the current device protection mode. These values are returned to the IPC_STRUCT.DATA register if invoked with IPC_STRUCT.DATA[0] set to ‘1’. Parameters are passed through the IPC_STRUCT.DATA register.

Note that only 32 bits are available to store the return value in the IPC structure. Therefore, the API takes a parameter ID type based on which it will return family ID and revision ID if the ID type is set to ‘0’, and silicon ID and protection state if the ID type is set to ‘1’.

Table 12-2. Silicon ID

<table>
<thead>
<tr>
<th>Cypress IDs</th>
<th>Memory Location</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>Family ID [7:0]</td>
<td>0xF0000FE0</td>
<td>Part Number [7:0]</td>
</tr>
<tr>
<td>Family ID [11:8]</td>
<td>0xF0000FE4</td>
<td>Part Number [3:0]</td>
</tr>
<tr>
<td>Major Revision</td>
<td>0xF0000FE8</td>
<td>Revision [7:4]</td>
</tr>
<tr>
<td>Minor Revision</td>
<td>0xF0000FEC</td>
<td>Rev and Minor Revision Field [7:4]</td>
</tr>
<tr>
<td>Silicon ID</td>
<td>SFLASH</td>
<td>Silicon ID [15:0]</td>
</tr>
<tr>
<td>Protection state</td>
<td>MMIO</td>
<td>Protection [3:0]</td>
</tr>
</tbody>
</table>

Parameters if DAP is Master

<table>
<thead>
<tr>
<th>Address</th>
<th>Value to be Written</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPC_STRUCT.DATA Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:24]</td>
<td>0x00</td>
<td>Silicon ID opcode.</td>
</tr>
<tr>
<td>Bits [15:8]</td>
<td>0 - returns 12-bit family ID and revision ID</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 - returns 16-bit silicon ID and protection state</td>
<td>ID type.</td>
</tr>
<tr>
<td>Bits [0]</td>
<td>0x1</td>
<td>Indicates that all the arguments are passed in DATA.</td>
</tr>
</tbody>
</table>

Parameters if CM0+/CM4 is Master

<table>
<thead>
<tr>
<th>Address</th>
<th>Value to be Written</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPC_STRUCT.DATA Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:0]</td>
<td>SRAM_SCRATCH_ADDR</td>
<td>SRAM address where the API parameters are stored. This must</td>
</tr>
<tr>
<td></td>
<td></td>
<td>be a 32-bit aligned address.</td>
</tr>
<tr>
<td>SRAM_SCRATCH Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:24]</td>
<td>0x00</td>
<td>Silicon ID opcode.</td>
</tr>
<tr>
<td>Bits [15:8]</td>
<td>0 - returns 12-bit family ID and revision ID</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 - returns 16-bit silicon ID and protection state</td>
<td>ID type.</td>
</tr>
<tr>
<td>Bits [0]</td>
<td>0xXX</td>
<td>Not used (don't care).</td>
</tr>
</tbody>
</table>
Nonvolatile Memory Programming

### Return if DAP Invoked the System Call

<table>
<thead>
<tr>
<th>Address</th>
<th>Return Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPC_STRUCT.DATA Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [7:0]</td>
<td>Silicon ID Lo</td>
<td>See the device datasheet for silicon ID values for different part numbers.</td>
</tr>
<tr>
<td>Bits [15:8]</td>
<td>Silicon ID Hi</td>
<td></td>
</tr>
<tr>
<td>Bits [19:16]</td>
<td>Minor Revision ID</td>
<td>See the PSoC 6 MCU Programming Specifications for these values.</td>
</tr>
<tr>
<td>Bits [23:20]</td>
<td>Major Revision ID</td>
<td></td>
</tr>
<tr>
<td>Bits [27:24]</td>
<td>0xXX</td>
<td>Not used (don't care).</td>
</tr>
<tr>
<td>Bits [31:28]</td>
<td>0xA = SUCCESS 0xF = ERROR</td>
<td>Status code (see 12.6 System Call Status for details).</td>
</tr>
</tbody>
</table>

### Return if CM0+/CM4 Invoked the System Call

<table>
<thead>
<tr>
<th>Address</th>
<th>Return Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRAM_SCRATCH Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [7:0]</td>
<td>Silicon ID Lo</td>
<td>See the device datasheet for silicon ID values for different part numbers.</td>
</tr>
<tr>
<td>Bits [15:8]</td>
<td>Silicon ID Hi</td>
<td></td>
</tr>
<tr>
<td>Bits [19:16]</td>
<td>Minor Revision ID</td>
<td>See the PSoC 6 MCU Programming Specifications for these values.</td>
</tr>
<tr>
<td>Bits [23:20]</td>
<td>Major Revision ID</td>
<td></td>
</tr>
<tr>
<td>Bits [27:24]</td>
<td>0xXX</td>
<td>Not used (don't care).</td>
</tr>
<tr>
<td>Bits [31:28]</td>
<td>0xA</td>
<td>Success status code.</td>
</tr>
</tbody>
</table>

### 12.5.2 Blow eFuse Bit

This function blows the addressed eFuse bit. The read value of a blown eFuse bit is ‘1’. These values are returned to the IPC_STRUCT.DATA register. Parameters are passed through the IPC_STRUCT.DATA register.

**Parameters if DAP is Master**

<table>
<thead>
<tr>
<th>Address</th>
<th>Value to be Written</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPC_STRUCT.DATA Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:24]</td>
<td>0x01</td>
<td>Blow eFuse bit opcode.</td>
</tr>
<tr>
<td>Bits [23:16]</td>
<td>Byte Address</td>
<td></td>
</tr>
<tr>
<td>Bits [10:8]</td>
<td>Bit Address</td>
<td></td>
</tr>
<tr>
<td>Bits [0]</td>
<td>0x1</td>
<td>Indicates that all the arguments are passed in DATA.</td>
</tr>
</tbody>
</table>

**Parameters if CM0+/CM4 is Master**

<table>
<thead>
<tr>
<th>Address</th>
<th>Value to be Written</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPC_STRUCT.DATA Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:0]</td>
<td>SRAM_SCRATCH_ADDR</td>
<td>SRAM address where the API parameters are stored. This must be a 32-bit aligned address.</td>
</tr>
<tr>
<td>SRAM_SCRATCH Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:24]</td>
<td>0x01</td>
<td>Blow eFuse bit opcode.</td>
</tr>
</tbody>
</table>
### 12.5.3 Read eFuse Byte

This function returns the eFuse contents of the addressed byte. The read value of a blown eFuse bit is ‘1’ and that of an unblown eFuse bit is ‘0’. These values are returned to the IPC_STRUCT.DATA register. Parameters are passed through the IPC_STRUCT.DATA register.

#### Parameters if DAP is Master

<table>
<thead>
<tr>
<th>Address</th>
<th>Value to be Written</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPC_STRUCT.DATA  Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:24]</td>
<td>0x03</td>
<td>Blow eFuse bit opcode.</td>
</tr>
<tr>
<td>Bits [23:8]</td>
<td>eFuse Address</td>
<td>Refer to the eFuse Memory chapter on page 112 for more details.</td>
</tr>
<tr>
<td>Bits [0]</td>
<td>0x1</td>
<td>Indicates all arguments are passed in DATA.</td>
</tr>
</tbody>
</table>

#### Parameters if CM0+/CM4 is Master

<table>
<thead>
<tr>
<th>Address</th>
<th>Value to be Written</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPC_STRUCT.DATA  Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:0]</td>
<td>SRAM_SCRATCH_ADDR</td>
<td>SRAM address where the API parameters are stored. This must be a 32-bit aligned address.</td>
</tr>
<tr>
<td>SRAM_SCRATCH Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:24]</td>
<td>0x02</td>
<td>Blow eFuse bit opcode.</td>
</tr>
<tr>
<td>Bits [23:8]</td>
<td>eFuse Address</td>
<td>Refer to the eFuse Memory chapter on page 112 for more details.</td>
</tr>
<tr>
<td>Bits [7:0]</td>
<td>0xXX</td>
<td>Not used (don't care).</td>
</tr>
</tbody>
</table>
Nonvolatile Memory Programming

Return if DAP Invoked the System Call

<table>
<thead>
<tr>
<th>Address</th>
<th>Return Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPC_STRUCT.DATA Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [23:0]</td>
<td>eFuse byte</td>
<td>Byte read from eFuse if status is success; otherwise, error code.</td>
</tr>
<tr>
<td>Bits [27:24]</td>
<td>0xXX</td>
<td>Not used (don't care).</td>
</tr>
<tr>
<td>Bits [31:28]</td>
<td>0xA = SUCCESS</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0xF = ERROR</td>
<td>Status code (see 12.6 System Call Status for details).</td>
</tr>
</tbody>
</table>

Return if CM0+/CM4 Invoked the System Call

<table>
<thead>
<tr>
<th>Address</th>
<th>Return Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRAM_SCRATCH Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [23:0]</td>
<td>eFuse byte</td>
<td>Byte read from eFuse if status is success; otherwise, error code.</td>
</tr>
<tr>
<td>Bits [27:24]</td>
<td>0xXX</td>
<td>Not used (don't care).</td>
</tr>
<tr>
<td>Bits [31:28]</td>
<td>0xA = SUCCESS</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0xF = ERROR</td>
<td>Status code (see 12.6 System Call Status for details).</td>
</tr>
</tbody>
</table>

12.5.4 Write Row

This function is used to program the flash. You must provide data to be loaded and the flash address to be programmed. The WriteRow parameter performs pre-program and erase, and then programs the flash page contents from the page latch.

The PSoC 6 MCU supports the Read While Write (RWW) feature, which allows flash to be read from a RWW sector that is not programmed/erased during a program/erase of another RWW sector. Each row consists of 512 bytes.

The user flash (UFLASH) in PSoC 6 MCU has four RWW sectors, UFLASH0 to UFLASH3, each 256KB in size.

Emulated EEPROM and Supervisory Flash (SFLASH) are additional RWW sectors apart from the main flash.

Note: When writing to flash in a non-blocking mode, the RWW sectors are used in pairs (512KB) as follows:
- UFLASH0 and UFLASH1
- UFLASH2 and UFLASH3.
- Emulated EEPROM and SFLASH.

RWW functionality is not applicable within the same sector pairs. For example, while writing to sector pair UFLASH0 and UFLASH1, sector pairs UFLASH2 and UFLASH3, and Emulated EEPROM and SFLASH can be read.

The API is implemented in three phases to make it non-blocking. The first phase sets up the flash for pre-program and erase operations and returns to the user code by exiting from NMI without releasing the IPC structure that invoked the API. Now, user code and interrupts can be handled but no NMI can be invoked.

Upon completion of the erase, an interrupt is generated by the flash macro, which will invoke the third phase of the WriteRow API to complete the ongoing erase operation successfully and start the program operation. API returns from NMI to user code after it sets up for program operation.

Upon completion of the program, an interrupt is generated by the flash macro, which will invoke the fourth phase of the WriteRow API to complete the ongoing program operation successfully; this completes the WriteRow API. SROM API will now return the pass or fail status and releases the IPC structure.

This API can also be called in blocking mode by setting the blocking parameter as ‘1’, in which case the API will return only after all flash operation completes.

The API returns a fail status if you do not have write access to flash according to SMPU settings. See the CPU Subsystem (CPUSS) chapter on page 30 for more details. After flash program operation is complete, the API will optionally compare the flash row with the contents in page latch for data integrity check. The function returns 0xF0000022 if the data integrity check fails.
Note that to be able to perform flash writes, the $V_{CCD}$ should be more than 0.99 V. If the device operating voltage is less than 0.99 V (the 0.9-V mode of operation), follow this sequence to perform any flash write operations.

1. Write the appropriate registers to increase voltage from 0.9 V to 1.1 V. Refer to Power Supply on page 122 for details on how to switch voltages.
2. Write VCC_SEL = 1.
3. Perform the flash write operations.
4. Write the appropriate registers to drop the regulated voltage from 1.1 V to 0.9 V.
5. Write VCC_SEL = 0.

**Parameters if DAP/CM0+/CM4 is Master**

<table>
<thead>
<tr>
<th>Address</th>
<th>Value to be Written</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPC_STRUCT.DAT A Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:0]</td>
<td>SRAM_SCRATCH_ADDR</td>
<td>SRAM address where the API parameters are stored. This must be a 32-bit aligned address.</td>
</tr>
<tr>
<td>SRAM_SCRATCH Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:24]</td>
<td>0x05</td>
<td>Write Row opcode.</td>
</tr>
<tr>
<td>Bits [23:16]</td>
<td>0xXX</td>
<td>Not used</td>
</tr>
<tr>
<td>Bits [15:8]</td>
<td>Blocking: 0x01 – API blocks CM0+ Other values - Non-blocking</td>
<td></td>
</tr>
<tr>
<td>Bits [7:0]</td>
<td>0xXX</td>
<td>Not used</td>
</tr>
<tr>
<td>SRAM_SCRATCH Register + 0x04</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [23:16]</td>
<td>Verify row: 0 - Data integrity check is not performed 1 - Data integrity check is performed</td>
<td></td>
</tr>
<tr>
<td>Bits [7:0]</td>
<td>0xXX</td>
<td>Not used (don't care).</td>
</tr>
<tr>
<td>SRAM_SCRATCH Register + 0x08</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:0]</td>
<td>Flash address to be programmed. This should be provided in 32-bit system address format. For example, to program the second half-word you need to provide either of the byte address 0x1000003/4.</td>
<td></td>
</tr>
<tr>
<td>SRAM_SCRATCH Register + 0x0C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:0]</td>
<td>Data word 0 (data provided should be proportional to the data size provided, data to be programmed into LSbs)</td>
<td></td>
</tr>
<tr>
<td>SRAM_SCRATCH Register + 0x0C + n*0x04</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:0]</td>
<td>Data word n (data to be programmed)</td>
<td></td>
</tr>
</tbody>
</table>

**Return if DAP/CM0+/CM4 Invoked the System Call**

<table>
<thead>
<tr>
<th>Address</th>
<th>Return Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRAM_SCRATCH Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [27:0]</td>
<td>Error code (if any)</td>
<td>See 12.6 System Call Status for details.</td>
</tr>
<tr>
<td>Bits [31:28]</td>
<td>0xA = SUCCESS/Program command ongoing in background 0xF = ERROR</td>
<td>Status code (see 12.6 System Call Status for details).</td>
</tr>
</tbody>
</table>
12.5.5  Program Row

This function programs the addressed flash page. You must provide the data to be loaded and flash address to be programmed. The flash page should be in the erased state before calling this function.

The function is implemented in two phases to make it non-blocking. The first phase sets up the flash for program operation and returns to user code by exiting from NMI without releasing the IPC structure that invoked the API. Now user code and interrupts can be handled but no NMI can be invoked.

Upon completion of the program operation, an interrupt is generated by the flash macro, which will invoke the second phase of the ProgramRow API to complete the ongoing program operation successfully. The SROM API will return the pass or fail status and releases the IPC structure.

After flash program operation is complete, the API will optionally compare the flash row with the contents in the page latch for data integrity check. It returns STATUS_PL_ROW_COMP_FA if data integrity check fails.

The values are returned to the IPC_STRUCT.DATA register. Parameters are passed through the IPC_STRUCT.DATA register.

Note that to be able to perform flash writes, the \( V_{CCD} \) should be more than 0.99 V. If the device operating voltage is less than 0.99 V (the 0.9-V mode of operation), follow this sequence to perform any flash write operations.

1. Write the appropriate registers to increase voltage from 0.9 V to 1.1 V. Refer to Power Supply on page 122 for details on how to switch voltages.
2. Write VCC_SEL = 1.
3. Perform the flash write operations.
4. Write the appropriate registers to drop the regulated voltage from 1.1 V to 0.9 V.
5. Write VCC_SEL = 0.

Parameters if DAP/CM0+/CM4 is Master

<table>
<thead>
<tr>
<th>Address</th>
<th>Value to Be Written</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPC_STRUCT.DATA Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:0]</td>
<td>SRAM_SCRATCH_ADDR</td>
<td>SRAM address where the API parameters are stored. This must be a 32-bit aligned address.</td>
</tr>
<tr>
<td>SRAM_SCRATCH Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits[31:24]</td>
<td>0x06</td>
<td>Program Row opcode.</td>
</tr>
<tr>
<td>Bits[23:16]</td>
<td>0xx</td>
<td>Not used</td>
</tr>
<tr>
<td>Bits[15:8]</td>
<td>Blocking: 0x01 – API blocks CM0+</td>
<td>Other values - Non-blocking</td>
</tr>
<tr>
<td>Bits[7:0]</td>
<td>0xx</td>
<td>Not used</td>
</tr>
<tr>
<td>SRAM_SCRATCH Register + 0x04</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [23:16]</td>
<td>Verify row: 0 - Data integrity check is not performed</td>
<td>1 - Data integrity check is performed</td>
</tr>
<tr>
<td>Bits [15:8]</td>
<td>Data location : 0 - page latch , 1- SRAM</td>
<td></td>
</tr>
<tr>
<td>Bits[7:0]</td>
<td>0xx</td>
<td>Not used (don't care).</td>
</tr>
<tr>
<td>SRAM_SCRATCH Register + 0x08</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:0]</td>
<td>Flash address to be programmed. This should be provided in 32-bit system address format. For example, to program the second half-word, provide either of the byte address 0x1000003/4.</td>
<td></td>
</tr>
</tbody>
</table>
## Nonvolatile Memory Programming

### Return if DAP/CM0+/CM4 Invoked the System Call

<table>
<thead>
<tr>
<th>Address</th>
<th>Return Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRAM_SCRATCH Register</td>
<td>Error code (if any)</td>
<td>See 12.6 System Call Status for details.</td>
</tr>
<tr>
<td>Bits [27:0]</td>
<td>0xA = SUCCESS/Program command ongoing in background</td>
<td></td>
</tr>
<tr>
<td>Bits [31:28]</td>
<td>0xF = ERROR</td>
<td>Status code (see 12.6 System Call Status for details).</td>
</tr>
</tbody>
</table>

### 12.5.6 Erase All

This function erases the entire flash macro specified. This API will erase only the main flash array. The API will check whether all data is '0' to confirm whether the erase is successful. It will return CHECKSUM NON_ZERO error status if a non-zero word is encountered in the available flash.

The values are returned to the IPC_STRUCT.DATA register. Parameters are passed through the IPC_STRUCT.DATA register.

Note that to be able to perform flash writes, the $V_{CCD}$ should be more than 0.99 V. If the device operating voltage is less than 0.99 V (the 0.9-V mode of operation), follow this sequence to perform any flash write operation.

1. Write the appropriate registers to increase voltage from 0.9 V to 1.1 V. Refer to Power Supply on page 122 for details on how to switch voltages.
2. Write $VCC_{SEL} = 1$.
3. Perform the flash write operations.
4. Write the appropriate registers to drop the regulated voltage from 1.1 V to 0.9 V.
5. Write $VCC_{SEL} = 0$.

#### Parameters if DAP is Master

<table>
<thead>
<tr>
<th>Address</th>
<th>Value to be Written</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPC_STRUCT.DATA Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:24]</td>
<td>0x0A</td>
<td>Erase All opcode.</td>
</tr>
<tr>
<td>Bits [0]</td>
<td>1</td>
<td>Indicates that all the arguments are passed in DATA.</td>
</tr>
</tbody>
</table>

#### Parameters if CM0+/CM4 is Master

<table>
<thead>
<tr>
<th>Address</th>
<th>Value to be Written</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPC_STRUCT.DATA Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [3:0]</td>
<td>SRAM_SCRATCH_ADDR</td>
<td>SRAM address where the API parameters are stored. This must be a 32-bit aligned address.</td>
</tr>
<tr>
<td>SRAM_SCRATCH Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:24]</td>
<td>0x0A</td>
<td>Erase All opcode.</td>
</tr>
<tr>
<td>Bits[23:0]</td>
<td>0xFFF</td>
<td>Not used (don't care).</td>
</tr>
</tbody>
</table>
Return if DAP Invoked the System Call

<table>
<thead>
<tr>
<th>Address</th>
<th>Return Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPC_STRUCT.DATA Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [23:20]</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>Bits [27:24]</td>
<td>0xXX</td>
<td>Not used (don’t care).</td>
</tr>
<tr>
<td>Bits [31:28]</td>
<td>0xA</td>
<td>Success status code.</td>
</tr>
</tbody>
</table>

Return if CM0+/CM4 Invoked the System Call

<table>
<thead>
<tr>
<th>Address</th>
<th>Return Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRAM_SCRATCH Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [23:20]</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>Bits [27:24]</td>
<td>0xXX</td>
<td>Not used (don’t care).</td>
</tr>
<tr>
<td>Bits [31:28]</td>
<td>0xA</td>
<td>Success status code.</td>
</tr>
</tbody>
</table>

12.5.7 Checksum

This function reads either the entire flash or a row of flash, and returns the sum of each byte read. Bytes 1 and 2 of the parameters select whether the checksum is performed on the entire flash or on a row of flash. This function will inherit the identity of the master that called the function. Hence if a non-secure master requests for either the whole or page checksum of a secured flash, then the fault exception will be raised by the hardware.

The values are returned to the IPC_STRUCT.DATA register. Parameters are passed through the IPC_STRUCT.DATA register.

Parameters if DAP is Master

<table>
<thead>
<tr>
<th>Address</th>
<th>Value to be Written</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPC_STRUCT.DATA Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:24]</td>
<td>0x0B</td>
<td>Checksum opcode.</td>
</tr>
<tr>
<td>Bits [23:22]</td>
<td>0 - main</td>
<td>Flash region.</td>
</tr>
<tr>
<td></td>
<td>1 - work</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2 - supervisory</td>
<td></td>
</tr>
<tr>
<td>Bits [21]</td>
<td>0 - page</td>
<td>Whole flash.</td>
</tr>
<tr>
<td></td>
<td>1 - whole flash</td>
<td></td>
</tr>
<tr>
<td>Bits [20:8]</td>
<td></td>
<td>Row ID.</td>
</tr>
<tr>
<td>Bits [0]</td>
<td>1</td>
<td>Indicates that all the arguments are passed in DATA.</td>
</tr>
</tbody>
</table>

Parameters if CM0+/CM4 is Master

<table>
<thead>
<tr>
<th>Address</th>
<th>Value to be Written</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPC_STRUCT.DATA Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:0]</td>
<td>SRAM_SCRATCH_ADDR</td>
<td>SRAM address where the API parameters are stored. This must be a 32-bit aligned address.</td>
</tr>
<tr>
<td>SRAM_SCRATCH Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:24]</td>
<td>0x0B</td>
<td>Checksum opcode.</td>
</tr>
</tbody>
</table>
12.5.8 Compute Hash

This function generates the hash of the flash region provided using the formula:

\[ H(n+1) = \{H(n)\times2+\text{Byte}\}\mod 127; \text{ where } H(0) = 0 \]

This function returns an invalid address status if called on an out-of-bound flash region. Note that CM0+ will inherit the protection context of the master, which invoked it before performing hash. The values are returned to the IPC_STRUCT.DATA register. Parameters are passed through the IPC_STRUCT.DATA register.

### Parameters if DAP/CM0+/CM4 is Master

<table>
<thead>
<tr>
<th>Address</th>
<th>Value to be Written</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPC_STRUCT.DATA Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:0]</td>
<td>SRAM_SCRATCH_ADDR</td>
<td>SRAM address where the API parameters are stored. This must be a 32-bit aligned address.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Address</th>
<th>Value to be Written</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRAM_SCRATCH Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:24]</td>
<td>0xXX</td>
<td>Not used (don't care).</td>
</tr>
<tr>
<td>Bits [15:8]</td>
<td>0x01 - CRC8 SAE others - Basic hash</td>
<td>Type</td>
</tr>
<tr>
<td>Bits [7:0]</td>
<td>0xXX</td>
<td>Not used (don't care)</td>
</tr>
</tbody>
</table>
Nonvolatile Memory Programming

Return if DAP/CM0+/CM4 Invoked the System Call

<table>
<thead>
<tr>
<th>Address</th>
<th>Return Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRAM_SCRATCH Register</td>
<td>Hash of the data</td>
<td>Hash of data if status is SUCCESS.</td>
</tr>
<tr>
<td>Bits [23:0]</td>
<td>Hash of the data</td>
<td>Hash of data if status is SUCCESS.</td>
</tr>
<tr>
<td>Bits [27:24]</td>
<td>0XX</td>
<td>Not used (don't care).</td>
</tr>
<tr>
<td>Bits [31:28]</td>
<td>0xA = SUCCESS 0xF = ERROR</td>
<td>Status code (see 12.6 System Call Status for details).</td>
</tr>
</tbody>
</table>
12.5.9 Erase Sector

This function erases the specified sub-sector. Each sub-sector consists of eight rows. The values are returned to the IPC_STRUCT.DATA register. Parameters are passed through the IPC_STRUCT.DATA register.

Note that to be able to perform flash writes, the \( V_{\text{CCD}} \) should be more than 0.99 V. If the device operating voltage is less than 0.99 V (the 0.9-V mode of operation), follow this sequence to perform any flash write operations.

1. Write the appropriate registers to increase voltage from 0.9 V to 1.1 V. Refer to Power Supply on page 122 for details on how to switch voltages.
2. Write \( \text{VCC\_SEL} = 1 \).
3. Perform the flash write operations.
4. Write the appropriate registers to drop the regulated voltage from 1.1 V to 0.9 V.
5. Write \( \text{VCC\_SEL} = 0 \).

Parameters if DAP/CM0+/CM4 is Master

<table>
<thead>
<tr>
<th>Address</th>
<th>Value to be Written</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPC_STRUCT.DATA Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:0] SRAM_SCRATCH_ADDR</td>
<td>SRAM address where the API parameters are stored. This must be a 32-bit aligned address.</td>
<td></td>
</tr>
<tr>
<td>SRAM_SCRATCH Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:24]</td>
<td>0x14</td>
<td>Erase Sector opcode.</td>
</tr>
<tr>
<td>Bits [23:16]</td>
<td>0x01 - Set FM interrupt mask Other - Do not set FM interrupt mask</td>
<td>Interrupt mask</td>
</tr>
<tr>
<td>Bits [15:8]</td>
<td>Blocking: 0x01 – API blocks CM0+ Other values – Non-blocking</td>
<td></td>
</tr>
<tr>
<td>Bits [7:0]</td>
<td>0xXX</td>
<td>Not used</td>
</tr>
<tr>
<td>SRAM_SCRATCH Register + 0x04</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:0]</td>
<td>Flash address to be erased. Should be provided in 32-bit system address format. For example, to erase the second sector you need to provide the 32-bit system address of any of the bytes in the second sector.</td>
<td></td>
</tr>
</tbody>
</table>

Return if DAP/CM0+/CM4 Invoked the System Call

<table>
<thead>
<tr>
<th>Address</th>
<th>Return Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRAM_SCRATCH Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [27:0]</td>
<td>Error code (if any)</td>
<td>See 12.6 System Call Status for details.</td>
</tr>
<tr>
<td>Bits [31:28]</td>
<td>0xA = SUCCESS 0xF = ERROR</td>
<td>Status code (see 12.6 System Call Status for details).</td>
</tr>
</tbody>
</table>
12.5.10  Soft Reset

This function resets the system by setting CM0+ AIRCR system reset bit. This will result in a system-wide reset, except debug logic. This API can also be used for selective reset of only the CM4 core based on the ‘Type’ parameter. The values are returned to the IPC_STRUCT.DATA register. Parameters are passed through the IPC_STRUCT.DATA register.

**Parameters if DAP is Master**

<table>
<thead>
<tr>
<th>Address</th>
<th>Value to Be Written</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPC_STRUCT.DATA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:24]</td>
<td>0x1B</td>
<td>Soft Reset opcode.</td>
</tr>
<tr>
<td>Bits [7:1]</td>
<td>0 - System reset</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 - Only CM4 resets</td>
<td></td>
</tr>
<tr>
<td>Bits[0]</td>
<td>0x1</td>
<td>Indicates all arguments are passed in DATA.</td>
</tr>
</tbody>
</table>

**Parameters if CM0+/CM4 is Master**

<table>
<thead>
<tr>
<th>Address</th>
<th>Value to Be Written</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPC_STRUCT.DATA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:0]</td>
<td>SRAM_SCRATCH_ADDR</td>
<td>SRAM address where the API parameters are stored. This must be a 32-bit aligned address.</td>
</tr>
<tr>
<td>SRAM_SCRATCH</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:24]</td>
<td>0x1B</td>
<td>Soft Reset opcode.</td>
</tr>
<tr>
<td>Bits[7:1]</td>
<td>0 - System reset</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 - Only CM4 resets</td>
<td></td>
</tr>
<tr>
<td>Bits[0]</td>
<td>0xXX</td>
<td>Not used (don't care).</td>
</tr>
</tbody>
</table>

**Return if DAP Invoked the System Call**

<table>
<thead>
<tr>
<th>Address</th>
<th>Return Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPC_STRUCT.DATA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [27:0]</td>
<td>Error code (if any)</td>
<td>See 12.6 System Call Status for details.</td>
</tr>
<tr>
<td>Bits [31:28]</td>
<td>0xA = SUCCESS</td>
<td>Status code (see 12.6 System Call Status for details).</td>
</tr>
<tr>
<td></td>
<td>0xF = ERROR</td>
<td></td>
</tr>
</tbody>
</table>

**Return if CM0+/CM4 Invoked the System Call**

<table>
<thead>
<tr>
<th>Address</th>
<th>Return Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRAM_SCRATCH</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [27:0]</td>
<td>Error code (if any)</td>
<td>See 12.6 System Call Status for details.</td>
</tr>
<tr>
<td>Bits [31:28]</td>
<td>0xA = SUCCESS</td>
<td>Status code (see 12.6 System Call Status for details).</td>
</tr>
<tr>
<td></td>
<td>0xF = ERROR</td>
<td></td>
</tr>
</tbody>
</table>
12.5.11 Erase Row

This function erases the specified page. You must provide the address of the row that needs to be erased. The values are returned to the IPC_STRUCT.DATA register. Parameters are passed through the IPC_STRUCT.DATA register.

Note that to be able to perform flash writes, the V\textsubscript{CDD} should be more than 0.99 V. If the device operating voltage is less than 0.99 V (the 0.9-V mode of operation), follow this sequence to perform any flash write operations.

1. Write the appropriate registers to increase voltage from 0.9 V to 1.1 V. Refer to Power Supply on page 122 for details on how to switch voltages.
2. Write VCC_SEL = 1.
3. Perform the flash write operations.
4. Write the appropriate registers to drop the regulated voltage from 1.1 V to 0.9 V.
5. Write VCC_SEL = 0.

Parameters if DAP/CM0+/CM4 is Master

<table>
<thead>
<tr>
<th>Address</th>
<th>Value to be Written</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPC_STRUCT.DATA Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:0]</td>
<td>SRAM_SCRATCH_ADDR</td>
<td>SRAM address where the API parameters are stored. This must be a 32-bit aligned address.</td>
</tr>
<tr>
<td>SRAM_SCRATCH Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits[31:24]</td>
<td>0x1C</td>
<td>Erase Row opcode.</td>
</tr>
<tr>
<td>Bits[23:16]</td>
<td>0xXX</td>
<td></td>
</tr>
<tr>
<td>Bits[15:8]</td>
<td>0x01 - API blocks CM0+ Other - Non-blocking</td>
<td></td>
</tr>
<tr>
<td>Bits[7:0]</td>
<td>0xXX</td>
<td>Not used (don't care)</td>
</tr>
<tr>
<td>SRAM_SCRATCH Register + 0x04</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:0]</td>
<td>Address</td>
<td>Flash address to be erased. This should be provided in the 32-bit system address format. For example, to erase the second row you need to provide the 32-bit system address of any of the bytes in the second page.</td>
</tr>
</tbody>
</table>

Return if DAP/CM0+/CM4 Invoked the System Call

<table>
<thead>
<tr>
<th>Address</th>
<th>Return Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRAM_SCRATCH Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits[27:0]</td>
<td>Error code (if any)</td>
<td>See 12.6 System Call Status for details.</td>
</tr>
<tr>
<td>Bits[31:28]</td>
<td>0xA = SUCCESS 0xF = ERROR</td>
<td>Status code (see 12.6 System Call Status for details).</td>
</tr>
</tbody>
</table>
12.5.12 Erase Sub Sector

This function erases the specified sub-sector. The values are returned to the IPC_STRUCT.DATA register. Parameters are passed through the IPC_STRUCT.DATA register.

Note that to be able to perform flash writes, the V\textsubscript{CCD} should be more than 0.99 V. If the device operating voltage is less than 0.99 V (the 0.9-V mode of operation), follow this sequence to perform any flash write operations.

1. Write the appropriate registers to increase voltage from 0.9 V to 1.1 V. Refer to Power Supply on page 122 for details on how to switch voltages.
2. Write VCC_SEL = 1.
3. Perform the flash write operations.
4. Write the appropriate registers to drop the regulated voltage from 1.1 V to 0.9 V.
5. Write VCC_SEL = 0.

Parameters if DAP/CM0+/CM4 is Master

<table>
<thead>
<tr>
<th>Address</th>
<th>Value to be Written</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bits [31:0]</td>
<td>SRAM_SCRATCH_ADDR</td>
<td>SRAM address where the API parameters are stored. This must be a 32-bit aligned address.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>SRAM_SCRATCH Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bits [31:24]</td>
</tr>
<tr>
<td>Bits[23:16]</td>
</tr>
<tr>
<td>Bits[15:8]</td>
</tr>
<tr>
<td>Bits[7:0]</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>SRAM_SCRATCH Register + 0x04</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bits [31:0]</td>
</tr>
</tbody>
</table>

Return if DAP/CM0+/CM4 Invoked the System Call

<table>
<thead>
<tr>
<th>Address</th>
<th>Return Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRAM_SCRATCH Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [27:0]</td>
<td>Error code (if any)</td>
<td>See 12.6 System Call Status for details.</td>
</tr>
<tr>
<td>Bits [31:28]</td>
<td>0xA = SUCCESS 0xF = ERROR</td>
<td>Status code (see 12.6 System Call Status for details).</td>
</tr>
</tbody>
</table>
12.6 System Call Status

At the end of every system call, a status code is written over the arguments in the IPC data structure or the SRAM address pointed by the IPC location. A success status is 0xAXXXXXXX, where X indicates don't care values or return data for system calls that return a value. A failure status is indicated by 0xF0000XX, where XX is the failure code.

Table 12-3. System Call Status

<table>
<thead>
<tr>
<th>Status Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xAXXXXXXX</td>
<td>Success – The X denotes a don't care value, which has a value of '0' returned by the SROM.</td>
</tr>
<tr>
<td>0xF0000001</td>
<td>Invalid protection state – This API is not available in current protection state.</td>
</tr>
<tr>
<td>0xF0000002</td>
<td>Invalid eFuse address.</td>
</tr>
<tr>
<td>0xF0000003</td>
<td>Invalid flash page latch address.</td>
</tr>
<tr>
<td>0xF0000004</td>
<td>Wrong or out-of-bound flash address.</td>
</tr>
<tr>
<td>0xF0000005</td>
<td>Row is write protected.</td>
</tr>
<tr>
<td>0xA0000009</td>
<td>Command in progress.</td>
</tr>
<tr>
<td>0xF000000A</td>
<td>Checksum of flash resulted in non-zero.</td>
</tr>
<tr>
<td>0xF0000021</td>
<td>Sector erase requested on SFLASH region.</td>
</tr>
<tr>
<td>0xF0000041</td>
<td>Bulk erase failed.</td>
</tr>
<tr>
<td>0xF0000042</td>
<td>Sector erase failed.</td>
</tr>
<tr>
<td>0xF0000043</td>
<td>Subsector erase failed.</td>
</tr>
<tr>
<td>0xF0000044</td>
<td>Verification of Bulk, Sector, or Subsector fails after program/erase.</td>
</tr>
<tr>
<td>0xF0000006</td>
<td>Client did not use its reserved IPC structure for invoking system call.</td>
</tr>
<tr>
<td>0xF0000007</td>
<td>CM4 was not in a known state when SoftReset was invoked.</td>
</tr>
<tr>
<td>0xF000000B</td>
<td>The opcode is not a valid API opcode.</td>
</tr>
<tr>
<td>0xF000000F</td>
<td>Returned when invalid arguments are passed to the API. For example, calling Silicon ID API with ID type of 0x5.</td>
</tr>
</tbody>
</table>
The eFuse memory consists of a set of eFuse bits. When an eFuse bit is programmed, or “blown”, its value can never be changed. Some of the eFuse bits are used to store various unchanging device parameters, including critical device factory trim settings, device life cycle stages (see the Device Security chapter on page 115), DAP security settings, and encryption keys. Other eFuse bits are available for custom use.

13.1 Features

The PSoC 6 MCU eFuses have the following features:

- A total of 1024 eFuse bits. 512 of them are available for custom purposes.
- The eFuse bits are programmed one at a time, in a manufacturing environment. The eFuse bits cannot be programmed in the field.
- Multiple eFuses can be read at the bit or byte level through a PDL API function call or an SROM call. An unblown eFuse reads as logic 0 and a blown eFuse reads as logic 1. There are no hardware connections from eFuse bits to elsewhere in the device.
- SROM system calls are available to program and read eFuses. See the Nonvolatile Memory Programming chapter on page 94. For detailed information on programming eFuses, see the PSoC 6 MCU Programming Specifications.

13.2 Architecture

The PSoC 6 MCU eFuses can be programmed only in a manufacturing environment. \( V_{DDIO0} \) must be set to 2.5 V, and the device must be in a specific test mode, entered through an XRES key. For more information, see the PSoC 6 MCU Programming Specifications.

Table 13-1 shows the usage of the PSoC 6 MCU eFuse bytes.

<table>
<thead>
<tr>
<th>Offset</th>
<th>No. of Bytes</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>20</td>
<td>Reserved</td>
<td>Reserved for PSoC 6 MCU system usage</td>
</tr>
<tr>
<td>20</td>
<td>16</td>
<td>SECURE_CMAC</td>
<td>Secure objects 128-bit CMAC</td>
</tr>
<tr>
<td>36</td>
<td>2</td>
<td>FLASH_BOOT_SIZE</td>
<td>Flash boot image size</td>
</tr>
<tr>
<td>38</td>
<td>1</td>
<td>SECURE_CMAC_ZEROS</td>
<td>Number of zeros in SECURE_CMAC</td>
</tr>
<tr>
<td>39</td>
<td>2</td>
<td>DEAD_ACCESS_RESTR</td>
<td>Access restrictions in DEAD life cycle stage</td>
</tr>
<tr>
<td>41</td>
<td>2</td>
<td>SECURE_ACCESS_RESTR</td>
<td>Access restrictions in SECURE life cycle stage</td>
</tr>
<tr>
<td>43</td>
<td>1</td>
<td>LIFECYCLE_STAGE</td>
<td>NORMAL, SECURE, and SECURE with DEBUG eFuse bits</td>
</tr>
<tr>
<td>44</td>
<td>8</td>
<td>Reserved</td>
<td>Reserved for PSoC 6 MCU system usage</td>
</tr>
<tr>
<td>52</td>
<td>12</td>
<td>Unused</td>
<td>Not used</td>
</tr>
<tr>
<td>64</td>
<td>64</td>
<td>CUSTOM_DATA</td>
<td>Custom data</td>
</tr>
</tbody>
</table>
14. Chip Operational Modes

PSoc 6 MCU is capable of executing firmware in four different modes. These modes dictate execution from different locations in flash and ROM, with different levels of hardware privileges. Only three of these modes are used in end-applications; debug mode is used exclusively to debug designs during firmware development. This chapter gives an overview of the PSoc 6 MCU operational modes. The power modes are explained in the Device Power Modes chapter on page 128.

14.1 Features

PSoc 6 MCU supports the following operational modes:

- Boot
- User
- Trusted
- Debug

14.2 Architecture

Following is an overview of the PSoc 6 MCU operational modes:

14.2.1 Boot

Boot mode is an operational mode where the device is configured by instructions hard-coded in the device ROM and from supervisory flash. This mode is entered after the end of a reset, provided no debug-acquire sequence is received by the device. Boot mode is a trusted mode; interrupts are disabled so that the boot firmware can set up the device for operation without being interrupted. In boot mode, hardware trim settings are loaded from flash to guarantee proper operation during power-up. When ROM boot code is executed, supervisory flash boot code execution begins after flash boot authentication. After both ROM boot and flash boot, the device enters user mode and code execution from user flash begins. This code in flash may include automatically generated instructions from the PSoc Creator IDE that will further configure the device.

14.2.2 User

User mode is an operational mode where normal user firmware from flash is executed. User mode cannot execute code from ROM. Firmware execution in this mode includes the automatically generated firmware by the PSoc Creator IDE and the firmware written by the user. The automatically generated firmware can govern both the firmware startup and portions of normal operation. The boot process transfers control to this mode after it has completed its tasks.

14.2.3 Trusted

Trusted mode is an operational mode that allows execution of special subroutines that are stored in the device ROM. These subroutines cannot be modified by the user and are used to execute proprietary code that is not meant to be interrupted or observed. Debugging is not allowed in the trusted mode.

Trusted ROM code can be executed only when the master is in protection context 0. Only the CM0+ (secure CPU) can attain protection context 0 upon a system reset or a trusted interrupt handler entry. See the Device Security chapter on page 115 for more details on protection states. Exit from this mode returns the device to user mode.
14.2.4 Debug

Debug mode is an operational mode that allows observation of the PSoC 6 MCU operational parameters. This mode is used to debug firmware during development. The debug mode is entered when a debugger connects to the device during the acquire time window, which occurs during the device reset. Debug mode allows IDEs such as PSoC Creator and Arm MDK to debug the firmware. Debug mode is available only on devices whose access restriction settings allow debugging. For NORMAL protection state, access restriction settings are stored in the supervisory flash (SFLASH). For DEAD and SECURE states, it is stored in eFuse. For more details on protection states, see the Device Security chapter on page 115. For more details on the debug interface, see the Program and Debug Interface chapter on page 85.
15. Device Security

The PSoC 6 MCU offers several features to protect user designs from unauthorized access or copying. Selecting a secure life cycle stage, enabling flash protection, and using hardware-based encryption can provide a high level of security.

Note: Because all programming, debug, and test interfaces are inaccessible when maximum device security is enabled, PSoC 6 MCUs with full device security enabled may not be returned for failure analysis.

15.1 Features

The PSoC 6 MCU provides the following device security features:

- Nonvolatile and irreversible life cycle stages that can limit program and debug access.
- Shared memory protection unit (SMPU) that provides flash protection at the sector level.
- Cryptographic function block that provides hardware-based encryption and decryption of data and code.

15.2 Architecture

15.2.1 Life Cycle Stages and Protection States

PSoC 6 MCUs have configurable, nonvolatile life cycle stages. Life cycle stages follow a strict, irreversible progression governed by writing to eFuse – a 1024-bit nonvolatile memory with each bit being one time programmable (OTP). The eFuse can hold unalterable keys and trim information. See the eFuse Memory chapter on page 112 for more details of the eFuse; see the Nonvolatile Memory Programming chapter on page 94 for eFuse access system calls.

Figure 15-1. PSoC 6 MCU Life Cycle Stage Transitions
The EFUSE_DATA_LIFECYCLE_STAGE eFuse governs the life-cycle stages.

The PSoC 6 MCU supports the following life cycle stages:
- **VIRGIN** – This stage is used by Cypress during assembly and testing. During this stage, trim values and flash boot are written into SFlash. Devices that are in this stage never leave the factory. In this stage, the boot ROM assumes that no other eFuse data or flash data is valid. Devices are transitioned to the Normal stage before they leave the factory.
- **NORMAL** – This is the life cycle stage of a device after trimming and testing is complete in the factory. All configuration and trimming information is complete. Valid flash boot code is programmed in the SFlash. To allow the OEM to check data integrity of trims, flash boot, and other objects from the factory, a hash (SHA-256 truncated to 128 bits) of these objects is stored in eFuse. This hash is referred to as Factory_HASH. In Normal mode, by default, there is full debug access to the CPUs and system. The device may be erased and programmed as needed.
- **SECURE** – This is the stage of a secure device. Before transitioning to this stage, the Secure_HASH must have been blown in eFuse and a valid application code must have been programmed in the main flash. In this stage, the protection state is set to Secure, and Secure DAP access restrictions are deployed. A secure device will boot only after successful authentication of its flash boot and application code.

After an MCU is in the Secure life cycle stage, it cannot go back to the Normal stage. SFlash cannot be programmed in this stage. The debug ports may be disabled depending on user preferences, so it is not possible to reprogram or erase the device with a hardware programmer/debugger. At this point, the firmware can only be updated by invoking a bootloader, which must be provided as part of device firmware.

Access restrictions in the SECURE state can be controlled by writing to the following eFuses:
- EFUSE_DATA_SECURE_ACCESS_RESTRICT0
- EFUSE_DATA_DEAD_ACCESS_RESTRICT1

Code should be tested in Normal and Secure with Debug stages before advancing to this stage. This is to prevent a configuration error that can cause the device to be inaccessible for programming and therefore, become unusable.

- **SECURE_WITH_DEBUG** – This is similar to the Secure stage, except that Normal access restrictions are applied to enable debugging. In this stage, a valid and secure flash boot code must have been programmed into the supervisory flash (SFlash) and its authentication code written to eFuse. Devices that are in the Secure with Debug stage cannot be changed back to either Secure or Normal stage.

- **RMA** – Customers can transition the device to the RMA stage (from Secure) when they want Cypress to perform failure analysis on the device. The customer should erase all sensitive data (including firmware) before invoking the system call that transitions the device to RMA. Secure erase should be performed by calling EraseRow/EraseSubSector/EraseSector/EraseAll SROM APIs five times repeatedly on the secure FLASH region before converting the device to RMA. See the Nonvolatile Memory Programming chapter on page 94 for more details on these SROM APIs.

When invoking the system call to transition to RMA, the customer must provide a certificate that authorizes Cypress to transition the device with a specific Unique ID to the RMA life cycle stage. The certificate will be signed by the customer using the same private key that is used to sign the user application image. The verification of the signature uses the same algorithm used by flash boot to authenticate the user application code. The same public key (injected by the OEM) stored in SFlash is used for the verification.

When a device is reset in the RMA life cycle stage, the boot will set access restrictions such that the DAP has access only to System AP and IPC MMIO registers for making system calls, and adequate RAM for communication. It will then wait for the “Open for RMA” system call from the DAP along with the certificate of authorization. This is the same certificate used in transitioning the device to RMA. The boot process will not initiate any firmware until it successfully executes the “Open for RMA” command. After the command is successful, the device will behave as though it were in the Virgin life cycle stage, but it cannot be transitioned to Virgin or any other stage. The life cycle stage stored in eFuse cannot be changed from RMA. Every time the device is reset, it must execute the “Open for RMA” command successfully before the device can be used.

A powered PSoC 6 MCU also has a volatile protection state that reflects its life cycle stage. The protection state is determined on boot by reading the eFuse values. More protection states exist than there are life cycle stages. Figure 15-2 illustrates the protection state transitions.
15.2 Device Security

### Protection State Transitions

- **UNKNOWN**
  - Transition is governed by the life cycle stage set by eFuse

- **VIRGIN**
- **NORMAL**
- **SECURE**
- **DEAD**

**Figure 15-2. Protection State Transitions**

Protection state is defined by the STATE field of the CPUSS_PROTECTION register.

- **STATE is 0**: UNKNOWN state.
- **STATE is 1**: VIRGIN state.
- **STATE is 2**: NORMAL state.
- **STATE is 3**: SECURE state.
- **STATE is 4**: DEAD state.

The CPUSS_PROTECTION register can be written only to affect the transitions defined in Figure 15-2. Any value written to this register that does not represent a transition in Figure 15-2 is rejected in hardware. A life cycle stage change (by writing to eFuse) does not immediately affect a protection state change. After writing the NORMAL, SECURE_WITH_DEBUG, or SECURE state in the eFuse, a reboot is required for the change of life cycle stage to take effect on the protection state.

The number of life cycle stages are fewer than the number of protection states. The additional protection states are:

- **UNKNOWN** – A device comes out of reset in this state. The ROM boot code needs to run through its courses (reading eFuses and checking integrity) to determine the life cycle stage of the device and select the proper protection state.
- **DEAD** – A device will enter the DEAD protection state when a corruption/error is detected in the boot process. In DEAD protection state, the system will not attempt to start any flash firmware and may restrict access to system resources to shield secure/sensitive information. Access restrictions in DEAD mode are controlled by EFUSE_DATA_SECURE_ACCESS_RESTRICT0 and EFUSE_DATA_SECURE_ACCESS_RESTRICT1 eFuses.

### Flash Security

PSoC 6 MCUs include a flexible flash-protection system that controls access to flash memory. This feature is designed to secure proprietary code, but it can also be used to protect against inadvertent writes to the bootloader portion of flash.

Flash memory is organized in sectors. Flash protection is provided by a shared memory protection unit (SMPU). The SMPU is intended to distinguish between different protection contexts and to distinguish secure from non-secure accesses.

For more details, see the Protection Units chapter on page 62.

#### 15.2.3 Hardware-Based Encryption

The PSoC 6 MCU has a cryptographic block (Crypto) that provides hardware implementation and acceleration of cryptographic functions. It implements symmetric key encryption and decryption, hashing, message authentication, random number generation (pseudo and true), and cyclic redundancy checking. It can work with internal as well as external memory. See the Cryptographic Function Block (Crypto) chapter on page 81 and Serial Memory Interface (SMIF) chapter on page 257 for more details.

#### 15.2.2 Flash Security

PSoC 6 MCUs include a flexible flash-protection system that controls access to flash memory. This feature is designed to
This section encompasses the following chapters:

- Power Supply and Monitoring chapter on page 120
- Device Power Modes chapter on page 128
- Backup System chapter on page 139
- Clocking System chapter on page 146
- Reset System chapter on page 161
- I/O System chapter on page 164
- Watchdog Timer chapter on page 186
- Trigger Multiplexer Block chapter on page 197
- Energy Profiler chapter on page 202
Top Level Architecture

System-Wide Resources Block Diagram

System Resources

Power
- Sleep Control
  - POR
  - BOD
  - OVP
  - LVD
  - REF
  - PWRSYS-LP/ULP
- Buck

Clock
- Clock Control
  - ILO
  - WDT
  - IMO
  - ECO
  - PLL
  - CSV
  - PLL

Reset
- Reset Control
  - XRES

Backup
- Backup Control
  - RTC
  - BREG
  - WCO

Power Modes
- Active/Sleep
- LPACTIVE/LPSLEEP
- Deep Sleep
- Hibernate
- Backup
16. Power Supply and Monitoring

The PSoC 6 MCU family supports an operating voltage range of 1.7 V to 3.6 V. It integrates multiple regulators including an on-chip single input multiple output (SIMO) buck converter to power the blocks within the device in various power modes. The device supports multiple power supply rails – $V_{DDD}$, $V_{DDA}$, $V_{DDIO}$, and $V_{BACKUP}$ – enabling the application to use a dedicated supply for different blocks within the device. For instance, $V_{DDA}$ is used to power analog peripherals such as ADC and opamps.

In addition, the device supports multiple supply rails and regulators for the BLE subsystem. These supply rails and regulators support various BLE power modes and states.

The PSoC 6 MCU family supports power-on-reset (POR), brownout detection (BOD), over-voltage protection (OVP), and low-voltage-detection (LVD) circuit for power supply monitoring and failure protection purposes.

16.1 Features

The power supply subsystem of the PSoC 6 MCU supports the following features:

- Operating voltage range of 1.7 V to 3.6 V
- User-selectable core logic operation at either 1.1 V or 0.9 V
- Three independent supply rails ($V_{DDD}$, $V_{DDA}$, and $V_{DDIO}$) for PSoC core peripherals and one independent supply rail ($V_{BACKUP}$) for backup domain
- Multiple on-chip regulators
  - One low-dropout (LDO) regulator to power peripherals in Active power mode
  - One SIMO buck converter with two outputs
  - Multiple low-power regulators to power peripherals operating in different low-power modes
  - Three LDOs powering various blocks in the BLE subsystem
- Two BOD circuit ($V_{DDD}$ and $V_{CCD}$) in all power modes except Hibernate mode
- LVD circuit to monitor $V_{DDD}$, $V_{AMUXA}$, $V_{AMUXB}$, $V_{BACKUP}$, or $V_{DDIO}$
- One OVP block monitoring $V_{CCD}$
16.2 Architecture

Figure 16-1. Power System Block Diagram

Legend:
- Regulators (LDO or Buck)
- Deep Sleep power supply/logic
- Active mode power supply/logic
- Retention power supply/logic
- Backup power supply/logic
- External power pad
- External IO pad
- Internal power rails

16.3 Power Supply

16.3.1 Regulators Summary

16.3.1.1 Core Regulators

The device includes the following core regulators to power peripherals and blocks in various power modes.

Linear Core Regulator

The device includes a linear LDO regulator to power the Active and Sleep mode peripherals. The regulator generates the core voltage (VCCD) required for Active mode operation of the peripherals from VDDD. The regulator is capable of providing 0.9 V and 1.1 V for core operation. See Core Operating Voltage on page 124. The regulator is available in Active and Sleep power modes. This regulator implements two sub-modes – high-current and low-current modes. LINREG_LPMODE bit [24] of the PWR_CTL register selects between the two modes of operation. The high-current mode is the normal operating mode, that is, the device operates to its full capacity in Active or Sleep power modes. In the low-current mode, the current output from the regulator is limited. This mode implements the Low-Power Active and Sleep power modes. The low-current mode sets a limitation on the capabilities and availability of resources in the Low-Power Active and Sleep modes. For details, see the Device Power Modes chapter on page 128.

By default, the linear regulator is powered on reset. The regulator can be disabled by setting the LINREG_DIS bit [23] of the PWR_CTL register. Note that the linear regulator should be turned OFF only when the following conditions are satisfied:

- Switching buck regulator is ON, VBuck1 output is enabled and connected to VCCD externally
- The load current requirement of the device from the VCCD supply does not exceed 20 mA. This should be ensured by the firmware by disabling power consuming high-frequency peripherals and reducing the system clock frequency.

If the linear regulator is turned OFF without the above conditions satisfied, it will result in VCCD brownout and the device will reset.

Switching (Buck) Core Regulator

The device includes a switching (buck) core regulator. The buck regulator included is a single input multiple (two) output (SIMO) regulator that can generate two outputs (VBuck1 and VRF) from a single input supply (VDD_NS). The buck requires only one inductor to generate both outputs. However, it requires two external capacitors, one for each output. Use the VRF output to power the BLE subsystem (VDCDC). Note that the VBuck1 output is also available in the Deep Sleep device power mode.
The buck regulator can be enabled by setting the BUCK_EN bit [30] of the PWR_BUCK_CTL register. Both the outputs can be enabled/disabled individually using the BUCK_OUTFx_EN bit [31] of the PWR_BUCK_CTLx registers. The VBUCK1 output supports voltages from 0.85 V to 1.20 V. Use either 0.9 V or 1.1 V for the VCCD operation. The VRF output supports voltages from 1.15 V to 1.50 V. It is recommended to use 1.3 V for BLE transmit power levels up to 0 dBm and 1.5 V for transmit power levels up to +4 dBm. The output selection can be made using BUCK_OUTFx_SEL bits in the PWR_BUCK_CTLx registers. In addition, the VRF output enable/disable can be controlled by hardware (BLE subsystem). This is enabled by setting the BUCK_OUTF2_HW_SEL bit [30] of the PWR_BUCK_CTL2 register. If enabled, the BUCK_OUTF2_EN bit is ignored and the hardware signal will be used to control the VRF output. For this reason, use VRF output to power the BLE subsystem. This enables the BLE subsystem to control the VRF output through hardware. Note that VRF and VBUCK1 have load limitations. Refer to the device datasheet for maximum load supported by the supplies, individually and combined.

When used to power the core peripherals, the buck regulator provides better power efficiency than the linear regulator, especially at higher VDDD. However, the buck regulator has less load current capability than the linear regulator. Therefore, when using the buck regulator, take care not to overload the regulator by running only the necessary peripherals at a lower frequency in firmware. Overload conditions can cause the buck output to drop and result in a brownout reset. Refer to the device datasheet for the load limitations on the buck regulator, recommended settings when used for VCCD and VDCDC, and its efficiency characteristics. Follow these steps in firmware when switching to the buck regulator for core (VCCD) operation without causing a brownout.

1. Make sure VBUCK1 and VCCD pins are shorted externally on the board. If the BLE subsystem is used then VRF should be used for BLE and VBUCK1 should be used for VCCD.
2. Change the core supply voltage to 50 mV more than the final buck voltage. For instance, if the final buck voltage is 0.9 V, then set the LDO output to 0.95 V and 1.15 V for 1.1 V buck operation. Set the ACT_REG_TRIM bits[4:0] of the PWR_TRIM_PWRSYS_CTL register to '0x0B' to switch to 0.9 V and '0x1B' to switch to 1.1 V buck operation. This is discussed in Core Operating Voltage.
3. Reduce the device current consumption by reducing clock frequency and switching off blocks to meet the SIMO buck regulator’s load capacity.
4. Disable low-power mode regulators. Because the SIMO buck regulator is available in the Deep Sleep device power mode, other deep-sleep regulators can be powered down. This is done by setting the following bits in the PWR_CTL register:
   c. NWELL_REG_DIS bit [22] – Disables the nwell regulator.
5. Set the buck output to the desired value by writing ‘2’ (for 0.9 V) or ‘5’ (for 1.1 V) to the BUCK_OUTF1_SEL bits[2:0] of the PWR_BUCK_CTL register.
7. Wait for the SIMO buck regulator to start up and settle.
8. Disable the linear regulator by setting the LINREG_DIS bit[23] of the PWR_CTL register.

After transitioning to the SIMO buck regulator, do not switch back to the linear regulator mode to ensure proper device operation. This should happen once during powerup.
Core Operating Voltage

PSoC 6 MCUs can operate at either 0.9 V (nominal) or 1.1 V (nominal) core voltage. On reset, the core is configured to operate at 1.1 V by default. At 0.9 V, power consumption is less, but there are some limitations. The maximum operating frequency for all HFCLK paths should not exceed 50 MHz, whereas the peripheral and slow clock should not exceed 25 MHz.

Follow these steps to change the PSoC 6 MCU core voltage:

1. While transitioning to 0.9 V, reduce the operating frequency to be within the HFCLK and peri clock limits defined in the device datasheet. Turn off blocks, if required, to be within the maximum current consumption limit of the linear regulator at 0.9 V.

2. Set the ACT_REG_TRIM bits[4:0] of the PWR_TRIM_PWR_SYS_CTL register to ’0x07’ for 0.9 V or ’0x17’ for 1.1 V. For the SIMO buck regulator, set the BUCK_OUT1_SEL bits[2:0] of the PWR_BUCK_CTL register to ’0x02’ for 0.9 V and ’0x05’ for 1.1 V.

3. In the case of 1.1 V to 0.9 V transition, the time it takes to discharge or settle to the new voltage may depend on the load. So the system can continue to operate while the voltage discharges.

4. In the case of 0.9 V to 1.1 V transition, wait 9 µs (or 200 µs for SIMO) for the regulator to stabilize to the new voltage. The clock frequency can be increased after the settling delay.

Notes:
- Refer to the device datasheet for characterized numbers for the settling intervals and load current limitations.
- When changing clock frequencies, make sure to update wait states of RAM/ROM/FLASH. Refer to the CPU Subsystem (CPUSS) chapter on page 30 for details on the wait states.

Other Low-power Regulators

In addition to the core active regulators, the device includes multiple low-power regulators for powering Deep Sleep peripherals/logic (VCCDPDSL), digital retention logic/SRAM (VCCRET), and N-wells (VNWELL) in the device. Note that VNWELL is not shown in Figure 16-1 because this rail is used across the device for powering all the N-wells in the chip. These rails are shorted to VCCD in Active/LPACTIVE and Sleep/LPSLEEP power modes. VCCRET powers all the Active mode logic that needs to be in retention in Deep Sleep mode.

Note that none of these power rails are available in Hibernate mode. In Hibernate mode, all the hibernate logic and peripherals operate from VDDD directly and a Hibernate wakeup resets the device. For details, refer to the Device Power Modes chapter on page 128.

16.3.1.2 BLE Subsystem Regulators

In addition to the core regulators, the device supports multiple LDOs as part of the BLE subsystem. These regulators can be categorized into Active and deep-sleep regulators. The Active mode (BLE active mode) regulators power the BLE transceiver blocks such as radio, RXADC, TXDAC, VCO, LNA, and PA. The deep-sleep regulator powers the BLE logic with retention. The Active regulators are powered from VDDC, pin, which can be connected to an external supply or the VRF output of the buck core regulator. The deep-sleep regulator is powered from VCCD/VCCDPDSL. In addition, the BLE subsystem includes a power rail (VDDR_HVL), which powers the BLE I/Os and peripherals such as ECO. The VDDR_HVL should be connected to a bypass capacitor externally. The supply is generated internally.

For details on the BLE subsystem regulators, refer to the Bluetooth Low Energy Subsystem (BLESS) chapter on page 468.

16.3.2 Power Pins and Rails

Table 16-1 lists all the power supply pins available in the device. The supply rails running inside the device (VCCDPDSL, VCCRET, VDDBCK, and VNWELL) are derived from these external supply pins/rails.

Table 16-1. Supply Pins

<table>
<thead>
<tr>
<th>Supply Pin</th>
<th>Ground Pin</th>
<th>Voltage Range Supported</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD or VDDD</td>
<td>VSS or VSSD</td>
<td>1.7 V to 3.6 V</td>
<td>VDD is a single supply input for multiple supplies and VDDD is a digital supply input. Either of the pins will be present in a given package.</td>
</tr>
<tr>
<td>VDD_NS</td>
<td>VSS_NS</td>
<td>1.7 V to 3.6 V</td>
<td>Supply input to the SIMO buck regulator on-chip.</td>
</tr>
<tr>
<td>VCCD</td>
<td>VSS or VSSD</td>
<td>Capacitor (0.9 V or 1.1 V)</td>
<td>Direct core supply or bypass capacitor for the internal regulator (LDO).</td>
</tr>
<tr>
<td>VBUCK1</td>
<td>VSS or VSSD</td>
<td>Capacitor (0.9 V to 1.2 V)</td>
<td>Buck regulator's first output can be connected to VCCD externally or connected to the bypass capacitor (4.7 µF) for powering external components.</td>
</tr>
</tbody>
</table>
16.3.3 Power Sequencing Requirements

$V_{DDD}$, $V_{BACKUP}$, $V_{DDIO}$, and $V_{DDA}$ do not have any sequencing limitation and can establish in any order. The presence of $V_{DDA}$ without $V_{DD}$ or $V_{DDD}$ can cause some leakage from $V_{DDA}$. However, it will not drive any analog or digital output. All the $V_{DDA}$ pins in packages that offer multiple $V_{DDA}$ supply pins, must be shorted externally (on the PCB). Note that the system will not exit reset until both $V_{DDD}$ and $V_{DDA}$ are established. However, it will not wait for other supplies to establish.

16.3.4 Backup Domain

The PSoC 6 MCU offers an independent backup supply option ($V_{BACKUP}$). This rail powers a small set of peripherals that includes an RTC, WCO, and a small number of retention registers. This rail is independent of all other rails and can exist even when other rails are absent. As Figure 16-1 shows, this pin sources the $V_{DDBAK}$ rail in the device. The $V_{DDBAK}$ rail is connected to $V_{DDD}$ when no $V_{BACKUP}$ supply exists. For details on the backup domain, refer to the Backup System chapter on page 139.

16.3.5 Power Supply Sources

The PSoC 6 MCU offers power supply options that support a wide range of application voltages and requirements. $V_{DDD}$ input supports a voltage range of 1.7 V to 3.6 V. If the application voltage is in this range, then the PSoC 6 MCU ($V_{DDD}$) can be interfaced directly to the application voltage. In applications that have voltage beyond this range, a suitable PMIC (Buck or Boost or Buck-Boost) should be used to bring the voltage to this range.

Other supply rails and pins such as $V_{DDA}$, $V_{DDIO}$, and $V_{BACKUP}$ exist independent of $V_{DDD}$ and $V_{CCD}$.

16.4 Voltage Monitoring

The PSoC 6 MCU offers multiple voltage monitoring and supply failure protection options. This includes POR, BOD, LVD, and OVP.

16.4.1 Power-On-Reset (POR)

POR circuits provide a reset pulse during the initial power ramp. POR circuits monitor $V_{DDD}$ voltage. Typically, the POR circuits are not very accurate about the trip-point.

POR circuits are used during initial chip power-up and then disabled. Refer to the device datasheet for details on the POR trip-point levels.

16.4.2 Brownout-Detect (BOD)

The BOD circuit protects the operating or retaining logic from possibly unsafe supply conditions by applying reset to the device. The PSoC 6 MCU offers two BOD circuits – high-voltage BOD (HVBOD) and low-voltage BOD (LVBOD). The HVBOD monitors the $V_{DDD}$ voltage and LVBOD monitors the $V_{CCD}$ voltage. Both BOD circuits generate a reset if a voltage excursion dips below the minimum $V_{DDD}/V_{CCD}$ voltage required for safe operation (see the device datasheet for details). The system will not come out of RESET until the supply is detected to be valid again.

The HVBOD circuit guarantees a reset in Active, LPACTIVE, Sleep, LPSLEEP, and Deep Sleep power modes before the system crashes, provided the $V_{DDD}$ supply ramp satisfies the datasheet maximum supply ramp limits in that mode.

---

### Table 16-1. Supply Pins

<table>
<thead>
<tr>
<th>Supply Pin</th>
<th>Ground Pin</th>
<th>Voltage Range Supported</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{RF}$</td>
<td>$V_{SS}$ or $V_{SSD}$</td>
<td>Capacitor (1.15 V to 1.5 V)</td>
<td>Buck regulator’s second output; connect a bypass capacitor (10 μF) to the pin.</td>
</tr>
<tr>
<td>$V_{DDA}$</td>
<td>$V_{SSA}$</td>
<td>1.7 V to 3.6 V</td>
<td>Analog supply voltage.</td>
</tr>
<tr>
<td>$V_{DDIO}$</td>
<td>$V_{SSIO}$</td>
<td>1.7 V to 3.6 V</td>
<td>Additional I/O supply voltage.</td>
</tr>
<tr>
<td>$V_{BACKUP}$</td>
<td>$V_{SS}$ or $V_{SSD}$</td>
<td>1.4 V to 3.6 V</td>
<td>Backup domain supply voltage.</td>
</tr>
<tr>
<td>$V_{DDBAK}$</td>
<td>$V_{SS}$ or $V_{SSD}$</td>
<td>1.75 V to 1.95 V</td>
<td>Supply voltage for BLE I/O system and ECO; connect an external bypass capacitor to the pin.</td>
</tr>
<tr>
<td>$V_{DDCDC}$</td>
<td>$V_{SS}$ or $V_{SSD}$</td>
<td>1.05 V to 1.5 V</td>
<td>Supply voltage for the BLE transceiver; $V_{RF}$ should be connected externally.</td>
</tr>
<tr>
<td>$V_{DDOR}$</td>
<td>$V_{SS}$ or $V_{SSD}$</td>
<td>Capacitor (1.05 V to 1.5 V)</td>
<td>Supply voltage for various blocks in the BLE subsystem; connected to $V_{DDCDC}$ externally.</td>
</tr>
<tr>
<td>$V_{IND1}$</td>
<td>–</td>
<td>Inductor</td>
<td>Inductor connection for the internal buck regulator.</td>
</tr>
<tr>
<td>$V_{IND2}$</td>
<td>–</td>
<td>Inductor</td>
<td>Inductor connection for the internal buck regulator.</td>
</tr>
</tbody>
</table>

a. Refer to the device datasheet for exact range and recommended connections.
Power Supply and Monitoring

There is no BOD support in Hibernate mode. Applications that require BOD support should not use Hibernate mode and should disable it. Refer to the Device Power Modes chapter on page 128 for details.

The LVBO, operating on V_CCD, is not as robust as the HVBO. The limitation is because of the small voltage detection range available for LVBO on the minimum allowed V_CCD. In applications that supply V_CCD externally, the BOD should be implemented in the PMIC because the LVBO does not guarantee a safe operation of V_CCD.

For details on the BOD trip-points, supported supply ramp rate, and BOD detector response time, refer to the device datasheet.

16.4.3 Low-Voltage-Detect (LVD)

An LVD circuit monitors external supply voltage and accurately detects depletion of the energy source. The LVD generates an interrupt to cause the system to take preventive measures.

The LVD can be configured to monitor V_DD, V_AMUXA, V_AMUXB, or V_DDIO. The HVLVD1_SRCSEL bits [6:4] of the PWR_LVD_CTL register selects the source of the LVD. The LVD support up to 15 voltage levels (thresholds) to monitor between 1.2 V to 3.1 V. The HVLVD1_TRIPSEL bits [3:0] of the PWR_LVD_CTL register select the threshold levels of the LVD. LVD should be disabled before selecting the threshold. The HVLVD1_EN bit [7] of the PWR_LVD_CTL register can be used to enable or disable the LVD.

Whenever the voltage level of the supply being monitored drops below the threshold, the LVD generates an interrupt. This interrupt status is available in the SRSS_INTR register. HVLVD1 bit [1] of the SRSS_INTR register indicates a pending LVD interrupt. The SRSS_INTR_MASK register decides whether LVD interrupts are forwarded to the CPU or not.

Note that the LVD circuit is available only in Active, LPACTIVE, Sleep, and LPSLEEP power modes. If an LVD is required in Deep Sleep mode, then the device should be configured to periodically wake up from Deep Sleep mode using a Deep Sleep wakeup source. This makes sure an LVD check is performed during Active/LPACTIVE mode.

When enabling the LVD circuit, it is possible to receive a false interrupt during the initial settling time. Firmware can mask this by waiting for 8 µs after setting the HVLVD1_EN bit in the PWR_LVD_CTL register. The recommended firmware procedure to enable the LVD function is:

1. Ensure that the HVLVD1 bit in the SRSS_INTR_MASK register is 0 to prevent propagating a false interrupt.
2. Set the required trip-point in the HVLVD1_TRIPSEL field of the PWR_LVD_CTL register.
3. Configure the LVD edge (falling/rising/both) that triggers the interrupt by configuring HVLVD1_EDGE_SEL bits[1:0] of SRSS_INTR_CFG register. By default, the configuration disables the interrupt. Note: LVD logic may falsely detect a falling edge during Deep Sleep entry. This applies only when HVLVD1_EDGE_SEL is set to FALLING(2) or BOTH(3). Firmware can workaround this condition by disabling falling edge detection before entering Deep Sleep, and re-enabling it after exiting Deep Sleep.
4. Enable the LVD by setting the HVLVD1_EN bit in the PWR_LVD_CTL register. This may cause a false LVD event.
5. Wait at least 8 µs for the circuit to stabilize.
6. Clear any false event by setting the HVLVD1 bit in the SRSS_INTR register. The bit will not clear if the LVD condition is truly present.
7. Unmask the interrupt by setting the HVLVD1 bit in SRSS_INTR_MASK.

For details on supported LVD thresholds, refer to the device datasheet and the PWR_LVD_CTL register definition in the PSoC 63 with BLE Registers TRM.
16.4.4 Over-Voltage Protection (OVP)

The PSoC 6 MCU offers an over-voltage protection circuit that monitors the \( V_{CCD} \) supply. Similar to the BOD circuit, the OVP circuit protects the device from unsafe supply conditions by applying a reset. As the name suggests, the OVP circuit applies a device reset, when the \( V_{CCD} \) supply goes above the maximum allowed voltage. The OVP circuit can generate a reset in all device power modes except the Hibernate mode.

16.5 Register List

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWR_CTL</td>
<td>Power Mode Control register - controls the device power mode options and allows observation of current state</td>
</tr>
<tr>
<td>PWR_BUCK_CTL</td>
<td>Buck Control register - controls the VBUCK1 output and master buck enable</td>
</tr>
<tr>
<td>PWR_BUCK_CTL2</td>
<td>Buck Control register 2 - controls the VRF output</td>
</tr>
<tr>
<td>PWR_LVD_CTL</td>
<td>LVD Configuration register</td>
</tr>
<tr>
<td>SRSS_INTR</td>
<td>SRSS Interrupt register - shows interrupt requests from the SRSS peripheral</td>
</tr>
<tr>
<td>SRSS_INTR_MASK</td>
<td>SRSS Interrupt Mask register - controls forwarding of the interrupt to CPU</td>
</tr>
<tr>
<td>SRSS_INTR_SET</td>
<td>SRSS Interrupt Set register - sets interrupts; this register is used for firmware testing</td>
</tr>
<tr>
<td>SRSS_INTR_MASKED</td>
<td>SRSS Interrupt Masked register - logical AND of corresponding SRSS interrupt request (SRSS Interrupt register) and mask bits (SRSS Interrupt Mask register)</td>
</tr>
</tbody>
</table>
17. Device Power Modes

The PSoC 6 MCU can operate in six power modes. These modes are intended to minimize the average power consumption in an application. The power modes supported by PSoC 6 MCUs, in the order of decreasing power consumption, are:

- **Active** – all peripherals are available
- **Low-Power Active (LPACTIVE)** – most peripherals including the CPU are available, but with limited capability
- **Sleep** – all peripherals except the CPU are available
- **Low-Power Sleep (LPSLEEP)** – most peripherals except the CPU are available, but with limited capability
- **Deep Sleep** – only low-frequency peripherals are available
- **Hibernate** – device and I/O states are frozen and the device resets on wakeup

Active, Sleep, and Deep Sleep are standard Arm-defined power modes supported by the Arm CPUs and instruction set architecture (ISA). LPACTIVE, LPSLEEP, and Hibernate modes are additional low-power modes supported by PSoC 6 MCUs. LPACTIVE and LPSLEEP are similar to Active and Sleep modes, respectively; however, the high-current components are either frequency- or current-limited or OFF. The Hibernate mode is the lowest power mode in the PSoC 6 MCU and on wakeup, the CPU and all peripherals go through a reset.

17.1 Features

The PSoC 6 MCU power modes have the following features:

- All six power modes aimed at optimizing power consumption in an application
- LPActive mode with most peripherals, including the CPU, available for operation
- Low-power Deep Sleep mode with support for multiple wakeup sources and configurable amount of SRAM retention
- Ultra-low-power Hibernate mode with wakeup from I/O, comparator, and timer alarms

The power consumption in different power modes is controlled by using the following methods:

- Enabling and disabling clocks to peripherals
- Powering on/off clock sources
- Powering on/off peripherals and parts inside the PSoC 6 MCU
17.2 Architecture

Table 17-1 summarizes the power modes available in PSoC 6 MCUs, their description, and details on their entry and exit conditions.

Table 17-1. PSoC 6 MCU Power Modes

<table>
<thead>
<tr>
<th>Power Mode</th>
<th>Description</th>
<th>Entry Condition</th>
<th>Wakeup Sources</th>
<th>Wakeup Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active</td>
<td>Primary mode of operation; all peripherals are available (programmable).</td>
<td>Manual register write from LPACTIVE mode, wakeup from Sleep/Deep Sleep modes, and external resets, brownout, and power on resets.</td>
<td>Not applicable</td>
<td>Not applicable</td>
</tr>
<tr>
<td>Low-Power Active</td>
<td>Similar to Active mode; most peripherals are available with limited capability.</td>
<td>Manual register write from Active mode and wakeup from LPSLEEP/Deep Sleep modes.</td>
<td>Not applicable</td>
<td>Not applicable</td>
</tr>
<tr>
<td>Sleep</td>
<td>Both CPUs in Sleep mode; all other peripherals are available.</td>
<td>Manual register write from Active mode.</td>
<td>Any interrupt to CPU</td>
<td>Interrupt</td>
</tr>
<tr>
<td>Low-Power Sleep</td>
<td>Sleep mode equivalent to Low-Power Active mode.</td>
<td>Manual register write from LPACTIVE mode.</td>
<td>Any interrupt to CPU</td>
<td>Interrupt</td>
</tr>
<tr>
<td>Deep Sleep</td>
<td>All high-frequency clocks and peripherals are turned off. Low-frequency clock (32 kHz) and low-power analog and digital peripherals are available for operation and as wakeup sources. SRAM is retained (programmable).</td>
<td>Manual register write from Active or LPACTIVE modes.</td>
<td>GPIO interrupt, low-power comparator, SCB, CTBm, watchdog timer, and RTC alarmsa</td>
<td>Interrupt</td>
</tr>
<tr>
<td>Hibernate</td>
<td>GPIO states are frozen. All peripherals and clocks in the device are completely turned off except low-power comparator and backup domain. Wakeup is possible through WAKEUP pins, XRES, low-power comparator and RTC alarms. Device resets on wakeup.</td>
<td>Manual register write from Active or LPACTIVE modes.</td>
<td>WAKEUP pin, low-power comparator, watchdog timer, and RTC alarmsa</td>
<td>Reset</td>
</tr>
</tbody>
</table>

a. RTC (along with WCO) is part of the backup domain and is available irrespective of the device power mode. RTC alarms are capable of waking up the device from any power mode.
b. Watchdog timer is capable of generating a hibernate wakeup. See the Watchdog Timer chapter on page 186 for details.

17.2.1 Active and Sleep Modes

The Active and Sleep modes are the standard Arm-defined power modes supported by both Cortex-M4 and Cortex-M0+ cores.

In the Active mode, the CPU executes code along with all logic and memory powered. The firmware may decide to enable or disable specific peripherals and power domains depending on the application and power requirement. All the peripherals are available for use in Active mode. The device enters Active mode upon any device reset.

In the Sleep mode, the CPU clock is turned off and the CPU enters sleep. Note that in the PSoC 6 MCU, Cortex-M4 and Cortex-M0+ both support their own CPU sleep modes and each CPU can be in sleep independent of the state of the other CPU. But the device is said to be in Sleep mode, when both the cores are in CPU sleep. All other peripherals available in Active mode are also available in Sleep mode. Any peripheral interrupt, masked to the CPU, can wake up the CPU to Active mode.

17.2.2 Low-Power Active/Sleep Modes

Low-Power Active (LPACTIVE) mode is similar to Active mode with some performance tradeoffs made to achieve lower system current. These tradeoffs include reduced operating clock frequency, limited high-frequency clock sources, and lower core operating voltage. Table 17-5 provides the list of resources available in LPACTIVE mode along with the limitations.

To transition from Active mode to LPACTIVE mode, set the LINREG_LPMODE bit [24] of the PWR_CTL register. For the transition to be successful, the LPM_READY bit [5] of the PWR_CTL register should read ‘1’. Otherwise, the device remains in Active mode until the bit is set and transitions to LPACTIVE mode only after it is set. The LPM_READY bit provides the ready status of the device’s capability to enter low-power modes. In addition, PORBOD_LPMODE, BGREF_LPMODE, and VREFBUF_LPMODE bits of the PWR_CTL register can be used to move POR/BOD circuits, bandgap reference
circuit, and voltage reference buffer to low-power modes. Refer to the PSoC 6 with BLE Registers TRM for details.

Low-Power Sleep (LPSLEEP) relates to LPACTIVE mode in the same way as Sleep mode relates to Active mode. The peripherals available in LPACTIVE mode are also available in LPSLEEP mode, except the CPU.

17.2.3 Deep Sleep Mode

In Deep Sleep mode, all the high-speed clock sources are OFF. This in turn makes the high-speed peripherals unusable in Deep Sleep mode. However, low-speed clock sources and peripherals continue to operate, if configured and enabled by the firmware. In addition, the peripherals that do not need a clock or receive clock from their external interface (I²C or SPI slave) continue to operate, if configured for Deep Sleep operation. The PSoC 6 MCU provides an option to configure the amount of SRAM, in blocks of 32 KB, that must be retained during Deep Sleep mode.

Note that both Cortex-M0+ and Cortex-M4 can enter the Deep Sleep mode independently. However, the entire device enters Deep Sleep mode only when both the CPUs are in deep sleep. On wakeup, the CPU that was woken up enters Active/LPACTIVE mode and the other CPU will be in Deep Sleep mode. The system will enter Active/LPACTIVE mode. The device can enter Deep Sleep mode after the following conditions are met:

- The LPM_READY bit of the PWR_CTL register should read '1'. This ensures the device is ready to enter low-power modes. If the bit reads '0', then the device will enter normal CPU sleep instead of deep sleep until the bit is set, which instant the device automatically enters Deep Sleep mode, if requested.

- Both Cortex-M0+ and Cortex-M4 should be in deep sleep. This is achieved by setting the SLEEPDEEP bit [2] of the SCR register of both Cortex-M0+ and Cortex-M4.

- The HIBERNATE bit [31] of the PWR_HIBERNATE register should be cleared; otherwise, the device will enter Hibernate mode.

In this mode, the Active mode regulator is turned off and a lower power, Deep Sleep regulator sources all the peripherals active in Deep Sleep mode. Alternatively, the SIMO buck regulator can be used to power the Deep Sleep peripherals. See the Power Supply and Monitoring chapter on page 120 for details. Table 17-5 provides the list of resources available in Deep Sleep mode.

Interrupts from low-speed, asynchronous, or low-power analog peripherals can cause a CPU wakeup from Deep Sleep mode. Note that when a debugger is running on either core, the device enters Sleep mode instead of Deep Sleep mode on a Deep Sleep request.

PSoC 6 uses buffered writes. Therefore, writes to an MMIO register or memory can take few a cycles from the write instruction execution. The only way to ensure that the write operation is complete is by reading the same location after the write. It is recommended to follow a write by a read to the same location before executing a WFI/WFE instruction to enter Deep Sleep mode.

17.2.4 Hibernate Mode

Hibernate mode is the lowest power mode of the device when external supplies are still present and XRES is deasserted. It is intended for applications in a dormant state.

In this mode, both the Active mode regulator and deep-sleep regulator are turned off and GPIO states are frozen. Wakeup is facilitated through dedicated wakeup pins and a low-power comparator output. Note that the low-power comparator operating in Hibernate mode requires external voltages for comparison and wakeup event generation.

Internal references are not available in Hibernate mode. Optionally, RTC alarm from the backup domain or watchdog timer (16-bit free-running WDT) interrupt can generate a Hibernate wakeup signal. Set the MASK_HIBALARM bit [18] of the PWR_HIBERNATE register to enable the RTC alarm wakeup from Hibernate mode.

The device goes through a reset on wakeup. I/O pins are tristated upon wakeup (reset), unless they were explicitly frozen before entering the Hibernate mode. To differentiate between other system resets and a Hibernate mode wakeup, the TOKEN bits [7:0] of the PWR_HIBERNATE register can be used as described in the Low-power Mode Transitions on page 134. The PWR_HIBERNATE (except the HIBERNATE bit [31]) register along with the PWR_HIB_DATA register are retained through the Hibernate wakeup sequence and can be used by the application for retaining some content through the Hibernate wakeup sequence. Note that these registers are reset by other reset events. On a Hibernate wakeup event, the HIBERNATE bit [31] of the PWR_HIBERNATE register is cleared.

The brownout detect (BOD) block is not available in Hibernate mode. As a result, the device does not recover from a brownout event in Hibernate mode. Do not enter Hibernate mode in applications that require brownout detection, that is, applications where the supply is not stable. In addition, make sure the supply is stable for at least 250 μs before the device enters Hibernate mode. To prevent accidental entry into Hibernate mode in applications that cannot meet these requirements, an option to disable the Hibernate mode is provided. Set the HIBERNATE_DISABLE bit [30] of the PWR_HIBERNATE register to disable the Hibernate mode in the device. Note that this bit is a write-once bit during execution and is cleared only on reset. Note that the debug functionality will be lost and debugger will disconnect on entering Hibernate mode.
17.2.5 Other Operation Modes

In addition to the power modes discussed in the previous sections, there are two other states or modes the device can be in – Reset/OFF state and Backup domain. You do not need a firmware action to enter these states or an interrupt or wakeup event to exit them. The device may be in these states, if it is not in any of the modes described earlier. In fact, backup is not a device state but a power domain that can exist independent of the device power supply and reset sources.

17.2.5.1 Backup Domain

The PSoC 6 MCU offers an independent backup supply option that can be supplied through a separate Vbackup pin. For details on the backup domain and the powering options, refer to the Backup System chapter on page 139. This domain powers a real-time clock (RTC) block, WCO, and a small set of backup registers. Because the power supply to these blocks come from a dedicated Vbackup pin, these blocks continue to operate even when the device power is disconnected or held in reset. The RTC present in the backup domain provides an option to wake up the device from any power mode. The RTC can be clocked by an external crystal (WCO) or the internal low-speed oscillator (ILO). However, ILO is available only if the device is powered – the device should not be in the OFF or Reset state. Using ILO is not recommended for timekeeping purpose; however, it can be used for wakeup from Hibernate power mode.

17.2.5.2 Reset/OFF State

Reset is the device state when an external reset (XRES pin) is applied or when POR/BOD is asserted. Reset is not a power mode. During the Reset state, all the components in the device are powered down and I/Os are tristated, keeping the power consumption to a minimum.

The OFF state simply represents the device state with no power applied. Even in the device OFF state, the backup domain can continue to receive power (Vbackup pin) and run the peripherals present. The Reset and OFF states are discussed for completeness of all possible states the device can be in. These states can be used in a system to further optimize power consumption. For instance, the system can control the supply of the PSoC 6 MCU by enabling or disabling the regulator output powering the device.
17.3 Power Mode Transitions

Figure 17-1 shows various states the device can be in along with possible power mode transition paths. The transitions are described in detail in later sections.

Figure 17-1. Power Mode Transitions in PSoC 6 MCU
17.3.1 Power-up Transitions

Table 17-2 summarizes various power-up transitions, their type, triggers, and actions.

<table>
<thead>
<tr>
<th>Initial State</th>
<th>Final State</th>
<th>Type</th>
<th>Trigger</th>
<th>Actions</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFF</td>
<td>XRES</td>
<td>External</td>
<td>Power rail ( V_{DDD} ) ramps up above POR voltage level with XRES pin asserted.</td>
<td>1. All high-voltage logic is reset</td>
</tr>
</tbody>
</table>
|               | Reset       | External   | Power rail \( V_{DDD} \) ramps up above POR voltage level with XRES pin de-asserted. | 1. All high-voltage logic is reset  
2. Low-voltage (internal Active and Deep Sleep mode) regulators and references are ramped up  
3. All low-voltage logic (logic operating from internal regulators) is reset  
4. IMO clock is started |
| XRES          | Reset       | External   | XRES is de-asserted with \( V_{DDD} \) present and above POR level.      | 1. Low-voltage regulators and references are ramped up  
2. All low-voltage logic is reset  
3. IMO clock is started |
| Reset         | Active      | Internal   | Reset sequence completes. This transition can also be caused by internal resets. | 1. Clock is released to the system  
2. System reset is de-asserted  
3. CPU starts execution |

Device Power Modes
### 17.3.2 Low-power Mode Transitions

Table 17-3 discusses various low-power mode transitions.

Table 17-3. Low-power Mode Transitions

<table>
<thead>
<tr>
<th>Initial State</th>
<th>Final State</th>
<th>Type</th>
<th>Trigger</th>
<th>Actions</th>
</tr>
</thead>
</table>
| Active        | LPACTIVE    | Internal | Firmware action 1. Configure the system to not exceed the maximum load capability of the linear regulator low-power mode.  
2. Wait until the LPM_READ bit[5] of the PWRCTL register reads ‘1’, indicating the low-power circuits are ready.  
3. Set the following bits of the PWRCTL register, to put the corresponding circuit in low-power mode:  
   a. LinReg_LPMODE bit[24] – Linear regulator low-power mode;  
      Not required when using SIMO buck regulator.  
   c. BGREF_LPMODE bit[26] – Bandgap reference circuit low-power mode.  
4. Wait 1 µs for the circuits to enter low-power mode.  
5. Disable active reference by setting the ACT_REF_DIS bit[30] of the PWR_CTL register. | 1. Device is put into LPACTIVE mode with most peripherals available with limited capabilities. |
| LPACTIVE      | Active      | Internal | Firmware action 1. Clear the following bits of the PWR_CTL register to put the corresponding circuit in normal power mode:  
   a. LinReg_LPMODE bit[24] – Linear regulator low-power mode;  
      Not required when using the SIMO buck regulator.  
2. Wait 8 µs for the circuits to settle.  
3. Make sure the ACT_REF_OK bit[31] of the PWR_CTL reads ‘1’ for the active reference to be up and running.  
4. Clear the BGREF_LPMODE bit[26] of the PWR_CTL register for the bandgap reference to return to normal mode.  
5. Wait 1 µs for the bandgap reference to settle. | 1. Device is put into normal Active mode with all peripherals available with full capabilities. |
### Device Power Modes

#### Table 17-3. Low-power Mode Transitions

<table>
<thead>
<tr>
<th>Initial State</th>
<th>Final State</th>
<th>Type</th>
<th>Trigger</th>
<th>Actions</th>
</tr>
</thead>
</table>
| Active/LPACTIVE | Active/LPACTIVE| Internal   | Firmware action Execute WFI/WFE (on both Cortex-M4 and Cortex-M0+) but an interrupt arrives before entering the low-power mode. | 1. Device aborts entry to low-power mode.  
2. Services the interrupt and stays in Active/LPACTIVE mode. |
| Active/LPACTIVE | Sleep/LPSLEEP  | Internal   | Firmware action  
2. Optionally, set the SLEEPONEXIT bit [1] of the SCR register, if the CPU runs only on interrupts. When this bit is set, the CPU does not return to application code after the WFI/WFE instruction is executed. The CPU wakes up on any enabled (masked to CPU) interrupt or event and enters Sleep/Deep Sleep mode as soon as it exits the interrupt or services the event.  
3. Optionally, set the SEVONPEND bit [4] of the SCR register if the application must wake up the CPU from any pending interrupt. If this bit is set, any interrupt that enters a pending state wakes up the CPU. This includes all the disabled (unmasked) interrupts to CPU.  
4. Execute WFI/WFE instruction on both CPUs. | 1. CPU clocks are gated off  
2. CPU waits for an interrupt or event to wake it up. |
| Active/LPACTIVE | Deep Sleep     | Internal   | Firmware action Perform these steps to enter Deep Sleep mode (LPM_READY bit [5] of the PWR_CTL register should read ‘1’ before performing these steps):  
3. Optionally, set the SLEEPONEXIT bit [1] of the SCR register if the CPU runs only on interrupts. When this bit is set, the CPU does not return to application code after the WFI/WFE instruction is executed. The CPU wakes up on any enabled (masked to CPU) interrupt or event and enters Sleep/Deep Sleep mode as soon as it exits the interrupt or services the event.  
4. Optionally, set the SEVONPEND bit [4] of the SCR register if the application needs to wake up the CPU from any pending interrupt. If this bit is set, any interrupt that enters a pending state wakes up the CPU. This includes all the disabled (unmasked) interrupts to CPU.  
5. Read the SCR register before executing a WFI/WFE instruction to ensure the write operation is complete. PSoC 6 uses buffered writes and any write transfer just before executing WFI/WFE instruction should be followed by a read to the same memory location. This ensures that the write operation has taken effect before entering Deep Sleep mode. Execute WFI/WFE instruction on both CPUs.  
6. If no peripheral is active, the device enters Deep Sleep mode. Otherwise, it enters Sleep/LPSLEEP mode. | 1. CPU enters low-power mode.  
2. High-frequency clocks are shut down.  
3. I/O cells are frozen.  
4. Retention is enabled and non-retention logic is reset.  
5. Active regulator is disabled and deep-sleep regulator takes over. |
Perform these steps to enter Hibernate mode (LPM_READY bit [5] of the PWR_CTL register should read ‘1’ before performing these steps):

1. Set the TOKEN bits [7:0] of the PWR_HIBERNATE register (optional) and PWR_HIB_DATA register to some application-specific branching data that can be used on a wakeup event from Hibernate mode.
2. Set the UNLOCK bits [8:15] of the PWR_HIBERNATE register to 0x3A, this ungates writes to FREEZE and HIBERNATE bits of the PWR_HIBERNATE register.
3. Configure wakeup pins polarity (POLARITY_HIBPIN bits [23:20]), wakeup pins mask (MASK_HIBPIN bits [27:24]) and wakeup alarm mask (MASK_HIBALARM bit [18]) in the PWR_HIBERNATE register based on the application requirement.
4. Optionally, set the FREEZE bit [17] of the PWR_HIBERNATE register to freeze the I/O pins.
5. Set the HIBERNATE bit [31] of the PWR_HIBERNATE register to enter Hibernate mode.
6. Ensure that the write operation to the PWR_HIBERNATE register is complete by reading the PWR_HIBERNATE register. Otherwise, instead of entering Hibernate mode, the CPU may start executing instructions after the write instruction. When the write is followed by a WFI/WFE instruction, the WFI/WFE can prevent the write from taking effect. On completion of the, the device automatically enters Hibernate mode.

<table>
<thead>
<tr>
<th>Initial State</th>
<th>Final State</th>
<th>Type</th>
<th>Trigger</th>
<th>Actions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active/LPACTIVE</td>
<td>Hibernate</td>
<td>Internal</td>
<td>Firmware action</td>
<td>1. CPU enters low-power mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2. Both high-frequency and low-frequency clocks are shut down.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3. Retention is enabled and non-retention logic is reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>4. Both Active and deep-sleep regulators are powered down. The peripherals that are active in the Hibernate domain operate directly out of VDD.</td>
</tr>
</tbody>
</table>
17.3.3  Wakeup Transitions

Table 17-4 shows various wakeup transitions and actions associated with them.

Table 17-4.  Wakeup Transitions

<table>
<thead>
<tr>
<th>Initial State</th>
<th>Final State</th>
<th>Type</th>
<th>Trigger</th>
<th>Actions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sleep/ LPSLEEP</td>
<td>Active/ LPACTIVE</td>
<td>Internal/External</td>
<td>Peripheral interrupt</td>
<td>1. Clock to CPU is ungated.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Any peripheral interrupt</td>
<td>2. Peripheral interrupt is serviced by CPU.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Deep Sleep</td>
<td>Active/ LPACTIVE</td>
<td>Internal/External</td>
<td>Deep Sleep interrupt</td>
<td>1. Active regulator and references are enabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Any Deep Sleep interrupt</td>
<td>2. Retention is disabled and non-retention reset is de-asserted.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3. High-frequency clocks are turned on.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>4. I/O cells are unfrozen.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>5. CPU exits low-power mode and services the interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> If only one CPU wakes up from the Deep Sleep interrupt,</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>then the other CPU remains in the Deep Sleep state until its Deep</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Sleep interrupt wakes it up. However, the system will wake up to</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Active or LPACTIVE mode. Note that a Deep Sleep</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>interrupt can wake up either one or both CPUs depending on the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>WIC configuration for the CPU. See the Interrupts chapter on</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>page 47.</td>
</tr>
<tr>
<td>Hibernate</td>
<td>Reset</td>
<td>External</td>
<td>Wakeup pin, RTC</td>
<td>1. Device is reset and goes through a Reset to Active power-up</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>alarm, or low-power</td>
<td>transition.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>comparator output asserts</td>
<td>2. Optionally, read the TOKEN bits [7:0] of the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PWR_HIBERNATE and PWR_HIB_DATA registers for application-specific</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>branching from Hibernate wakeup.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3. Optionally, set the I/O drive modes, read the I/O frozen output,</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>and set the I/O output to the read value.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>4. Unfreeze the I/O cells by clearing the FREEZE bit [17] of the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PWR_HIBERNATE register.</td>
</tr>
</tbody>
</table>

17.4  Summary

Table 17-5 captures various device components and their availability during the device power modes/states.

Table 17-5.  Resources Available in Different Power Modes

<table>
<thead>
<tr>
<th>Component</th>
<th>Power Modes</th>
<th>Active</th>
<th>LPACTIVE&lt;sup&gt;a&lt;/sup&gt;</th>
<th>Sleep</th>
<th>LPSLEEP&lt;sup&gt;b&lt;/sup&gt;</th>
<th>Deep Sleep</th>
<th>Hibernate</th>
<th>XRES</th>
<th>Power Off with Backup</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core functions</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CPU</td>
<td></td>
<td>On</td>
<td>On</td>
<td>Sleep</td>
<td>Sleep</td>
<td>Retention</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>SRAM</td>
<td></td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>Retention</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>Flash</td>
<td></td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>High Speed Clock</td>
<td></td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>(IMO, ECO, PLL, FLL)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LVD</td>
<td></td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>ILO</td>
<td></td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>Peripherals</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMIF</td>
<td></td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>Retention</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>UDB</td>
<td></td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>SAR ADC</td>
<td></td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>CTBm</td>
<td></td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>On (lower GBW)</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
</tbody>
</table>
Device Power Modes

Table 17-5. Resources Available in Different Power Modes

<table>
<thead>
<tr>
<th>Component</th>
<th>Power Modes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Active</td>
</tr>
<tr>
<td>TCPWM</td>
<td>On</td>
</tr>
<tr>
<td>CSD</td>
<td>On</td>
</tr>
<tr>
<td>BLE</td>
<td>On</td>
</tr>
<tr>
<td>LCD</td>
<td>On</td>
</tr>
<tr>
<td>SCB</td>
<td>On</td>
</tr>
<tr>
<td>GPIO</td>
<td>On</td>
</tr>
<tr>
<td>Watchdog timer</td>
<td>On</td>
</tr>
<tr>
<td>Multi-Counter WDT</td>
<td>On</td>
</tr>
<tr>
<td>XRES</td>
<td>On</td>
</tr>
<tr>
<td>POR</td>
<td>On</td>
</tr>
<tr>
<td>BOD</td>
<td>On</td>
</tr>
<tr>
<td>Watchdog reset</td>
<td>On</td>
</tr>
<tr>
<td>WCO, RTC, alarms</td>
<td>On</td>
</tr>
</tbody>
</table>

\(^{a}\) In the LPACTIVE/LPSLEEP modes, the maximum device current should not exceed 25 mA (refer to the datasheet for min/max numbers). Firmware should enable/disable blocks and reduce the clock frequencies appropriately to ensure power consumption does not exceed the limit.

\(^{b}\) Only the SCB with Deep Sleep support is available in the Deep Sleep power mode; other SCBs are not available in the Deep Sleep power mode.

\(^{c}\) Watchdog interrupt can generate a Hibernate wakeup. See the Watchdog Timer chapter on page 186 for details.

17.5 Register List

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWR_CTL</td>
<td>Power Mode Control register – controls the device power mode options and allows observation of current state</td>
</tr>
<tr>
<td>PWR_HIBERNATE</td>
<td>Hibernate Mode register – controls various Hibernate mode entry/exit related options</td>
</tr>
<tr>
<td>PWR_HIB_DATA</td>
<td>Hibernate Mode Data register – data register that is retained through a hibernate wakeup sequence</td>
</tr>
<tr>
<td>CM4_SCS_SCR</td>
<td>Cortex-M4 System Control register – controls the CPU level Sleep/Deep Sleep decisions on WFI/WFE instruction execution</td>
</tr>
<tr>
<td>CM0P_SCS_SCR</td>
<td>Cortex-M0+ System Control register – controls the CPU level Sleep/Deep Sleep decisions on WFI/WFE instruction execution</td>
</tr>
</tbody>
</table>
18. Backup System

The Backup domain adds an “always on” functionality to PSoC 6 MCUs using a separate power domain supplied by a backup supply (V_BACKUP) such as a battery or supercapacitor. It contains a real-time clock (RTC) with alarm feature, supported by a 32768-Hz watch crystal oscillator (WCO), and power-management IC (PMIC) control.

Backup is not a power mode; it is a power domain with its own power supply, which can be active during any of the device power modes. For more details, see the Power Supply and Monitoring chapter on page 120 and Device Power Modes chapter on page 128.

18.1 Features

- Fully-featured RTC
  - Year/Month/Date, Day-of-Week, Hour : Minute : Second fields
  - All fields binary coded decimal (BCD)
  - Supports both 12-hour and 24-hour formats
  - Automatic leap year correction
- Configurable alarm function
  - Alarm on Month/Date, Day-of-Week, Hour : Minute : Second fields
  - Two independent alarms
- 32768-Hz WCO with calibration
- Automatic backup power switching
- Built-in supercapacitor charger
- External PMIC control
- 32-byte backup registers
18.2 Architecture

The Backup system includes an accurate WCO that can generate the clock required for the RTC with the help of an external crystal or external clock inputs. The RTC has a programmable alarm feature, which can generate interrupts to the CPU. An AHB-Lite interface provides firmware access to MMIO registers in the Backup domain.

An automatic backup power switch selects the VDDD supply required to run the blocks in the Backup domain – either VDDD (main power) or VBACKUP (backup battery/supercapacitor power).

The domain also has backup registers that can store 32 bytes of data and retain its contents even when the main supply (VDDD) is OFF as long as the backup supply (VBACKUP) is present. The Backup system can also control an external PMIC that supplies VDDD.

18.3 Power Supply

Power to the backup system (VDBAK) is automatically switched between VDDD (main supply) and VBACKUP (Backup domain supply). VBACKUP is typically connected to an independent supply derived from a battery or supercapacitor (see the Power Supply and Monitoring chapter on page 120 for more details).

There are no VBACKUP versus VDDD sequencing restrictions for the power selector switch. Either VBACKUP or VDDD may be removed during normal operation, and the Backup system will remain powered.

The VDBAK_CTL bitfield in the BACKUP_CTL register controls the behavior of the power selector switch. See the PSoC 6 with BLE Registers TRM for details of this register. Possible options are:

- VDBAK_CTL = 0 (Default mode): Selects VDDD when the brownout detector in the system resources is enabled and no brownout situation is detected (see the Power Supply and Monitoring chapter on page 120 for more details). Otherwise, it selects the highest supply among VDDD and VBACKUP.
- VDBAK_CTL = 1, 2, or 3: Always selects VBACKUP for debug purposes.

If a supercapacitor is connected to VBACKUP, the PSoC 6 MCU can charge the supercapacitor while VDDD is available. Supercapacitor charging can be enabled by writing “3C” to the EN_CHARG_KEY bitfield in the BACKUP_CTL register. Note that this feature is for charging supercapacitors only and cannot safely charge a battery. Do not write this key when VBACKUP is connected to a battery. Battery charging must be handled at the board level using external circuitry.

Note: If VDDD and VBACKUP are connected on the PCB, the Backup domain may require an explicit reset triggered by firmware using the RESET bitfield in the BACKUP_RESET register. This firmware reset is required if the VBACKUP supply was invalid during a previous power supply ramp-up or brownout event. It is not necessary to reset the Backup domain if the RES_CAUSE register indicates a non-power-related reset as the reset cause, or if the PSoC 6 MCU just woke from the Hibernate power mode and the supply is
assumed to have been valid the entire time. It is possible to
monitor the $V_{\text{BACKUP}}$ supply using an ADC attached to
AMUXBUS-A by setting the VBACKUP_MEAS bit in the
BACKUP_CTL register. Note that the $V_{\text{BACKUP}}$ signal is
scaled by 40 percent so it is within the supply range of the
ADC. See the SAR ADC chapter on page 439 for more
details on how to connect the ADC to AMUXBUS-A.

18.4 Clocking

The RTC primarily runs from a 32768-Hz clock, after it is
scaled down to one-second ticks. This clock signal can
come from either of these internal sources:

- Watch-crystal oscillator (WCO). This is a high-accuracy
clock generator that is suitable for RTC applications and
requires a 32768-Hz external crystal populated on the
application board. WCO can also operate without
crystal, using external clock/sine wave inputs. These
additional operating modes are explained later in this
section. WCO is supplied by the Backup domain and can
therefore run without VDDD present.

- Alternate Backup Clock (ALTBAK): This option allows the
use of LFCLK generated by the System Resources
Subsystem (SRSS) as the Backup domain clock. Note
that LFCLK is not available in all device power modes or
when the VDDD is removed. (See the Device Power
Modes chapter on page 128 for more detail.)

Clock glitches can propagate into the Backup system
when LFCLK is enabled or disabled by the SRSS. In
addition, LFCLK may not be as accurate as WCO
depending on the actual source of LFCLK. Because of
these reasons, LFCLK is not recommended for RTC
applications. Also, if the WCO is intended as the clock
source then choose it directly instead of routing through
LFCLK.

For more details on these clocks and calibration, see the
Clocking System chapter on page 146.

The RTC clock source can be selected using the CLK_SEL
bitfield in the BACKUP_CTL register. The WCO_EN bit in
the BACKUP_CTL register can be used to enable or disable
the WCO. If the WCO operates with an external crystal,
make sure the WCO_BYPASS bit in the BACKUP_CTL
register is cleared before enabling the WCO. In addition, the
PRESCALER bitfield in BACKUP_CTL must be configured
for a prescaler value of 32768.

Note: External crystal and bypass capacitors of proper
values must be connected to WCO_IN and WCO_OUT and
pins. See the device datasheet for details of component
values and electrical connections. In addition, GPIOs must
be configured for WCO_OUT and WCO_IN signals. See the
I/O System chapter on page 164 to know how to configure
the GPIOs.

18.4.1 WCO with External Clock/Sine
Wave Input

The WCO can also operate from external clock/sine wave
inputs. In these modes, WCO must be bypassed by setting
the WCO_BYPASS bit in the BACKUP_CTL register before
enabling the WCO. Also, GPIOs must be configured for
WCO_OUT and WCO_IN signals (in Analog mode). The
external clock/sine wave input modes, prescaler settings,
and electrical connections are as follows:

- 32768-Hz external clock mode: In this mode, WCO_IN is
floating and WCO_OUT is externally driven by a 32768-
Hz square wave clock toggling between ground and
VDDD supply levels. In this configuration, the WCO_OUT
pin functions as a digital input pin for the external clock.
The PRESCALER bitfield in BACKUP_CTL must be
configured for a prescaler value of 32768.

- 60-Hz external clock mode: This mode can be used for
deriving a clock from the 60-Hz AC mains supply. In this
mode, WCO_OUT is floating and WCO_IN is driven with
an external sine wave with zero DC offset, derived from
the 60-Hz/120-V mains through a 100:1 capacitive
divider. For example, a suitable capacitive divider can be
formed by connecting a 220-pF/6-V capacitor between
WCO_IN and ground, and a 2.2-pF/200-V capacitor
between WCO_IN and the 60-Hz/120-V mains input.
The PRESCALER bitfield in BACKUP_CTL must be
configured for a prescaler value of 60.

- 50-Hz external clock mode: This mode is similar to the
60-Hz mode, and can be used for 50-Hz/220-V mains
standard. The capacitive divider explained previously
can be modified to fit this type of supply by having a 1-pF
/250-V capacitor between WCO_IN and the mains input.
The PRESCALER bitfield in BACKUP_CTL must be
configured for a prescaler value of 50.

18.4.2 Calibration

The absolute frequency of the clock input can be calibrated
using the BACKUP_CAL_CTL register. Calibration only
works when the PRESCALER bitfield in BACKUP_CTL is
set to 32768.

CALIB_VAL is a 6-bit field in the BACKUP_CAL_CTL
register that holds the calibration value for absolute
frequency (at a fixed temperature). One bit of this field
translates into 128 ticks to be added or removed from the
clock count. Therefore, each bit translates to a change of
1.085 ppm ($= 128/(60*60*32768)$).

The CALIB_SIGN field in the BACKUP_CAL_CTL register
controls whether the ticks are added (it takes fewer clock
ticks to count one second) or subtracted (it takes more clock
ticks to count one second).

For more information, see the BACKUP_CAL_CTL register
in the PSoC 63 with BLE Registers TRM.
18.5 Reset

The PSoC 6 MCU reset sources that monitor device power supply such as power-on reset (POR) and brownout reset (BOD) cannot reset the backup system as long as the backup supply ($V_{DDBAK}$) is present. Moreover, internal and external resets such as watchdog timer (WDT) reset and XRES cannot reset the backup system. The backup system is reset only when:

- all the power supplies are removed from the Backup domain, also known as a "cold-start".
- the firmware triggers a Backup domain reset using the RESET bitfield in the BACKUP_RESET register.

18.6 Real-Time Clock

The RTC consists of seven binary coded decimal (BCD) fields and one control bit as follows:

Table 18-1. RTC Fields

<table>
<thead>
<tr>
<th>Bitfield Name</th>
<th>Number of Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTC_SEC</td>
<td>7</td>
<td>Calendar seconds in BCD, 0-59</td>
</tr>
<tr>
<td>RTC_MIN</td>
<td>7</td>
<td>Calendar minutes in BCD, 0-59</td>
</tr>
<tr>
<td>CTRL_12HR</td>
<td>1</td>
<td>Select the 12-hour or 24-hour mode: 1=12HR, 0=24HR</td>
</tr>
<tr>
<td>RTC_DAY</td>
<td>3</td>
<td>Calendar day of the week in BCD, 1-7</td>
</tr>
<tr>
<td>RTC_DATE</td>
<td>6</td>
<td>Calendar day of the month in BCD, 1-31</td>
</tr>
<tr>
<td>RTC_MON</td>
<td>4</td>
<td>Calendar month in BCD, 1-12</td>
</tr>
<tr>
<td>RTC_YEAR</td>
<td>8</td>
<td>Calendar year in BCD, 0-99 (Can be used to represent years 2000-2099)</td>
</tr>
</tbody>
</table>

BCD encoding indicates that each four-bit nibble represents one decimal digit. Constant bits are omitted in the RTC implementation. For example, the maximum RTC_SEC is 59, which can be represented as two binary nibbles 0101b 1001b. However, the most significant bit is always zero and is therefore omitted, making the RTC_SEC a 7-bit field.

The RTC supports both 12-hour format with AM/PM flag, and 24-hour format for "hours" field. The RTC also includes a "day of the week" field, which counts from 1 to 7. You should define which weekday is represented by a value of ‘1’.

The RTC implements automatic leap year correction for the Date field (day of the month). If the Year is divisible by 4, the month of February (Month=2) will have 29 days instead of 28. When the year reaches 2100 - the Year field rolls over from 99 to 00 - the leap year correction will be wrong (2100 is flagged as a leap year which it is not); therefore, an interrupt is raised to allow the firmware to take appropriate actions. This interrupt is called the century interrupt.

User registers containing these bitfields are BACKUP_RTC_TIME and BACKUP_RTC_DATE. See the corresponding register descriptions in the PSoC 63 with BLE Registers TRM for details. As the user registers are in the high-frequency bus-clock domain and the actual RTC registers run from the low-frequency 32768-Hz clock, reading and writing RTC registers require special care. These processes are explained in the following section.

18.6.1 Reading RTC User Registers

To start a read transaction, the firmware should set the READ bit in the BACKUP_RTC_RW register. When this bit is set, the RTC registers will be copied to user registers and frozen so that a coherent RTC value can safely be read by the firmware. The read transaction is completed by clearing the READ bit.

The READ bit cannot be set if:

- RTC is still busy with a previous operation (that is, the RTC_BUSY bit in the BACKUP_STATUS register is set)
- WRITE bit in the BACKUP_RTC_RW register is set

The firmware should verify that the above bits are not set before setting the READ bit.

18.6.2 Writing to RTC User Registers

When the WRITE bit in the BACKUP_RTC_RW register is set, data can be written into the RTC user registers; otherwise, writes to the RTC user registers are ignored. When all the RTC writes are done, the firmware must clear the WRITE bit for the RTC update to take effect. After the
WRITE bit is cleared, the hardware will copy all the new data on one single WCO clock edge to ensure coherency to the actual RTC registers.

The WRITE bit cannot be set if:

- RTC is still busy with a previous operation (that is, the RTC_BUSY bit in the BACKUP_STATUS register is set)
- READ bit in the BACKUP_RTC_RW register is set

The firmware should make sure that the values written to the RTC fields form a coherent legal set. The hardware does not check the validity of the written values. Writing illegal values results in undefined behavior of the RTC.

When in the middle of an RTC update with the WRITE bit set, and a brownout, reset, or entry to Deep Sleep or Hibernate mode occurs, the write operation will not be complete. This is because the WRITE bit will be cleared by a reset, and the RTC update is triggered only when this bit is cleared by a WRITE transaction. If the write operation is in progress (RTC_BUSY), data corruption can occur if the system is reset or enters Deep Sleep or Hibernate mode.

18.7 Alarm Feature

The Alarm feature allows the RTC to be used to generate an interrupt, which may be used to wake up the system from Sleep, Deep Sleep, and Hibernate power modes.

The Alarm feature consists of six fields corresponding to the fields of the RTC: Month/Date, Day-of-Week, and Hour : Minute : Second. Each Alarm field has an enable bit that needs to be set to enable matching; if the bit is cleared, then the field will be ignored for matching.

The Alarm bitfields are as follows:

Table 18-2. Alarm Bitfields

<table>
<thead>
<tr>
<th>Bitfield Name</th>
<th>Number of Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALARM_SEC</td>
<td>7</td>
<td>Alarm seconds in BCD, 0-59</td>
</tr>
<tr>
<td>ALARM_SEC_EN</td>
<td>1</td>
<td>Alarm second enable: 0=disable, 1=enable</td>
</tr>
<tr>
<td>ALARM_MIN</td>
<td>7</td>
<td>Alarm minutes in BCD, 0-59</td>
</tr>
<tr>
<td>ALARM_MIN_EN</td>
<td>1</td>
<td>Alarm minutes enable: 0=disable, 1=enable</td>
</tr>
<tr>
<td>ALARM_HOUR</td>
<td>6</td>
<td>Alarm hours in BCD, value depending on the 12-hour or 24-hour mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>In 12-hour mode, bit ALARM_HOUR[5] = 0 for AM and 1 for PM, bits ALARM_HOUR[4:0] = 1–12</td>
</tr>
<tr>
<td></td>
<td></td>
<td>In 24-hour mode, bits ALARM_HOUR[5:0] = 0–23</td>
</tr>
<tr>
<td>ALARM_HOUR_EN</td>
<td>1</td>
<td>Alarm hour enable: 0=disable, 1=enable</td>
</tr>
<tr>
<td>ALARM_DAY</td>
<td>3</td>
<td>Calendar day of the week in BCD, 1-7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>You should define the meaning of the values</td>
</tr>
<tr>
<td>ALARM_DAY_EN</td>
<td>1</td>
<td>Alarm day of the week enable: 0=disable, 1=enable</td>
</tr>
<tr>
<td>ALARM_DATE</td>
<td>6</td>
<td>Alarm day of the month in BCD, 1-31</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Leap year corrected</td>
</tr>
<tr>
<td>ALARM_DATE_EN</td>
<td>1</td>
<td>Alarm day of the month enable: 0=disable, 1=enable</td>
</tr>
<tr>
<td>ALARM_MON</td>
<td>4</td>
<td>Alarm month in BCD, 1-12</td>
</tr>
<tr>
<td>ALARM_MON_EN</td>
<td>1</td>
<td>Alarm month enable: 0=disable, 1=enable</td>
</tr>
<tr>
<td>ALM_EN</td>
<td>1</td>
<td>Master enable for alarm.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Alarm is disabled. Fields for date and time are ignored.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Alarm is enabled. If none of the date and time fields are enabled, then this alarm triggers once every second.</td>
</tr>
</tbody>
</table>

If the master enable (ALM_EN) is set, but all alarm fields for date and time are disabled, an alarm interrupt will be generated once every second. Note that there is no alarm field for Year because the life expectancy of a chip is about 20 years and thus setting an alarm for a certain year means that the alarm matches either once or never in the lifetime of the chip.

The PSoC 6 MCU has two independent alarms. See the BACKUP_ALM1_TIME, BACKUP_ALM1_DATE, BACKUP_ALM2_TIME, and BACKUP_ALM2_DATE registers in the PSoC 63 with BLE Registers TRM for details.

Note that the alarm user registers, similar to RTC user registers, require certain special steps before read/write operations, as explained in sections Reading RTC User Registers on page 142 and Writing to RTC User Registers on page 142.

Interrupts must be properly configured for the RTC to generate interrupts/wake up events. Also, to enable RTC interrupts to wake up the device from Hibernate mode, the MASK_HIBALARM bit in the PWR_HIBERNATE register must be set. See the Device Power Modes chapter on page 128 and Interrupts chapter on page 47 for details.
The BACKUP_INTR_MASK register can be used to disable certain interrupts from the backup system.

Table 18-3. Interrupt Mask Bits

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALARM1</td>
<td>Mask bit for interrupt generated by ALARM1</td>
</tr>
<tr>
<td>ALARM2</td>
<td>Mask bit for interrupt generated by ALARM2</td>
</tr>
<tr>
<td>CENTURY</td>
<td>Mask bit for century interrupt (interrupt generated when the Year field rolls over from 99 to 00)</td>
</tr>
</tbody>
</table>

The RTC alarm can also control an external PMIC as explained in the following section.

### 18.8 PMIC Control

The backup system can control an external PMIC that supplies $V_{DDO}$. PMIC enable is an active-high output that is available at a certain pin PMIC_Wakeup_Out. See the device datasheet for the location of this pin. This pin can be connected to the “enable” input of a PMIC.

Table 18-4 shows the bitfields in BACKUP_PMIC_CTL.

Table 18-4. PMIC Control Bits

<table>
<thead>
<tr>
<th>Bitfield Name</th>
<th>Number of Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>UNLOCK</td>
<td>8</td>
<td>This byte must be set to 0x3A for PMIC to be disabled. Any other value in this field will cause writes to PMIC_EN to be ignored. Do not change PMIC_EN in the same write cycle as setting/clearing the UNLOCK code; do these in separate write cycles.</td>
</tr>
<tr>
<td>POLARITY</td>
<td>1</td>
<td>Reserved for future use. Keep this bit at ‘1’.</td>
</tr>
<tr>
<td>PMIC_EN_OUTEN</td>
<td>1</td>
<td>Output enable of the PMIC_EN pin.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: PMIC_EN pin output is HI-Z. This allows the PMIC_EN pin to be used as a GPIO. The HI-Z condition is kept only if the UNLOCK key (0x3A) is present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: PMIC_EN pin output is enabled.</td>
</tr>
<tr>
<td>PMIC_ALWAYSEN</td>
<td>1</td>
<td>Override normal PMIC controls to prevent errant firmware from accidentally turning off the PMIC.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Normal operation; PMIC_EN and PMIC_OUTEN work as explained in their bitfield descriptions.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: PMIC_EN is forced set; PMIC_EN and PMIC_OUTEN are ignored. This bit is a write-once bit that cannot be cleared until the next Backup domain reset.</td>
</tr>
<tr>
<td>PMIC_EN</td>
<td>1</td>
<td>Enable external PMIC (hardware output available at pin PMIC_Wakeup_Out). This bit is enabled by default. This bit will only clear if the UNLOCK field was written correctly in a previous write operation and PMIC_ALWAYSEN = 0.</td>
</tr>
</tbody>
</table>

Note that two writes to the BACKUP_PMIC_CTL register are required to change the PMIC_EN setting. The first write should update the desired settings (including the UNLOCK code) but should not change PMIC_EN or PMIC_EN_OUTEN. The second write must use the same bit values as the first one except desired PMIC_EN/PMIC_EN_OUTEN settings.

When the PMIC_EN bit is cleared by firmware, the external PMIC is disabled and the system functions normally until $V_{DDO}$ is no longer present (OFF with Backup mode). The firmware can set this bit if it does so before $V_{DDO}$ is actually removed. The time between firmware disabling the PMIC_EN bit and the actual removal of $V_{DDO}$ depends on the external PMIC and supply-capacitor characteristics.

Additionally, PMIC can be turned on by one of these events:

- An RTC Alarm/Century Interrupt
- A logic high input at the PMIC_Wakeup_In pin. See the device datasheet for the location of this pin. This allows a mechanical button or an external input from another device to wake up the system and enable the PMIC. The POLARITY bit in the BACKUP_PMIC_CTL register must be set to ‘1’ to use this feature. The same wakeup pin PMIC_Wakeup_In can wake up the device from
Hibernate mode. See the Device Power Modes chapter on page 128 for details.

Make sure that one or more of these events are configured properly, and a battery or supercapacitor is connected to $V_{\text{BACKUP}}$ with sufficient charge to power the backup system until one of these events occur. Otherwise, the PMIC may continue to be in the disabled state with the PSoC 6 MCU unable to enable it again.

18.9 Backup Registers

The Backup domain has eight registers (BACKUP_BREG0 to BACKUP_BREG7), which can be used to store 32 bytes of important information/flags. These registers retain their contents even when the main supply ($V_{\text{DD}}$) is off as long as backup supply ($V_{\text{BACKUP}}$) is present. These registers can also be used to store information that must be retained when the device enters Hibernate mode.

18.10 Register List

Table 18-5. Backup Registers

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BACKUP_CTL</td>
<td>Main control register (including power and clock)</td>
</tr>
<tr>
<td>BACKUP_RTC_RW</td>
<td>RTC read/write control register</td>
</tr>
<tr>
<td>BACKUP_STATUS</td>
<td>Status register</td>
</tr>
<tr>
<td>BACKUP_RTC_TIME</td>
<td>Calendar seconds, minutes, hours, and day of week</td>
</tr>
<tr>
<td>BACKUP_RTC_DATE</td>
<td>Calendar day of month, month, and year</td>
</tr>
<tr>
<td>BACKUP_ALM1_TIME</td>
<td>Alarm 1 seconds, minute, hours, and day of week</td>
</tr>
<tr>
<td>BACKUP_ALM1_DATE</td>
<td>Alarm 1 day of month, and month</td>
</tr>
<tr>
<td>BACKUP_ALM2_TIME</td>
<td>Alarm 2 seconds, minute, hours, and day of week</td>
</tr>
<tr>
<td>BACKUP_ALM2_DATE</td>
<td>Alarm 2 day of month, and month</td>
</tr>
<tr>
<td>BACKUP_INTR</td>
<td>Interrupt request register</td>
</tr>
<tr>
<td>BACKUP_INTR_MASK</td>
<td>Interrupt mask register</td>
</tr>
<tr>
<td>BACKUP_INTR_MASKED</td>
<td>Interrupt masked request register</td>
</tr>
<tr>
<td>BACKUP_PMIC_CTL</td>
<td>PMIC control register</td>
</tr>
<tr>
<td>BACKUP_BREG0</td>
<td>Backup registers</td>
</tr>
<tr>
<td>BACKUP_BREG7</td>
<td></td>
</tr>
<tr>
<td>BACKUP_RESET</td>
<td>Reset register for the backup domain</td>
</tr>
</tbody>
</table>
19. Clocking System

PSoc 6 MCU provides flexible clocking options with on-chip crystal oscillators, phase lock loop, frequency lock loop, and supports multiple external clock sources.

19.1 Features

The PSoC 6 MCU clock system includes these resources:

- Three internal clock sources:
  - 8-MHz internal main oscillator (IMO)
  - 32-kHz internal low-speed oscillator (ILO)
  - Precision 32-kHz internal low-speed oscillator (PILO)

- Three external clock sources
  - External clock (EXTCLK) generated using a signal from an I/O pin
  - External 4–33.33 MHz crystal oscillator (ECO)
  - External 32-kHz watch crystal oscillator (WCO)

- One frequency lock loop (FLL) with 24–100 MHz output range
- One phase-locked loop (PLL) with 10.625–200 MHz output range
19.2 Architecture

Figure 19-1 gives a generic view of the clocking system in PSoC 6 MCUs.
19.3 Clock Sources

19.3.1 Internal Main Oscillator (IMO)

The IMO is an accurate, high-speed internal (crystal-less) oscillator that produces a fixed frequency of 8 MHz. The IMO output can be used by the PLL or FLL to generate a wide range of higher frequency clocks, or it can be used directly by the high-frequency root clocks.

When USB is present the USB Start-of-Frame (SOF) signal is used to trim the IMO to ensure that the IMO matches the accuracy of the USB SOF. The ENABLE_LOCK bitfield in the CR1 register of the USB block needs to be set for this feature to work.

The IMO is available only in (LP) Active and (LP) Sleep modes.

19.3.2 External Crystal Oscillator (ECO)

The PSoC 6 MCU contains an oscillator to drive an external 4-MHz to 33.33-MHz crystal. This clock source is built using an oscillator circuit in PSoC. The circuit employs an external crystal that needs to be populated on the external crystal pins of the PSoC 6 MCU.

The ECO can be enabled by using the CLK_ECO_CONFIG ECO_EN register bitfields.

19.3.2.1 ECO Trimming

The ECO supports a wide variety of crystals and ceramic resonators with the nominal frequency range specification of $f = 4 \text{ MHz} - 33.333 \text{ MHz}$. The crystal manufacturer typically provides numerical values for parameters, namely the maximum drive level (DL), the equivalent series resistance (ESR), and the parallel load capacitance ($C_L$). These parameters can be used to calculate the transconductance ($g_m$) and the maximum peak to peak ($V_{pp}$).

Max peak to peak value: $V_{pp} = 2 \times \sqrt{\frac{2 \times DL \times ESR}{4\pi f \times C_L}}$

Transconductance: $g_m = 4 \times 5 \times (2\pi f \times C_L)^2 \times ESR$

ECO does not support $V_{pp}$ less than 0.5 V. Similarly, $g_m$ cannot be greater than or equal to 18 mA/V.

The following fields are found in the CLK_TRIM_ECO_CTL register. The Amplitude trim (ATRIM) and WDTRIM settings control the trim for amplitude of the oscillator output. ATRIM sets the crystal drive level when automatic gain control (AGC) is enabled (CLK_ECO_CONFIG.AGC_EN = 1). AGC must be enabled for $V_{pp} < 2 \text{ V}$ and disabled for all other cases.

**WARNING:** Take care when disabling AGC because driving a crystal beyond its rated limit can permanently damage the crystal.

Based on the $V_{pp}$ value, the ATRIM and WDTRIM values are set as shown in Table 19-1 and Table 19-2.

Table 19-1. ATRIM Settings

<table>
<thead>
<tr>
<th>$V_{pp}$</th>
<th>ATRIM</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{pp} &lt; 0.6 \text{ V}$</td>
<td>0x00</td>
</tr>
<tr>
<td>$V_{pp} &lt; 0.7 \text{ V}$</td>
<td>0x02</td>
</tr>
<tr>
<td>$V_{pp} &lt; 0.8 \text{ V}$</td>
<td>0x04</td>
</tr>
<tr>
<td>$V_{pp} &lt; 0.9 \text{ V}$</td>
<td>0x06</td>
</tr>
<tr>
<td>$V_{pp} &lt; 1.025 \text{ V}$</td>
<td>0x08</td>
</tr>
<tr>
<td>$V_{pp} &lt; 1.15 \text{ V}$</td>
<td>0x0A</td>
</tr>
<tr>
<td>$V_{pp} &lt; 1.275 \text{ V}$</td>
<td>0x0C</td>
</tr>
<tr>
<td>$V_{pp} &gt; 1.275 \text{ V}$</td>
<td>0x0E</td>
</tr>
</tbody>
</table>

Table 19-2. WDTRIM Settings

<table>
<thead>
<tr>
<th>$V_{pp}$</th>
<th>WDTRIM</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{pp} &lt; 0.6 \text{ V}$</td>
<td>0x00</td>
</tr>
<tr>
<td>$V_{pp} &lt; 0.8 \text{ V}$</td>
<td>0x02</td>
</tr>
<tr>
<td>$V_{pp} &lt; 1.0 \text{ V}$</td>
<td>0x04</td>
</tr>
<tr>
<td>$V_{pp} &gt; 1.0 \text{ V}$</td>
<td>0x06</td>
</tr>
</tbody>
</table>

The GTRIM sets up the trim for amplifier gain based on the calculated $g_m$, as shown in Table 19-3.

Table 19-3. GTRIM Settings

<table>
<thead>
<tr>
<th>$g_m$</th>
<th>GTRIM</th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_m &lt; 4.5 \text{ mA/V}$</td>
<td>0x01</td>
</tr>
<tr>
<td>$g_m = 4.5 \text{ mA/V}$</td>
<td>0x00</td>
</tr>
<tr>
<td>$g_m &gt; 4.5 \text{ mA/V}$</td>
<td>INT ($g_m / 4.5\text{mA/V}$)</td>
</tr>
</tbody>
</table>

RTRIM sets up the trim for filter characteristics based on the frequency, as shown in Table 19-4.

Table 19-4. RTRIM Settings

<table>
<thead>
<tr>
<th>Nominal Frequency $f$ (MHz)</th>
<th>RTRIM</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f &gt; 28.6 \text{ MHz}$</td>
<td>0x00</td>
</tr>
<tr>
<td>$28.6 \text{ MHz} \geq f &gt; 23.33\text{MHz}$</td>
<td>0x01</td>
</tr>
<tr>
<td>$23.33 \text{ MHz} \geq f &gt; 16.5 \text{ MHz}$</td>
<td>0x02</td>
</tr>
<tr>
<td>$16.5 \text{ MHz} \geq f$</td>
<td>0x03</td>
</tr>
</tbody>
</table>
FTRIM sets up the trim for filter characteristics based on ATRIM, as shown in Table 19-5.

### Table 19-5. FTRIM Settings

<table>
<thead>
<tr>
<th>Nominal Frequency f (MHz)</th>
<th>FTRIM</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATRIM &lt; 2</td>
<td>0x00</td>
</tr>
<tr>
<td>4 &gt; ATRIM ≥ 2</td>
<td>0x01</td>
</tr>
<tr>
<td>6 &gt; ATRIM ≥ 4</td>
<td>0x02</td>
</tr>
<tr>
<td>8 &gt; ATRIM ≥ 6</td>
<td>0x03</td>
</tr>
<tr>
<td>10 &gt; ATRIM ≥ 8</td>
<td>0x04</td>
</tr>
<tr>
<td>12 &gt; ATRIM ≥ 10</td>
<td>0x05</td>
</tr>
<tr>
<td>14 &gt; ATRIM ≥ 12</td>
<td>0x06</td>
</tr>
<tr>
<td>ATRIM ≥ 14</td>
<td>0x07</td>
</tr>
</tbody>
</table>

First, set up the trim values based on Table 19-1 through Table 19-5 and then enable the ECO. After the ECO is enabled, the CLK_ECO_STATUS register can be checked to ensure it is ready.

#### 19.3.3 External Clock (EXTCLK)

The external clock is a 4- to 33.33-MHz range clock that can be sourced from a signal on a designated I/O pin. This clock can be used as the source clock for either the PLL or FLL, or can be used directly by the high-frequency clocks.

When manually configuring a pin as an input to EXTCLK, the drive mode of the pin must be set to high-impedance digital to enable the digital input buffer. See the I/O System chapter on page 164 for more details. Consult the device datasheet to determine the specific pin used for EXTCLK.

#### 19.3.4 Alternate High-Frequency Clock (ALTHF)

ALTHF is an alternate high-frequency clock. This clock is generated outside of the clocking system described in this chapter. For PSoC 63, this clock is the ECO that is connected to the BLE subsystem. The ALTHF path allows routing the BLE ECO into the clocking system so that it can be used as a source for the PLL/FLL or directly as the source for the high-frequency clocks. For more information on this clock, consult the Bluetooth Low Energy Subsystem (BLESS) chapter on page 468.

#### 19.3.5 Internal Low-speed Oscillator (ILO)

The ILO operates with no external components and outputs a stable clock at 32.768 kHz nominal. The ILO is relatively low power and low accuracy. It is available in all power modes. If the ILO is to remain active in Hibernate mode, and across power-on-reset (POR) or brownout detect (BOD), the HVILO_BACKUP bit must be set in the CLK_ILO_CONFIG register.

The ILO can be used as the clock source for:
- **CLK_LF**: CLK_LF in turn can be used as a source for the backup domain (CLK_BAK). CLK_BAK runs the real-time clock (RTC). This can be useful if you do not wish to populate a WCO. Although the ILO is not suitable as an RTC due to its poor accuracy, it can be used as a HIBERNATE wakeup source using the wakeup alarm facility in the RTC. In this case, the VDDQ rail must be supplied during HIBERNATE for the ILO to run, and the HVILO_BACKUP bit must be set in the CLK_ILO_CONFIG register. CLK_LF is also the source of the MCWDT timers; see the Watchdog Timer chapter on page 186 for details.
- **DSI_Mux**: The ILO can be routed to the digital signal interconnect (DSI) mux and can then be routed as the source of the FLL, or directly as a source for one of the high-frequency clocks. However, this is not recommended due to the low accuracy of the ILO.

The ILO is always the source of the watchdog timer (WDT).

The ILO is enabled and disabled with the ENABLE bit of the CLK_ILO_CONFIG register. Always leave the ILO enabled as it is the source of the WDT.

If the WDT is enabled, the only way to disable the ILO is to first clear the WDT_LOCK bit in the WDT_CTL register and then clear the ENABLE bit in the CLK_ILO_CONFIG register. If the WDT_LOCK bit is set, any register write to disable the ILO will be ignored. Enabling the WDT will automatically enable the ILO.

The calibration counters described in Clock Calibration Counters on page 160 can be used to measure the ILO against a high-accuracy clock such as the ECO. This result can then be used to determine how the ILO must be adjusted. The ILO can be trimmed using the CLK_TRIM_ILO_CTL register. The trim step sizes are 1.5 percent of the ILO frequency.

#### 19.3.6 Precision Internal Low-speed Oscillator (PILO)

PILO is an additional source that can provide a more accurate 32.768-kHz clock than ILO when periodically calibrated using a high-accuracy clock such as the ECO. The PILO works in Deep Sleep and higher modes. It does not work in Hibernate mode.

The PILO can be used as the clock source for:
- **CLK_LF**: CLK_LF in turn can be used as a source for the backup domain (CLK_BAK). CLK_BAK runs the RTC. When Hibernate mode is entered or VDDQ is removed the PILO is disabled, which can lead to corruption of the RTC timers/counters. If this is unacceptable use the ILO or WCO. The PILO does not run in Hibernate mode.
- **DSI_Mux**: The PILO can be routed to the DSI mux and can then be routed as the source of the FLL, or directly as a source for one of the high-frequency clocks.
The PILO is enabled by first writing to the PILO_EN bit in the CLK_PILO_CONFIG register, then waiting 1 msec, and then writing ‘1’ to the PILO_RESET_N and PILO_CLK_EN bits of the same register. To disable the PILO, write ‘0’ to PILO_EN, CLK_PILO_CONFIG, and PILO_RESET_N at the same time.

Periodic calibration to a high-accuracy clock (such as ECO) is required to maintain accuracy. The calibration counters described in Clock Calibration Counters on page 160 can be used to measure the PILO against a high-accuracy clock such as the ECO. This result can then be used to determine how the PILO must be adjusted. The PILO can be adjusted in 8-Hz steps using the PILO_FFREQ field of CLK_PILO_CONFIG.

19.3.7 Watch Crystal Oscillator (WCO)

The WCO is a highly accurate 32.768-kHz clock source. It is the primary clock source for the RTC. The WCO can also be used as a source for CLK_LF.

The WCO can be enabled and disabled by setting the WCO_EN bit in the CTL register for the backup domain. The WCO can also be bypassed and an external 32.768-kHz clock can be routed on a WCO output pin. This is done by setting the WCO_BYPASS bit in the CTL register for the backup domain.

19.4 Clock Generation

19.4.1 Phase-Locked Loop (PLL)

The PSoC 6 MCU contains one PLL, which resides on Clock Path 1. It is capable of generating a clock output in the range 10.625–200 MHz; the input frequency must be between 4 and 64 MHz. This makes it possible to use the IMO to generate much higher clock frequencies for the rest of the system.

The PLL is configured following these steps:

**Note:** \( f_{\text{ref}} \) is the input frequency of the PLL, that is, the frequency of input clock, such as 8 MHz for the IMO.

1. Determine the desired reference clock frequency \( f_{\text{ref}} \) and output frequency \( f_{\text{out}} \). Calculate the reference (REFERENCE_DIV), feedback (FEEDBACK_DIV), and output (OUTPUT_DIV) dividers subject to the following constraints:
   a. PFD frequency (phase detector frequency). \( f_{\text{pd}} = \frac{f_{\text{ref}}}{\text{REFERENCE_DIV}} \). It must be in the range 4 MHz to 8 MHz. There may be multiple reference divider values that meet this constraint.
   b. VCO frequency. \( f_{\text{vco}} = f_{\text{pd}} \times \text{FEEDBACK_DIV} \). It must be in the range 170 MHz to 400 MHz. There may be multiple feedback divider values that meet this constraint with different REFERENCE_DIV choices.
   c. Output frequency. \( f_{\text{out}} = \frac{f_{\text{vco}}}{\text{OUTPUT_DIV}} \). It must be in the range 10.625 MHz to 200 MHz. Note that your device may not be capable of operating at this frequency; check the device datasheet. It may not be possible to get the desired frequency due to granularity; therefore, consider the frequency error of the two closest choices.
   d. Choose the best combination of divider parameters depending on the application. Some possible decision-making factors are: minimum output frequency error, lowest power consumption (lowest \( f_{\text{vco}} \)), or lowest jitter (highest \( f_{\text{vco}} \)).

2. Program the divider settings in the appropriate CLK_PLL_CONFIG register. Do not enable the PLL on the same cycle as configuring the dividers. Do not change the divider settings while the PLL is enabled.

3. Enable the PLL (CLK_PLL_CONFIG.ENABLE = 1). Wait at least 1 µs for PLL circuits to start.

4. Wait until the PLL is locked before using the output. By default, the PLL output is bypassed to its reference clock and will automatically switch to the PLL output when it is locked. This behavior can be changed using PLL_CONFIG.BYPASS_SEL. The status of the PLL can be checked by reading CLK_PLL_STATUS. This register contains a bit indicating the PLL has locked. It also contains a bit indicating if the PLL lost the lock status.

19.4.2 Frequency Lock Loop (FLL)

The PSoC 6 MCU contains one frequency lock loop (FLL), which resides on Clock Path 0. The FLL is capable of generating a clock output in the range 24 MHz to 100 MHz;
the input frequency must be between 0.001 and 100 MHz, and must be at least 2.5 times less than the CCO frequency. This makes it possible to use the IMO to generate much higher clock frequencies for the rest of the system.

The FLL is similar in purpose to a PLL but is not equivalent:
- FLL can start up (lock) much faster than the PLL.
- It consumes less current than the PLL.
- FLL does not lock the phase. At the heart of the FLL is a current-controlled oscillator (CCO). The output frequency of this CCO is controlled by adjusting the trim of the CCO; this is done in hardware and is explained in detail later in this section.
- FLL can produce up to 100-MHz clock with good duty cycle through its divided clock output.
- FLL reference clock can be the WCO (32 kHz), IMO (8 MHz), or any other periodic clock source.

**Note:** The CCO frequency must be at least 2.5 times greater than the reference frequency.

The CCO can output a stable frequency in the 48 MHz to 200 MHz range. This range is divided into five sub-ranges as shown by Table 19-6.

<table>
<thead>
<tr>
<th>CCO Range</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>f_min</td>
<td>48 MHz</td>
<td>64 MHz</td>
<td>85 MHz</td>
<td>113 MHz</td>
<td>150 MHz</td>
</tr>
<tr>
<td>f_max</td>
<td>64 MHz</td>
<td>85 MHz</td>
<td>113 MHz</td>
<td>150 MHz</td>
<td>200 MHz</td>
</tr>
</tbody>
</table>

**Note:** The output of the CCO has an option to enable a divide by two or not. For this device, the divide by two must always be enabled. The output range of the FLL is as shown in Table 19-6.

Within each range, the CCO output is controlled via a 9-bit trim field. This trim field is updated via hardware based on the control algorithm described below.

A reference clock must be provided to the FLL. This reference clock is typically the IMO, but could be many different clock sources. The FLL compares the reference clock against the CCO clock to determine how to adjust the CCO trim. Specifically, the FLL will count the number of CCO clock cycles inside a specified window of reference clock cycles. The number of reference clock cycles to count is set by the FLL_REF_DIV field in the CLK_FLL_CONFIG2 register.

After the CCO clocks are counted, they are compared against an ideal value and an error is calculated. The ideal value is programmed into the FLL_MULT field of the CLK_FLL_CONFIG register.

As an example, the reference clock is the IMO (8 MHz), the desired CCO frequency is 100 MHz, the value for FLL_REF_DIV is set to 146. This means that the FLL will count the number of CCO clocks within 146 clock periods of the reference clock. In one clock cycle of the reference clock (IMO), there should be 100 / 8 = 12.5 clock cycles of the CCO. Multiply this number by 146 and the value of FLL_MULT should be 1825.

If the FLL counts a value different from 1825, it attempts to adjust the CCO such that it achieves 1825 the next time it counts. This is done by scaling the error term with FLL_LF_IGAIN and FLL_LF_PGAIN found in CLK_FLL_CONFIG3. Figure 19-3 shows how the error (err) term is multiplied by FLL_LF_IGAIN and FLL_LF_PGAIN and then summed with the current trim to produce a new trim value for the CCO. The CCO_LIMIT field in the CLK_FLL_CONFIG4 can be used to put an upper limit on the trim adjustment; this is not needed for most situations.
The FLL determines whether it is “locked” by comparing the error term with the LOCK_TOL field in the CLK_FLL_CONFIG2 register. When the error is less than LOCK_TOL the FLL is considered locked.

After each adjustment to the trim the FLL can be programmed to wait a certain number of reference clocks before doing a new measurement. The number of reference clocks to wait is set in the SETTLING_COUNT field of CLK_FLL_CONFIG3. Set this such that the FLL waits ~1 µs before a new count. Therefore, if the 8-MHz IMO is used as the reference this field should be programmed to ‘8’.

When configuring the FLL there are two important factors that must be considered: lock time and accuracy. Accuracy is the closeness to the intended output frequency. These two numbers are inversely related to each other via the value of REF_DIV. Higher REF_DIV values lead to higher accuracy, whereas lower REF_DIV values lead to faster lock times.

In the example used previously the 8-MHz IMO was used as the reference, and the desired FLL output was 100 MHz. For that example, there are 12.5 CCO clocks in one reference clock. If the value for REF_DIV is set to ‘1’ then FLL_MULT must be set to either ‘13’ or ‘12’. This will result in a CCO output of either 96 MHz or 104 MHz, and an error of 4 percent from the desired 100 MHz. Therefore, the best way to improve this is to increase REF_DIV. However, the larger REF_DIV is, the longer each measurement cycle takes, thus increasing the lock time. In this example, REF_DIV was set to 146. This means each measurement cycle takes 146 * (1/8 MHz) = 18.25 µs, whereas when REF_DIV is set to 1, each measurement cycle takes 1 * (1/ 8 MHz) 0.125 µs.

Another issue with lower REF_DIV values is that the minimum LOCK_TOL is 1, so the output of the CCO can have an error of ±1. In the example where REF_DIV = 1 and FLL_MULT = 13, the MULT value can really be 12, 13, or 14 and still be locked. This means the output of the FLL may vary between 96 and 112 MHz, which may not be desirable.

Thus, a choice must be made between faster lock times and more accurate FLL outputs. The biggest change to make for this is the value of REF_DIV. The following section describes how to configure all of the FLL registers and gives some example equations to set REF_DIV N for best accuracy.

### 19.4.2.1 Configuring the FLL

This section provides a guide to calculate FLL parameters. The following steps use the best accuracy method.

In the following equations:

\[ N = \text{REF\_DIV} \]

\[ M = \text{FLL\_MULT} \]

1. Set CCO\_RANGE in the CLK\_FLL\_CONFIG4 register.
   a. Determine the output frequency of the FLL.
   b. Calculate the CCO frequency. The CCO frequency = 2 * FLL output frequency.
   c. Use Table 19-7 to determine the CCO range.
   d. Write CCO range into CCO\_RANGE in the CLK\_FLL\_CONFIG4 register.

<table>
<thead>
<tr>
<th>CCO Range</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>f_{min}</td>
<td>48 MHz</td>
<td>64 MHz</td>
<td>85 MHz</td>
<td>113 MHz</td>
<td>150 MHz</td>
</tr>
<tr>
<td>f_{max}</td>
<td>64 MHz</td>
<td>85 MHz</td>
<td>113 MHz</td>
<td>150 MHz</td>
<td>200 MHz</td>
</tr>
</tbody>
</table>

2. Set the FLL\_OUTPUT\_DIV in CLK\_FLL\_CONFIG. Set the output divider to ‘1’.

3. Set FLL\_REF\_DIV in CLK\_FLL\_CONFIG2.

FLL\_REF\_DIV divides the FLL input clock. The FLL counts the number of CCO clocks within one period of the divided reference clock. A general equation to calculate the reference divider is as follows:

\[
N = \text{ROUNDUP} \left( \frac{2 \times f_{\text{ref}}}{\frac{C\text{CO\_Trim\_Step}}{f_{\text{CCO\_Target}}}} \right)
\]

Equation 19-1
The CCO\textsubscript{TrimStep} is found in Table 19-8.

### Table 19-8. CCO Trim Steps

<table>
<thead>
<tr>
<th>CCO</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCO_Trim_Steps</td>
<td>0.0011</td>
<td>0.0011</td>
<td>0.0011</td>
<td>0.0011</td>
<td>0.00117</td>
</tr>
</tbody>
</table>

A larger \( N \) results in better precision on the FLL output, but longer lock times; a smaller \( N \) will result in faster lock times, but less precision.

**Note:** When the WCO is used as the reference clock, \( N \) must be set to 19.

4. Set FLL\_MULT in CLK\_FLL\_CONFIG.

FLL\_MULT is the ratio between the desired CCO frequency and the divided input frequency. This is the ideal value for the counter that counts the number of CCO clocks in one period of the divided input frequency.

\[
M = \frac{f_{CCO\_target}}{f_{ref}} \times \frac{N}{f_{ref}}
\]

5. Set the FLL\_LF\_IGAIN and FLL\_LF\_PGAIN in CLK\_FLL\_CONFIG3.

Within each range of the CCO there are 512 steps of adjustment for the CCO frequency. These steps are controlled by CCO\_FREQ in the CLK\_FLL\_CONFIG4 register. The FLL automatically adjusts CCO\_FREQ based on the output of the FLL counter.

The output of the counter gives the number of CCO clocks, over one period of the divided reference clock, by which the FLL is off. This value is then multiplied by the sum of FLL\_LF\_IGAIN and FLL\_LF\_PGAIN. The result of this multiplication is then summed with the value currently in the CCO\_FREQ register.

To determine the values for IGAIN and PGAIN use the following equation:

\[
I_{GAIN} < \left( \frac{0.85}{K_{CCO} \times \frac{N}{f_{ref}}} \right)
\]

Find the value of IGAIN closest but not over the values in the gain row in Table 19-9.

### Table 19-9. IGAIN and PGAIN Register Values

<table>
<thead>
<tr>
<th>Register Value</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain Value</td>
<td>1/256</td>
<td>1/128</td>
<td>1/64</td>
<td>1/32</td>
<td>1/16</td>
<td>1/8</td>
<td>1/4</td>
<td>1/2</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>8</td>
</tr>
</tbody>
</table>

Program FLL\_LF\_IGAIN with the register value that corresponds to the chosen gain value.

Take the IGAIN value from the register and use it in the following equation:

\[
P_{GAIN} < I_{GAIN_{reg}} - \frac{0.85}{K_{CCO} \times \frac{N}{f_{ref}}}
\]

Find the value of PGAIN closest but not over the values in the gain row in Table 19-9. Program FLL\_PF\_IGAIN with the register value that corresponds to the chosen gain value.

For best performance Pgain\_reg + igain\_reg should be as close as possible to calculated IGAIN without exceeding it.
kCCO is the gain of the CCO; Table 19-10 lists the kCCO for each CCO range.

**Table 19-10. kCCO Values**

<table>
<thead>
<tr>
<th>CCO Range</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>kCCO</td>
<td>48109.38</td>
<td>64025.65</td>
<td>84920</td>
<td>113300</td>
<td>154521.85</td>
</tr>
</tbody>
</table>

6. Set SETTLING_COUNT in CLK_FLL_CONFIG3. SETTLING_COUNT is the number of reference clocks to wait for the CCO to settle after it has changed. It is best to set this such that the settling time is around 1 µs.

   \[
   \text{Equation 19-5}
   \]

Do not set the settling time to anything less than 1 µs, greater will lead to longer lock times.

7. Set LOCK_TOL in CLK_FLL_CONFIG2. LOCK_TOL determines how much error the FLL can tolerate at the output of the counter that counts the number of CCO clocks in one period of the divided reference clock. A higher tolerance can be used to lock more quickly or track a less accurate source. The tolerance should be set such that the FLL does not unlock under normal conditions. A lower tolerance means a more accurate output, but if the input reference is unstable then the FLL may unlock.

   The following equation can be used to help determine the value:

   \[
   \text{Equation 19-6}
   \]

   \[
   \text{LOCK}_\text{TOL} = M \times \left( \frac{1 + \text{CCO}_{\text{accuracy}}}{1 - \text{ref}_{\text{accuracy}}} \right) - 1
   \]

   CCO (accuracy) = 0.25% or 0.0025
   ref (accuracy) is the accuracy of the reference clock

8. Set CCO_FREQ in CLK_FLL_CONFIG4. This field determines the frequency the FLL starts at before any measurement. The nearer the FLL is to the desired frequency, the faster it will lock.

   \[
   \text{Equation 19-7}
   \]

   \[
   \text{CCO}_{\text{FREQ}} = \text{ROUPNPDUP} \left( \frac{\log\left( \frac{f_CCO_{\text{target}}}{f_CCO_{\text{base}}} \right)}{\log(1 + \text{CCO}_{\text{Trim}_{\text{input}}})} \right)
   \]

   \[
   \text{f}_{CCO_{\text{Base}}} \text{ can be found in } \text{SETTLING_COUNT} = 1 \mu s \times \text{f}_{\text{ref}}
   \]

<table>
<thead>
<tr>
<th>CCO Range</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCO_{Base}</td>
<td>43600</td>
<td>58100</td>
<td>77200</td>
<td>103000</td>
<td>132000</td>
</tr>
</tbody>
</table>

9. Calculating Precision, Accuracy, and Lock Time of FLL

   To calculate the precision and accuracy of the FLL, the accuracy of the input source must be considered.

   The precision is the larger of:

   \[
   \text{Equation 19-8}
   \]

   \[
   \text{Precision}_{\text{FLL}} = \text{f}_{\text{ref}} \times \left( 1 + \text{f}_{\text{ref}}(\text{accuracy}) \right)
   \]

   Or

   \[
   \text{(CCO}_{\text{Trim}_{\text{Steps}}} / 2)
   \]

   Example: The desired FLL output is 100 MHz, thus CCO target is 200 MHz. The 1 percent accurate 8 MHz IMO is used as the reference input. N is calculated to be 69.

   \[
   \text{Precision}_{\text{FLL}} = ((8 \text{ MHz} \times 1.01) / (69 \times 200 \text{ MHz})) = 0.585\%, \text{ which is equal to the (CCO}_{\text{Trim}_{\text{Steps}}} / 2)
   \]
The accuracy of the FLL output is the precision multiplied by the lock tolerance. If the CCO goes beyond this range, then the FLL will unlock.

\[
\text{Accuracy}_{\text{FLL}} = \text{Precision}_{\text{FLL}} \times \text{LOCK}_{\text{TOL}}
\]

The value for the reference divider N should be tuned such that it achieves the best precision/accuracy versus lock time.

The lock time depends on the time for each adjustment step in the locking process:

\[
\text{Step Time} = \left( \frac{N}{f_{\text{ref}}} \right) + \left( \frac{\text{Ref Settling}}{f_{\text{ref}}} \right)
\]

Multiply this number by the number of steps it takes to lock to determine lock time. Typically, the FLL locks within the first ~10 steps.

19.5 Clock Trees

The PSoC 6 MCU clocks are distributed throughout the device, as shown in Figure 19-1. The clock trees are described in this section:

- Path Clocks
- High-Frequency Root Clocks (CLK_HF[i])
- Low-Frequency Clock (CLK_LF)
- Timer Clock (CLK_TIMER)
- Analog Pump Clock (CLK_PUMP)

19.5.1 Path Clocks

The PSoC 6 MCU has five clock paths: CLK_PATH0 contains the FLL, CLK_PATH1 contains the PLL, and CLK_PATH2-4 are a direct connection to the high-frequency root clocks. Note that the FLL and PLL can be bypassed if they are not needed. These paths are the input sources for the high-frequency clock roots.

Each clock path has a mux to determine which source clock will clock that path. This configuration is done in CLK_PATH_SELECT register.

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PATH_MUX[2:0]</td>
<td>Selects the source for clk_path[i]</td>
</tr>
<tr>
<td>0: IMO</td>
<td></td>
</tr>
<tr>
<td>1: EXTCLK</td>
<td></td>
</tr>
<tr>
<td>2: ECO</td>
<td></td>
</tr>
<tr>
<td>3: ALTHF</td>
<td></td>
</tr>
<tr>
<td>4: DSI_MUX</td>
<td></td>
</tr>
<tr>
<td>5-7: Reserved.</td>
<td>Do not use</td>
</tr>
</tbody>
</table>

The DSI mux is configured through the CLK_DSI_SELECT register.

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PATH_MUX[2:0]</td>
<td>Selects the source for the DSI_MUX[i]</td>
</tr>
<tr>
<td>0: dsi_out[0]</td>
<td></td>
</tr>
<tr>
<td>1: dsi_out[1]</td>
<td></td>
</tr>
<tr>
<td>2-15: Reserved.</td>
<td>Do not use</td>
</tr>
<tr>
<td>16: ILO</td>
<td></td>
</tr>
<tr>
<td>17: WCO</td>
<td></td>
</tr>
<tr>
<td>18: Reserved.</td>
<td>Do not use</td>
</tr>
<tr>
<td>19: PILO</td>
<td></td>
</tr>
<tr>
<td>20-31: Reserved</td>
<td>Do not use</td>
</tr>
</tbody>
</table>

19.5.2 High-Frequency Root Clocks

The PSoC 6 MCU has five high-frequency root clocks (CLK_HF[i]). Each CLK_HF has a particular destination on the device, as shown in Table 19-13.

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK_HF[0]</td>
<td>Root clock for both CPUs, PERI, and AHB infrastructure</td>
</tr>
<tr>
<td>CLK_HF[1]</td>
<td>Root clock for the PDM/PCM and I2S audio subsystem</td>
</tr>
<tr>
<td>CLK_HF[2]</td>
<td>Root clock for the Serial Memory Interface subsystem</td>
</tr>
<tr>
<td>CLK_HF[3]</td>
<td>Root clock for USB communications</td>
</tr>
<tr>
<td>CLK_HF[4]</td>
<td>Clock output on clk_ext pin (when used as an output)</td>
</tr>
</tbody>
</table>

Note that each CLK_HF is an input into the DSI.

Each high-frequency root clock has a mux to determine its source. This configuration is done in the CLK_ROOT_SELECT register.

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ROOT_MUX[3:0]</td>
<td>HFCLK input clock selection</td>
</tr>
<tr>
<td>0: Select CLK_PATH0</td>
<td></td>
</tr>
<tr>
<td>1: Select CLK_PATH1</td>
<td></td>
</tr>
<tr>
<td>2: Select CLK_PATH2</td>
<td></td>
</tr>
<tr>
<td>3: Select CLK_PATH3</td>
<td></td>
</tr>
<tr>
<td>4: Select CLK_PATH4</td>
<td></td>
</tr>
</tbody>
</table>
Each CLK_HF has a pre-divider, which is set in the CLK_ROOT_SELECT register.

### 19.5.3 Low-Frequency Clock

The low-frequency clock (CLK_LF) in the PSoC 6 MCU has three input options: ILO, PILO, and WCO.

CLK_LF is the source for the multi-counter watchdog timers (MCWDT), and can also be a source for the RTC.

The source of CLK_LF is set in the LFCLK_SEL bit of the CLK_SELECT register.

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ROOT_DVI[5:4]</td>
<td>Selects predivider value for the clock root and DSI input</td>
</tr>
<tr>
<td>0: No Divider</td>
<td>1: Divide clock by 2</td>
</tr>
<tr>
<td>1: Divide clock by 2</td>
<td></td>
</tr>
<tr>
<td>2: Divide clock by 4</td>
<td></td>
</tr>
<tr>
<td>3: Divide clock by 8</td>
<td></td>
</tr>
</tbody>
</table>

CLK_HF[1-4] can be enabled and disabled. CLK_HF[0] is always enabled as it is the source of the CPU. To enable and disable CLK_HF[1-4] set the ENABLE bit in the CLK_ROOT_SELECT register.

### 19.5.5 CTBm Alternate Pump Clock

Under certain conditions the CTBm requires a clock to run its internal voltage pump. One of the sources can come from the clock generation system, the other source is one of the peripheral clock dividers described in 19.7 Peripheral Clock Dividers. Note that this clock is not shown in Figure 19-1.

The clock from the clock generation system can be sourced from one of the path clocks. It can also be divided down by 2, 4, 8, or 16. This clock can be disabled to save power. To configure the pump clock, use the CLK_SELECT register.

### 19.5.6 Group Clocks (clk_sys)

On the PSoC 6 platform, peripherals are grouped. Each group has a dedicated group clock (also referred to as clk_sys). The group clock sets the clock rate for the AHB interface on the peripheral; it also sets the clock rate for the trigger outputs and trigger input synchronization. Each group clock as an eight-bit divider located in the CLOCK_CTL register in the PERI_GROUP_STRUCT in the PERI register set. For a majority of applications these dividers should be left at default (divide by 1). Advanced applications may have to change this divider.

### 19.5.7 Additional Clocks

The timer clock (CLK_TIMER) can be used as a clock source for the energy profiler or the CPU SYSTICK timer. The source for CLK_TIMER can either be the IMO or CLK_HF[0]. This selection is made in the TIMER_SEL bitfield of the CLK_TIMER_CTL register. Several dividers can be applied to this clock, which are found in the CLK_TIMER_CTL register.
19.6  CLK_HF[0] Distribution

clk_hf[0] is the root clock for the CPU subsystem and for the peripheral clock dividers.

Figure 19-4.  CLK_HF[0] Distribution

19.6.1  CLK_FAST

CLK_FAST clocks the Cortex-M4 processor. This clock is a divided version of CLK_HF[0]. The divider for this clock is set in the CM4_CLOCK_CONTROL register of the CPU subsystem.

19.6.2  CLK_PERI

CLK_PERI is the source clock for all programmable peripheral clock dividers and for the Cortex-M0+ processor. It is a divided version of CLK_HF[0]. The divider for this clock is set in the PERI_INT_DIV bitfields of the CM0_CLOCK_CTL register.

19.6.3  CLK_SLOW

CLK_SLOW is the source clock for the Cortex-M0+. This clock is a divided version of CLK_PERI. The divider for this clock is set in the SLOW_INT_DIV bitfields of the CM0_CLOCK_CTL register.

19.7  Peripheral Clock Dividers

The PSoC 6 MCU peripherals such as SCBs and TCPWMs require a clock. These peripherals can be clocked only by a peripheral clock divider.

The PSoC 6 MCU has 29 peripheral clock dividers (PCLK). It has eight 8-bit dividers, sixteen 16-bit dividers. Four fractional 16.5-bit dividers (16 integer bits, five fractional bits), and one 24.5-bit divider (24 integer bits, five fractional bits). The output of any of these dividers can be routed to any peripheral.

19.7.1  Fractional Clock Dividers

Fractional clock dividers allow the clock divisor to include a fraction of 0..31/32. For example, a 16.5-bit divider with an integer divide value of 3 generates a 16-MHz clock from a 48-MHz CLK_PERI. A 16.5-bit divider with an integer divide value of 4 generates a 12-MHz clock from a 48-MHz CLK_PERI. A 16.5-bit divider with an integer divide value of 3 and a fractional divider of 16 generates a 48 / (3 + 16/32) = 48 / 3.5 = 13.7-MHz clock from a 48-MHz CLK_PERI. Not all 13.7-MHz clock periods are equal in size; half of them will be three CLK_PERI cycles and half of them will be two CLK_PERI cycles.

Fractional dividers are useful when a high-precision clock is required (for example, for a UART/SPI serial interface). Fractional dividers are not used when a low jitter clock is required, because the clock periods have a jitter of one CLK_PERI cycle.

19.7.2  Peripheral Clock Divider Configuration

The peripheral clock dividers are configured using registers from the peripheral block; specifically DIV_CMD, DIV_8_CTL, DIV_16_CTL, DIV_16_5_CTL, DIV_24_5_CTL, and CLOCK_CTL registers.

First the clock divider needs to be configured. This is done via the DIV_8_CTL, DIV_16_CTL, DIV_16_5_CTL, and DIV_24_5_CTL registers. There is one register for each divider; for example, there are eight DIV_8_CTL registers as there are eight 8-bit dividers. In these registers, set the value of the integer divider; if it is a fractional divider then set the fraction portion as well.

After the divider is configured use the DIV_CMD register to enable the divider. This is done by setting the DIV_SEL to the divider number you want to enable, and setting the TYPE_SEL to the divider type. For example, if you wanted to enable the 0th 16.5-bit divider, write ‘0’ to DIV_SEL and ‘2’ to TYPE_SEL. If you wanted to enable the tenth 16-bit divider, write ‘10’ to DIV_SEL and ‘1’ to TYPE_SEL. See the PSoC 63 with BLE Registers TRM for more details.
19.7.2.1 Phase Aligning Dividers

For specific use cases, you must generate clocks that are phase-aligned. For example, consider the generation of two gated clocks at 24 and 12 MHz, both of which are derived from a 48-MHz CLK_PERI. If phase alignment is not considered, the generated gated clocks appear as follows.

![Figure 19-5. Non Phase-Aligned Clock Dividers](image)

These clock signals may or may not be acceptable, depending on the logic functionality implemented on these two clocks. If the two clock domains communicate with each other, and the slower clock domain (12 MHz) assumes that each high/’1’ pulse on its clock coincides with a high/’1’ phase pulse in the higher clock domain (24 MHz), the phase misalignment is not acceptable. To address this, it is possible to have PCLK dividers produce clock signals that are phase-aligned with any of the other (enabled) clock dividers. Therefore, if (enabled) divider x is used to generate the 24-MHz clock, divider y can be phase-aligned to divider x and used to generate the 12-MHz clock. The generated gated clocks appear as follows.

![Figure 19-6. Phase-Aligned Clock Dividers](image)

Phase alignment also works for fractional divider values. If (enabled) divider x is used to generate the 38.4-MHz clock (divide by 18/32), divider y can be phase-aligned to divider x and used to generate the 19.2-MHz clock (divide by 216/32). The generated gated clocks appear as follows.

![Figure 19-7. Phase-Aligned Fractional Dividers](image)
Divider phase alignment requires that the divider to which it is phase-aligned is already enabled. This requires the dividers to be enabled in a specific order. This order can be represented by a divider dependency graph.

Phase alignment is implemented by controlling the start moment of the divider counters in hardware. When a divider is enabled, the divider counters are set to ‘0’. The divider counters will only start incrementing from ‘0’ to the programmed integer and fractional divider values when the divider to which it is phase-aligned has an integer counter value of ‘0’.

Note that the divider and clock multiplexer control register fields are all retained during the Deep Sleep power mode. However, the divider counters that are used to implement the integer and fractional clock dividers are not. These counters are set to ‘0’ during the Deep Sleep mode. Therefore, when transitioning from Deep Sleep to Active mode, all dividers (and clock signals) are enabled and phase-aligned by design.

Phase alignment is accomplished by setting the PA_DIV_SEL and PA_DIV_TYPE bits in the DIV_CMD register before enabling the clock. For example, to align the fourth 8-bit divider to the third 16-bit divider, set DIV_SEL to ‘4’, TYPE_SEL to ‘0’, PA_DIV_SEL to ‘3’, and PA_TYPE_SEL to ‘1’.

19.7.2.2 Connecting Dividers to Peripheral

The PSoC 6 MCU has 58 peripherals, which can connect to one of the programmable dividers. Table 19-17 lists those peripherals.

### Table 19-17. PSoC 6 MCU Clock Dividers to Peripherals

<table>
<thead>
<tr>
<th>Clock Number</th>
<th>Destination</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>scb[0].clock</td>
</tr>
<tr>
<td>1</td>
<td>scb[1].clock</td>
</tr>
<tr>
<td>2</td>
<td>scb[2].clock</td>
</tr>
<tr>
<td>3</td>
<td>scb[3].clock</td>
</tr>
<tr>
<td>4</td>
<td>scb[4].clock</td>
</tr>
<tr>
<td>5</td>
<td>scb[5].clock</td>
</tr>
<tr>
<td>6</td>
<td>scb[6].clock</td>
</tr>
<tr>
<td>7</td>
<td>scb[7].clock</td>
</tr>
<tr>
<td>8</td>
<td>scb[8].clock</td>
</tr>
<tr>
<td>9</td>
<td>udb.clocks[0]</td>
</tr>
<tr>
<td>10</td>
<td>udb.clocks[1]</td>
</tr>
<tr>
<td>11</td>
<td>udb.clocks[2]</td>
</tr>
<tr>
<td>12</td>
<td>udb.clocks[3]</td>
</tr>
<tr>
<td>13</td>
<td>udb.clocks[4]</td>
</tr>
<tr>
<td>14</td>
<td>udb.clocks[5]</td>
</tr>
<tr>
<td>15</td>
<td>udb.clocks[6]</td>
</tr>
<tr>
<td>16</td>
<td>udb.clocks[7]</td>
</tr>
<tr>
<td>17</td>
<td>smartio[8].clock</td>
</tr>
<tr>
<td>18</td>
<td>smartio[9].clock</td>
</tr>
<tr>
<td>19</td>
<td>tcpwm[0].clocks[0]</td>
</tr>
<tr>
<td>20</td>
<td>tcpwm[0].clocks[1]</td>
</tr>
<tr>
<td>21</td>
<td>tcpwm[0].clocks[2]</td>
</tr>
<tr>
<td>22</td>
<td>tcpwm[0].clocks[3]</td>
</tr>
<tr>
<td>23</td>
<td>tcpwm[0].clocks[4]</td>
</tr>
<tr>
<td>24</td>
<td>tcpwm[0].clocks[5]</td>
</tr>
<tr>
<td>25</td>
<td>tcpwm[0].clocks[6]</td>
</tr>
<tr>
<td>26</td>
<td>tcpwm[0].clocks[7]</td>
</tr>
<tr>
<td>27</td>
<td>tcpwm[1].clocks[0]</td>
</tr>
<tr>
<td>28</td>
<td>tcpwm[1].clocks[1]</td>
</tr>
<tr>
<td>29</td>
<td>tcpwm[1].clocks[2]</td>
</tr>
<tr>
<td>30</td>
<td>tcpwm[1].clocks[3]</td>
</tr>
<tr>
<td>31</td>
<td>tcpwm[1].clocks[4]</td>
</tr>
<tr>
<td>32</td>
<td>tcpwm[1].clocks[5]</td>
</tr>
<tr>
<td>33</td>
<td>tcpwm[1].clocks[6]</td>
</tr>
<tr>
<td>34</td>
<td>tcpwm[1].clocks[7]</td>
</tr>
<tr>
<td>35</td>
<td>tcpwm[1].clocks[8]</td>
</tr>
<tr>
<td>36</td>
<td>tcpwm[1].clocks[9]</td>
</tr>
<tr>
<td>37</td>
<td>tcpwm[1].clocks[10]</td>
</tr>
<tr>
<td>39</td>
<td>tcpwm[1].clocks[12]</td>
</tr>
<tr>
<td>40</td>
<td>tcpwm[1].clocks[13]</td>
</tr>
<tr>
<td>41</td>
<td>tcpwm[1].clocks[14]</td>
</tr>
<tr>
<td>42</td>
<td>tcpwm[1].clocks[15]</td>
</tr>
<tr>
<td>43</td>
<td>tcpwm[1].clocks[16]</td>
</tr>
<tr>
<td>44</td>
<td>tcpwm[1].clocks[17]</td>
</tr>
<tr>
<td>45</td>
<td>tcpwm[1].clocks[18]</td>
</tr>
<tr>
<td>46</td>
<td>tcpwm[1].clocks[19]</td>
</tr>
<tr>
<td>47</td>
<td>tcpwm[1].clocks[20]</td>
</tr>
<tr>
<td>48</td>
<td>tcpwm[1].clocks[21]</td>
</tr>
<tr>
<td>49</td>
<td>tcpwm[1].clocks[22]</td>
</tr>
<tr>
<td>50</td>
<td>tcpwm[1].clocks[23]</td>
</tr>
<tr>
<td>51</td>
<td>csd.clock</td>
</tr>
<tr>
<td>52</td>
<td>lcd.clock</td>
</tr>
<tr>
<td>53</td>
<td>Reserved</td>
</tr>
<tr>
<td>54</td>
<td>cpuss_clock_trace_in</td>
</tr>
<tr>
<td>55</td>
<td>pass_clock_ctdac</td>
</tr>
<tr>
<td>56</td>
<td>pass_clock_pump_peri</td>
</tr>
<tr>
<td>57</td>
<td>pass_clock_sar</td>
</tr>
<tr>
<td>58</td>
<td>usb_clock_dev_brs</td>
</tr>
</tbody>
</table>

To connect a peripheral to a specific divider, the CLOCK_CTRL register is used. There is one CLOCK_CTRL register for each entry in Table 19-17. For example, to select the twelfth 16-bit divider for tcpwm[1].clocks[2] write to the twenty-ninth CLOCK_CTRL register, set the DIV_SEL to ‘12’, and the TYPE_SEL to ‘1’.
19.8 Clock Calibration Counters

A feature of the clocking system in PSoC 6 MCUs is built-in hardware calibration counters. These counters can be used to compare the frequency of two clock sources against one another. The primary use case is to take a higher accuracy clock such as the ECO and use it to measure a lower accuracy clock such as the ILO or PILO. The result of this measurement can then be used to trim the ILO and PILO.

There are two counters: Calibration Counter 1 is clocked off of Calibration Clock 1 (generally the high-accuracy clock) and it counts down; Calibration Counter 2 is clocked off of Calibration Clock 2 and it counts up. When Calibration Counter 1 reaches 0, Calibration Counter 2 stops counting up and its value can be read. From that value the frequency of Calibration Clock 2 can be determined with the following equation.

\[
\text{Calibration Clock 2 Frequency} = \frac{\text{Counter 2 Final Value}}{\text{Counter 1 Initial Value}} \times \text{Calibration Clock 1 Frequency}
\]

For example, if Calibration Clock 1 = 8 MHz, Counter 1 = 1000, and Counter 2 = 5

Calibration Clock 1 Frequency = \((5/1000) \times 8\) MHz = 40 kHz.

Calibration Clock 1 and Calibration Clock 2 are selected with the CLK_OUTPUT_FAST register. All clock sources are available as a source for these two clocks. CLK_OUTPUT_SLOW is also used to select the clock source.

Calibration Counter 1 is programmed in CLK_CAL_CNT1. Calibration Counter 2 can be read in CLK_CAL_CNT2.

When Calibration Counter 1 reaches 0, the CAL_COUNTER_DONE bit is set in the CLK_CAL_CNT1 register.
20. Reset System

The PSoC 6 MCU family supports several types of resets that guarantee error-free operation during power up and allow the device to reset based on user-supplied external hardware or internal software reset signals. The PSoC 6 MCU also contains hardware to enable the detection of certain resets.

20.1 Features

The PSoC 6 MCU has these reset sources:

- Power-on reset (POR) to hold the device in reset while the power supply ramps up to the level required for the device to function properly
- Brownout reset (BOD) to reset the device if the power supply falls below the device specifications during normal operation
- External reset (XRES) to reset the device using an external input
- Watchdog timer (WDT) reset to reset the device if the firmware execution fails to periodically service the watchdog timer
- Software initiated reset to reset the device on demand using firmware
- Logic-protection fault resets to reset the device if unauthorized operating conditions occur
- Clock-supervision logic resets to reset the device when clock-related errors occur
- Hibernate wakeup reset to bring the device out of the Hibernate low-power mode

20.2 Architecture

The following sections provide a description of the reset sources available in the PSoC 6 MCU family.

Note: None of these sources can reset the Backup system. The Backup domain is reset only when all the power supplies are removed from it, also known as a “cold start” or if the firmware triggers a reset using the BACKUP_RESET register. For more details, see the Backup System chapter on page 139.

20.2.1 Power-on Reset

Power-on reset is provided to keep the system in a reset state during power-up. POR holds the device in reset until the supply voltage, $V_{DD}$, reaches the datasheet specification. The POR activates automatically at power-up. See the Power Supply and Monitoring chapter on page 120 for more details.

POR events do not set a reset cause status bit, but can be partially inferred by the absence of any other reset source. If no other reset event is detected, then the reset is caused by POR, BOD, or XRES.

20.2.2 Brownout Reset

Brownout reset monitors the chip digital voltage supply $V_{DD}$ and generates a reset if $V_{DD}$ falls below the minimum logic operating voltage specified in the device datasheet. See the Power Supply and Monitoring chapter on page 120 for more details.

BOD events do not set a reset cause status bit, but in some cases they can be detected. In some BOD events, $V_{DD}$ will fall below the minimum logic operating voltage specified by the datasheet, but remain above the minimum logic retention voltage. Thus, some BOD events may be distinguished from POR events by checking for logic retention. This is explained further in Identifying Reset Sources on page 162.
20.2.3 Watchdog Timer Reset

Watchdog timer reset causes a reset if the WDT is not serviced by the firmware within a specified time limit. See the Watchdog Timer chapter on page 186 for more details.

The RESET_HWWDT bit or RESET_SWWDT0 to RESET_SWWDT3 status bits of the RES_CAUSE register is set when a watchdog reset occurs. This bit remains set until cleared by the firmware or until a POR, XRES, or BOD reset occurs. All other resets leave this bit unaltered.

For more details, see the Watchdog Timer chapter on page 186.

20.2.4 Software Initiated Reset

Software initiated reset is a mechanism that allows the CPU to request a reset. The Cortex-M0+ and Cortex-M4 Application Interrupt and Reset Control registers (CM0_AIRCR and CM4_AIRCR, respectively) can request a reset by writing a ‘1’ to the SYSRESETREQ bit of the respective registers.

Note that a value of 0x5FA should be written to the VECTKEY field of the AIRCR register before setting the SYSRESETREQ bit; otherwise, the processor ignores the write. See the CPU Subsystem (CPUSS) chapter on page 30 for details.

The RESET_SOFT status bit of the RES_CAUSE register is set when a software reset occurs. This bit remains set until cleared by firmware or until a POR, XRES, or BOD reset occurs. All other resets leave this bit unaltered.

20.2.5 External Reset

External reset (XRES) is a reset triggered by an external signal that causes immediate system reset when asserted. The XRES pin is active low – a logic ‘1’ on the pin has no effect and a logic ‘0’ causes reset. The pin is pulled to logic ‘1’ inside the device. XRES is available as a dedicated pin. For detailed pinout, refer to the pinout section of the device datasheet.

The XRES pin holds the device in reset as long as the pin input is ‘0’. When the pin is released (changed to logic ‘1’), the device goes through a normal boot sequence. The logical thresholds for XRES and other electrical characteristics are listed in the Electrical Specifications section of the device datasheet. XRES is available in all power modes, but cannot reset the Backup system.

An XRES event does not set a reset cause status bit, but can be partially inferred by the absence of any other reset source. If no other reset event is detected, then the reset is caused by POR, BOD, or XRES.

20.2.6 Logic Protection Fault Reset

Logic protection fault reset detects any unauthorized protection violations and causes the device to reset if they occur. One example of a protection fault is reaching a debug breakpoint while executing privileged code. For details about privilege code, see Trusted on page 113.

The RESET_ACT_FAULT or RESET_DPSLP_FAULT bits of the RES_CAUSE register is set when a protection fault occurs in Active or Deep Sleep modes, respectively. These bits remain set until cleared or until a POR, XRES, or BOD reset occurs. All other resets leave this bit unaltered.

20.2.7 Clock-Supervision Logic Reset

Clock-supervision logic initiates a reset due to the loss of a high-frequency clock or watch-crystal clock, or due to a high-frequency clock error.

The RESET_CSV_WCO_LOSS bit of the RES_CAUSE register is set when the clock supervision logic requests a reset due to the loss of a watch-crystal clock (if enabled).

The RESET_CSV_HF_LOSS is a 16-bit field in the RES_CAUSE2 register that can be used to identify resets caused by the loss of a high-frequency clock. Similarly, the RESET_CSV_HF_FREQ field can be used to identify resets caused by the frequency error of a high-frequency clock.

For more information on clocks, see the Clocking System chapter on page 146.

20.2.8 Hibernate Wakeup Reset

Hibernate wakeup reset occurs when one of the Hibernate wakeup sources performs a device reset to return to the Active power mode. See the Device Power Modes chapter on page 128 for details on Hibernate mode and available wakeup sources.

TOKEN is an 8-bit field in the PWR_HIBERNATE register that is retained through a Hibernate wakeup sequence. The firmware can use this bitfield to differentiate hibernate wakeup from a general reset event. Similarly, the PWR_HIB_DATA register can retain its contents through a Hibernate wakeup reset, but is cleared when XRES is asserted.

20.3 Identifying Reset Sources

When the device comes out of reset, it is often useful to know the cause of the most recent or even older resets. This is achieved through the RES_CAUSE and RES_CAUSE2 registers. These registers have specific status bits allocated for some of the reset sources. These registers record the occurrences of WDT reset, software reset, logic-protection fault, and clock-supervision resets. However, these registers do not record the occurrences of POR, BOD, XRES, or Hibernate wakeup resets. The bits in these registers are set
on the occurrence of the corresponding reset and remain set after the reset, until cleared by the firmware or a loss of retention, such as a POR, XRES, or BOD.

Hibernate wakeup resets can be detected by examining the TOKEN field in the PWR_HIBERNATE register as described previously. Hibernate wakeup resets that occur as a result of an XRES cannot be detected. The other reset sources can be inferred to some extent by the status of the RES_CAUSE and RES_CAUSE2 registers, as shown in Table 20-1.

Table 20-1. Reset Cause Bits to Detect Reset Source

<table>
<thead>
<tr>
<th>Register</th>
<th>Bitfield</th>
<th>Number of Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES_CAUSE</td>
<td>RESET_HWWDT</td>
<td>1</td>
<td>A hardware WDT reset has occurred since the last power cycle.</td>
</tr>
<tr>
<td>RES_CAUSE</td>
<td>RESET_ACT_FAULT</td>
<td>1</td>
<td>Fault logging system requested a reset from its Active logic.</td>
</tr>
<tr>
<td>RES_CAUSE</td>
<td>RESET_DPSLP_FAULT</td>
<td>1</td>
<td>Fault logging system requested a reset from its Deep Sleep logic.</td>
</tr>
<tr>
<td>RES_CAUSE</td>
<td>RESET_CSV_WCO_LOSS</td>
<td>1</td>
<td>Clock supervision logic requested a reset due to loss of a watch-crystal clock.</td>
</tr>
<tr>
<td>RES_CAUSE</td>
<td>RESET_SOFT</td>
<td>1</td>
<td>A CPU requested a system reset through its SYSRESETREQ. This can be done via a debugger probe or in firmware.</td>
</tr>
<tr>
<td>RES_CAUSE</td>
<td>RESET_MCWDT0</td>
<td>1</td>
<td>Multi-counter WDT reset #0 has occurred since the last power cycle.</td>
</tr>
<tr>
<td>RES_CAUSE</td>
<td>RESET_MCWDT1</td>
<td>1</td>
<td>Multi-counter WDT reset #1 has occurred since the last power cycle.</td>
</tr>
<tr>
<td>RES_CAUSE</td>
<td>RESET_MCWDT2</td>
<td>1</td>
<td>Multi-counter WDT reset #2 has occurred since the last power cycle.</td>
</tr>
<tr>
<td>RES_CAUSE</td>
<td>RESET_MCWDT3</td>
<td>1</td>
<td>Multi-counter WDT reset #3 has occurred since the last power cycle.</td>
</tr>
<tr>
<td>RES_CAUSE2</td>
<td>RESET_CSV_HF_LOSS</td>
<td>16</td>
<td>Clock supervision logic requested a reset due to loss of a high-frequency clock. Each bit index K corresponds to a clk_hf&lt;K&gt;. Unimplemented clock bits return zero.</td>
</tr>
<tr>
<td>RES_CAUSE2</td>
<td>RESET_CSV_HF_FREQ</td>
<td>16</td>
<td>Clock supervision logic requested a reset due to frequency error of a high-frequency clock. Each bit index K corresponds to a clk_hf&lt;K&gt;. Unimplemented clock bits return zero.</td>
</tr>
</tbody>
</table>

For more information, see the RES_CAUSE and RES_CAUSE2 registers in the PSoC 63 with BLE Registers TRM.

If these methods cannot detect the cause of the reset, then it can be one of the non-recorded and non-retention resets: BOD, POR, or XRES. These resets cannot be distinguished using on-chip resources.

## 20.4 Register List

Table 20-2. Reset System Register List

<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES_CAUSE</td>
<td>Reset cause observation register</td>
</tr>
<tr>
<td>RES_CAUSE2</td>
<td>Reset cause observation register 2</td>
</tr>
<tr>
<td>PWR_HIBERNATE</td>
<td>Hibernate power mode control register. Contains a TOKEN field that can be used to detect the Hibernate wakeup reset</td>
</tr>
<tr>
<td>PWR_HIB_DATA</td>
<td>Retains its contents through Hibernate wakeup reset</td>
</tr>
<tr>
<td>CM4_AIRCR</td>
<td>Application interrupt and reset control register of Cortex-M4</td>
</tr>
<tr>
<td>CM0_AIRCR</td>
<td>Application interrupt and reset control register of Cortex-M0+</td>
</tr>
</tbody>
</table>
21. I/O System

This chapter explains the PSoC 6 MCU I/O system, its features, architecture, operating modes, and interrupts. The I/O system provides the interface between the CPU core and peripheral components to the outside world. The flexibility of PSoC 6 MCUs and the capability of its I/O to route most signals to most pins greatly simplifies circuit design and board layout. The GPIO pins in the PSoC 6 MCU family are grouped into ports; a port can have a maximum of eight GPIOs.

21.1 Features

The PSoC 6 MCU GPIOs have these features:
- Analog and digital input and output capabilities
- Eight drive strength modes
- Separate port read and write registers
- Overvoltage tolerant (OVT-GPIO) pins
- Separate I/O supplies and voltages for up to six groups of I/O
- Edge-triggered interrupts on rising edge, falling edge, or on both edges, on all GPIO
- Slew rate control
- Hold mode for latching previous state (used to retain the I/O state in Deep Sleep mode)
- Selectable CMOS and low-voltage LVTTL input buffer mode
- CapSense support
- Smart I/O provides the ability to perform Boolean functions in the I/O signal path
- Segment LCD drive support

21.2 Architecture

The PSoC 6 MCU is equipped with analog and digital peripherals. Figure 21-1 shows an overview of the routing between the peripherals and pins.
GPIO pins are connected to I/O cells. These cells are equipped with an input buffer for the digital input, providing high input impedance and a driver for the digital output signals. The digital peripherals connect to the I/O cells via the high-speed I/O matrix (HSIOM). The HSIOM for each pin contains multiplexers to connect between the selected peripheral and the pin. HSIOM also bridges the connection between the digital system interconnect (DSI) and the pins. This enables routing of pin signals to the DSI-connected digital UDB peripherals. Analog peripherals such as SAR ADC, Continuous Time Block (CTB), Low-Power Comparator (LPCOMP), and CapSense are either connected to the GPIO pins directly or through the AMUXBUS.
21.2.1 I/O Cell Architecture

Figure 21-2 shows the I/O cell architecture present in every GPIO cell. It comprises an input buffer and an output driver that connect to the HSIOM multiplexers for digital input and output signals. Analog peripherals connect directly to the pin for point to point connections or use of the AMUXBUS.

Figure 21-2. GPIO and GPIO_OVT Cell Architecture

```
GPIO_PRTx_CFG,IDRIVE_MODEy]
GPIO_PRTx_CFG,IN,ENy]
GPIO_PRTx_INTR,EDGEy]
GPIO_PRTx_INTR,IN,INy]
GPIO_PRTx_INTR,MASK[EDGEy]
GPIO_PRTx_INTR,MASK[EDGEDGEy]
GPIO_PRTx_INTR,SETy[EDGEy]
GPIO_PRTx_INTR,CFG,EDGEy_SEL]

GPIO, Edge Detect

x = Port Number
y = Pin Number

GPIO, PRTx_IN[], INy]
DSI
ACTIVE[15:0]
DEEP_SLEEP[7:0]

GPIO, PRTx_CFG,OUT,SLOWy]
GPIO, PRTx_CFG,OUT,DRIVE SELy]

HSIOM, PRTx, PORT_SEL[1:0]Oy, SEL]

GPIO, PRTx, OUT, OUTy]
DSI
DSI
DSI
ACT,IVE, 0, (TCPWM)
ACTIVE, 1, (SCB)
ACTIVE, 2, (CAN)
ACTIVE[15:3] 13
DEEP_SLEEP, 0, (LCO, COM)
DEEP_SLEEP, 1, (LCO, SEG)
DEEP_SLEEP, 2, (SCB)
DEEP_SLEEP[7:3] 5

Note: HSIOM selection connects OUT and OUT, EN. ACTIVE[2:0] and DEEP, SLEEP[2:0] connections are examples. See Device Datasheet for specific connections to HSIOM ACTIVE and DEEP, SLEEP selections.

GPIO, PRTx, CFG, DRIVE, MODEy]

Dedicated Analog Resources (SAR, ADC, LPCOMP)

DSI
AMUXBUS-A (CapSense Source, SAR ADC)
AMUXBUS-B (CapSense Shield, SAR ADC)
```
21.2.2 Digital Input Buffer

The digital input buffer provides a high-impedance buffer for the external digital input. The buffer is enabled or disabled by the IN_EN[7:0] bit of the Port Configuration Register (GPIO_PRTx_CFG, where x is the port number).

The input buffer is connected to the HSIOM for routing to the CPU port registers and selected peripherals. Writing to the HSIOM port select register (HSIOM_PORT_SELx) selects the pin connection. See the device datasheet for the specific connections available for each pin.

If a pin is connected only to an analog signal, the input buffer should be disabled to avoid crowbar currents.

Each pin's input buffer trip point and hysteresis are configurable for the following modes:
- CMOS + I²C
- TTL

These buffer modes are selected by the VTRIP_SEL[7:0]_0 bit of the Port Input Buffer Configuration register (GPIO_PRTx_CFG_IN).

21.2.3 Digital Output Driver

Pins are driven by the digital output driver. It consists of circuitry to implement different drive modes and slew rate control for the digital output signals. The HSIOM selects the control source for the output driver. The three primary types of control sources are CPU registers, configurable digital peripherals instantiated in the programmable UDB/DSI fabric, and fixed-function digital peripherals. A particular HSIOM connection is selected by writing to the HSIOM port select register (HSIOM_PORT_SELx).

Six groups of I/Os are powered by different sources. Table 21-1 shows the allocation of ports in different banks and the respective bank supply source.

Table 21-1. I/O Banks

<table>
<thead>
<tr>
<th>Ports</th>
<th>I/O Supply Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port 0</td>
<td>VBACKUP/VSSIO_B</td>
</tr>
<tr>
<td>Port 1</td>
<td>VDDD/VSSIO_B</td>
</tr>
<tr>
<td>Port 2, Port 3, Port 4</td>
<td>VDDIO_R/VSSIO_R</td>
</tr>
<tr>
<td>Port 5, Port 6, Port 7, Port 8</td>
<td>VDDIO_1/VSSIO_1</td>
</tr>
<tr>
<td>Port 9, Port 10</td>
<td>VDDIO_A/VSSIO_A</td>
</tr>
<tr>
<td>Port 11, Port 12, Port 13</td>
<td>VDDIO_0/VSSIO_0</td>
</tr>
</tbody>
</table>

Each GPIO pin has ESD diodes to clamp the pin voltage to the I/O supply source. Ensure that the voltage at the pin does not exceed the I/O supply voltage VDDIO/VDD/VDDA or drop below VSSIO/VSSP/VSSA. For the absolute maximum and minimum GPIO voltage, see the device datasheet.

The digital output driver can be enabled or disabled in hardware by using the DSI signal from a peripheral or the output data register (GPIO_PRTx_OUT) associated with the output pin. See 21.3 High-Speed I/O Matrix for details on peripheral source selections supporting output enable control.

21.2.3.1 Drive Modes

Each I/O is individually configurable to one of eight drive modes by the DRIVE_MODE[7:0] field of the Port Configuration register, GPIO_PRTx_CFG. Table 21-2 lists the drive modes. Drive mode ‘1’ is reserved and should not be used in most designs. CPU register, UDB/DSI instantiated digital peripherals, and AMUXBUS connections support seven discrete drive modes to maximize design flexibility. Fixed-function digital peripherals, such as SCB and TCPWM blocks, support modified functionality for the same seven drive modes compatible with fixed peripheral signaling. Figure 21-3 shows simplified output driver diagrams of the pin view for the CPU register and UDB/DSI-based digital peripherals on each of the eight drive modes. Figure 21-4 is a simplified output driver diagram that shows the pin view for fixed-function-based peripherals for each of the eight drive modes.
Table 21-2. Drive Mode Settings

<table>
<thead>
<tr>
<th>Drive Mode</th>
<th>Value</th>
<th>CPU Register, AMUXBUS, UDB/DSI Digital Peripheral</th>
<th>Fixed-Function Digital Peripheral</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>OUT_EN = 1</td>
<td>OUT_EN = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OUT = 1</td>
<td>OUT = 0</td>
</tr>
<tr>
<td>High Impedance</td>
<td>0</td>
<td>HI-Z</td>
<td>HI-Z</td>
</tr>
<tr>
<td>Reserved</td>
<td>1</td>
<td>Strong 1</td>
<td>Strong 0</td>
</tr>
<tr>
<td>Reserved</td>
<td>1</td>
<td>Strong 1</td>
<td>Strong 0</td>
</tr>
<tr>
<td>Resitive Pull Up</td>
<td>2</td>
<td>Weak 1</td>
<td>Strong 1</td>
</tr>
<tr>
<td>Resitive Pull Down</td>
<td>3</td>
<td>Strong 1</td>
<td>Strong 0</td>
</tr>
<tr>
<td>Open Drain, Drives Low</td>
<td>4</td>
<td>HI-Z</td>
<td>HI-Z</td>
</tr>
<tr>
<td>Open Drain, Drives High</td>
<td>5</td>
<td>Strong 1</td>
<td>Strong 1</td>
</tr>
<tr>
<td>Strong</td>
<td>6</td>
<td>Strong 1</td>
<td>Strong 0</td>
</tr>
<tr>
<td>Resitive Pull Up and Down</td>
<td>7</td>
<td>Weak 1</td>
<td>Strong 1</td>
</tr>
</tbody>
</table>

Figure 21-3. CPU and DSI/UDB I/O Drive Mode Block Diagram

0. High Impedance

1. Reserved

2. Resitive Pull up

3. Resitive Pull down

4. Open Drain Drives Low

5. Open Drain Drives High

6. Strong

7. Resitive Pull Up and Down
I/O System

High-Impedance

This is the standard high-impedance (HI-Z) state recommended for analog and digital inputs. For digital signals, the input buffer is enabled; for analog signals, the input buffer is typically disabled to reduce crowbar current and leakage in low-power designs. To achieve the lowest device current, unused GPIOs must be configured to the high-impedance drive mode with input buffer disabled. High-impedance drive mode with input buffer disabled is also the default pin reset state.

Resistive Pull-Up or Resistive Pull-Down

Resistive modes provide a series resistance in one of the data states and strong drive in the other. Pins can be used for either digital input or digital output in these modes. If resistive pull-up is required, a ‘1’ must be written to that pin’s Data Register bit. If resistive pull-down is required, a ‘0’ must be written to that pin’s Data Register. Interfacing mechanical switches is a common application of these drive modes. The resistive modes are also used to interface PSoC with open drain drive lines. Resistive pull-up is used when the input is open drain low and resistive pull-down is used when the input is open drain high.

Open Drain Drives High and Open Drain Drives Low

Open drain modes provide high impedance in one of the data states and strong drive in the other. Pins are useful as digital inputs or outputs in these modes. Therefore, these modes are widely used in bidirectional digital communication. Open drain drive high mode is used when the signal is externally pulled down and open drain drive low is used when the signal is externally pulled high. A common application for the open drain drives low mode is driving I²C bus signal lines.

Strong Drive

The strong drive mode is the standard digital output mode for pins; it provides a strong CMOS output drive in both high and low states. Strong drive mode pins should not be used as inputs under normal circumstances. This mode is often used for digital output signals or to drive external devices.

Resistive Pull-Up and Resistive Pull-Down

In the resistive pull-up and pull-down mode, the GPIO will have a series resistance in both logic 1 and logic 0 output states. The high data state is pulled up while the low data state is pulled down. This mode is useful when the pin is driven by other signals that may cause shorts.

Slew Rate Control

GPIO pins have fast and slow output slew rate options for the strong drivers configured using the SLOW bit of the port output configuration register (GPIO_PRTx_CFG_OUT). By default, this bit is cleared and the port works in fast slew mode. This bit can be set if a slow slew rate is required. Slower slew rate results in reduced EMI and crosstalk and are recommended for low-frequency signals or signals without strict timing constraints.
When configured for fast slew rate, the drive strength can be set to one of four levels using the DRIVE_SEL field of the port output configuration register (GPIO_PRTx_CFG_OUT). The drive strength field determines the active portion of the output drivers used and can affect the slew rate of output signals. Drive strength options are full drive strength (default), one-half strength, one-quarter strength, and one-eighth strength. Drive strength must be set to full drive strength when the slow slew rate bit (SLOW) is set.

### 21.2.3.3 GPIO-OVT Pins

Select device pins are overvoltage tolerant (OVT) and are useful for interfacing to busses or other signals that may exceed the pin’s VDDIO supply, or where the whole device supply or pin VDDIO may not be always present. They are identical to regular GPIOs with the additional feature of being overvoltage tolerant. GPIO-OVT pins have hardware to compare VDDIO to the pin voltage. If the pin voltage exceeds VDDIO, the output driver is disabled and the pin driver is tristated. This results in negligible current sink at the pin.

Note that in overvoltage conditions, the input buffer data will not be valid if the external source’s specification of VOH and VOL do not match the trip points of the input buffer defined by the current VDDIO voltage.

### 21.3 High-Speed I/O Matrix

The high-speed I/O matrix (HSIOM) is a set of high-speed multiplexers that route internal CPU and peripheral signals to and from GPIOs. HSIOM allows GPIOs to be shared with multiple functions and multiplexes the pin connection to a user-selected peripheral. The HSIOM_PRTx_PORT_SEL[1:0] registers allow a single selection from up to 32 different connections to each pin as listed in Table 21-3.

<table>
<thead>
<tr>
<th>SELy_SEL</th>
<th>Name</th>
<th>Digital Driver Signal Source</th>
<th>Digital Input Signal Destination</th>
<th>Analog Switches</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>GPIO</td>
<td>OUT Register 1</td>
<td>IN Register</td>
<td>0</td>
<td>GPIO_PRTx_OUT register controls OUT</td>
</tr>
<tr>
<td>1</td>
<td>GPIO_DSI</td>
<td>OUT Register DSI OUT_EN</td>
<td>IN Register</td>
<td>0</td>
<td>GPIO_PRTx_OUT register controls OUT, DSI controls OUT_EN</td>
</tr>
<tr>
<td>2</td>
<td>DSI_DSI</td>
<td>DSI OUT DSI OUT_EN</td>
<td>DSI IN</td>
<td>0</td>
<td>DSI controls OUT and OUT_EN</td>
</tr>
<tr>
<td>3</td>
<td>DSI_GPIO</td>
<td>DSI OUT OUT Register</td>
<td>DSI IN</td>
<td>0</td>
<td>DSI controls OUT, GPIO_PRTx_OUT register controls OUT_EN</td>
</tr>
<tr>
<td>4</td>
<td>AMUXA</td>
<td>OUT Register 1</td>
<td>IN Register</td>
<td>1</td>
<td>Analog mux bus A connected to pin</td>
</tr>
<tr>
<td>5</td>
<td>AMUXB</td>
<td>OUT Register 1</td>
<td>IN Register</td>
<td>0</td>
<td>Analog mux bus B connected to pin</td>
</tr>
<tr>
<td>6</td>
<td>AMUXA_DSI</td>
<td>OUT Register DSI OUT_EN</td>
<td>IN Register</td>
<td>DSI OUT</td>
<td>DSI controls analog mux bus A connection to pin, GPIO_PRTx_OUT register controls OUT, DSI OUT_EN controls OUT_EN</td>
</tr>
<tr>
<td>7</td>
<td>AMUXB_DSI</td>
<td>OUT Register DSI OUT_EN</td>
<td>IN Register</td>
<td>0</td>
<td>DSI controls analog mux bus B connection to pin, GPIO_PRTx_OUT register controls OUT, DSI OUT_EN controls OUT_EN</td>
</tr>
<tr>
<td>8</td>
<td>ACT_0</td>
<td>Active Source OUT</td>
<td>Active Source OUT_EN</td>
<td>0</td>
<td>Active functionality 0 - See the device datasheet for specific pin connectivity</td>
</tr>
<tr>
<td>9</td>
<td>ACT_1</td>
<td>Active Source OUT</td>
<td>Active Source OUT_EN</td>
<td>0</td>
<td>Active functionality 1 - See the device datasheet for specific pin connectivity</td>
</tr>
<tr>
<td>10</td>
<td>ACT_2</td>
<td>Active Source OUT</td>
<td>Active Source OUT_EN</td>
<td>0</td>
<td>Active functionality 2 - See the device datasheet for specific pin connectivity</td>
</tr>
<tr>
<td>11</td>
<td>ACT_3</td>
<td>Active Source OUT</td>
<td>Active Source OUT_EN</td>
<td>0</td>
<td>Active functionality 3 - See the device datasheet for specific pin connectivity</td>
</tr>
<tr>
<td>12</td>
<td>DS_0</td>
<td>Deep Sleep Source OUT</td>
<td>Deep Sleep OUT</td>
<td>0</td>
<td>Deep Sleep functionality 0 - See the device datasheet for specific pin connectivity</td>
</tr>
<tr>
<td>13</td>
<td>DS_1</td>
<td>Deep Sleep Source OUT</td>
<td>Deep Sleep OUT</td>
<td>0</td>
<td>Deep Sleep functionality 1 - See the device datasheet for specific pin connectivity</td>
</tr>
</tbody>
</table>
Table 21-3. HSIOM Connections

<table>
<thead>
<tr>
<th>SELy_SEL</th>
<th>Name</th>
<th>Digital Driver Signal Source</th>
<th>Digital Input Signal Destination</th>
<th>Analog Switches AMUXA</th>
<th>AMUXB</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>14</td>
<td>DS_2</td>
<td>Deep Sleep Source OUT</td>
<td>Deep Sleep Source OUT_EN</td>
<td>Deep Sleep IN</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>15</td>
<td>DS_3</td>
<td>Deep Sleep Source OUT</td>
<td>Deep Sleep Source OUT_EN</td>
<td>Deep Sleep IN</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>16</td>
<td>ACT_4</td>
<td>Active Source OUT</td>
<td>Active Source OUT_EN</td>
<td>Active Source IN</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>17</td>
<td>ACT_5</td>
<td>Active Source OUT</td>
<td>Active Source OUT_EN</td>
<td>Active Source IN</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>18</td>
<td>ACT_6</td>
<td>Active Source OUT</td>
<td>Active Source OUT_EN</td>
<td>Active Source IN</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>19</td>
<td>ACT_7</td>
<td>Active Source OUT</td>
<td>Active Source OUT_EN</td>
<td>Active Source IN</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>20</td>
<td>ACT_8</td>
<td>Active Source OUT</td>
<td>Active Source OUT_EN</td>
<td>Active Source IN</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>21</td>
<td>ACT_9</td>
<td>Active Source OUT</td>
<td>Active Source OUT_EN</td>
<td>Active Source IN</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>22</td>
<td>ACT_10</td>
<td>Active Source OUT</td>
<td>Active Source OUT_EN</td>
<td>Active Source IN</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>23</td>
<td>ACT_11</td>
<td>Active Source OUT</td>
<td>Active Source OUT_EN</td>
<td>Active Source IN</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>24</td>
<td>ACT_12</td>
<td>Active Source OUT</td>
<td>Active Source OUT_EN</td>
<td>Active Source IN</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>25</td>
<td>ACT_13</td>
<td>Active Source OUT</td>
<td>Active Source OUT_EN</td>
<td>Active Source IN</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>26</td>
<td>ACT_14</td>
<td>Active Source OUT</td>
<td>Active Source OUT_EN</td>
<td>Active Source IN</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>27</td>
<td>ACT_15</td>
<td>Active Source OUT</td>
<td>Active Source OUT_EN</td>
<td>Active Source IN</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>28</td>
<td>DS_4</td>
<td>Deep Sleep Source OUT</td>
<td>Deep Sleep Source OUT_EN</td>
<td>Deep Sleep IN</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>29</td>
<td>DS_5</td>
<td>Deep Sleep Source OUT</td>
<td>Deep Sleep Source OUT_EN</td>
<td>Deep Sleep IN</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>30</td>
<td>DS_6</td>
<td>Deep Sleep Source OUT</td>
<td>Deep Sleep Source OUT_EN</td>
<td>Deep Sleep IN</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>31</td>
<td>DS_7</td>
<td>Deep Sleep Source OUT</td>
<td>Deep Sleep Source OUT_EN</td>
<td>Deep Sleep IN</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**Note:** The Active and Deep Sleep sources are pin dependent. See the “Pinouts” section of the device datasheet for more details on the features supported by each pin.
21.4 I/O State on Power Up

During power up, all the GPIOs are in high-impedance analog state and the input buffers are disabled. During runtime, GPIOs can be configured by writing to the associated registers. Note that the pins supporting debug access port (DAP) connections (SWD lines) are always enabled as SWD lines during power up. The DAP connection does not provide pull-up or pull-down resistors; therefore, if left floating some crowbar current is possible. The DAP connection can be disabled or reconfigured for general-purpose use through the HSIOM only after the device boots and starts executing code.

21.5 Behavior in Low-Power Modes

Table 21-4 shows the status of GPIOs in low-power modes.

Table 21-4. GPIO in Low-Power Modes

<table>
<thead>
<tr>
<th>Low-Power Mode</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sleep</td>
<td><img src="Image" alt="Standard GPIO, GPIO-OVT, and SIO pins are active and can be driven by most peripherals such as CapSense, TCPWM, and SCB, which can operate in Sleep mode." /> Inputs buffers are active; thus an interrupt on any I/O can be used to wake the CPU.</td>
</tr>
<tr>
<td>Deep Sleep</td>
<td><img src="Image" alt="GPIO, GPIO-OVT, and SIO pins, connected to Deep Sleep domain peripherals, are functional. All other pins are frozen and will maintain the last output driver state and configuration." /> Pin interrupts are functional on all I/Os and can be used to wake the device.</td>
</tr>
<tr>
<td>Hibernate</td>
<td><img src="Image" alt="Pin output states and configuration are latched and remain in the frozen state." /> Pin interrupts are functional only on select IOs and can be used to wake the device. See the device datasheet for specific hibernate pin connectivity.</td>
</tr>
</tbody>
</table>

21.6 Input and Output Synchronization

For digital input and output signals routed to the UDB array, the I/Os provide synchronization with an internal clock or a digital signal used as a clock. By default, HFCLK is used for synchronization but any other clock can also be used.

This feature is implemented using the UDB port adapter. See the **Universal Digital Blocks (UDB) chapter on page 372** for details on the port adapter.

21.7 Interrupt

All port pins have the capability to generate interrupts. There are two routing possibilities for pin signals to generate interrupts, as shown in Figure 21-5.

![Figure 21-5. Interrupt Signal Routing](Image)

- Pin signal through the “GPIO Edge Detect” block with direct connection to the CPU interrupt controller
- Pin signal through the port adapter and DSI to the CPU interrupt controller

Figure 21-6 shows the GPIO Edge Detect block architecture.
An edge detector is present at each pin. It is capable of detecting rising edge, falling edge, and both edges without any reconfiguration. The edge detector is configured by writing into the \texttt{EDGEx\_SEL} bits of the Port Interrupt Configuration register, \texttt{GPIO\_PRTx\_INTR\_CFG}, as shown in Table 21-5.

### Table 21-5. Edge Detector Configuration

<table>
<thead>
<tr>
<th>\texttt{EDGE_SEL}</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Interrupt is disabled</td>
</tr>
<tr>
<td>01</td>
<td>Interrupt on Rising Edge</td>
</tr>
<tr>
<td>10</td>
<td>Interrupt on Falling Edge</td>
</tr>
<tr>
<td>11</td>
<td>Interrupt on Both Edges</td>
</tr>
</tbody>
</table>

Writing ‘1’ to the corresponding status bit clears the pin edge state. Clear the edge state status bit is important; otherwise, an interrupt can occur repeatedly for a single trigger or respond only once for multiple triggers, which is explained later in this section. When the Port Interrupt Control Status register is read at the same time an edge is occurring on the corresponding port, it can result in the edge not being properly detected. Therefore, when using GPIO interrupts, read the status register only inside the corresponding interrupt service routine and not in any other part of the code.

Firmware and the debug interface are able to trigger a hardware interrupt from any pin by setting the corresponding bit in the \texttt{GPIO\_PRTx\_INTR\_SET} register.

In addition to the pins, each port provides a glitch filter connected to its own edge detector. This filter can be driven by one of the pins of a port. The selection of the driving pin is done by writing to the \texttt{FLT\_SEL} field of the \texttt{GPIO\_PRTx\_INTR\_CFG} register as shown in Table 21-6.

### Table 21-6. Glitch Filter Input Selection

<table>
<thead>
<tr>
<th>\texttt{FLT_SEL}</th>
<th>Selected Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>Pin 4 is selected</td>
</tr>
<tr>
<td>101</td>
<td>Pin 5 is selected</td>
</tr>
<tr>
<td>110</td>
<td>Pin 6 is selected</td>
</tr>
<tr>
<td>111</td>
<td>Pin 7 is selected</td>
</tr>
</tbody>
</table>

When a port pin edge occurs, you can read the Port Interrupt Status register, \texttt{GPIO\_PRTx\_INTR}, to know which pin caused the edge. This register includes both the latched information on which pin detected an edge and the current pin status. This allows the CPU to read both information in a single read operation. This register has an additional use – to clear the latched edge state.

The \texttt{GPIO\_PRTx\_INTR\_MASK} register enables forwarding of the \texttt{GPIO\_PRTx\_INTR} edge detect signal to the interrupt controller when a ‘1’ is written to a pin’s corresponding bitfield. The \texttt{GPIO\_PRTx\_INTR\_MASKED} register can then be read to determine the specific pin that generated the interrupt signal forwarded to the interrupt controller. The masked edge detector outputs of a port are then ORed together and routed to the interrupt controller (NVIC in the CPU subsystem). Thus, there is only one interrupt vector per port.

The masked and ORed edge detector block output is routed to the Interrupt Source Multiplexer shown in Figure 7-3 on page 49, which gives an option of Level and Rising Edge detection. If the Level option is selected, an interrupt is triggered repeatedly as long as the Port Interrupt Status register bit is set. If the Rising Edge detect option is selected, an interrupt is triggered only once if the Port Interrupt Status register is not cleared. Thus, the interrupt status bit must be cleared if the Edge Detect block is used.

Each port has a dedicated interrupt vector when the interrupt signal is routed through the fixed-function route. However, when the signal is routed though the DSI, interrupt vector is flexible and can occupy any of the DSI-connected interrupt lines of the NVIC. See the \textbf{Interrupts chapter on page 47} for details.
All of the port interrupt vectors are also ORed together into a single interrupt vector for use on devices with more ports than there are interrupt vectors available. To determine the port that triggered the interrupt, the GPIO_INTR_CAUSEx registers can be read. A ‘1’ present in a bit location indicates that the corresponding port has a pending interrupt. The indicated GPIO_PRTx_INTR register can then be read to determine the pin source.

When the signal is routed through the DSI, bypassing the Edge Detect block, the edge detection is configurable in the Interrupt Source Multiplexer block. If the multiplexer is configured as Level, the interrupt is triggered repeatedly as long as the pin signal is high. Use the Rising Edge detect option when this route is selected to generate only one interrupt.

21.8 Peripheral Connections

21.8.1 Firmware-Controlled GPIO

For standard firmware-controlled GPIO using registers, the GPIO mode must be selected in the HSIOM_PORT_SELx register.

The GPIO_PRTx_OUT register is used to read and write the output buffer state for GPIOs. A write operation to this register changes the GPIO's output driver state to the written value. A read operation reflects the output data written to this register and the resulting output driver state. It does not return the current logic level present on GPIO pins, which may be different. Using the GPIO_PRTx_OUT register, read-modify-write sequences can be safely performed on a port that has both input and output GPIOs.

In addition to the data register, three other registers – GPIO_PRTx_SET, GPIO_PRTx_CLR, and GPIO_PRTx_INV – are provided to set, clear, and invert the output data respectively on specific pins in a port without affecting other pins. This avoids the need for read-modify-write operations in most use cases. Writing ‘1’ to these register bitfields will set, clear, or invert the respective pin; writing ‘0’ will have no affect on the pin state.

GPIO_PRTx_IN is the port I/O pad register, which provides the actual logic level present on the GPIO pin when read. Writes to this register have no effect.

21.8.2 Analog I/O

Analog resources, such as LPCOMP, SAR ADC, and CTB, which require low-impedance routing paths have dedicated pins. Dedicated analog pins provide direct connections to specific analog blocks. They help improve performance and should be given priority over other pins when using these analog resources. See the device datasheet for details on these dedicated pins of the PSoC 6 MCUs.

To configure a GPIO as a dedicated analog I/O, it should be configured in high-impedance analog mode (see Table 21-2) with input buffer disabled. The respective connection should be enabled via registers in the specific analog resource.

To configure a GPIO as an analog pin connecting to AMUXBUS, it should be configured in high-impedance analog mode with the input buffer disabled and then routed to the correct AMUXBUS using the HSIOM_PORT_SELx register.

While it is preferred for analog pins to disable the input buffer, it is acceptable to enable the input buffer if simultaneous analog and digital input features are required.

21.8.2.1 AMUXBUS Connection and DSI

There are two methods of connecting a pin to AMUXBUS A or B. The pin may be statically connected with a register write or have the connection dynamically controlled by UDB based logic routed through the DSI. Static connection is made by selecting AMUXA or AMUXB in the HSIOM_PORT_SELx register. Dynamic hardware-controlled connection is made by selecting AMUXA_DSI or AMUXB_DSI in the HSIOM_PORT_SELx register, enabling you to implement hardware AMUXBUS switching.

To properly configure a pin as AMUXBUS input, follow these steps:
1. If the connection is dynamically controlled by hardware, the pin output and output enable signals must be connected to a pin selection signal generated and routed to the pin by the UDB/DSI system.
2. Configure the GPIO_PRTx_CFG register to set the pin in high-Impedance mode with input buffer disabled, enabling analog connectivity on the pin.
3. Configure the HSIOM_PORT_SELx register to connect the pin to AMUXBUS A or B. For static connections, select AMUXA or AMUXB. For dynamic connections, select AMUXA_DSI or AMUXB_DSI.

21.8.3 LCD Drive

All GPIOs have the capability of driving an LCD common or segment line. HSIOM_PORT_SELx registers are used to select pins for the LCD drive. See the LCD Direct Drive chapter on page 358 for details.

21.8.4 CapSense

The pins that support CapSense can be configured as CapSense widgets such as buttons, slider elements, touchpad elements, or proximity sensors. CapSense also requires external capacitors and optional shield lines. See the PSoC 4 and PSoC 6 MCU CapSense Design Guide for more details.
21.9 Smart I/O

The Smart I/O block adds programmable logic to an I/O port. This programmable logic integrates board-level Boolean logic functionality such as AND, OR, and XOR into the port. The Smart I/O block has these features:

- Integrate board-level Boolean logic functionality into a port
- Ability to preprocess HSIOM input signals from the GPIO port pins
- Ability to post-process HSIOM output signals to the GPIO port pins

21.9.1 Overview

The Smart I/O block is positioned in the signal path between the HSIOM and the I/O port. The HSIOM multiplexes the output signals from fixed-function peripherals and CPU to a specific port pin and vice-versa. The Smart I/O block is placed on this signal path, acting as a bridge that can process signals between port pins and HSIOM, as shown in Figure 21-7.

![Figure 21-7. Smart I/O Interface](image)

The signal paths supported through the Smart I/O block as shown in Figure 21-7 are as follows:

1. Implement self-contained logic functions that directly operate on port I/O signals
2. Implement self-contained logic functions that operate on HSIOM signals
3. Operate on and modify HSIOM output signals and route the modified signals to port I/O signals
4. Operate on and modify port I/O signals and route the modified signals to HSIOM input signals

The following sections discuss the Smart I/O block components, routing, and configuration in detail. In these sections, GPIO signals (io_data) refer to the input/output signals from the I/O port; device or chip (chip_data) signals refer to the input/output signals from HSIOM.

21.9.2 Block Components

The internal logic of the Smart I/O includes these components:

- Clock/reset
- Synchronizers
- Three-input lookup table (LUT)
- Data unit

- Support in all device power modes except Hibernate
- Integrate closely to the I/O pads, providing shortest signal paths with programmability

21.9.2.1 Clock and Reset

The clock and reset component selects the Smart I/O block’s clock (clk_block) and reset signal (rst_block_n). A single clock and reset signal is used for all components in the block. The clock and reset sources are determined by the CLOCK_SRC[4:0] bitfield of the SMARTIO_PRTx_CTL register. The selected clock is used for the synchronous logic in the block components, which includes the I/O input synchronizers, LUT, and data unit components. The selected reset is used to asynchronously reset the synchronous logic in the LUT and data unit components.

Note that the selected clock (clk_block) for the block’s synchronous logic is not phase-aligned with other synchronous logic in the device, operating on the same clock. Therefore, communication between Smart I/O and other synchronous logic should be treated as asynchronous.

The following clock sources are available for selection:

- GPIO input signals “io_data_in[7:0]”. These clock sources have no associated reset.
- HSIOM output signals “chip_data[7:0]”. These clock sources have no associated reset.
- Smart I/O clock (clk_smartio). This is derived from the system clock (clk_sys) using a peripheral clock divider. See the Clocking System chapter on page 146 for details on peripheral clock dividers. This clock is available only in Active and Sleep power modes. The clock can have one out of two associated resets:
rst_sys_act_n and rst_sys_dpslp_n. These resets determine in which system power modes the block synchronous state is reset; for example, rst_sys_act_n is intended for Smart I/O synchronous functionality in the Active power mode and reset is activated in the Deep Sleep power mode.

- Low-frequency system clock (clk_lf). This clock is available in Deep Sleep power mode. This clock has an associated reset, rst_lf_dpslp_n.

When the block is enabled, the selected clock (clk_block) and associated reset (rst_block_n) are provided to the fabric components. When the fabric is disabled, no clock is released to the fabric components and the reset is activated (the LUT and data unit components are set to the reset value of ‘0’).

The I/O input synchronizers introduce a delay of two clk_block cycles (when synchronizers are enabled). As a result, in the first two cycles, the block may be exposed to stale data from the synchronizer output. Hence, during the first two clock cycles, the reset is activated and the block is in bypass mode.

<table>
<thead>
<tr>
<th>Table 21-7. Clock and Reset Register Control</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Register[BIT_POS]</strong></td>
</tr>
</tbody>
</table>
| SMARTIO_PRT0_CTL[12:8] | CLK_SRC[4:0] | Clock (clk_block)/reset (rst_block_n) source selection:
- “0”: io_data[0]/’1’
- ...“7”: io_data[7]/’1’
- “8”: chip_data[0]/’1’
- ...
- “15”: chip_data[7]/’1’
- “16”: clk_smartio/rst_sys_act_n; asserts reset in any power mode other than Active; that is, Smart I/O is active only in Active power mode with clock from the peripheral divider.
- “17”: clk_smartio/rst_sys_dpslp_n. Smart I/O is active in all power modes with a clock from the peripheral divider. However, the clock will not be active in Deep Sleep power mode.
- “19”: clk_lf/rst_lf_dpslp_n. Smart I/O is active in all power modes with a clock from ILO.
- “20”-“30”: Clock source is a constant ‘0’. Any of these clock sources should be selected when Smart I/O is disabled to ensure low power consumption.
- “31”: clk_sys/’1’. This selection is not intended for clk_sys operation. However, for asynchronous operation, three clk_sys cycles after enabling, the Smart I/O is fully functional (reset is de-activated). To be used for asynchronous (clockless) block functionality.

### 21.9.2.2 Synchronizer

Each GPIO input signal and device input signal (HSIOM input) can be used either asynchronously or synchronously. To use the signals synchronously, a double flip-flop synchronizer, as shown in Figure 21-8, is placed on both these signal paths to synchronize the signal to the Smart I/O clock (clk_block). The synchronization for each pin/input is enabled or disabled by setting or clearing the IO_SYNC_EN[i] bitfield for GPIO input signal and CHIP_SYNC_EN[i] for HSIOM signal in the SMARTIO_PRTx_SYNC_CTL register, where ‘i’ is the pin number.

**Figure 21-8. Smart I/O Clock Synchronizer**
21.9.2.3 **Lookup Table (LUT)**

Each Smart I/O block contains eight lookup table (LUT) components. The LUT component consists of a three-input LUT and a flip-flop. Each LUT block takes three input signals and generates an output based on the configuration set in the SMARTIO_PRTx_LUT_CTLy register (y denotes the LUT number). For each LUT, the configuration is determined by an 8-bit lookup vector LUT[7:0] and a 2-bit opcode OPC[1:0] in the SMARTIO_PRTx_LUT_CTLy register. The 8-bit vector is used as a lookup table for the three input signals. The 2-bit opcode determines the usage of the flip-flop. The LUT configuration for different opcodes is shown in Figure 21-9.

The SMARTIO_PRTx_LUT_SELy registers select the three input signals (tr0_in, tr1_in, and tr2_in) going into each LUT. The input can come from the following sources:

- Data unit output
- Other LUT output signals (tr_out)
- HSIOM output signals (chip_data[7:0])
- GPIO output signals (io_data[7:0])

LUT_TR0_SEL[3:0] bits of the SMARTIO_PRTx_LUT_SELy register selects the tr0_in signal for the y\textsuperscript{th} LUT. Similarly, LUT_TR1_SEL[3:0] bits and LUT_TR2_SEL[3:0] bits select the tr1_in and tr2_in signals, respectively. See Table 21-8 for details.
Table 21-8. LUT Register Control

<table>
<thead>
<tr>
<th>Register[BIT_POS]</th>
<th>Bit Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMARTIO_PRTx_LUT_CTLy[7:0]</td>
<td>LUT[7:0]</td>
<td>LUT configuration. Depending on the LUT opcode (LUT_OPC), the internal state, and the LUT input signals tr0_in, tr1_in, and tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state.</td>
</tr>
<tr>
<td>SMARTIO_PRTx_LUT_CTLy[9:8]</td>
<td>LUT_OPC[1:0]</td>
<td>LUT opcode specifies the LUT operation as illustrated in Figure 21-9.</td>
</tr>
<tr>
<td>SMARTIO_PRTx_LUT_SELy[3:0]</td>
<td>LUT_TR0_SEL[3:0]</td>
<td>LUT input signal “tr0_in” source selection:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;0&quot;: Data unit output</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;1&quot;: LUT 1 output</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;2&quot;: LUT 2 output</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;3&quot;: LUT 3 output</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;4&quot;: LUT 4 output</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;5&quot;: LUT 5 output</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;6&quot;: LUT 6 output</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;7&quot;: LUT 7 output</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;8&quot;: chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;9&quot;: chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;10&quot;: chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;11&quot;: chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;12&quot;: io_data[0] (for LUTs 0, 1, 2, 3); io_data[4] (for LUTs 4, 5, 6, 7)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;13&quot;: io_data[1] (for LUTs 0, 1, 2, 3); io_data[5] (for LUTs 4, 5, 6, 7)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;14&quot;: io_data[2] (for LUTs 0, 1, 2, 3); io_data[6] (for LUTs 4, 5, 6, 7)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;15&quot;: io_data[3] (for LUTs 0, 1, 2, 3); io_data[7] (for LUTs 4, 5, 6, 7)</td>
</tr>
<tr>
<td>SMARTIO_PRTx_LUT_SELy[11:8]</td>
<td>LUT_TR1_SEL[3:0]</td>
<td>LUT input signal “tr1_in” source selection:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;0&quot;: LUT 0 output</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;1&quot;: LUT 1 output</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;2&quot;: LUT 2 output</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;3&quot;: LUT 3 output</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;4&quot;: LUT 4 output</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;5&quot;: LUT 5 output</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;6&quot;: LUT 6 output</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;7&quot;: LUT 7 output</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;8&quot;: chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;9&quot;: chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;10&quot;: chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;11&quot;: chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;12&quot;: io_data[0] (for LUTs 0, 1, 2, 3); io_data[4] (for LUTs 4, 5, 6, 7)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;13&quot;: io_data[1] (for LUTs 0, 1, 2, 3); io_data[5] (for LUTs 4, 5, 6, 7)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;14&quot;: io_data[2] (for LUTs 0, 1, 2, 3); io_data[6] (for LUTs 4, 5, 6, 7)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&quot;15&quot;: io_data[3] (for LUTs 0, 1, 2, 3); io_data[7] (for LUTs 4, 5, 6, 7)</td>
</tr>
<tr>
<td>SMARTIO_PRTx_LUT_SELy[19:16]</td>
<td>LUT_TR2_SEL[3:0]</td>
<td>LUT input signal “tr2_in” source selection. Encoding is the same as for LUT_TR1_SEL.</td>
</tr>
</tbody>
</table>
21.9.2.4 Data Unit (DU)

Each Smart I/O block includes a data unit (DU) component. The DU consists of a simple 8-bit datapath. It is capable of performing simple increment, decrement, increment/decrement, shift, and AND/OR operations. The operation performed by the DU is selected using a 4-bit opcode DU_OPC[3:0] bitfield in the SMARTIO_PRTx_DU_CTL register.

The DU component supports up to three input trigger signals (tr0_in, tr1_in, tr2_in) similar to the LUT component. These signals are used to initiate an operation defined by the DU opcode. In addition, the DU also includes two 8-bit data inputs (data0_in[7:0] and data1_in[7:0]) that are used to initialize the 8-bit internal state (data[7:0]) or to provide a reference. The 8-bit data input source is configured as:

- Constant ‘0x00’
- io_data_in[7:0]
- chip_data_in[7:0]
- DATA[7:0] bitfield of SMARTIO_PRTx_DATA register
The trigger signals are selected using the DU_TRx_SEL[3:0] bitfield of the SMARTIO_PRTx_DU_SEL register. The DUT_DATAx_SEL[1:0] bits of the SMARTIO_PRTx_DU_SEL register select the 8-bit input data source. The size of the DU (number of bits used by the datapath) is defined by the DU_SIZE[2:0] bits of the SMARTIO_PRTx_DU_CTL register. See Table 21-9 for register control details.

Table 21-9. Data Unit Register Control

<table>
<thead>
<tr>
<th>Register[BIT_POS]</th>
<th>Bit Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMARTIO_PRTx_DU_CTL[2:0]</td>
<td>DU_SIZE[2:0]</td>
<td>Size/width of the data unit (in bits) is DU_SIZE+1. For example, if DU_SIZE is 7, the width is 8 bits.</td>
</tr>
</tbody>
</table>
| SMARTIO_PRTx_DU_CTL[11:8] | DU_OPC[3:0]  | Data unit opcode specifies the data unit operation: "1": INCR  
|                     |               | "2": DECR  
|                     |               | "3": INCR_WRAP  
|                     |               | "4": DECR_WRAP  
|                     |               | "5": INCR_DECR  
|                     |               | "6": INCR_DECR_WRAP  
|                     |               | "7": ROR  
|                     |               | "8": SHR  
|                     |               | "9": AND OR  
|                     |               | "10": SHR_MAJ3  
|                     |               | "11": SHR_EQL  
|                     |               | Otherwise: Undefined. |
| SMARTIO_PRTx_DU_SEL[3:0] | DU_TR0_SEL[3:0] | Data unit input signal "tr0_in" source selection: "0": Constant '0'.  
|                     |               | "1": Constant '1'.  
|                     |               | "2": Data unit output.  
|                     |               | 10–3: LUT 7–0 outputs.  
|                     |               | Otherwise: Undefined. |
| SMARTIO_PRTx_DU_SEL[11:8] | DU_TR1_SEL[3:0] | Data unit input signal "tr1_in" source selection. Encoding same as DU_TR0_SEL |
| SMARTIO_PRTx_DU_SEL[19:16] | DU_TR2_SEL[3:0] | Data unit input signal "tr2_in" source selection. Encoding same as DU_TR0_SEL |
| SMARTIO_PRTx_DU_SEL[25:24] | DU_DATA0_SEL[1:0] | Data unit input data "data0_in" source selection: "0": 0x00  
|                     |               | "1": chip_data[7:0].  
|                     |               | "2": io_data[7:0].  
|                     |               | "3": SMARTIO_PRTx_DATA.DATA[7:0] register field. |
| SMARTIO_PRTx_DU_SEL[29:28] | DU_DATA1_SEL[1:0] | Data unit input data "data1_in" source selection. Encoding same as DU_DATA0_SEL. |
| SMARTIO_PRTx_DATA[7:0] | DATA[7:0]     | Data unit input data source. |

The DU generates a single output trigger signal (tr_out). The internal state (du_data[7:0]) is captured in flip-flops and requires clk_block.

The following pseudo code describes the various datapath operations supported by the DU opcode. Note that “Comb” describes the combinatorial functionality – that is, functions that operate independent of previous output states. “Reg” describes the registered functionality – that is, functions that operate on inputs and previous output states (registered using flip-flops).

```c
// The following is shared by all operations.
mask = (2 ^ (DU_SIZE+1) - 1)
data_eql_data1_in = (data & mask) == (data1_in & mask));
data_eql_0 = (data & mask) == 0);
data_incr = (data + 1) & mask;
data_decr = (data - 1) & mask;
```
data0_masked = data_in0 & mask;

// INCR operation: increments data by 1 from an initial value (data0) until it reaches a
// final value (data1).
Comb: tr_out = data_eql_data1_in;
Reg: data <= data;
if (tr0_in) data <= data0_masked; // tr0_in is reload signal - loads masked data0
  // into data
else if (tr1_in) data <= data_eql_data1_in ? data : data_incr; // increment data until
  // it equals data1

// INCR_WRAP operation: operates similar to INCR but instead of stopping at data1, it wraps
// around to data0.
Comb: tr_out = data_eql_data1_in;
Reg: data <= data;
if (tr0_in) data <= data0_masked;
else if (tr1_in) data <= data_eql_data1_in ? data0_masked : data_incr;

// DECR operation: decrements data from an initial value (data0) until it reaches 0.
Comb: tr_out = data_eql_0;
Reg: data <= data;
if (tr0_in) data <= data0_masked;
else if (tr1_in) data <= data_eql_0 ? data : data_decr;

// DECR_WRAP operation: works similar to DECR. Instead of stopping at 0, it wraps around to
// data0.
Comb: tr_out = data_eql_0;
Reg: data <= data;
if (tr0_in) data <= data0_masked;
else if (tr1_in) data <= data_eql_0 ? data0_masked : data_decr;

// INCR_DEC operation: combination of INCR and DECR. Depending on trigger signals it either
// starts incrementing or decrementing. Increment stops at data1 and decrement stops at 0.
Comb: tr_out = data_eql_data1_in | data_eql_0;
Reg: data <= data;
if (tr0_in) data <= data0_masked; // Increment operation takes precedence over
  // decrement when both signal are available
else if (tr1_in) data <= data_eql_data1_in ? data : data_incr;
else if (tr2_in) data <= data_eql_0 ? data : data_decr;

// INCR_DEC_WRAP operation: same functionality as INCR_DEC with wrap around to data0 on
// reaching the limits.
Comb: tr_out = data_eql_data1_in | data_eql_0;
Reg: data <= data;
if (tr0_in) data <= data0_masked;
else if (tr1_in) data <= data_eql_data1_in ? data0_masked : data_incr;
else if (tr2_in) data <= data_eql_0 ? data0_masked : data_decr;

// ROR operation: rotates data right and LSb is sent out. The data for rotation is taken from
// data0.
Comb: tr_out = data[0];
Reg: data <= data;
if (tr0_in) data <= data0_masked;
else if (tr1_in) {
  data <= {0, data[7:1]} & mask; // Shift right operation
  data[du_size] <= data[0]; // Move the data[0] (LSb) to MSb
}
// SHR operation: performs shift register operation. Initial data (data0) is shifted out and data on tr2_in is shifted in.
Comb: tr_out = data[0];
Reg: data <= data;
   if (tr0_in) data <= data0_masked;
   else if (tr1_in) {
      data <= {0, data[7:1]} & mask; // Shift right operation
      data[du_size] <= tr2_in; // tr2_in Shift in operation
   }

// SHR_MAJ3 operation: performs the same functionality as SHR. Instead of sending out the shifted out value, it sends out a '1' if in the last three samples/shifted-out values (data[0]), the signal high in at least two samples. otherwise, sends a '0'. This function sends out the majority of the last three samples.
Comb: tr_out = (data == 0x03) | (data == 0x05) | (data == 0x06) | (data == 0x07);
Reg: data <= data;
   if (tr0_in) data <= data0_masked;
   else if (tr1_in) {
      data <= {0, data[7:1]} & mask;
      data[du_size] <= tr2_in;
   }

// SHR_EQL operation: performs the same operation as SHR. Instead of shift-out, the output is a comparison result (data0 == data1).
Comb: tr_out = data_eql_data1_in;
Reg: data <= data;
   if (tr0_in) data <= data0_masked;
   else if (tr1_in) {
      data <= {0, data[7:1]} & mask;
      data[du_size] <= tr2_in;
   }

// AND_OR operation: ANDs data1 and data0 along with mask; then, ORs all the bits of the ANDed output.
Comb: tr_out = | (data & data1_in & mask);
Reg: data <= data;
   if (tr0_in) data <= data0_masked;

21.9.3 Routing

The Smart I/O block includes many switches that are used to route the signals in and out of the block and also between various components present inside the block. The routing switches are handled through the PRTGIO_PRTx_LUT_SELy and SMARTIO_PRTx_DU_SEL registers. Refer to the PSoC 63 with BLE Registers TRM for details. The Smart I/O internal routing is shown in Figure 21-10. In the figure, note that LUT7 to LUT4 operate on io_data/chip_data[7] to io_data/chip_data[4] whereas LUT3 to LUT0 operate on io_data/chip_data[3] to io_data/chip_data[0].
Figure 21-10. Smart I/O Routing
21.9.4 Operation

The Smart I/O block should be configured and operated as follows:

1. Before enabling the block, all the components and routing should be configured as explained in “Block Components” on page 175.

2. In addition to configuring the components and routing, some block level settings must be configured correctly for desired operation.
   a. Bypass control: The Smart I/O path can be bypassed for a particular GPIO signal by setting the BYPASS[i] bitfield in the SMARTIO_PRTx_CTL register. When bit ‘i’ is set in the BYPASS[7:0] bitfield, the ith GPIO signal is bypassed to the HSIOM signal path directly – Smart I/O logic will not be present in that signal path. This is useful when the Smart I/O function is required only on select I/Os.
   b. Pipelined trigger mode: The LUT input multiplexers and the LUT component itself do not include any combinatorial loops. Similarly, the data unit also does not include any combinatorial loops. However, when one LUT interacts with the other or to the data unit, inadvertent combinatorial loops are possible. To overcome this limitation, the PIPELINE_EN bitfield of the SMARTIO_PRTx_CTL register is used. When set, all the outputs (LUT and DU) are registered before branching out to other components.

3. After the Smart I/O block is configured for the desired functionality, the block can be enabled by setting the ENABLED bitfield of the SMARTIO_PRTx_CTL register. If disabled, the Smart I/O block is put in bypass mode, where the GPIO signals are directly controlled by the HSIOM signals and vice-versa. The Smart I/O block must be configured; that is, all register settings must be updated before enabling the block to prevent glitches during register updates.

Table 21-10. Smart I/O Block Controls

<table>
<thead>
<tr>
<th>Register [BIT_POS]</th>
<th>Bit Name</th>
<th>Description</th>
</tr>
</thead>
</table>
| SMARTIO_PRTx_CTL[25] | PIPELINE_EN | Enable for pipeline register:  
'0': Disabled (register is bypassed).  
'1': Enabled |
| SMARTIO_PRTx_CTL[31] | ENABLED     | Enable Smart I/O. Should only be set to ‘1’ when the Smart I/O is completely configured:  
'0': Disabled (signals are bypassed; behavior as if BYPASS[7:0] = 0xFF). When disabled, the block (data unit and LUTs) reset is activated.  
If the block is disabled:  
- The PIPELINE_EN register field should be set to ‘1’, to ensure low power consumption.  
- The CLOCK_SRC register field should be set to 20 to 30 (clock is constant ‘0’), to ensure low power consumption.  
'1': Enabled. When enabled, it takes three clk_block clock cycles until the block reset is deactivated and the block becomes fully functional. This action ensures that the I/O pins' input synchronizer states are flushed when the block is fully functional. |
| SMARTIO_PRTx_CTL[7:0] | BYPASS[7:0] | Bypass of the Smart I/O, one bit for each I/O pin: BYPASS[i] for I/O pin i. When ENABLED is ‘1’, this field is used. When ENABLED is ‘0’, this field is not used and Smart I/O is always bypassed.  
'0': No bypass (Smart I/O is present in the signal path)  
'1': Bypass (Smart I/O is absent in the signal path) |
## 21.10 Registers

Table 21-11. I/O Registers

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO_PRTx_OUT</td>
<td>Port output data register reads and writes the output driver data for I/O pins in the port.</td>
</tr>
<tr>
<td>GPIO_PRTx_OUT_CLR</td>
<td>Port output data clear register clears output data of specific I/O pins in the port.</td>
</tr>
<tr>
<td>GPIO_PRTx_OUT_SET</td>
<td>Port output data set register sets output data of specific I/O pins in the port.</td>
</tr>
<tr>
<td>GPIO_PRTx_OUT_INV</td>
<td>Port output data invert register inverts output data of specific I/O pins in the port.</td>
</tr>
<tr>
<td>GPIO_PRTx_IN</td>
<td>Port input state register reads the current pin state present on I/O pin inputs.</td>
</tr>
<tr>
<td>GPIO_PRTx_INTR</td>
<td>Port interrupt status register reads the current pin interrupt state.</td>
</tr>
<tr>
<td>GPIO_PRTx_INTR_MASK</td>
<td>Port interrupt mask register configures the mask that forwards pin interrupts to the CPU's interrupt controller.</td>
</tr>
<tr>
<td>GPIO_PRTx_INTR_MASKED</td>
<td>Port interrupt masked status register reads the masked interrupt status forwarded to the CPU interrupt controller.</td>
</tr>
<tr>
<td>GPIO_PRTx_INTR_SET</td>
<td>Port interrupt set register allows firmware to set pin interrupts.</td>
</tr>
<tr>
<td>GPIO_PRTx_INTR_CFG</td>
<td>Port interrupt configuration register selects the edge detection type for each pin interrupt.</td>
</tr>
<tr>
<td>GPIO_PRTx_CFG</td>
<td>Port configuration register selects the drive mode and input buffer enable for each pin.</td>
</tr>
<tr>
<td>GPIO_PRTx_CFG_IN</td>
<td>Port input buffer configuration register configures the input buffer mode for each pin.</td>
</tr>
<tr>
<td>GPIO_PRTx_CFG_OUT</td>
<td>Port output buffer configuration register selects the output driver slew rate for each pin.</td>
</tr>
<tr>
<td>HSIOM_PORT_SELx</td>
<td>High-speed I/O Mux (HSIOM) port selection register selects the hardware peripheral connection to I/O pins.</td>
</tr>
</tbody>
</table>

**Note**  The ‘x’ in the GPIO register name denotes the port number. For example, GPIO_PTR1_OUT is the Port 1 output data register.
22. Watchdog Timer

The watchdog timer (WDT) is a hardware timer that automatically resets the device in the event of an unexpected firmware execution path. The WDT, if enabled, must be serviced periodically in firmware to avoid a reset. Otherwise, the timer elapses and generates a device reset. In addition, the WDT can be used as an interrupt source or a wakeup source in low-power modes.

The PSoC 6 MCU family includes one WDT and two multi-counter WDTS (MCWDT). The WDT has a 16-bit counter. Each MCWDT has two 16-bit counters and one 32-bit counter. Thus, the watchdog system has a total of seven counters – five 16-bit and two 32-bit. All 16-bit counters can generate a watchdog device reset. All seven counters can generate an interrupt on a match event.

22.1 Features

The PSoC 6 MCU WDT supports these features:

- One 16-bit free-running WDT with:
  - ILO as the input clock source
  - Device reset generation if not serviced within a configurable interval
  - Interrupt/wakeup generation in Active/LPACTIVE, Sleep/LPSLEEP, Deep Sleep, and Hibernate power modes
- Two MCWDTs, each supporting:
  - Device reset generation if not serviced within a configurable interval
  - LFCLK (ILO, WCO, or PILO) as the input clock source
  - Periodic interrupt/wake up generation in Active/LPACTIVE, Sleep/LPSLEEP, and Deep Sleep power modes
  - Two 16-bit and one 32-bit independent counters
  - One 64-bit or one 48-bit (with one 16-bit independent counter), or two 32-bit cascaded counters

22.2 Architecture

Figure 22-1. Watchdog Timer Block Diagram
22.3 Free-running WDT

22.3.1 Overview

Figure 22-2 shows the functional overview of the WDT. The WDT has a free-running wraparound up-counter with a maximum of 16-bit resolution. The counter is clocked by the ILO. The timer has the capability to generate an interrupt on match and a reset event on the third unhandled interrupt. The number of bits used for a match comparison is configurable as depicted in Figure 22-2.

![Free-running WDT Functional Diagram](image)

When enabled, the WDT counts up on each rising edge of the ILO. When the counter value (WDT_CNT register) equals the match value stored in MATCH bits [15:0] of the WDT_MATCH register, an interrupt is generated. The match event does not reset the WDT counter and the WDT keeps counting until it reaches the 16-bit boundary (65535) at which point, it wraps around to 0 and counts up. The match interrupt is generated every time the counter value equals the match value.

The WDT_MATCH bit of the SRSS_INTR register is set whenever a WDT match interrupt occurs. This interrupt must be cleared by writing a ‘1’ to the same bit (WDT_MATCH bit of SRSS_INTR). Clearing the interrupt resets the watchdog. If the firmware does not clear the interrupt for two consecutive occasions, the third interrupt generates a device reset.

In addition, the WDT provides an option to set the number of bits to be used for comparison. The IGNORE_BITS bits [19:16] of the WDT_MATCH register is used for this purpose. These bits configure the number of MSBs to ignore from the 16-bit count value while performing the match. For instance, when the value of these bits equals 3, the MSb 3 bits are ignored while performing the match and the WDT counter behaves similar to a 13-bit counter. Note that these bits do not reduce the counter size – the WDT_CNT register still counts from 0 to 65535 (16-bit).

The WDT can be enabled or disabled using the WDT_EN bit [0] of the WDT_CTL register. The WDT_CTL register provides a mechanism to lock the WDT configuration registers. The WDT_LOCK bits [31:30] control the lock status of the WDT registers. These bits are special bits, which can enable the lock in a single write; to release the lock, two different writes are required. The WDT_LOCK bits protect the WDT_EN bit, WDT_MATCH register, CLK_ILO_CONFIG register, and LFCLK_SEL bits [1:0] of the CLK_SELECT register.

Table 22-1 explains various registers and bitfields used to configure and use the WDT.
22.3.2 Watchdog Reset

A watchdog is typically used to protect the device against firmware/system crashes or faults. When the WDT is used to protect against system crashes, the WDT interrupt bit should be cleared from a portion of the code that is not directly associated with the WDT interrupt. Otherwise, even if the main function of the firmware crashes or is in an endless loop, the WDT interrupt vector can still be intact and feed the WDT periodically.

The safest way to use the WDT against system crashes is to:

- Configure the watchdog reset period such that firmware is able to reset the watchdog at least once during the period, even along the longest firmware delay path.
- Reset (feed) the watchdog by clearing the interrupt bit regularly in the main body of the firmware code by writing a ‘1’ to the WDT_MATCH bit in the SRSS_INTR register. Note that this does not reset the watchdog counter, it feeds only the watchdog so that it does not cause a reset for the next two match events.

Do not reset the watchdog (clear interrupt) in the WDT interrupt service routine (ISR) if WDT is being used as a reset source to protect the system against crashes. Therefore, do not use the WDT reset feature and ISR together.

The recommended steps to use WDT as a reset source are as follows:

1. Make sure the WDT configuration is unlocked by clearing the WDT_LOCK bits[31:30] of the WDT_CTL register. Note that clearing the bits requires two writes to the register with each write clearing one bit as explained in Table 22-1.
2. Write the desired IGNORE_BITS in the WDT_MATCH register to set the counter resolution to be used for the match.
3. Write any match value to the WDT_MATCH register. The match value does not control the period of watchdog reset as the counter is not reset on a match event. This value provides an option to control only the first interrupt interval, after that the successive interrupts’ period is defined by the IGNORE_BITS. Approximate watchdog period is given by the following equation:

   \[
   \text{Watchdog reset period} = \text{ILO}_{\text{period}} \times (2 \times 2^{16 - \text{IGNOREBITS}} + \text{WDT_MATCH})
   \]

   Equation 22-1

4. Set the WDT_MATCH bit in the SRSS_INTR register to clear any pending WDT interrupt.
5. Enable ILO by setting the ENABLE bit [31] of the CLK_ILO_CONFIG register.
6. Enable the WDT by setting the WDT_EN bit in WDT_CTL register.

---

Table 22-1. Free-running WDT Configuration Options

<table>
<thead>
<tr>
<th>Register [Bit_Pos]</th>
<th>Bit_Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>WDT_CTL[0]</td>
<td>WDT_EN</td>
<td>Enable or disable the watchdog reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: WDT reset disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: WDT reset enabled</td>
</tr>
<tr>
<td>WDT_CTL[31:30]</td>
<td>WDT_LOCK</td>
<td>Lock or unlock write access to the watchdog configuration and clock related registers. When the bits are set, the lock is enabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: No effect</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Clear bit 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2: Clear bit 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3: Set both bit 0 and 1 (lock enabled)</td>
</tr>
<tr>
<td>WDT_CNT[15:0]</td>
<td>COUNTER</td>
<td>Current value of WDT counter</td>
</tr>
<tr>
<td>WDT_MATCH[15:0]</td>
<td>MATCH</td>
<td>Match value to a generate watchdog match event or interrupt</td>
</tr>
<tr>
<td>WDT_MATCH[19:16]</td>
<td>IGNORE_BITS</td>
<td>Number of MSbs of the WDT_CNT register to ignore for comparison with the MATCH value. Up to 12 MSbs can be ignored; settings above 12 act similar to a setting of 12.</td>
</tr>
<tr>
<td>SRSS_INTR[0]</td>
<td>WDT_MATCH</td>
<td>WDT interrupt request</td>
</tr>
<tr>
<td></td>
<td></td>
<td>This bit is set whenever a watchdog match event happens. The WDT interrupt is cleared by writing a ‘1’ to this bit</td>
</tr>
<tr>
<td>SRSS_INTR_MASK[0]</td>
<td>WDT_MATCH</td>
<td>Mask for the WDT interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: WDT interrupt is not masked to CPU</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: WDT interrupt is masked to CPU</td>
</tr>
</tbody>
</table>
7. Lock the WDT and ILO configuration by writing ‘3’ to the WDT_LOCK bits. This also locks the LFCLK_SEL bits of the CLK_SELECT register.
8. In the firmware, write ‘1’ to the WDT_MATCH bit in the SRSS_INT register to feed (clear interrupt) the watchdog.

22.3.3 Watchdog Interrupt

In addition to generating a device reset, the WDT can be used to generate interrupts. The watchdog counter can send interrupt requests to the CPU in Active power modes and to the wakeup interrupt controller (WIC) in Sleep and Deep Sleep power modes. In addition, the watchdog is capable of waking up the device from Hibernate power mode. It works as follows:

- **Active/LPACTIVE Mode**: In Active/LPACTIVE power mode, the WDT can send the interrupt to the CPU. The CPU acknowledges the interrupt request and executes the ISR. Clear the interrupt in the ISR.

- **Sleep/LPSLEEP or Deep Sleep Mode**: In this mode, the CPU subsystem is powered down. Therefore, the interrupt request from the WDT is directly sent to the WIC, which then wakes up the CPU. The CPU acknowledges the interrupt request and executes the ISR. Clear the interrupt in the ISR firmware.

- **Hibernate Mode**: In this mode, the entire device except a few peripherals (such as WDT and LPCOMP) are powered down. Any interrupt to wake up the device in this mode results in a device reset. Hence, there is no interrupt service routine or mechanism associated with this mode.

For more details on device power modes, see the [Device Power Modes chapter on page 128](#).

Because of its free-running nature, the WDT should not be used for periodic interrupt generation. Use the MCWDT instead; see [22.4 Multi-Counter WDTs](#). The MCWDT counters can be used to generate periodic interrupts. If absolutely required, follow these steps to use the WDT as a periodic interrupt generator:

1. Write the desired IGNORE_BITS in the WDT_MATCH register to set the counter resolution to be used for the match.
2. Write the desired match value to the WDT_MATCH register.
3. Set the WDT_MATCH bit in the SRSS_INTR register to clear any pending WDT interrupt.
4. Enable the WDT interrupt to CPU by setting the WDT_MATCH bit in SRSS_INTR_MASK.
5. Enable SRSS interrupt to the CPU by configuring the appropriate ISER register (See the [Interrupts chapter on page 47](#) for details).
6. In the ISR, clear the WDT interrupt and add the desired match value to the existing match value. By doing so, another interrupt is generated when the counter reaches the new match value (period).

Note that interrupt servicing and watchdog reset cannot be used simultaneously using the free-running WDT.

22.4 Multi-Counter WDTs

22.4.1 Overview

Figure 22-3 shows the functional overview of a single multi-counter WDT block. The PSoC 6 MCU includes two MCWDT blocks. Each MCWDT block includes two 16-bit counters (MCWDTx_WDT0 and MCWDTx_WDT1) and one 32-bit counter (MCWDTx_WDT2). These counters can be configured to work independently or in cascade (up to 64-bit). The 16-bit counters have the ability to generate an interrupt and reset the device. The 32-bit counter can only generate an interrupt. All the counters are clocked by LFCLK.

**Note**: Because the PSoC 6 MCU includes two CPUs (Cortex-M0+ and Cortex-M4), associate one MCWDT block to only one CPU during runtime. Although both the MCWDT blocks are available to both the CPUs, a single MCWDT is not intended to be used by multiple CPUs simultaneously.
22.4.1.1 WDT0 and WDT1 Counters Operation

MCWDTx_WDT0 and MCWDTx_WDT1 are 16-bit up counters, which can be configured to be a 16-bit free-running counter or a counter with any 16-bit period. These counters can be used to generate an interrupt or reset.

The WDT_CTR0 bits [15:0] and WDT_CTR1 bits [16:31] of the MCWDTx_CNTLLOW register holds the current counter values of WDT0 and WDT1 respectively. The WDT_MATCH0 bits [15:0] and WDT_MATCH1 bits [16:31] of the MCWDTx_MATCH register store the match value for WDT0 and WDT1 respectively. The WDT_MODEx bits of the MCWDTx_CONFIG register configure the action the watchdog counter takes on a match event (WDT_MATCHx == WDT_CTRx). The WDT0/WDT1 counters perform the following actions:

- Assert interrupt (WDT_INTx) on match
- Assert a device reset on match
- Assert an interrupt on match and a device reset on the third unhandled interrupt

In addition to generating reset and interrupt, the match event can be configured to clear the counters. This is done by setting the WDT_CLEARx bit of the MCWDTx_CONFIG register. WDT0/WDT1 counter operation is shown in Figure 22-4.
Watchdog Timer

Figure 22-4. WDT0/WDT1 Operation

Table 22-2. WDT0 and WDT1 Configuration Options

<table>
<thead>
<tr>
<th>Register [Bit_Pos]</th>
<th>Bit_Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCWDTx_CONFIG[1:0]</td>
<td>WDT_MODE0</td>
<td>WDT action on a match event (WDT_CTRx == WDT_MATCHx)</td>
</tr>
<tr>
<td>MCWDTx_CONFIG[9:8]</td>
<td>WDT_MODE1</td>
<td>0: Do nothing</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Assert interrupt (WDT_INTx)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2: Assert device reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3: Assert interrupt on match and a device reset on the third unhandled interrupt</td>
</tr>
<tr>
<td>MCWDTx_CONFIG[2]</td>
<td>WDT_CLEAR0</td>
<td>Clear the WDTx counter on match. In other words, (WDT_MATCHx + 1) acts similar</td>
</tr>
<tr>
<td>MCWDTx_CONFIG[10]</td>
<td>WDT_CLEAR1</td>
<td>to a period for the WDTx counter.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Free-running counter</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Clear WDT_CTRx bits on match</td>
</tr>
<tr>
<td>MCWDTx_CNTLOW[15:0]</td>
<td>WDT_CTR0</td>
<td>Current watchdog counter value. Bits[15:0] contain the current value of WDT0</td>
</tr>
<tr>
<td>MCWDTx_CNTLOW[16:31]</td>
<td>WDT_CTR1</td>
<td>counter and bits[31:16] contain the current value of WDT1 counter.</td>
</tr>
<tr>
<td>MCWDTx.Match[15:0]</td>
<td>WDT_MATCH0</td>
<td>Watchdog match value</td>
</tr>
<tr>
<td>MCWDTx.Match[16:31]</td>
<td>WDT_MATCH1</td>
<td>Changing WDT_MATCH requires 1.5 LFCLK cycles to come into effect. After</td>
</tr>
<tr>
<td></td>
<td></td>
<td>changing WDT_MATCH, do not enter the Deep Sleep mode for at least one LFCLK</td>
</tr>
<tr>
<td></td>
<td></td>
<td>cycle to ensure the WDT updates to the new setting.</td>
</tr>
</tbody>
</table>
22.4.1.2 WDT2 Counter Operation

The MCWDTx_WDT2 is a 32-bit free-running counter, which can be configured to generate an interrupt. The MCWDTx_CNTHIGH register holds the current value of the WDT2 counter. WDT2 does not support a match feature. However, it can be configured to generate an interrupt when one of the counter bits toggle. The WDT_BITS2 bits [28:24] of the MCWDTx_CONFIG register selects the bit on which the WDT2 interrupt is asserted. WDT_MODE2 bit [16] of the MCWDTx_CONFIG register decides whether to assert an interrupt on bit toggle or not. Figure 22-5 shows the WDT2 counter operation.

Figure 22-5. WDT2 Operation
Watchdog Timer

22.4.2 Enabling and Disabling WDT

The WDT counters are enabled by setting the WDT_ENABLEEx bit in the MCWDTx_CTL register and are disabled by clearing it. Enabling or disabling a WDT requires 1.5 LFCLK cycles to come into effect. Therefore, the WDT_ENABLEEx bit value must not be changed more than once in that period and the WDT_ENABLEx bit of the MCWDTx_CTL register can be used to monitor enabled/disabled state of the counter.

The WDT_RESETx bit of the MCWDTx_CTL register clears the corresponding WDTx counter when set in firmware. The hardware clears the bit after the WDTx counter resets. This option is useful when the WDT0 or WDT1 is configured to generate a device reset on a match event. In such cases, the device resets when the counter reaches the match value. Thus, setting the WDT_RESET0 or WDT_RESET1 bit resets the WDT0 or WDT1 counter respectively, preventing device reset.

After WDT is enabled, do not write to the WDT configuration (MCWDTx_CONFIG) and control (MCWDTx_CTL) registers. Accidental corruption of WDT registers can be prevented by setting the WDT_LOCK bits [31:30] of the MCWDTx_CTL register. If the application requires updating the match value (WDT_MATCH) when the WDT is running, the WDT_LOCK bits must be cleared. The WDT_LOCK bits require two different writes to clear both the bits. Writing a ‘1’ to the bits clears bit 0. Writing a ‘2’ clears bit 1. Writing a ‘3’ sets both the bits and writing ‘0’ does not have any effect. Note that the WDT_LOCK bits protects only MCWDTx_CTL (except the WDT_LOCK bits), MCWDTx_CONFIG, and MCWDTx_MATCH registers. The LFCLK select registers are protected by the free-running WDT lock bits.

### Table 22-3. WDT2 Configuration Options

<table>
<thead>
<tr>
<th>Register [Bit_Pos]</th>
<th>Bit_Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCWDTx_CONFIG[16]</td>
<td>WDT_MODE2</td>
<td>WDT2 mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Free-running counter</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Free-running counter with interrupt (WDT_INTx) request generation when specified, but in MCWDTx_CNTHIGH register toggles</td>
</tr>
<tr>
<td>MCWDTx_CONFIG[28:24]</td>
<td>WDT_BITS2</td>
<td>Bit to monitor for WDT2 interrupt assertion</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Asserts when bit [0] of MCWDTx_CNTHIGH register toggles (interrupt every tick)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>......</td>
</tr>
<tr>
<td></td>
<td></td>
<td>31: Asserts when bit [0] of MCWDTx_CNTHIGH register toggles (interrupt every 2^{31} ticks)</td>
</tr>
<tr>
<td>MCWDTx_CNTHIGH[31:0]</td>
<td>WDT_CTR2</td>
<td>Current counter value of WDT2</td>
</tr>
</tbody>
</table>

### Table 22-4. Watchdog Configuration Options

<table>
<thead>
<tr>
<th>Register [Bit_Pos]</th>
<th>Bit_Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCWDTx_CTL[0]</td>
<td>WDT_ENABLE0</td>
<td>Enable WDT counter x</td>
</tr>
<tr>
<td>MCWDTx_CTL[8]</td>
<td>WDT_ENABLE1</td>
<td>0: Counter is disabled</td>
</tr>
<tr>
<td>MCWDTx_CTL[16]</td>
<td>WDT_ENABLE2</td>
<td>1: Counter is enabled</td>
</tr>
<tr>
<td>MCWDTx_CTL[1]</td>
<td>WDT_ENABLED0</td>
<td>Indicates the actual enabled/disabled state of the counter. This bit should be monitored after changing the WDT_ENABLEEx bit, to receive an acknowledgment of the change</td>
</tr>
<tr>
<td>MCWDTx_CTL[9]</td>
<td>WDT_ENABLED1</td>
<td></td>
</tr>
<tr>
<td>MCWDTx_CTL[17]</td>
<td>WDT_ENABLED2</td>
<td></td>
</tr>
<tr>
<td>MCWDTx_CTL[3]</td>
<td>WDT_RESET0</td>
<td>Reset WDT counter x to 0. Hardware clears the bit when the reset is complete</td>
</tr>
<tr>
<td>MCWDTx_CTL[11]</td>
<td>WDT_RESET1</td>
<td>0: Software - No action, Hardware - Counter is reset after software sets this bit</td>
</tr>
<tr>
<td>MCWDTx_CTL[19]</td>
<td>WDT_RESET2</td>
<td>1: Software - Resets the counter, Hardware - Counter is not reset after software sets this bit</td>
</tr>
<tr>
<td>MCWDTx_CTL[31:30]</td>
<td>WDT_LOCK</td>
<td>Locks or unlocks write access to the MCWDTx_CTL (except the WDT_LOCK bits), MCWDTx_CONFIG, and MCWDTx_MATCH registers. When the bits are set, the lock is enabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: No effect</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Clears bit 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2: Clears bit 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3: Sets both bit 0 and 1 (lock enabled)</td>
</tr>
</tbody>
</table>
Note: When the watchdog counters are configured to generate an interrupt every LFCLK cycle, make sure you read the MCWDTx_INTR register after clearing the watchdog interrupt (setting the WDT_INTx bit in the MCWDTx_INTR register). Failure to do this may result in missing the next interrupt. Hence, the interrupt cycle becomes LFCLK/2.

22.4.3 Watchdog Cascade Options

The cascade configuration shown in Figure 22-3 provides an option to increase the WDT counter resolution. The WDTCASCADE0_1 bit [3] of the MCWDTx_CONFIG register cascades WDT0 and WDT1 and the WDTCASCADE1_2 bit [11] of the MCWDTx_CONFIG register cascades WDT1 and WDT2. Note that cascading two 16-bit counters does not provide a 32-bit counter; instead, you get a 16-bit period counter with a 16-bit prescaler. For example, when cascading WDT0 and WDT1, WDT0 acts as a prescaler for WDT1 and the prescaler value is defined by the WDT_MATCH0 bits [15:0] in the MCWDTx_MATCH register. The WDT1 has a period defined by WDT_MATCH1 bits [31:16] in the MCWDTx_MATCH register. The same logic applies to WDT1 and WDT2 cascading.

Table 22-5. Watchdog Cascade Options

<table>
<thead>
<tr>
<th>Register [Bit_Pos]</th>
<th>Bit_Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCWDTx_CONFIG[3]</td>
<td>WDTCASCADE0_1</td>
<td>Cascade WDT0 and WDT1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: WDT0 and WDT1 are independent counters</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: WDT1 increments two cycles after WDT_CTR0 == WDT_MATCH0</td>
</tr>
<tr>
<td>MCWDTx_CONFIG[11]</td>
<td>WDTCASCADE1_2</td>
<td>Cascade WDT1 and WDT2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: WDT1 and WDT2 are independent counters</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: WDT2 increments two cycles after WDT_CTR1 == WDT_MATCH1</td>
</tr>
</tbody>
</table>

When using cascade (WDTCASCADE0_1 or WDTCASCADE1_2 set), resetting the counters when the prescaler or lower counter is at its match value with the counter configured to clear on match, results in the upper counter incrementing to 1 instead of remaining at 0. This behavior can be corrected by issuing a second reset to the upper counter after approximately 100 µs from the first reset. Note that the second reset is required only when the first reset is issued while the prescaler counter value is at its match value. Figure 22-6 illustrates the behavior when WDT0 and WDT1 are cascaded along with the second reset timing.
In addition, the counters exhibit non-monotonicity in the following cascaded conditions:

- If WDT_CASCADE0_1 is set, then WDT_CTR1 does not increment the cycle after WDT_CTR0 = WDT_MATCH0.
- If WDT_CASCADE1_2 is set, then WDT_CTR2 does not increment the cycle after WDT_CTR1 = WDT_MATCH1.
- If both WDT_CASCADE0_1 and WDT_CASCADE1_2 are set, then WDT_CTR2 does not increment the cycle after WDT_CTR1 = WDT_MATCH1 and WDT_CTR1 does not increment the cycle after WDT_CTR0 = WDT_MATCH0.

When cascading is enabled, always read the WDT_CTR1 or WDT_CTR2 counter value only when the prescaler counter (WDT_CTR0 or WDT_CTR1) value is not 0. This makes sure the upper counter is incremented after a match event in the prescaler counter.

### 22.4.4 Watchdog Reset

WD0 and WD1 counters can be configured to generate a device reset similar to the free-running WDT reset. Follow these steps to use the WD0 or WD1 counter of a MCWDTx block to generate a system reset:

1. Configure the WDx to generate a reset using the WDT_MODEx bits in MCWDTx_CONFIG. Configure the WDT_MODE0 or WDT_MODE1 bits in MCWDTx_CONFIG to '2' (reset on match) or '3' (interrupt on match and reset on the third unhandled interrupt).

2. Optionally, set the WDT_CLEAR0 or WDT_CLEAR1 bit in the MCWDTx_CONFIG register for WD0 or WD1 to reset the corresponding watchdog counter to '0' on a match event. Otherwise, the counters are free running. See Table 22-2 on page 191 for details.

3. Calculate the watchdog reset period such that firmware is able to reset the watchdog at least once during the period, even along the longest firmware delay path. For WDT_MODEx == 2, match value is same as the watchdog period. For WDT_MODEx == 3, match value is one-third of the watchdog period. Write the calculated match value to the WDT_MATCH register for WD0 or WD1. Optionally, enable cascading to increase the interval. **Note:** The legal value for the WDT_MATCH field is 1 to 65535.

4. For WDT_MODEx == 2, set the WDT_RESETx bit in the MCWDTx_CONFIG register to reset the WDx counter to 0. For WDT_MODEx == 3, set the WDT_INTx bit in MCWDTx_INTR to clear any pending interrupts.

5. Enable WDx by setting the WDT_ENABLEx bit in the MCWDTx_CTL register. Wait until the WDT_ENABLEx bit is set.

6. Lock the MCWDTx configuration by setting the WDT_LOCK bits of the MCWDTx_CTL register.

7. In the firmware, feed (reset) the watchdog as explained in step 4.

Do not reset watchdog in the WDx ISR. It is also not recommended to use the same watchdog counter to generate a system reset and interrupt. For example, if WD0 is used to generate system reset against crashes, then WD1 or WD2 should be used for periodic interrupt generations.

### 22.4.5 Watchdog Interrupt

When configured to generate an interrupt, the WDT_INTx bits of the MCWDTx_INTR register provide the status of any pending watchdog interrupts. The firmware must clear the interrupt by setting the WDT_INTx. The WDT_INTx bits of the MCWDTx_INTR_MASK register mask the corresponding WDx interrupt of the MCWDTx block to the CPU.

Follow these steps to use WDx as a periodic interrupt generator:

1. Write the desired match value to the WDT_MATCH register for WD0/WD1 or the WDT_BITS2 value to the MCWDTx_CONFIG register for WD2. **Note:** The legal value for the WDT_MATCH field is 1 to 65535.

2. Configure the WDx to generate an interrupt using the WDT_MODEx bits in MCWDTx_CONFIG. Configure the WDT_MODE0 or WDT_MODE1 bits in MCWDTx_CONFIG for WD0 or WD1 to '1' (interrupt on match) or '3' (interrupt on match and reset on third unhandled interrupt). For WD2, set the WDT_MODE2 bit in the MCWDTx_CONFIG register.

3. Set the WDT_INT bit in MCWDTx_INTR to clear any pending interrupt.

4. Set the WDT_CLEAR0 or WDT_CLEAR1 bit in the MCWDTx_CONFIG register for WD0 or WD1 to reset the corresponding watchdog counter to '0' on a match event.

5. Mask the WDx interrupt to the CPU by setting the WDT_INTx bit in the MCWDTx_INTR_MASK register.

6. Enable WDx by setting the WDT_ENABLEx bit in the MCWDTx_CTL register. Wait until the WDT_ENABLEx bit is set.

7. Enable MCWDTx interrupt to the CPU by configuring the appropriate ISER register. Refer to the Interrupts chapter on page 47.

8. In the ISR, clear the WDx interrupt by setting the WDT_INTx bit in the MCWDTx_INTR register.

Note that interrupts from all three WDx counters of the MCWDT block are mapped as a single interrupt to the CPU. In the interrupt service routine, the WDT_INTx bits of the MCWDTx_INTR register can be read to identify the interrupt source. However, each MCWDT block has its own interrupt to the CPU. For details on interrupts, see the Interrupts chapter on page 47.

The MCWDT block can send interrupt requests to the CPU in Active power mode and to the WIC in Sleep and Deep power modes.
Sleep power modes. It works similar to the free-running WDT.

### 22.5 Reset Cause Detection

The `RESET_WDT` bit [0] in the `RES_CAUSE` register indicates the reset generated by the free-running WDT. The `RESET_MCWDTx` bit in the `RES_CAUSE` register indicates the reset generated by the MCWDTx block. These bits remain set until cleared or until a power-on reset (POR), brownout reset (BOD), or external reset (XRES) occurs. All other resets leave this bit unaltered.

For more details, see the Reset System chapter on page 161.

### 22.6 Register List

Table 22-6. WDT Registers

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>WDT_CTL</td>
<td>Watchdog Counter Control Register</td>
</tr>
<tr>
<td>WDT_CNT</td>
<td>Watchdog Counter Count Register</td>
</tr>
<tr>
<td>WDT_MATCH</td>
<td>Watchdog Counter Match Register</td>
</tr>
<tr>
<td>MCWDTx_MCWDT_CNTLOW</td>
<td>Multi-counter WDT Sub-counters 0/1</td>
</tr>
<tr>
<td>MCWDTx_MCWDT_CNTHIGH</td>
<td>Multi-counter WDT Sub-counter 2</td>
</tr>
<tr>
<td>MCWDTx_MCWDT_MATCH</td>
<td>Multi-counter WDT Counter Match Register</td>
</tr>
<tr>
<td>MCWDTx_MCWDT_CONFIG</td>
<td>Multi-counter WDT Counter Configuration</td>
</tr>
<tr>
<td>MCWDTx_MCWDT_CTL</td>
<td>Multi-counter WDT Counter Control</td>
</tr>
<tr>
<td>MCWDTx_MCWDT_INTR</td>
<td>Multi-counter WDT Counter Interrupt Register</td>
</tr>
<tr>
<td>MCWDTx_MCWDT_INTR_SET</td>
<td>Multi-counter WDT Counter Interrupt Set Register</td>
</tr>
<tr>
<td>MCWDTx_MCWDT_INTR_MASK</td>
<td>Multi-counter WDT Counter Interrupt Mask Register</td>
</tr>
<tr>
<td>MCWDTx_MCWDT_INTR_MASKED</td>
<td>Multi-counter WDT Counter Interrupt Masked Register</td>
</tr>
<tr>
<td>CLK_SELECT</td>
<td>Clock Selection Register</td>
</tr>
<tr>
<td>CLK_ILO_CONFIG</td>
<td>ILO Configuration</td>
</tr>
<tr>
<td>SRSS_INTR</td>
<td>SRSS Interrupt Register</td>
</tr>
<tr>
<td>SRSS_INTR_SET</td>
<td>SRSS Interrupt Set Register</td>
</tr>
<tr>
<td>SRSS_INTR_MASK</td>
<td>SRSS Interrupt Mask Register</td>
</tr>
<tr>
<td>SRSS_INTR_MASKED</td>
<td>SRSS Interrupt Masked Register</td>
</tr>
<tr>
<td>RES_CAUSE</td>
<td>Reset Cause Observation Register</td>
</tr>
</tbody>
</table>
Every peripheral in the PSoC 6 MCU is interconnected using trigger signals. Trigger signals are means by which peripherals denote an occurrence of an event or a state. These triggers are used as means to affect or initiate some action in other peripherals. The trigger multiplexer block helps to route triggers from a source peripheral block to a destination.

23.1 Features

- Ability to connect any trigger signal from one peripheral to another
- Two-layer architecture with 15 trigger groups
- Supports a software trigger, which can trigger any signal in the block
- Ability to configure a trigger multiplexer with trigger manipulation features in hardware such as inversion and edge/level detection

23.2 Architecture

The trigger signals in the PSoC 6 MCU are digital signals generated by peripheral blocks to denote a state such as FIFO level, or an event such as the completion of an action. These trigger signals typically serve as initiator of other actions in other peripheral blocks. An example is an ADC peripheral block sampling three channels. After the conversion is complete, a trigger signal will be generated, which in turn triggers a DMA channel that transfers the ADC data to a memory buffer. This example is shown in Figure 23-1.

A PSoC 6 MCU has multiple peripheral blocks; each of these blocks can be connected to other blocks through trigger signals, based on the system implementation. To support this, the PSoC 6 MCU has hardware, which is a series of multiplexers used to route the trigger signals from potential sources to destinations. This hardware is called the trigger multiplexer block. The trigger multiplexer can connect to any trigger signal emanating out of any peripheral block in the PSoC 6 MCU and route it to any other peripheral to initiate or affect an operation at the destination peripheral block.

23.2.1 Trigger Multiplexer Group

The trigger multiplexer block is implemented using several trigger multiplexers. A trigger multiplexer selects a signal from a set of trigger output signals from different peripheral blocks to route it to a specific trigger input of another peripheral block. The multiplexers are grouped into trigger groups. All the trigger multiplexers in a trigger group have similar input options and are designed to feed similar destination signals. Hence the trigger group can be considered as a block that multiplexes multiple inputs to multiple outputs. This concept is illustrated in Figure 23-2.
23.2.2 Trigger Multiplexer Block Architecture

Multiple trigger multiplexer groups in a device are combined to form the trigger multiplexer block. The trigger multiplexer block is responsible for the entire trigger routing in the device. The trigger multiplexer block is architected into two layers. Each layer is formed by a separate set of multiple trigger groups.

The input side has reduction multiplexer groups, which have input options that are trigger outputs coming from the different peripheral blocks and routes it to different intermediate trigger signals. These intermediate signals are routed out to peripheral trigger inputs through the distribution trigger groups that form the output side layer.

Figure 23-3 shows the architecture of the trigger multiplexer block in the PSoC 6 MCU. All the trigger signals coming from different peripheral blocks in the device are routed to the trigger multiplexer inputs. The reduction multiplexer groups take care of reducing these trigger multiplexer inputs to intermediate signals. These intermediate signals form as inputs to the distribution multiplexer groups and are multiplexed into trigger multiplexer outputs, which are connected to different peripheral blocks as their trigger inputs signals.

The reduction multiplexer group layer and the distribution multiplexer group layer are implemented using multiple trigger multiplexer groups. Figure 23-3 illustrates a generic trigger multiplexer block implementation with a reduction multiplexer layer of N trigger groups and a distribution multiplexer layer of M trigger groups.
23.2.3 Trigger Multiplexer Routing

The use case of a trigger multiplexer block is to route trigger signals from a source peripheral signal to a destination peripheral. To accomplish this, you must:

1. Identify the reduction trigger group and the distribution trigger group that will be used to accomplish the routing. The trigger groups are typically numbered continuously. A consecutive set of trigger group numbers will represent all reduction multiplexers and another set will represent the distribution multiplexers. See Table 23-1 for more details. The reduction trigger multiplexer group can be identified based on the trigger input signal or from what peripheral block the trigger signal is sourced. The distribution multiplexer group is determined based on the output or to what peripheral block the trigger needs to be routed.

2. After the two groups are identified, identify the specific trigger multiplexer in the group that must be configured. To route a signal from a source to the destination you should configure two trigger multiplexers, one from a reduction group and another from a distribution group.

3. Configuring the trigger multiplexers is similar for both reduction and distribution multiplexers. All the multiplexers have the same register structure. A PERI.TR_GROUP.TR_OUT_CTL register is associated with every trigger multiplexer in the block. You can configure the input that is connected to the multiplexer’s output by configuring the TR_SEL bits in this register. Some multiplexers also allow enabling trigger manipulation features such as inversion and edge/level detection. These features can also be enabled in the PERI.TR_GROUP.TR_OUT_CTL register, associated with the trigger multiplexer.

23.2.4 Software Triggers

All input and output signals to a trigger multiplexer can be triggered from software. This is accomplished by writing into the PERI.TR_CMD register. This register allows you to trigger the corresponding signal for a number of peripheral clock cycles.

The PERI.TR_CMD[GROUP_SEL] bitfield selects the trigger group of the signal being activated. The PERI.TR_CMD[OUT_SEL] bitfield determines whether the trigger signal is in output or input of the multiplexer. PERI.TR_CMD[TR_SEL] selects the specific line in the trigger group.

The PERI.TR_CMD[COUNT] bitfield sets up the number of peripheral clocks the trigger will be activated.

The PERI.TR_CMD[ACTIVATE] bitfield is set to ‘1’ to activate the trigger line specified. Hardware resets this bit.
after the trigger is deactivated after the number of cycles set by the PERI.TR_CMD[COUNT].

Trigger signals that are software triggered may have some implications. If the output of a distribution multiplexer is being triggered, only the peripheral block trigger that the signal feeds is triggered. If an input of a reduction multiplexer is being triggered, then all the peripheral routes that connect to this signal through the trigger multiplexer block will be triggered. You should be aware of the routing that is being configured before deciding on the trigger signal. For distribution multiplexers, each trigger group will have its own clock_source, which will be used for trigger_manipulation and for generating software_trigger.

23.3 PSoC 6 MCU Trigger Multiplexer Block

The trigger multiplexer block architecture can vary between device families. Figure 23-4 illustrates the trigger multiplexer block architecture of the PSoC 6 MCU. Note that there are reduction and distribution multiplexer groups in the architecture. Trigger groups 0 to 8 are distribution multiplexer groups and trigger groups 9 to 14 are reduction multiplexer groups. Table 23-1 provides a summary of all trigger groups and their usage.

This architecture has exceptions to the two-layer architecture such as the paths to USB burst-end signals and UDB acknowledge signals. These signals require only one trigger multiplexer to be configured for routing.

23.4 Register List

Table 23-1. Register List

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PERI.TR_CMD</td>
<td>Trigger command register. The control enables software activation of a specific input trigger or output trigger of the trigger multiplexer structure.</td>
</tr>
<tr>
<td>PERI.TR_GROUP.TR_OUT_CTL</td>
<td>This register specifies the input trigger for a specific output trigger in a trigger group.</td>
</tr>
</tbody>
</table>
Figure 23-4. PSoC 6 MCU Trigger Multiplexer Block Architecture
24. Energy Profiler

The PSoC 6 MCU Profiler enables measurement of the relative amount of energy consumed by particular peripherals. Functions such as DMA transfers or buffered serial communications can happen asynchronously, and are not directly tied to the CPU or code execution. Traditional energy profilers correlate energy consumption to the program counter, which helps you understand when power is consumed. The profiler provides additional insight into the device so you can identify an asynchronous activity that causes energy consumption. In other words, the profiler helps you understand where power is consumed.

The profiler manages a set of counters. You configure an available counter to monitor a particular source. Depending on the nature of the source, you count either duration (reference clock cycles) or the number of events.

However, an event from one source may use more or less energy than an event from another source. Each source has a predetermined coefficient. You can use this coefficient to adjust the counter value proportional to the amount of energy consumed by the source. This enables the profiler to determine the relative amount of energy consumed by that source as compared to other sources.

The ability to monitor specific peripherals enables you to understand and optimize energy consumption, including:
- Identify the cause of energy consumption
- Identify the cause of energy consumption unrelated to currently executing code on the CPUs

24.1 Features

The profiler has these features and capabilities:
- A variety of sources you can monitor (DMA, flash read, serial bus communication, and so forth)
- Support for eight counters, to monitor up to eight sources simultaneously
- For each counter you specify:
  - what source to monitor (can be changed dynamically if required)
  - what to measure (duration or events)
  - what reference clock to use for the count (only affects duration)
- Enables identifying the cause of energy consumption by asynchronous events
- Provides ability to easily detect energy usage that may be difficult to measure by external monitoring
- Provides an absolute count of events or reference clock cycles for each monitored source
- Provides the relative energy consumption for each monitored source (based on the coefficient for that source)
24.2 Architecture

The profiler supports up to 32 counters. The actual number of counters is hardware dependent.

24.2.1 Profiler Design

With the profiler you can monitor:

- Peripherals that operate asynchronously to software
- CPU activity

This includes flash access, DMA, and other processes. See Available Monitoring Sources on page 204.

You can measure total energy consumption directly using external hardware. The profiler measures energy consumption indirectly, and requires no external probe or measuring device.

The profiler counts either the amount of time that a source is active (duration) or the number of events that occur. To derive relative energy consumption for each source, you can multiply the absolute count (reference clock cycles or events) for that source by a counter value weighting coefficient. The profiler does not report the actual amount of energy consumed.

Many of the sources available for monitoring are asynchronous operations where the cause of energy consumption may be difficult to identify using external hardware. See Available Monitoring Sources on page 204.

Your application may use a system resource or peripheral that is not among the profiler sources, for example an ADC. A complete understanding of your application's energy consumption requires that you profile those parts of your code that use those other systems. For example, you could determine the time the peripheral is in use, and then derive energy use based on power consumption data from the data sheet, or external power monitoring.

All counters that are in use start and stop at the same time. The time between start and stop is called the profiling window, or the profiling session. During the profiling session, each counter increments at its own rate based on the monitored signal and (if measuring duration) the selected reference clock. See Start and Stop Profiling on page 206.

Before starting a profiling session, configure the counters you want to use. See Configure and Enable a Counter on page 206.

You can get interim results during a profiling session, or final results after you stop profiling. See Get the Results on page 207.
24.2.2 Available Monitoring Sources

You specify which source a counter monitors. The available sources vary per device series. You can find constants in a header file named `<series>_config.h` (part of the Peripheral Driver Library). For example, Table 24-1 lists the sources in `psoc63_config.h`.

Table 24-1. Available Signals to Monitor

<table>
<thead>
<tr>
<th>Value</th>
<th>Symbol</th>
<th>Count</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>PROFILE_ONE</td>
<td>Duration</td>
<td>Constant One</td>
</tr>
<tr>
<td>1</td>
<td>CPUSS_MONITOR_CM0</td>
<td>Events</td>
<td>CM0+ active cycle count</td>
</tr>
<tr>
<td>2</td>
<td>CPUSS_MONITOR_CM4</td>
<td>Events</td>
<td>CM4 active cycle count</td>
</tr>
<tr>
<td>3</td>
<td>CPUSS_MONITOR_FLASH</td>
<td>Events</td>
<td>Flash read count</td>
</tr>
<tr>
<td>4</td>
<td>CPUSS_MONITOR_DW0_AHB</td>
<td>Events</td>
<td>DW0 AHB transfer count (DMA transfer)</td>
</tr>
<tr>
<td>5</td>
<td>CPUSS_MONITOR_DW1_AHB</td>
<td>Events</td>
<td>DW1 AHB transfer count (DMA transfer)</td>
</tr>
<tr>
<td>6</td>
<td>CPUSS_MONITOR_CRYPTO</td>
<td>Events</td>
<td>Crypto memory access count</td>
</tr>
<tr>
<td>7</td>
<td>USB_MONITOR_AHB</td>
<td>Events</td>
<td>USB AHB transfer count</td>
</tr>
<tr>
<td>8</td>
<td>SCB0_MONITOR_AHB</td>
<td>Events</td>
<td>SCB 0 AHB transfer count</td>
</tr>
<tr>
<td>9</td>
<td>SCB1_MONITOR_AHB</td>
<td>Events</td>
<td>SCB 1 AHB transfer count</td>
</tr>
<tr>
<td>10</td>
<td>SCB2_MONITOR_AHB</td>
<td>Events</td>
<td>SCB 2 AHB transfer count</td>
</tr>
<tr>
<td>11</td>
<td>SCB3_MONITOR_AHB</td>
<td>Events</td>
<td>SCB 3 AHB transfer count</td>
</tr>
<tr>
<td>12</td>
<td>SCB4_MONITOR_AHB</td>
<td>Events</td>
<td>SCB 4 AHB transfer count</td>
</tr>
<tr>
<td>13</td>
<td>SCB5_MONITOR_AHB</td>
<td>Events</td>
<td>SCB 5 AHB transfer count</td>
</tr>
<tr>
<td>14</td>
<td>SCB6_MONITOR_AHB</td>
<td>Events</td>
<td>SCB 6 AHB transfer count</td>
</tr>
<tr>
<td>15</td>
<td>SCB7_MONITOR_AHB</td>
<td>Events</td>
<td>SCB 7 AHB transfer count</td>
</tr>
<tr>
<td>16</td>
<td>SCB8_MONITOR_AHB</td>
<td>Events</td>
<td>SCB 8 AHB transfer count</td>
</tr>
<tr>
<td>17–20</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>SMIF_MONITOR_SMIF_SPI_SELECT0</td>
<td>Duration</td>
<td>SPI select to memory 0 active</td>
</tr>
<tr>
<td>22</td>
<td>SMIF_MONITOR_SMIF_SPI_SELECT1</td>
<td>Duration</td>
<td>SPI select to memory 1 active</td>
</tr>
<tr>
<td>23</td>
<td>SMIF_MONITOR_SMIF_SPI_SELECT2</td>
<td>Duration</td>
<td>SPI select to memory 2 active</td>
</tr>
<tr>
<td>24</td>
<td>SMIF_MONITOR_SMIF_SPI_SELECT3</td>
<td>Duration</td>
<td>SPI select to memory 3 active</td>
</tr>
<tr>
<td>25</td>
<td>SMIF_MONITOR_SMIF_SPI_SELECT_ANY</td>
<td>Duration</td>
<td>SPI select to any of the memories 0-3 active</td>
</tr>
<tr>
<td>26</td>
<td>BLESS_EXT_LNA_RX_CTL_OUT</td>
<td>Duration</td>
<td>BLE Rx radio active</td>
</tr>
<tr>
<td>27</td>
<td>BLESS_EXT_PA_TX_CTL_OUT</td>
<td>Duration</td>
<td>BLE Tx radio active</td>
</tr>
</tbody>
</table>

24.2.3 Counter Value Weighting (Energy Coefficients)

The profiler counts reference clock cycles or events for the monitored source. This count represents the absolute number of clock cycles or events that occurred for the monitored source during the profiling session. If that is sufficient for your purposes, you do not need to use a coefficient.

However, different sources may consume relatively more or less energy per count. You can use a counter value weighting coefficient to adjust the counter value to reflect relative energy consumption. You can use any value for the coefficient that returns useful data.

The profiler is under development, and coefficients have not yet been defined. This document will be updated when they become available.

24.2.4 Reference Clocks

Each monitored source has its own clock reference, called the sample clock. Table 24-2 lists the six choices for the sample clock. You may use one of two CLK_PROFILE sources, or one of four CLK_REF sources.
The counter units of the profiler are clocked using either CLK_HF or CLK_PERI as CLK_PROFILE. You configure CLK_HF in system resources and CLK_PERI in the CPU subsystem. See Clocking System chapter on page 146 for details on clocks. In addition, there are four available reference clocks: CLK_TIMER, CLK_IMO, CLK_ECO, and CLK_LF. Any of the six clock sources can be used as the sample clock.

If you measure events, the sample clock is selected automatically to be either CLK_HF or CLK_PERI depending on the monitored source. The count represents the number of events that occurred during the profiling session. The profiler counts the edges of the monitored signal, using either CLK_HF or CLK_PERI to detect edges.

If you measure duration, you specify the sample clock from one of the six choices listed in Table 24-2. When you measure duration, while the monitored source is active, the counter increments at each cycle of the sample clock. The profiler synchronizes reference clocks with CLK_PROFILE. As a result the four available reference clocks cannot exceed CLK_PROFILE/2.

To measure duration accurately, the sample clock should have a stable frequency throughout the profiling session. If your application remains in active power states, you can use CLK_HF as the sample clock. CLK_HF gives you the greatest resolution in your results.

The profiler can be enabled in Active, Sleep, LPACTIVE, and LPSLEEP modes. However, clock frequencies can change based on the power state of the application. The source clock frequency should be stable throughout the profiling session to ensure reliable data. If your application goes into low-power states during the profiling session, CLK_HF or CLK_PERI do not provide a stable frequency because the frequency of CLK_PROFILE can vary across power states. For example, CLK_HF frequency drops to CLK_IMO frequency in low-power states. The fastest stable reference clock across the four power modes is CLK_TIMER configured to be CLK_IMO/2.

High-frequency clocks are not available in Deep Sleep and Hibernate power modes, so the profiler is disabled. The configuration registers maintain state through Deep Sleep. Profiler data is lost (registers are not maintained) in Hibernate mode. See the Device Power Modes chapter on page 128.

Table 24-2. Available Sample Clock Sources for the Profiler

<table>
<thead>
<tr>
<th>Value</th>
<th>Clock Source</th>
<th>Symbol</th>
<th>Clock Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Timer</td>
<td>CLK_TIMER</td>
<td>CLK_REF</td>
</tr>
<tr>
<td>1</td>
<td>Internal main oscillator</td>
<td>CLK_IMO</td>
<td>CLK_REF</td>
</tr>
<tr>
<td>2</td>
<td>External crystal oscillator</td>
<td>CLK_ECO</td>
<td>CLK_REF</td>
</tr>
<tr>
<td>3</td>
<td>Low frequency clock</td>
<td>CLK_LF</td>
<td>CLK_REF</td>
</tr>
<tr>
<td>4</td>
<td>High-frequency clock</td>
<td>CLK_HF</td>
<td>CLK_PROFILE</td>
</tr>
<tr>
<td>5</td>
<td>Peripheral clock</td>
<td>CLK_PERI</td>
<td>CLK_PROFILE</td>
</tr>
</tbody>
</table>

24.3 Using the Profiler

This section describes the steps required to use the profiler effectively. To use the profiler, you add instrumentation code to your application, to set or read values in particular registers. See the PSoC 63 with BLE Registers TRM for details.

At the highest level you perform these tasks:
- Enable the profiling block
- Configure and enable counters
- Start and stop profiling
- Handle counter overflow
- Get the results
- Exit gracefully

You can monitor as many sources as there are available counters. The actual number of available counters is hardware dependent. The value is defined in the symbol PROFILE_PRFL_CNT_NR in the <series>_config.h file. For example, the psoc63_config.h file defines this value as ‘8’.

Instead of manipulating registers directly, you can use the Peripheral Driver Library (PDL). The PDL provides a software API to manage the profiler. The software driver maintains an array of data for each counter, including the source you want to
monitor, whether you are monitoring duration or events, the reference clock, the counter value weighting coefficient, and an overflow count for each counter. It provides function calls to configure and enable a counter, start and stop a profiling session, and calculate the results for each counter. The PDL API handles all register and bit access.

Refer to the PDL API Reference for more information. The PDL installer puts the documentation here:
<PDL directory>\doc\pdl_api_reference_manual.html

24.3.1 Enable or Disable the Profiler

Before performing any operations, enable the profiling block. See Table 24-3. This does not enable individual counters or start a profiling session.

Table 24-3. Enabling the Profiler

<table>
<thead>
<tr>
<th>Task</th>
<th>Register</th>
<th>Bitfield</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Enable the profiler</td>
<td>CTL</td>
<td>ENABLED</td>
<td>0 = disabled 1 = enabled</td>
</tr>
</tbody>
</table>

24.3.2 Configure and Enable a Counter

Each counter has a CTL register that holds configuration information. For each counter you specify:

- The source you want to monitor
- What you want to measure (events or duration)
- The reference clock for the counter (affects only duration)

You also enable each counter individually. See Table 24-4.

Table 24-4. Configuring and Enabling a Counter

<table>
<thead>
<tr>
<th>Task</th>
<th>Register</th>
<th>Bitfield</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Specify source</td>
<td>CTL</td>
<td>MON_SEL</td>
<td>Table 24-1 on page 204</td>
</tr>
<tr>
<td>Specify events or duration</td>
<td>CTL</td>
<td>CNT_DURATION</td>
<td>0 = events 1 = duration. See Table 24-1 on page 204</td>
</tr>
<tr>
<td>Specify the reference clock</td>
<td>CTL</td>
<td>REF_CLK_SEL</td>
<td>Table 24-2 on page 205</td>
</tr>
<tr>
<td>Enable the counter</td>
<td>CTL</td>
<td>ENABLED</td>
<td>0 = disabled 1 = enabled</td>
</tr>
</tbody>
</table>

The count value is a 32-bit register. If that is not a sufficiently large number for your purposes, you must also enable the profiling interrupt for the counter. See Handle Counter Overflow on page 207.

When gathering data, you may want to know the actual number of clock cycles that occurred during the profiling session. To get this number, configure a counter to use:

- PROFILE_ONE as the monitored source
- duration (not events)
- a reference clock

The count for that counter is the actual number of reference clock cycles that occurred during the profiling session.

24.3.3 Start and Stop Profiling

After configuring and enabling the counters you want to use, you can start and stop a profiling session. You may wish to ensure that all counters are set to zero before beginning the profiling session. See Table 24-5.

Table 24-5. Starting or Stopping a Profiling Session

<table>
<thead>
<tr>
<th>Task</th>
<th>Register</th>
<th>Bitfield</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clear all counters</td>
<td>CMD</td>
<td>CLEAR_ALL_CNT</td>
<td>1 = reset all counters to zero</td>
</tr>
<tr>
<td>Start profiling</td>
<td>CMD</td>
<td>START_TR</td>
<td>1 = start profiling</td>
</tr>
<tr>
<td>Stop profiling</td>
<td>CMD</td>
<td>STOP_TR</td>
<td>1 = stop profiling</td>
</tr>
</tbody>
</table>
By design, all counters that are in use start and stop simultaneously. During the profiling session, each counter increments at its own rate based on the monitored signal and (if measuring duration) the reference clock.

24.3.4 Handle Counter Overflow

Each profiling counter is a 32-bit number. If this is not sufficient for your purposes, then you must handle counter overflow. To do so you must:

- Enable the profiling interrupt for the particular counter
- Provide an interrupt handler

For example, your interrupt handler could maintain an overflow counter for each profiling counter. See the Interrupts chapter on page 47 for details about interrupts.

Counter overflow involves the interaction of three registers, INTR, INTR_MASK, and INTR_MASKED. Each of these registers has one bit per profiling counter.

When an overflow occurs for a particular counter, hardware sets the corresponding bit in the INTR register. You typically do not read this register.

To enable the profiling interrupt for a particular counter, set the corresponding bit in the INTR_MASK register.

When an interrupt occurs, your interrupt handler reads the bits in the INTR_MASKED register. This register reflects a bitwise AND between the INTR register (an overflow interrupt has occurred for a particular counter) and the INTR_MASK register (this counter has the interrupt enabled). When a bit is set in the INTR_MASKED register, the corresponding counter is enabled and has experienced an overflow.

You can artificially trigger an overflow interrupt to test your code. The INTR_SET register also has one bit per counter. For debug purposes, software can set the appropriate bit to activate a specific overflow interrupt. This enables debug of the interrupt without waiting for hardware to cause the interrupt.

24.3.5 Get the Results

For each of your enabled counters, read the counter value in the CNT register for that counter. This is your absolute count. If you are tracking counter overflow, then the absolute count is 0x1 0000 0000 * overflow count + counter value.

To derive relative energy consumption for your monitored sources, for each counter, multiply the absolute count by a counter value weighting coefficient. See Counter Value Weighting (Energy Coefficients) on page 204.

The common use case is to get results after you stop profiling. However, you can get a snapshot of the results without stopping the profiler. In this case, however, the profiler is still counting and the results are changing as you gather the data.

After completing a profiling session, you may wish to repeat the same profile. Clear all counters to zero, and then start and stop profiling. See Start and Stop Profiling on page 206. If you are handling counter overflow, set your overflow counters to zero as well.

You can also reconfigure any or all counters to gather different data. See Configure and Enable a Counter on page 206. Reconfigure the profiler, and start another profiling session.

24.3.6 Exit Gracefully

When finished, you should disable the profiler. To do this make sure that you:

- Stop profiling (see Start and Stop Profiling on page 206)
- Clear any profiling configuration (see Configure and Enable a Counter on page 206)
- Disable the profiling interrupt if you have set it up (see Handle Counter Overflow on page 207)
- Disable the profiler itself (see Enable or Disable the Profiler on page 206)
Section D: Digital Subsystem

This section encompasses the following chapters:

- Serial Communications Block (SCB) chapter on page 209
- Serial Memory Interface (SMIF) chapter on page 257
- Timer, Counter, and PWM chapter on page 273
- Inter-IC Sound Bus chapter on page 307
- PDM-PCM Converter chapter on page 318
- Universal Serial Bus (USB) Device Mode chapter on page 326
- Universal Serial Bus (USB) Host chapter on page 342
- LCD Direct Drive chapter on page 358
- Universal Digital Blocks (UDB) chapter on page 372

Top Level Architecture

Digital System Block Diagram

[Diagram showing the system interconnect, peripheral interconnect, programmable digital blocks, and other subsystems, including Serial Comm, Serial Memory Interface, DMA, USB, Audio Subsystem, LCD, and Power Modes (Active/Sleep, LPActive, LPSleep, Hibernate, Backup)].

Power Modes
- Active/Sleep
- LPActive/LPSleep
- Hibernated
- Backup
25. Serial Communications Block (SCB)

The Serial Communications Block (SCB) supports three serial communication protocols: Serial Peripheral Interface (SPI), Universal Asynchronous Receiver Transmitter (UART), and Inter Integrated Circuit (I²C or IIC). Only one of the protocols is supported by an SCB at any given time. PSoC 6 MCUs have nine SCBs. Eight out of nine SCB blocks support SPI, UART, and I²C. One SCB supports only I²C slave mode and SPI slave mode; this is the only SCB that is available in the Deep Sleep power mode.

25.1 Features

The SCB supports the following features:

■ Standard SPI master and slave functionality with Motorola, Texas Instruments, and National Semiconductor protocols
■ Standard UART functionality with SmartCard reader, Local Interconnect Network (LIN), and IrDA protocols
  □ Standard LIN slave functionality with LIN v1.3 and LIN v2.1/2.2 specification compliance
■ Standard I²C master and slave functionality
■ EZ mode for SPI and I²C slaves; allows for operation without CPU intervention, available only on Deep Sleep-capable SCB
■ CMD_RESP mode for SPI and I²C slaves; allows for operation without CPU intervention, available only on Deep Sleep-capable SCB
■ Low-power (Deep Sleep) mode of operation for SPI and I²C slaves (using external clocking), available only on Deep Sleep-capable SCB
■ Deep Sleep wakeup on I²C slave address match or SPI slave selection; available only on Deep Sleep-capable SCB
■ Trigger outputs for connection to DMA
■ Multiple interrupt sources to indicate status of FIFOs and transfers

25.2 Architecture

The operation modes supported by SCB are described in the following sections.

25.2.1 Buffer Modes

Each SCB has 256 bytes of dedicated RAM for transmit and receive operation. This RAM can be configured in three different modes (FIFO, EZ, or CMD_RESP). The following sections give a high-level overview of each mode. The sections on each protocol will provide more details.

■ Masters can only use FIFO mode
■ Slaves can use all three modes. **Note:** EZ Mode and CMD Response Mode are available only on the Deep Sleep-capable SCB
■ UART only uses FIFO mode

25.2.1.1 FIFO Mode

In this mode the RAM is split into two 128-byte FIFOs, one for transmit (Tx) and one for receive (Rx). The FIFOs can be configured to be 8 bits x 128 elements or 16 bits x 64 elements.
FIFO mode of operation is available only in Active and Sleep power modes. However, the \( I^2C \) address or SPI slave select can be used to wake the device from Deep Sleep on the Deep Sleep-capable SCB.

Statuses are provided for both the Rx and Tx buffers. There are multiple interrupt sources available, which indicate the status of the FIFOs, such as full or empty; see “SCB Interrupts” on page 253.

25.2.1.2 EZ Mode

In easy (EZ) mode the RAM is used as a single 256-byte buffer. The external master sets a base address and reads and writes start from that base address.

EZ Mode is available only for SPI slave and \( I^2C \) slave. It is available only on the Deep Sleep-capable SCB.

EZ mode is available in Active, Sleep, and Deep Sleep power modes.

25.2.1.3 CMD_RESP Mode

Command Response (CMD_RESP) mode is similar to EZ mode except that the base address is provided by the CPU not the external master.

CMD_RESP mode is available only for SPI slave and \( I^2C \) slave. It is available only on the Deep Sleep-capable SCB.

CMD_RESP mode operation is available in Active, Sleep, and Deep Sleep power modes.

25.2.2 Clocking Modes

The SCB can be clocked either by an internal clock provided by the peripheral clock dividers, or it can be clocked by the external master.

- UART, SPI Master, and \( I^2C \) Master modes must use the internal clock, called clk_scb in the rest of this chapter.
- Only SPI slave and \( I^2C \) slave can use the clock from and external master, and only the Deep Sleep capable SCB supports this.

Internally- and externally-clocked slave functionality is determined by two register fields of the SCB CTRL register:

- EC_AM_MODE indicates whether SPI slave selection or \( I^2C \) address matching is internally (‘0’) or externally (‘1’) clocked.
- EC_OP_MODE indicates whether the rest of the protocol operation (besides SPI slave selection and \( I^2C \) address matching) is internally (‘0’) or externally (‘1’) clocked.

It is important to realize that:

- FIFO mode is not supported with externally-clocked operation (EC_OP_MODE is ‘1’)
- EZ and CMD_RESP modes are supported with externally clocked operation (EC_OP_MODE is ‘1’)

The following table provides an overview of which clocking modes and which buffer modes are supported for each communication mode:

<table>
<thead>
<tr>
<th></th>
<th>Internally clocked (IC)</th>
<th>Externally clocked (EC)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>FIFO</td>
<td>EZ</td>
</tr>
<tr>
<td>( I^2C ) master</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>( I^2C ) slave</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>( I^2C ) master-slave</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>SPI master</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>SPI slave</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>UART transmitter</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>UART receiver</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>

---

a. In Deep Sleep mode the external-clocked logic can handle slave address matching, it then triggers an interrupt to wake up the CPU. The slave can be programmed to stretch the clock, or NACK until internal logic takes over. This applies only to the Deep Sleep-capable SCB.

b. In Deep Sleep mode the external-clocked logic can handle slave selection detection, it then triggers an interrupt to wake up the CPU. Writes will be ignored and reads will return 0xFF until internal logic takes over. This applies only to the Deep Sleep-capable SCB.
25.3 Serial Peripheral Interface (SPI)

The SPI protocol is a synchronous serial interface protocol. Devices operate in either master or slave mode. The master initiates the data transfer. The SCB supports single-master-multiple-slaves topology for SPI. Multiple slaves are supported with individual slave select lines.

In the PSoC 6 MCU, eight out of nine SCB blocks support full SPI and one SCB supports only SPI slave mode; this SCB is also available in Deep Sleep power mode and allows externally-clocked operations.

25.3.1 Features

- Supports master and slave functionality
- Supports three types of SPI protocols:
  - Motorola SPI – modes 0, 1, 2, and 3
  - Texas Instruments SPI, with coinciding and preceding data frame indicator – mode 1 only
  - National Semiconductor (MicroWire) SPI – mode 0 only
- Master supports up to four slave select lines
- Each slave select has configurable active polarity (high or low)
- Slave select can be programmed to stay active for a whole transfer, or just for each byte
- Master supports late sampling for better timing margin
- Master supports continuous SPI clock
- Data frame size programmable from 4 bits to 16 bits
- Programmable oversampling
- MSb or LSb first
- Median filter available for inputs
- Supports FIFO Mode, EZ Mode (slave only), and CMD_RESP mode (slave only).

25.3.2 General Description

Figure 25-1 illustrates an example of SPI master with four slaves.

![Figure 25-1. SPI Example](image)
A standard SPI interface consists of four signals as follows.

- **SCLK**: Serial clock (clock output from the master, input to the slave).
- **MOSI**: Master-out-slave-in (data output from the master, input to the slave).
- **MISO**: Master-in-slave-out (data input to the master, output from the slave).
- **Slave Select** (SS): Typically an active low signal (output from the master, input to the slave).

A simple SPI data transfer involves the following: The master selects a slave by driving its SS line, then it drives data on the MOSI line and a clock on the SCLK line. The slave uses either of the edges of SCLK depending on the configuration to capture the data on the MOSI line; it also drives data on the MISO line, which is captured by the master.

By default, the SPI interface supports a data frame size of eight bits (1 byte). The data frame size can be configured to any value in the range 4 to 16 bits. The serial data can be transmitted either most significant bit (MSb) first or least significant bit (LSb) first.

Three different variants of the SPI protocol are supported by the SCB:

- **Motorola SPI**: This is the original SPI protocol.
- **Texas Instruments SPI**: A variation of the original SPI protocol, in which data frames are identified by a pulse on the SS line.
- **National Semiconductors SPI**: A half-duplex variation of the original SPI protocol.

### 25.3.3 SPI Modes of Operation

#### 25.3.3.1 Motorola SPI

The original SPI protocol was defined by Motorola. It is a full duplex protocol. Multiple data transfers may happen with the SS line held at ‘0’. When not transmitting data, the SS line is held at ‘1’ and SCLK is typically pulled low.

**Clock Modes of Motorola SPI**

The Motorola SPI protocol has four different clock modes based on how data is driven and captured on the MOSI and MISO lines. These modes are determined by clock polarity (CPOL) and clock phase (CPHA).

Clock polarity determines the value of the SCLK line when not transmitting data. CPOL = ‘0’ indicates that SCLK is ‘0’ when not transmitting data. CPOL = ‘1’ indicates that SCLK is ‘1’ when not transmitting data.

Clock phase determines when data is driven and captured. CPHA = 0 means sample (capture data) on the leading (first) clock edge, while CPHA = 1 means sample on the trailing (second) clock edge, regardless of whether that clock edge is rising or falling. With CPHA = 0, the data must be stable for setup time before the first clock cycle.

- **Mode 0**: CPOL is ‘0’, CPHA is ‘0’: Data is driven on a falling edge of SCLK. Data is captured on a rising edge of SCLK.
- **Mode 1**: CPOL is ‘0’, CPHA is ‘1’: Data is driven on a rising edge of SCLK. Data is captured on a falling edge of SCLK.
- **Mode 2**: CPOL is ‘1’, CPHA is ‘0’: Data is driven on a rising edge of SCLK. Data is captured on a falling edge of SCLK.
- **Mode 3**: CPOL is ‘1’, CPHA is ‘1’: Data is driven on a falling edge of SCLK. Data is captured on a rising edge of SCLK.

Figure 25-2 illustrates driving and capturing of MOSI/MISO data as a function of CPOL and CPHA.
Figure 25-2. SPI Motorola, 4 Modes

CPOL = 0  CPHA = 0
SCLK
MISO / MOSI
MSb
Lsb

CPOL = 0  CPHA = 1
SCLK
MISO / MOSI
MSb
Lsb

CPOL = 1  CPHA = 0
SCLK
MISO / MOSI
MSb
Lsb

CPOL = 1  CPHA = 1
SCLK
MISO / MOSI
MSb
Lsb

Figure 25-3 illustrates a single 8-bit data transfer and two successive 8-bit data transfers in mode 0 (CPOL is '0', CPHA is '0').

Figure 25-3. SPI Motorola Data Transfer Example

CPOL = 0, CPHA = 0 single data transfer
SCLK
MOSI
MSb
Lsb

CPOL = 0, CPHA = 0 two successive data transfers
SCLK
MOSI
MSb
Lsb
MSb
Lsb
MSb
Lsb
MSb
Lsb

Configuring SCB for SPI Motorola Mode

To configure the SCB for SPI Motorola mode, set various register bits in the following order:

1. Select SPI by writing '01' to the MODE (bits [25:24]) of the SCB_CTRL register.
2. Select SPI Motorola mode by writing '00' to the MODE (bits [25:24]) of the SCB_SPI_CTRL register.
3. Select the mode of operation in Motorola by writing to the CPHA and CPOL fields (bits 2 and 3 respectively) of the SCB_SPI_CTRL register.
4. Follow steps 2 to 4 mentioned in "Enabling and Initializing SPI" on page 223.

For more information on these registers, see the *PSoC 63 with BLE Registers TRM*

25.3.3.2 Texas Instruments SPI

The Texas Instruments’ SPI protocol redefines the use of the SS signal. It uses the signal to indicate the start of a data transfer, rather than a low active slave select signal, as in the case of Motorola SPI. The start of a transfer is indicated by a high active pulse of a single bit transfer period. This pulse may occur one cycle before the transmission of the first data bit, or may coincide with the transmission of the first data bit. The TI SPI protocol supports only mode 1 (CPOL is '0' and CPHA is ‘1’): data is driven on a rising edge of SCLK and data is captured on a falling edge of SCLK.

Figure 25-4 illustrates a single 8-bit data transfer and two successive 8-bit data transfers. The SELECT pulse precedes the first data bit. Note how the SELECT pulse of the second data transfer coincides with the last data bit of the first data transfer.

Figure 25-5 illustrates a single 8-bit data transfer and two successive 8-bit data transfers. The SELECT pulse coincides with the first data bit of a frame.
Configuring SCB for SPI TI Mode

To configure the SCB for SPI TI mode, set various register bits in the following order:

1. Select SPI by writing '01' to the MODE (bits [25:24]) of the SCB_CTRL register.
2. Select SPI TI mode by writing '01' to the MODE (bits [25:24]) of the SCB_SPI_CTRL register.
3. Select the mode of operation in TI by writing to the SELECT_PRECEDE field (bit 1) of the SCB_SPI_CTRL register ('1' configures the SELECT pulse to precede the first bit of next frame and '0' otherwise).
4. Follow steps 2 to 4 mentioned in “Enabling and Initializing SPI” on page 223.

For more information on these registers, see the PSoC 63 with BLE Registers TRM.

25.3.3 National Semiconductors SPI

The National Semiconductors’ SPI protocol is a half-duplex protocol. Rather than transmission and reception occurring at the same time, they take turns. The transmission and reception data sizes may differ. A single 'idle' bit transfer period separates transfers from reception. However, successive data transfers are not separated by an idle bit transfer period.

The National Semiconductors SPI protocol supports only mode 0.

Figure 25-6 illustrates a single data transfer and two successive data transfers. In both cases, the transmission data transfer size is eight bits and the reception data transfer size is four bits.
Configuring SCB for SPI NS Mode

To configure the SCB for SPI NS mode, set various register bits in the following order:

1. Select SPI by writing '01' to the MODE (bits [25:24]) of the SCB_CTRL register.
2. Select SPI NS mode by writing '10' to the MODE (bits [25:24]) of the SCB_SPI_CTRL register.
3. Follow steps 2 to 4 mentioned in "Enabling and Initializing SPI" on page 223.

For more information on these registers, see the PSoC 63 with BLE Registers TRM.

25.3.4 SPI Buffer Modes

SPI can operate in three different buffer modes – FIFO, EZ, and CMD_RESP modes. The buffer is used in different ways in each of these modes. The following subsections explain each of these buffer modes in detail.

25.3.4.1 FIFO Mode

The FIFO mode has a Tx FIFO for the data being transmitted and an Rx FIFO for the data received. Each FIFO is constructed out of the SRAM buffer. The FIFOs are either 64 elements deep with 16-bit data elements or 128 elements deep with 8-bit data elements. The width of a FIFO is configured using the CTRL.BYTE_MODE bitfield of the SCB.

FIFO mode of operation is available only in Active and Sleep power modes, and not in the Deep Sleep mode.

Transmit and receive FIFOs allow write and read accesses. A write access to the transmit FIFO uses the TX_FIFO_WR register. A read access from the receive FIFO uses the RX_FIFO_RD register.

Transmit and receive FIFO status information is available through status registers, TX_FIFO_STATUS and RX_FIFO_STATUS. You can define a programmable
threshold that indicates a number of FIFO entries, a trigger/event is generated when the following conditions are met:

- The transmit FIFO has a TX_FIFO_CTRL.TRIGGER_LEVEL. A trigger/event is generated when the number of entries in the transmit FIFO is less than TX_FIFO_CTRL.TRIGGER_LEVEL.
- The receive FIFO has an RX_FIFO_CTRL.TRIGGER_LEVEL. A trigger/event is generated when the number of receive FIFO entries is greater than the RX_FIFO_CTRL.TRIGGER_LEVEL.

These triggers can be connected to a DMA channel.

Furthermore, numerous interrupt status bits are provided for both the Rx and Tx FIFOs. These can be found looking at INTR_TX and INTR_RX.

Deep Sleep to Active Transition

EC_AM = 1, EC_OP = 0, FIFO Mode.

MISO transmits 0xFF until internally-clocked logic takes over and CPU writes to Tx FIFO. Data on MOSI is ignored until internally clocked logic takes over. When the internally clocked logic takes over, there is no guarantee that the internal clock will be at the correct frequency due to PLL/FLL locking times. This may lead to corrupted data in the Rx FIFO. Therefore, clear the Rx FIFO before writing new data into the Tx FIFO after the transition from Deep Sleep to Active. Another option is to disable clk_scb before going to Deep Sleep, and then wait to enable it until the PLL and FLL have stabilized. The external master needs to be aware that when it reads 0xFF on MISO the device is not ready yet.

25.3.4.2 EZSPI Mode

The easy SPI (EZSPI) protocol is based on the Motorola SPI operating in any mode (0, 1, 2, or 3). It allows communication between master and slave without the need for CPU intervention. In the PSoC 6 MCU, only one SCB block supports EZSPI mode; the Deep Sleep-capable SCB.

The EZSPI protocol defines a single memory buffer with an 8-bit EZ address that indexes the buffer (256-entry array of eight bit per entry) located on the slave device. The EZ address is used to address these 256 locations. All EZSPI data transfers have 8-bit data frames.

The CPU writes and reads to the memory buffer through the SCB_EZ_DATA registers. These accesses are word accesses, but only the least significant byte of the word is used.

EZSPI has three types of transfers: a write of the EZ address from the master to the slave, a write of data from the master to an addressed slave memory location, and a read by the master from an addressed slave memory location.

Note: When multiple bytes are read or written the master must keep SSEL low during the entire transfer.
Serial Communications Block (SCB)

FIGURE 25-7. EZSPI Example

Command 0x00 : Write EZ address

Command 0x01 : Write DATA

Command 0x02 : Read DATA

LEGEND:
CPOL : Clock Polarity
CPHA : Clock Phase
SCLK : SPI Interface Clock
MISO : SPI Master-In-Slave-Out
MOSI : SPI Master-Out-Slave-In
0x00 : Write EZ address
0x01 : Write DATA
0x02 : Read DATA
0xFE : slave ready
0xFF : slave busy

EZ buffer (32 bytes SRAM)
Configuring SCB for EZSPI Mode

By default, the SCB is configured for non-EZ mode of operation. To configure the SCB for EZSPI mode, set the register bits in the following order:

1. Select EZ mode by writing ‘1’ to the EZ_MODE bit (bit 10) of the SCB_CTRL register.
2. Follow the steps in “Configuring SCB for SPI Motorola Mode” on page 214.
3. Follow steps 2 to 4 mentioned in “Enabling and Initializing SPI” on page 223.

For more information on these registers, see the PSoC 6 with BLE Registers TRM.

Deep Sleep to Active Transition

- **EC_AM = 1, EC_OP = 0, EZ Mode.** MISO transmits 0xFF until the internally-clocked logic takes over. Data on MOSI is ignored until the internally-clocked logic takes over. When this happens, there is no guarantee that the internal clock will be at the correct frequency due to PLL/FLL locking times. This may lead to corrupted data on MISO and corrupted data in the EZ memory. Therefore, disable clk_scb before going to Deep Sleep, and then wait to enable it until the PLL/FLL have stabilized. The external master needs to be aware that when it reads 0xFF on MISO the device is not ready yet.

- **EC_AM = 1, EC_OP = 1, EZ Mode.** When transitioning from Deep Sleep to Active mode, there is no guarantee that the internal clock will be at the correct frequency due to PLL/FLL locking times. This situation limits the SPI SCLK frequency to 2 MHz. After the FLL/PLL outputs have stabilized, the clock can run faster.

25.3.4.3 Command-Response Mode

The command-response mode is defined only for an SPI slave. In the PSoC 6 MCU, only one SCB supports the command-response mode. This mode has a single memory buffer, a base read address, a current read address, a base write address, and a current write address that are used to index the memory buffer. The base addresses are provided by the CPU. The current addresses are used by the slave to index the memory buffer for sequential accesses of the memory buffer. The memory buffer holds 256 8-bit data elements. The base and current addresses are in the range [0, 255].

The CPU writes and reads to the memory buffer through the SCB_EZ_DATA registers. These accesses are word accesses, but only the least significant byte of the word is used.

The slave interface accesses the memory buffer using the current addresses. At the start of a write transfer (SPI slave selection), the base write address is copied to the current write address. A data element write is to the current write address location. After the write access, the current address is incremented by ‘1’. At the start of a read transfer, the base read address is copied to the current read address. A data element read is to the current read address location. After the read data element is transmitted, the current read address is incremented by ‘1’.

If the current addresses equal the last memory buffer address (address equals 255), the current addresses are not incremented. Subsequent write accesses will overwrite any previously written value at the last buffer address. Subsequent read accesses will continue to provide the (same) read value at the last buffer address. The bus master should be aware of the memory buffer capacity in command-response mode.

The base addresses are provided through CMD_RESP_CTRL. The current addresses are provided through CMD_RESP_STATUS. At the end of a transfer (SPI slave de-selection), the difference between a base and current address indicates how many read/write accesses were performed. The block provides interrupt cause fields to identify the end of a transfer. Command-response mode operation is available in Active, Sleep, and Deep Sleep power modes.

The command-response mode has two phases of operation:

- **Write phase** – The write phase begins with a selection byte, which has its last bit set to ‘0’ indicating a write. The master writes 8-bit data elements to the slave’s memory buffer following the selection byte. The slave’s current write address is set to the slave’s base write address. Received data elements are written to the current write address memory location. After each memory write, the current write address is incremented.

- **Read phase** – The read phase begins with a selection byte, which has its last bit set to ‘1’ indicating a read. The master reads 8-bit data elements from the slave’s memory buffer. The slave’s current read address is set to the slave’s base read address. Transmitted data elements are read from the current address memory location. After each read data element is transferred, the current read address is incremented.

During the reception of the first byte, the slave (MISO) transmits either 0x62 (ready) or a value different from 0x62 (busy). When disabled or reset, the slave transmits 0xFF (busy). The byte value can be used by the master to determine whether the slave is ready to accept the SPI request.
Note that a slave’s base addresses are updated by the CPU and not by the master.

**Deep Sleep to Active Transition**

EC_AM = 1, EC_OP = 1, CMD_RESP Mode.

When transitioning from Deep Sleep to Active mode there is no guarantee that the internal clock will be at the correct frequency due to PLL/FLL locking times. This situation limits the SPI SCLK frequency to 2 MHz. After the FLL/PLL outputs have stabilized the clock can run faster.

### Configuring SCB for CMD_RESP Mode

By default, the SCB is configured for non-CMD_RESP mode of operation. To configure the SCB for CMD_RESP mode, set the register bits in the following order:

1. Select the CMD_RESP mode by writing ‘1’ to the CMD_RESP_MODE bit (bit 12) of the SCB_CTRL register.
2. Follow the steps in “Configuring SCB for SPI Motorola Mode” on page 214.
3. Follow steps 2 to 4 mentioned in “Enabling and Initializing SPI” on page 223.

For more information on these registers, see the *PSoC 63 with BLE Registers TRM*.
25.3.5 Clocking and Oversampling

25.3.5.1 Clock Modes

The SCB SPI supports both internally and externally clocked operation modes. Two bitfields (EC_AM_MODE and EC_OP_MODE) in the SCB_CTRL register determine the SCB clock mode. EC_AM_MODE indicates whether SPI slave selection is internally (0) or externally (1) clocked. EC_OP_MODE indicates whether the rest of the protocol operation (besides SPI slave selection) is internally (0) or externally (1) clocked.

An externally-clocked operation uses a clock provided by the external master (SPI SCLK). Note: In the PSoC 6 MCU only the Deep Sleep-capable SCB supports externally-clock mode of operation and only for SPI slave mode.

An internally-clocked operation uses the programmable clock dividers. For more information on system clocking, see the Clocking System chapter on page 146.

The SCB_CTRL bitfields EC_AM_MODE and EC_OP_MODE can be configured in the following ways.

- **EC_AM_MODE** is ‘0’ and **EC_OP_MODE** is ‘0’: Use this configuration when only Active mode functionality is required.
  - FIFO mode: Supported.
  - EZ mode: Supported.
  - Command-response mode: Not supported. The slave (MISO) transmits a value different from a ready (0x62) byte during the reception of the first byte if command-response mode is attempted in this configuration.

- **EC_AM_MODE** is ‘1’ and **EC_OP_MODE** is ‘0’: Use this configuration when both Active and Deep Sleep functionality are required. This configuration relies on the externally-clocked functionality to detect the slave selection and relies on the internally-clocked functionality to access the memory buffer.
  - FIFO mode: Supported. The slave (MISO) transmits a busy (0xFF) byte during the reception of the first byte.
  - EZ mode: Supported.
  - CMD_RESP mode: Supported.

If **EC_OP_MODE** is ‘1’, the external interface logic accesses the memory buffer on the external interface clock (SPI SCLK). This allows for EZ and CMD_RESP mode functionality in Active and Deep Sleep power modes.

In Active system power mode, the memory buffer requires arbitration between external interface logic (on SPI SCLK) and the CPU interface logic (on system peripheral clock). This arbitration always gives the highest priority to the external interface logic (host accesses). The external interface logic takes two serial interface clock/bit periods for SPI. During this period, the internal logic is denied service to the memory buffer. The PSoC 6 MCU provides two programmable options to address this “denial of service”:

- **If the BLOCK bitfield of SCB_CTRL is ‘1’:** An internal logic access to the memory buffer is blocked until the memory buffer is granted and the external interface logic has completed access. This option provides normal SCB register functionality, but the blocking time introduces additional internal bus wait states.

<table>
<thead>
<tr>
<th></th>
<th>Internally clocked (IC)</th>
<th>Externally clocked (EC)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><strong>FIFO</strong></td>
<td><strong>EZ</strong></td>
</tr>
<tr>
<td>SPI master</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>SPI slave</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>

* In SPI slave FIFO mode, the external-clock logic does selection detection, then triggers an interrupt to wake up the CPU. Writes will be ignored and reads will return 0xFF until the CPU is ready and the FIFO is populated.
If the BLOCK bitfield of SCB_CTRL is ‘0’: An internal logic access to the memory buffer is not blocked, but fails when it conflicts with an external interface logic access. A read access returns the value 0xFFFF:FFFF and a write access is ignored. This option does not introduce additional internal bus wait states, but an access to the memory buffer may not take effect. In this case, the following failures are detected:

- Read Failure: A read failure is easily detected because the returned value is 0xFFFF:FFFF. This value is unique as non-failing memory buffer read accesses return an unsigned byte value in the range 0x0000:0000-0x0000:00ff.
- Write Failure: A write failure is detected by reading back the written memory buffer location, and confirming that the read value is the same as the written value.

For both options, a conflicting internal logic access to the memory buffer sets INTR_TX.BLOCKED field to ‘1’ (for write accesses) and INTR_RX.BLOCKED field to ‘1’ (for read accesses). These fields can be used as either status fields or as interrupt cause fields (when their associated mask fields are enabled).

If a series of read or write accesses is performed and CTRL.BLOCKED is ‘0’, a failure is detected by comparing the “logical-or” of all read values to 0xFFFF:FFFF and checking the INTR_TX.BLOCKED and INTR_RX.BLOCKED fields to determine whether a failure occurred for a series of write or read operations.

### 25.3.5.2 Using SPI Master to Clock Slave

In a normal SPI Master mode transmission, the SCLK is generated only when the SCB is enabled and data is being transmitted. This can be changed to always generate a clock on the SCLK line while the SCB is enabled. This is used when the slave uses the SCLK for functional operations other than just the SPI functionality. To enable this, write ‘1’ to the SCLK CONTINUOUS (bit 5) of the SCB_SPI_CTRL register.

### 25.3.5.3 Oversampling and Bit Rate

#### SPI Master Mode

The SPI master does not support externally clocked mode. In internally clocked mode, the logic operates under internal clock. The internal clock has higher frequency than the interface clock (SCLK), such that the master can oversample its input signals (MISO).

The OVS (bits [3:0]) of the SCB_CTRL register specify the oversampling. The oversampling rate is calculated as the value in OVS register + 1. In SPI master mode, the valid range for oversampling is 4 to 16, when MISO is used; if MISO is not used then the valid range is 2 to 16. The bit rate is calculated as follows.

\[
\text{Bit Rate} = \frac{\text{Input Clock}}{\text{OVS} + 1}
\]

Hence, with an input clock of 100 MHz, the maximum bit rate is 25 Mbps with MISO, or 50 Mbps without MISO.

The numbers above indicate how fast the SCB hardware can run SCLK. It does not indicate that the master will be able to correctly receive data from a slave at those speeds. To determine that, the path delay of MISO must be calculated. It can be calculated using the following equation:

\[
\frac{1}{2} \times t_{SCLK} \times t_{SCLK\_PCB\_D} + t_{DSO} + t_{SCLK\_PCB\_D} + t_{DSI}
\]

Where:

- \( t_{SCLK} \) is the period of the SPI clock
- \( t_{SCLK\_PCB\_D} \) is the SCLK PCB delay from master to slave
- \( t_{DSO} \) is the total internal slave delay, time from SCLK edge at slave pin to MISO edge at slave pin
- \( t_{SCLK\_PCB\_D} \) is the MISO PCB delay from slave to master
- \( t_{DSI} \) is the master setup time

Most slave datasheets will list \( t_{DSO} \). It may have a different name; look for MISO output valid after SCLK edge. Most master datasheets will also list \( t_{DSI} \), or master setup time. \( t_{SCLK\_PCB\_D} \) and \( t_{SCLK\_PCB\_D} \) must be calculated based on specific PCB geometries.
If after doing these calculations the desired speed cannot be achieved then consider using the MISO late sample feature of the SCB. MISO late sample tells the SCB to sample the incoming MISO signal on the next edge of SCLK, thus allowing for ½ SCLK cycle more timing margin, see Figure 25-9.

![Figure 25-9. MISO Sampling Timing](image)

This changes the equation to:

\[ t_{SCLK} \geq t_{SCLK\_PCB\_D} + t_{DSO} + t_{SCLK\_PCB\_D} + t_{DSI} \]  

Equation 25-3

Because late sample allows for better timing, leave it enabled all the time. The t_{DSI} specification in the PSoC 6 MCU datasheet assumes late sample is enabled.

Note: The SPI_CTRL.LATE_MISO_SAMPLE is set to ‘0’ by default.

SPI Slave Mode

In SPI slave mode, the OVS field (bits [3:0]) of SCB_CTRL register is not used. The data rate is determined by Equation 25-1 and Equation 25-2. Late MISO sample is determined by the external master in this case, not by SPI_CTRL.LATE_MISO_SAMPLE.

For PSoC 6 MCUs, t_{DSO} is given in the device datasheet. For internally-clocked mode, it is proportional to the frequency of the internal clock. For example it may be 20 ns + 3 *t_{CLK\_SCB}. Assuming 0 ns PCB delays, and a 0 ns external master t_{DSI} Equation 25-1 can be re-arranged to \( t_{CLK\_SCB} \leq (t_{SCLK} - 40 \text{ ns})/6 \).

25.3.6 Enabling and Initializing SPI

The SPI must be programmed in the following order:

1. Program protocol specific information using the SCB_SPI_CTRL register. This includes selecting the sub-modes of the protocol and selecting master-slave functionality. EZSPI and CMD_RESP can be used with slave mode only.
2. Program the generic transmitter and receiver information using the SCB_TX_CTRL and SCB_RX_CTRL registers:
   a. Specify the data frame width. This should always be 8 for EZSPI and CMD_RESP.
   b. Specify whether MSb or LSb is the first bit to be transmitted/received. This should always be MSb first for EZSPI and CMD_RESP.
3. Program the transmitter and receiver FIFOs using the SCB_TX_FIFO_CTRL and SCB_RX_FIFO_CTRL registers respectively, as shown in SCB_TX_FIFO_CTRL/SCB_RX_FIFO_CTRL registers. Only for FIFO mode.
   a. Set the trigger level.
   b. Clear the transmitter and receiver FIFO and Shift registers.
4. Enable the block (write a ‘1’ to the ENABLED bit of the SCB_CTRL register). After the block is enabled, control bits should not be changed. Changes should be made after disabling the block; for example, to modify the operation mode (from Motorola mode to TI mode) or to go from externally clocked to internally clocked operation. The change takes effect only after the block is re-enabled. Note that re-enabling the block causes re-initialization and the associated state is lost (for example, FIFO content).
25.3.7 I/O Pad Connection

25.3.7.1 SPI Master

Figure 25-10 and Table 25-3 list the use of the I/O pads for SPI Master.

Figure 25-10. SPI Master I/O Pad Connections

Table 25-3. SPI Master I/O Pad Connection Usage

<table>
<thead>
<tr>
<th>I/O Pads</th>
<th>Drive Mode</th>
<th>On-chip I/O Signals</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>spi_clk</td>
<td>Normal output mode</td>
<td>spi_clk_out_en</td>
<td>Transmit a clock signal</td>
</tr>
<tr>
<td></td>
<td></td>
<td>spi_clk_out</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>spi_clk_in</td>
<td></td>
</tr>
<tr>
<td>spi_select</td>
<td>Normal output mode</td>
<td>spi_select_out_en</td>
<td>Transmit a select signal</td>
</tr>
<tr>
<td></td>
<td></td>
<td>spi_select_out</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>spi_select_in</td>
<td></td>
</tr>
<tr>
<td>spi_mosi</td>
<td>Normal output mode</td>
<td>spi_mosi_out_en</td>
<td>Transmit a data element</td>
</tr>
<tr>
<td></td>
<td></td>
<td>spi_mosi_out</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>spi_mosi_in</td>
<td></td>
</tr>
<tr>
<td>spi_miso</td>
<td>Input only</td>
<td>spi_miso_in</td>
<td>Receive a data element</td>
</tr>
</tbody>
</table>
25.3.7.2 SPI Slave

Figure 25-11 and Table 25-4 list the use of I/O pads for SPI Slave.

### Table 25-4. SPI Slave I/O Signal Description

<table>
<thead>
<tr>
<th>I/O Pads</th>
<th>Drive Mode</th>
<th>On-chip I/O Signals</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>spi_clk</td>
<td>Normal output mode</td>
<td>spi_clk_in</td>
<td>Receive a clock signal</td>
</tr>
<tr>
<td>spi_select</td>
<td>Normal output mode</td>
<td>spi_select_in</td>
<td>Receive a select signal</td>
</tr>
<tr>
<td>spi_mosi</td>
<td>Normal output mode</td>
<td>spi_mosi_in</td>
<td>Receive a data element</td>
</tr>
<tr>
<td>spi_miso</td>
<td>Input only</td>
<td>spi_miso_out_en</td>
<td>Transmit a data element</td>
</tr>
</tbody>
</table>
25.3.8 SPI Registers

The SPI interface is controlled using a set of 32-bit control and status registers listed in Table 25-5. For more information on these registers, see the *PSoC 63 with BLE Registers TRM*.

Table 25-5. SPI Registers

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCB_CTRL</td>
<td>Enables the SCB, selects the type of serial interface (SPI, UART, I²C), and selects internally and externally clocked operation, and EZ and non-EZ modes of operation.</td>
</tr>
<tr>
<td>SCB_STATUS</td>
<td>In EZ mode, this register indicates whether the externally clocked logic is potentially using the EZ memory.</td>
</tr>
<tr>
<td>SCB_SPI_CTRL</td>
<td>Configures the SPI as either a master or a slave, selects SPI protocols (Motorola, TI, National) and clock-based submodes in Motorola SPI (modes 0,1,2,3), selects the type of SS signal in TI SPI.</td>
</tr>
<tr>
<td>SCB_SPI_STATUS</td>
<td>Indicates whether the SPI bus is busy and sets the SPI slave EZ address in the internally clocked mode.</td>
</tr>
<tr>
<td>SCB_TX_CTRL</td>
<td>Specifies the data frame width and specifies whether MSb or LSb is the first bit in transmission.</td>
</tr>
<tr>
<td>SCB_RX_CTRL</td>
<td>Performs the same function as that of the SCB_TX_CTRL register, but for the receiver. Also decides whether a median filter is to be used on the input interface lines.</td>
</tr>
<tr>
<td>SCB_TX_FIFO_CTRL</td>
<td>Specifies the trigger level, clears the transmitter FIFO and shift registers, and performs the FREEZE operation of the transmitter FIFO.</td>
</tr>
<tr>
<td>SCB_RX_FIFO_CTRL</td>
<td>Performs the same function as that of the SCB_TX_FIFO_CTRL register, but for the receiver.</td>
</tr>
<tr>
<td>SCB_TX_FIFO_WR</td>
<td>Holds the data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation.</td>
</tr>
<tr>
<td>SCB_RX_FIFO_WR</td>
<td>Holds the data frame read from the receiver FIFO. Reading a data frame removes the data frame from the FIFO - behavior is similar to that of a POP operation. This register has a side effect when read by software: a data frame is removed from the FIFO.</td>
</tr>
<tr>
<td>SCB_RX_FIFO_RD</td>
<td>Holds the data frame read from the receiver FIFO. Reading a data frame does not remove the data frame from the FIFO; behavior is similar to that of a PEEK operation.</td>
</tr>
<tr>
<td>SCB_TX_FIFO_STATUS</td>
<td>Indicates the number of bytes stored in the transmitter FIFO, the location from which a data frame is read by the hardware (read pointer), the location from which a new data frame is written (write pointer), and decides whether the transmitter FIFO holds the valid data.</td>
</tr>
<tr>
<td>SCB_RX_FIFO_STATUS</td>
<td>Performs the same function as that of the SCB_TX_FIFO_STATUS register, but for the receiver.</td>
</tr>
<tr>
<td>SCB_EZ_DATA</td>
<td>Holds the data in EZ memory location</td>
</tr>
</tbody>
</table>
25.4 UART

The Universal Asynchronous Receiver/Transmitter (UART) protocol is an asynchronous serial interface protocol. UART communication is typically point-to-point. The UART interface consists of two signals:

- Tx: Transmitter output
- Rx: Receiver input

Additionally, two side-band signals are used to implement flow control in UART. Note that the flow control applies only to Tx functionality.

- Clear to Send (CTS): This is an input signal to the transmitter. When active, it indicates that the slave is ready for the master to transmit data.
- Ready to Send (RTS): This is an output signal from the receiver. When active, it indicates that the receiver is ready to receive data.

In the PSoC 6 MCU, eight out of nine SCB blocks support full UART and one SCB does not support UART mode. The SCB that does not support UART is the Deep Sleep-capable SCB.

25.4.1 Features

- Supports UART protocol
  - Standard UART
  - Multi-processor mode
- SmartCard (ISO7816) reader
- IrDA
- Supports Local Interconnect Network (LIN)
  - Break detection
  - Baud rate detection
  - Collision detection (ability to detect that a driven bit value is not reflected on the bus, indicating that another component is driving the same bus)
- Data frame size programmable from 4 to 16 bits
- Programmable number of STOP bits, which can be set in terms of half bit periods between 1 and 4
- Parity support (odd and even parity)
- Median filter on Rx input
- Programmable oversampling
- Start skipping

25.4.2 General Description

Figure 25-12 illustrates a standard UART Tx and Rx.

Figure 25-12. UART Example

A typical UART transfer consists of a start bit followed by multiple data bits, optionally followed by a parity bit and finally completed by one or more stop bits. The start and stop bits indicate the start and end of data transmission. The parity bit is sent by the transmitter and is used by the receiver to detect single bit errors. Because the interface does not have a clock (asynchronous), the transmitter and receiver use their own clocks; thus, the transmitter and receiver need to agree on the baud rate.

By default, UART supports a data frame width of eight bits. However, this can be configured to any value in the range of 4 to 9. This does not include start, stop, and parity bits. The number of stop bits can be in the range of 1 to 4. The parity bit can be either enabled or disabled. If enabled, the type of parity can be set to either even parity or odd parity. The option of using the parity bit is available only in the Standard UART and SmartCard UART modes. For IrDA UART mode, the parity bit is automatically disabled.

Note: UART interface does not support external clocking operation. Hence, UART operates only in the Active and Sleep system power modes. UART also supports only the FIFO buffer mode.

25.4.3 UART Modes of Operation

25.4.3.1 Standard Protocol

A typical UART transfer consists of a start bit followed by multiple data bits, optionally followed by a parity bit and finally completed by one or more stop bits. The start bit value is always ‘0’, the data bits values are dependent on the data transferred, the parity bit value is set to a value guaranteeing an even or odd parity over the data bits, and the stop bit value is ‘1’. The parity bit is generated by the transmitter and can be used by the receiver to detect single bit transmission errors. When not transmitting data, the Tx line is ‘1’ – the same value as the stop bits.

Because the interface does not have a clock, the transmitter and receiver must agree upon the baud rate. The transmitter and receiver have their own internal clocks. The receiver clock runs at a higher frequency than the bit transfer frequency, such that the receiver may oversample the incoming signal.

The transition of a stop bit to a start bit is represented by a change from ‘1’ to ‘0’ on the Tx line. This transition can be
used by the receiver to synchronize with the transmitter clock. Synchronization at the start of each data transfer allows error-free transmission even in the presence of frequency drift between transmitter and receiver clocks. The required clock accuracy is dependent on the data transfer size.

The stop period or the amount of stop bits between successive data transfers is typically agreed upon between transmitter and receiver, and is typically in the range of 1 to 3-bit transfer periods.

Figure 25-13 illustrates the UART protocol.

**Figure 25-13. UART, Standard Protocol Example**

Two successive data transfers (7 data bits, 1 parity bit, 2 stop bits)

The receiver oversamples the incoming signal; the value of the sample point in the middle of the bit transfer period (on the receiver's clock) is used. Figure 25-14 illustrates this.

**Figure 25-14. UART, Standard Protocol Example (Single Sample)**

Alternatively, three samples around the middle of the bit transfer period (on the receiver's clock) are used for a majority vote to increase accuracy; this is enabled by enabling the MEDIAN filter in the RX_CTRL register. Figure 25-15 illustrates this.

**Figure 25-15. UART, Standard Protocol (Multiple Samples)**
Parity

This functionality adds a parity bit to the data frame and is used to identify single-bit data frame errors. The parity bit is always directly after the data frame bits.

The transmitter calculates the parity bit (when UART_TX_CTRL.PARITY_ENABLED is 1) from the data frame bits, such that data frame bits and parity bit have an even (UART_TX_CTRL.PARITY is 0) or odd (UART_TX_CTRL.PARITY is 1) parity. The receiver checks the parity bit (when UART_RX_CTRL.PARITY_ENABLED is 1) from the received data frame bits, such that data frame bits and parity bit have an even (UART_RX_CTRL.PARITY is 0) or odd (UART_RX_CTRL.PARITY is 1) parity.

Parity applies to both Tx and Rx functionality and dedicated control fields are available.
- Transmit functionality: UART_TX_CTRL.PARITY and UART_TX_CTRL.PARITY_ENABLED.
- Receive functionality: UART_RX_CTRL.PARITY and UART_RX_CTRL.PARITY_ENABLED.

When a receiver detects a parity error, the data frame is either put in Rx FIFO (UART_RX_CTRL.DROP_ON_PARITY_ERROR is 0) or dropped (UART_RX_CTRL.DROP_ON_PARITY_ERROR is 1).

The following figures illustrate the parity functionality (8-bit data frame).

![Figure 25-16. UART Parity Examples](image)

Start Skipping

Start skipping applies only to receive functionality. The standard UART mode supports “start skipping”. Regular receive operation synchronizes on the START bit period (a 1 to 0 transition on the UART Rx line), start skipping receive operation synchronizes on the first received data frame bit, which must be a ‘1’ (a 0 to 1 transition on UART Rx).

Start skipping is used to allow for wake up from system Deep Sleep mode using UART. The process is described as follows:
1. Before entering Deep Sleep power mode, UART receive functionality is disabled and the GPIO is programmed to set an interrupt cause to ‘1’ when UART Rx line has a ‘1’ to ‘0’ transition (START bit).
2. While in Deep Sleep mode, the UART receive functionality is not functional.
3. The GPIO interrupt is activated on the START bit and the system transitions from Deep Sleep to Active power mode.
4. The CPU enables UART receive functionality, with UART_RX_CTRL.SKIP_START bitfield set to ‘1’.
5. The UART receiver synchronizes data frame receipt on the next ‘0’ to ‘1’ transition. If the UART receive functionality is enabled in time, this is the transition from the START bit to the first received data frame bit.
6. The UART receiver proceeds with normal operation; that is, synchronization of successive data frames is on the START bit period.

![Figure 25-17 illustrates the process.](image)
Note that the above process works only for lower baud rates. The Deep Sleep to Active power mode transition and CPU enabling the UART receive functionality should take less than 1-bit period to ensure that the UART receiver is active in time to detect the '0' to '1' transition.

In step 4 of the above process, the firmware takes some time to finish the wakeup interrupt routine and enable the UART receive functionality before the block can detect the input rising edge on the UART Rx line.

If the above steps cannot be completed in less than 1 bit time, first send a “dummy” byte to the device to wake it up before sending real UART data. In this case, the SKIP_START bit can be left as 0.

**Break Detection**

Break detection is supported in the standard UART mode. This functionality detects when UART Rx line is low (0) for more than UART_CTRL.BREAK_WIDTH bit periods. The break width should be larger than the maximum number of low (0) bit periods in a regular data transfer, plus an additional 1-bit period. The additional 1-bit period is a minimum requirement and preferably should be larger. The additional bit periods account for clock inaccuracies between transmitter and receiver.

For example, for an 8-bit data frame with parity support, the maximum number of low (0) bit periods is 10 (START bit, 8 '0' data frame bits, and one '0' parity bit). Therefore, the break width should be larger than 10 + 1 = 11 (UART_CTRL.BREAK_WIDTH can be set to 11).

Note that the break detection applies only to receive functionality. A UART transmitter can generate a break by temporarily increasing TX_CTRL.DATA_WIDTH and transmitting an all zeroes data frame. A break is used by the transmitter to signal a special condition to the receiver. This condition may result in a reset, shut down, or initialization sequence at the receiver.

Break detection is part of the LIN protocol. When a break is detected, the INTR_RX.BREAK_DETECT interrupt cause is set to ‘1’. Figure 25-18 illustrates a regular data frame and break frame (8-bit data frame, parity support, and a break width of 12-bit periods).
Flow Control

The standard UART mode supports flow control. Modern flow control controls the pace at which the transmitter transfers data to the receiver. Modern flow control is enabled through the UART_FLOW_CTRL.CTS_ENABLED register field. When this field is ‘0’, the transmitter transfers data when its Tx FIFO is not empty. When ‘1’, the transmitter transfers data when UART CTS line is active and its Tx FIFO is not empty.

Note that the flow control applies only to Tx functionality. Two UART side-band signal are used to implement flow control:

- **UART RTS (uart_rts_out):** This is an output signal from the receiver. When active, it indicates that the receiver is ready to receive data (RTS: Ready to Send).
- **UART CTS (uart_cts_in):** This is an input signal to the transmitter. When active, it indicates that the transmitter can transfer data (CTS: Clear to Send).

The receiver’s uart_rts_out signal is connected to the transmitter’s uart_cts_in signal. The receiver’s uart_rts_out signal is derived by comparing the number of used receive FIFO entries with the UART_FLOW_CTRL.TRIGGER_LEVEL field. If the number of used receive FIFO entries are less than UART_FLOW_CTRL.TRIGGERLEVEL, uart_rts_out is activated.

Typically, the UART side-band signals are active low. However, sometimes active high signaling is used. Therefore, the polarity of the side-band signals can be controlled using bitfields UART_FLOW_CTRL.RTS_POLARITY and UART_FLOW_CTRL.CTS_POLARITY. Figure 25-19 gives an overview of the flow control functionality.

![Figure 25-19. UART Flow Control Connection](image)

### 25.4.3.2 UART Multi-Processor Mode

The UART_MP (multi-processor) mode is defined with single-master-multi-slave topology, as Figure 25-20 shows. This mode is also known as UART 9-bit protocol because the data field is nine bits wide. UART_MP is part of Standard UART mode.

![Figure 25-20. UART MP Mode Bus Connections](image)

The main properties of UART_MP mode are:

- Single master with multiple slave concept (multi-drop network).
- Each slave is identified by a unique address.
- Using 9-bit data field, with the ninth bit as address/data flag (MP bit). When set high, it indicates an address byte; when set low it indicates a data byte. A data frame is illustrated in Figure 25-21.
- Parity bit is disabled.
The SCB can be used as either master or slave device in UART_MP mode. Both SCB_TX_CTRL and SCB_RX_CTRL registers should be set to 9-bit data frame size. When the SCB works as UART_MP master device, the firmware changes the MP flag for every address or data frame. When it works as UART_MP slave device, the MP_MODE field of the SCB_UART_RX_CTRL register should be set to ‘1’. The SCB_RX_MATCH register should be set for the slave address and address mask. The matched address is written in the RX_FIFO when ADDR_ACCEPT field of the SCB_CTRL register is set to ‘1’. If the received address does not match its own address, then the interface ignores the following data, until next address is received for compare.

### 25.4.3.3 UART Local Interconnect Network (LIN) Mode

The LIN protocol is supported by the SCB as part of the standard UART. LIN is designed with single-master-multi-slave topology. There is one master node and multiple slave nodes on the LIN bus. The SCB UART supports both LIN master and slave functionality. The LIN specification defines both physical layer (layer 1) and data link layer (layer 2). Figure 25-22 illustrates the UART_LIN and LIN transceiver.

LIN protocol defines two tasks:
- **Master task**: This task involves sending a header packet to initiate a LIN transfer.
- **Slave task**: This task involves transmitting or receiving a response.

The master node supports master task and slave task; the slave node supports only slave task, as shown in Figure 25-23.
LIN Frame Structure

LIN is based on the transmission of frames at pre-determined moments of time. A frame is divided into header and response fields, as shown in Figure 25-24.

- The header field consists of:
  - Break field (at least 13 bit periods with the value ‘0’).
  - Sync field (a 0x55 byte frame). A sync field can be used to synchronize the clock of the slave task with that of the master task.
  - Identifier field (a frame specifying a specific slave).
- The response field consists of data and checksum.

In LIN protocol communication, the least significant bit (LSb) of the data is sent first and the most significant bit (MSb) last. The start bit is encoded as zero and the stop bit is encoded as one. The following sections describe all the byte fields in the LIN frame.

Break Field

Every new frame starts with a break field, which is always generated by the master. The break field has logical zero with a minimum of 13 bit times and followed by a break delimiter. The break field structure is as shown in Figure 25-25.

Sync Field

This is the second field transmitted by the master in the header field; its value is 0x55. A sync field can be used to synchronize the clock of the slave task with that of the master task for automatic baud rate detection. Figure 25-26 shows the LIN sync field structure.

Protected Identifier (PID) Field

A protected identifier field consists of two sub-fields: the frame identifier (bits 0-5) and the parity (bit 6 and bit 7). The PID field structure is shown in Figure 25-27.

- Frame identifier: The frame identifiers are split into three categories
  - Values 0 to 59 (0x3B) are used for signal carrying frames
  - 60 (0x3C) and 61 (0x3D) are used to carry diagnostic and configuration data
  - 62 (0x3E) and 63 (0x3F) are reserved for future protocol enhancements
- Parity: Frame identifier bits are used to calculate the parity

Figure 25-27 shows the PID field structure.
Data. In LIN, every frame can carry a minimum of one byte and maximum of eight bytes of data. Here, the LSb of the data byte is sent first and the MSb of the data byte is sent last.

Checksum. The checksum is the last byte field in the LIN frame. It is calculated by inverting the 8-bit sum along with carryover of all data bytes only or the 8-bit sum with the carryover of all data bytes and the PID field. There are two types of checksums in LIN frames. They are:

- Classic checksum: the checksum calculated over all the data bytes only (used in LIN 1.x slaves).
- Enhanced checksum: the checksum calculated over all the data bytes along with the protected identifier (used in LIN 2.x slaves).

LIN Frame Types

The type of frame refers to the conditions that need to be valid to transmit the frame. According to the LIN specification, there are five different types of LIN frames. A node or cluster does not have to support all frame types.

Unconditional Frame. These frames carry the signals and their frame identifiers (of 0x00 to 0x3B range). The subscriber will receive the frames and make it available to the application; the publisher of the frame will provide the response to the header.

Event-Triggered Frame. The purpose of an event-triggered frame is to increase the responsiveness of the LIN cluster without assigning too much of the bus bandwidth to polling of multiple slave nodes with seldom occurring events. Event-triggered frames carry the response of one or more unconditional frames. The unconditional frames associated with an event triggered frame should:

- Have equal length
- Use the same checksum model (either classic or enhanced)
- Reserve the first data field to its protected identifier
- Be published by different slave nodes
- Not be included directly in the same schedule table as the event-triggered frame

Sporadic Frame. The purpose of the sporadic frames is to merge some dynamic behavior into the schedule table without affecting the rest of the schedule table. These frames have a group of unconditional frames that share the frame slot. When the sporadic frame is due for transmission, the unconditional frames are checked whether they have any updated signals. If no signals are updated, no frame will be transmitted and the frame slot will be empty.

Diagnostic Frames. Diagnostic frames always carry transport layer, and contains eight data bytes. The frame identifier for diagnostic frame is:

- Master request frame (0x3C), or
- Slave response frame (0x3D)

Before transmitting a master request frame, the master task queries its diagnostic module to see whether it will be transmitted or whether the bus will be silent. A slave response frame header will be sent unconditionally. The slave tasks publish and subscribe to the response according to their diagnostic modules.

Reserved Frames. These frames are reserved for future use; their frame identifiers are 0x3E and 0x3F.

LIN Go-To-Sleep and Wake-Up

The LIN protocol has the feature of keeping the LIN bus in Sleep mode, if the master sends the go-to-sleep command. The go-to-sleep command is a master request frame (ID = 0x3C) with the first byte field is equal to 0x00 and rest set to 0xFF. The slave node application may still be active after the go-to-sleep command is received. This behavior is application specific. The LIN slave nodes automatically enter Sleep mode if the LIN bus inactivity is more than four seconds.

Wake-up can be initiated by any node connected to the LIN bus – either LIN master or any of the LIN slaves by forcing the bus to be dominant for 250 µs to 5 ms. Each slave should detect the wakeup request and be ready to process headers within 100 ms. The master should also detect the wakeup request and start sending headers when the slave nodes are active.

To support LIN, a dedicated (off-chip) line driver/receiver is required. Supply voltage range on the LIN bus is 7 V to 18 V. Typically, LIN line drivers will drive the LIN line with the value provided on the SCB Tx line and present the value on the LIN line to the SCB Rx line. By comparing Tx and Rx lines in the SCB, bus collisions can be detected (indicated by the SCB_UART_ARB_LOST field of the SCB_INTR_TX register).

Configuring the SCB as Standard UART Interface

To configure the SCB as a standard UART interface, set various register bits in the following order:

1. Configure the SCB as UART interface by writing ‘10b’ to the MODE field (bits [25:24]) of the SCB_CTRL register.
2. Configure the UART interface to operate as a Standard protocol by writing ‘00’ to the MODE field (bits [25:24]) of the SCB_UART_CTRL register.
3. To enable the UART MP Mode or UART LIN Mode, write ‘1’ to the MP_MODE (bit 10) or LIN_MODE (bit 12) respectively of the SCB_UART_RX_CTRL register.

4. Follow steps 2 to 4 described in “Enabling and Initializing the UART” on page 237.

For more information on these registers, see the PSoC 63 with BLE Registers TRM.

25.4.3.4 SmartCard (ISO7816)

ISO7816 is asynchronous serial interface, defined with single-master-single slave topology. ISO7816 defines both Reader (master) and Card (slave) functionality. For more information, refer to the ISO7816 Specification. Only the master (reader) function is supported by the SCB. This block provides the basic physical layer support with asynchronous character transmission. The UART_TX line is connected to SmartCard I/O line by internally multiplexing between UART_TX and UART_RX control modules.

The SmartCard transfer is similar to a UART transfer, with the addition of a negative acknowledgement (NACK) that may be sent from the receiver to the transmitter. A NACK is always ‘0’. Both master and slave may drive the same line, although never at the same time.

A SmartCard transfer has the transmitter drive the start bit and data bits (and optionally a parity bit). After these bits, it enters its stop period by releasing the bus. Releasing results in the line being ‘1’ (the value of a stop bit). After one bit transfer period into the stop period, the receiver may drive a NACK on the line (a value of ‘0’) for one bit transfer period. This NACK is observed by the transmitter, which reacts by extending its stop period by one bit transfer period. For this protocol to work, the stop period should be longer than one bit transfer period. Note that a data transfer with a NACK takes one bit transfer period longer, than a data transfer without a NACK. Typically, implementations use a tristate driver with a pull-up resistor, such that when the line is not transmitting data or transmitting the Stop bit, its value is ‘1’.

The communication Baud rate for ISO7816 is given as:

Baud rate = f_{7816} \times (D/F)

Where f_{7816} is the clock frequency, F is the clock rate conversion integer, and D is the baud rate adjustment integer.

By default, F = 372, D = 1, and maximum clock frequency is 5 MHz. Thus, maximum baud rate is 13.4 kbps. Typically, a 3.57-MHz clock is selected; the baud rate will then be 9.6 kbps.

Configuring SCB as UART SmartCard Interface

To configure the SCB as a UART SmartCard interface, set various register bits in the following order; note that PSoC Creator does all this automatically with the help of GUIs. For more information on these registers, see the PSoC 63 with BLE Registers TRM.

1. Configure the SCB as UART interface by writing ‘10b’ to the MODE (bits [25:24]) of the SCB_CTRL register.
2. Configure the UART interface to operate as a SmartCard protocol by writing ‘01’ to the MODE (bits [25:24]) of the SCB_UART_CTRL register.
3. Follow steps 2 to 4 described in “Enabling and Initializing the UART” on page 237.
25.4.3.5 *Infrared Data Association (IrDA)*

The SCB supports the IrDA protocol for data rates of up to 115.2 kbps using the UART interface. It supports only the basic physical layer of IrDA protocol with rates less than 115.2 kbps. Hence, the system instantiating this block must consider how to implement a complete IrDA communication system with other available system resources.

The IrDA protocol adds a modulation scheme to the UART signaling. At the transmitter, bits are modulated. At the receiver, bits are demodulated. The modulation scheme uses a Return-to-Zero-Inverted (RZI) format. A bit value of ‘0’ is signaled by a short ‘1’ pulse on the line and a bit value of ‘1’ is signaled by holding the line to ‘0’. For these data rates (<=115.2 kbps), the RZI modulation scheme is used and the pulse duration is 3/16 of the bit period. The sampling clock frequency should be set 16 times the selected baud rate, by configuring the SCB_OVS field of the SCB_CTRL register. In addition, the PSoC 6 MCU SCB supports a low-power IrDA receiver mode, which allows it to detect pulses with a minimum width of 1.41 µs.

Different communication speeds under 115.2 kbps can be achieved by configuring corresponding block clock frequency. Additional allowable rates are 2.4 kbps, 9.6 kbps, 19.2 kbps, 38.4 kbps, and 57.6 kbps. Figure 25-29 shows how a UART transfer is IrDA modulated.

![Figure 25-29. IrDA Example](par)

**Configuring the SCB as a UART IrDA Interface**

To configure the SCB as a UART IrDA interface, set various register bits in the following order; note that PSoC Creator does all this automatically with the help of GUIs. For more information on these registers, see the [PSoC 63 with BLE Registers TRM](#).

1. Configure the SCB as a UART interface by writing ‘10b’ to the MODE (bits [25:24]) of the SCB_CTRL register.
2. Configure the UART interface to operate as IrDA protocol by writing ‘10’ to the MODE (bits [25:24]) of the SCB_UART_CTRL register.
3. Enable the Median filter on the input interface line by writing ‘1’ to MEDIAN (bit 9) of the SCB_RX_CTRL register.
4. Configure the SCB as described in “Enabling and Initializing the UART” on page 237.
25.4.4 Clocking and Oversampling

The UART protocol is implemented using the SCB input clock as an oversampled multiple of the baud rate. For example, to implement a 100-kHz UART, SCB input clock should be set to 1 MHz and the oversample factor set to ‘10’. The oversampling is set using the SCB_CTRL.OVS register field. The oversampling value is SCB_CTRL.OVS + 1. In the UART standard sub-mode (including LIN) and the SmartCard sub-mode, the valid range for the OVS field is [7, 15].

In UART transmit IrDA sub-mode, this field indirectly specifies the oversampling. Oversampling determines the interface clock per bit cycle and the width of the pulse. This sub-mode has only one valid OVS value—16; the pulse width is roughly 3/16 of the bit period (for all bit rates).

In UART receive IrDA sub-mode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6, and 115.2 kbps), this field indirectly specifies the oversampling. In normal transmission mode, this pulse is approximately 3/16 of the bit period (for all bit rates). In low-power transmission mode, this pulse is potentially smaller (down to 1.62 µs typical and 1.41 µs minimal) than 3/16 of the bit period (for less than 115.2 kbps bit rates).

Pulse widths greater than or equal to two SCB input clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two clock cycles and greater than or equal to one SCB input clock cycle may be detected by the receiver. Pulse widths less than one SCB input clock cycle will not be detected by the receiver. Note that the RX_CTRL.MEDIAN should be set to ‘1’ for IrDA receiver functionality.

The SCB input clock and the oversampling together determine the IrDA bit rate. Refer to the PSoC 63 with BLE Registers TRM for more details on the OVS values for different baud rates.

25.4.5 Enabling and Initializing the UART

The UART must be programmed in the following order:

1. Program protocol specific information using the UART_TX_CTRL, UART_RX_CTRL, and UART_FLOW_CTRL registers. This includes selecting the submodes of the protocol, transmitter-receiver functionality, and so on.

2. Program the generic transmitter and receiver information using the SCB_TX_CTRL and SCB_RX_CTRL registers.
   a. Specify the data frame width.
   b. Specify whether MSb or LSb is the first bit to be transmitted or received.

3. Program the transmitter and receiver FIFOs using the SCB_TX_FIFO_CTRL and SCB_RX_FIFO_CTRL registers, respectively.
   a. Set the trigger level.
   b. Clear the transmitter and receiver FIFO and Shift registers.

4. Enable the block (write a ‘1’ to the ENABLE bit of the SCB_CTRL register). After the block is enabled, control bits should not be changed. Changes should be made after disabling the block; for example, to modify the operation mode (from SmartCard to IrDA). The change takes effect only after the block is re-enabled. Note that re-enabling the block causes re-initialization and the associated state is lost (for example FIFO content).
25.4.6 I/O Pad Connection

25.4.6.1 Standard UART Mode

Figure 25-30 and Table 25-6 list the use of the I/O pads for the Standard UART mode.

Figure 25-30. Standard UART Mode I/O Pad Connections

<table>
<thead>
<tr>
<th>I/O Pads</th>
<th>Drive Mode</th>
<th>On-chip I/O Signals</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>uart_tx</td>
<td>Normal output mode</td>
<td>uart_tx_out_en</td>
<td>Transmit a data element</td>
</tr>
<tr>
<td></td>
<td></td>
<td>uart_tx_out</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>uart_tx_in</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Input only</td>
<td>uart_rx_in</td>
<td>Receive a data element</td>
</tr>
</tbody>
</table>

Table 25-6. UART I/O Pad Connection Usage

25.4.6.2 SmartCard Mode

Figure 25-31 and Table 25-7 list the use of the I/O pads for the SmartCard mode.

Figure 25-31. SmartCard Mode I/O Pad Connections

<table>
<thead>
<tr>
<th>I/O Pads</th>
<th>Drive Mode</th>
<th>On-chip I/O Signals</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>uart_tx</td>
<td>Open drain (pull-up)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>uart_tx_out_en</td>
<td>Used to receive a data element.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>uart_tx_out</td>
<td>Receive a negative acknowledgement of a transmitted data element</td>
</tr>
<tr>
<td></td>
<td></td>
<td>uart_tx_in</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>uart_rx_out_en</td>
<td>Transmit a data element.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>uart_rx_out</td>
<td>Transmit a negative acknowledgement to a received data element.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>uart_rx_in</td>
<td></td>
</tr>
</tbody>
</table>

Table 25-7. SmartCard Mode I/O Pad Connections
25.4.6.3  **LIN Mode**

Figure 25-32 and Table 25-8 list the use of the I/O pads for LIN mode.

![Figure 25-32. LIN Mode I/O Pad Connections](image)

<table>
<thead>
<tr>
<th>I/O Pads</th>
<th>Drive Mode</th>
<th>On-chip I/O Signals</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>uart_tx</td>
<td>Normal output</td>
<td>uart_tx_out_en</td>
<td>Transmit a data element.</td>
</tr>
<tr>
<td></td>
<td>mode</td>
<td>uart_tx_out</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>uart_rx_in</td>
<td></td>
</tr>
<tr>
<td>uart_rx</td>
<td>Input only</td>
<td>uart_rx_in</td>
<td>Receive a data element.</td>
</tr>
</tbody>
</table>

25.4.6.4  **IrDA Mode**

Figure 25-33 and Table 25-9 list the use of the I/O pads for IrDA mode.

![Figure 25-33. IrDA Mode I/O Pad Connections](image)

<table>
<thead>
<tr>
<th>I/O Pads</th>
<th>Drive Mode</th>
<th>On-chip I/O Signals</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>uart_tx</td>
<td>Normal output</td>
<td>uart_tx_out_en</td>
<td>Transmit a data element.</td>
</tr>
<tr>
<td></td>
<td>mode</td>
<td>uart_tx_out</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>uart_rx_in</td>
<td></td>
</tr>
<tr>
<td>uart_rx</td>
<td>Input only</td>
<td>uart_rx_in</td>
<td>Receive a data element.</td>
</tr>
</tbody>
</table>
25.4.7 UART Registers

The UART interface is controlled using a set of 32-bit registers listed in Table 25-10. For more information on these registers, see the *PSoC 63 with BLE Registers TRM*.

Table 25-10. UART Registers

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCB_CTRL</td>
<td>Enables the SCB; selects the type of serial interface (SPI, UART, ( \tilde{I}^2 C ))</td>
</tr>
<tr>
<td>SCB_UART_CTRL</td>
<td>Used to select the sub-modes of UART (standard UART, SmartCard, IrDA), also used for local loop back control.</td>
</tr>
<tr>
<td>SCB_UART_RX_STATUS</td>
<td>Used to specify the BR_COUNTER value that determines the bit period. This is used to set the accuracy of the SCB clock. This value provides more granularity than the OVS bit in SCB_CTRL register.</td>
</tr>
<tr>
<td>SCB_UART_TX_CTRL</td>
<td>Used to specify the number of stop bits, enable parity, select the type of parity, and enable retransmission on NACK.</td>
</tr>
<tr>
<td>SCB_UART_RX_CTRL</td>
<td>Performs same function as SCB_UART_TX_CTRL but is also used for enabling multi processor mode, LIN mode drop on parity error, and drop on frame error.</td>
</tr>
<tr>
<td>SCB_TX_CTRL</td>
<td>Used to specify the data frame width and to specify whether MSb or LSb is the first bit in transmission.</td>
</tr>
<tr>
<td>SCB_RX_CTRL</td>
<td>Performs the same function as that of the SCB_TX_CTRL register, but for the receiver. Also decides whether a median filter is to be used on the input interface lines.</td>
</tr>
<tr>
<td>SCB_UART_FLOW_CONTROL</td>
<td>Configures flow control for UART transmitter.</td>
</tr>
</tbody>
</table>
25.5  Inter Integrated Circuit (I\textsuperscript{2}C)

This section explains the I\textsuperscript{2}C implementation in the PSoC 6 MCU. For more information on the I\textsuperscript{2}C protocol specification, refer to the I\textsuperscript{2}C-bus specification available on the NXP website. In PSoC 6 MCUs, eight out of nine SCB blocks support full I\textsuperscript{2}C and one SCB supports only I\textsuperscript{2}C slave mode; this SCB is also available in Deep Sleep power mode and allows externally-clocked operations.

25.5.1  Features

This block supports the following features:
- Master, slave, and master/slave mode
- Standard-mode (100 kbps), fast-mode (400 kbps), and fast-mode plus (1000 kbps) data-rates
- 7-bit slave addressing
- Clock stretching
- Collision detection
- Programmable oversampling of I\textsuperscript{2}C clock signal (SCL)
- Auto ACK when Rx FIFO not full, including address
- General address detection
- FIFO Mode
- EZ and CMD_RESP modes

25.5.2  General Description

Figure 25-34 illustrates an example of an I\textsuperscript{2}C communication network.

The standard I\textsuperscript{2}C bus is a two wire interface with the following lines:
- Serial Data (SDA)
- Serial Clock (SCL)

I\textsuperscript{2}C devices are connected to these lines using open collector or open-drain output stages, with pull-up resistors (Rp). A simple master/slave relationship exists between devices. Masters and slaves can operate as either transmitter or receiver. Each slave device connected to the bus is software addressable by a unique 7-bit address.
25.5.3 Terms and Definitions

Table 25-11 explains the commonly used terms in an I\textsuperscript{2}C communication network.

<table>
<thead>
<tr>
<th>Term</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmitter</td>
<td>The device that sends data to the bus</td>
</tr>
<tr>
<td>Receiver</td>
<td>The device that receives data from the bus</td>
</tr>
<tr>
<td>Master</td>
<td>The device that initiates a transfer, generates clock signals, and terminates a transfer</td>
</tr>
<tr>
<td>Slave</td>
<td>The device addressed by a master</td>
</tr>
<tr>
<td>Multi-master</td>
<td>More than one master can attempt to control the bus at the same time</td>
</tr>
<tr>
<td>Arbitration</td>
<td>Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the winning message is not corrupted</td>
</tr>
<tr>
<td>Synchronization</td>
<td>Procedure to synchronize the clock signals of two or more devices</td>
</tr>
</tbody>
</table>

25.5.3.1 Clock Stretching

When a slave device is not yet ready to process data, it may drive a ‘0’ on the SCL line to hold it down. Due to the implementation of the I/O signal interface, the SCL line value will be ‘0’, independent of the values that any other master or slave may be driving on the SCL line. This is known as clock stretching and is the only situation in which a slave drives the SCL line. The master device monitors the SCL line and detects it when it cannot generate a positive clock pulse (‘1’) on the SCL line. It then reacts by delaying the generation of a positive edge on the SCL line, effectively synchronizing with the slave device that is stretching the clock. The SCB on the PSoC 6 MCU can and will stretch the clock.

25.5.3.2 Bus Arbitration

The I\textsuperscript{2}C protocol is a multi-master, multi-slave interface. Bus arbitration is implemented on master devices by monitoring the SDA line. Bus collisions are detected when the master observes an SDA line value that is not the same as the value it is driving on the SDA line. For example, when master 1 is driving the value ‘1’ on the SDA line and master 2 is driving the value ‘0’ on the SDA line, the actual line value will be ‘0’ due to the implementation of the I/O signal interface. Master 1 detects the inconsistency and loses control of the bus. Master 2 does not detect any inconsistency and keeps control of the bus.

25.5.4 I\textsuperscript{2}C Modes of Operation

I\textsuperscript{2}C is a synchronous single master, multi-master, multi-slave serial interface. Devices operate in either master mode, slave mode, or master/slave mode. In master/slave mode, the device switches from master to slave mode when it is addressed. Only a single master may be active during a data transfer. The active master is responsible for driving the clock on the SCL line. Table 25-12 illustrates the I\textsuperscript{2}C modes of operation.

Table 25-12. I\textsuperscript{2}C Modes

<table>
<thead>
<tr>
<th>Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slave</td>
<td>Slave only operation (default)</td>
</tr>
<tr>
<td>Master</td>
<td>Master only operation</td>
</tr>
<tr>
<td>Multi-master</td>
<td>Supports more than one master on the bus</td>
</tr>
</tbody>
</table>

Data transfer through the I\textsuperscript{2}C bus follows a specific format. Table 25-13 lists some common bus events that are part of an I\textsuperscript{2}C data transfer. The Write Transfer and Read Transfer sections explain the I\textsuperscript{2}C bus bit format during data transfer.

Table 25-13. I\textsuperscript{2}C Bus Events Terminology

<table>
<thead>
<tr>
<th>Bus Event</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>START</td>
<td>A HIGH to LOW transition on the SDA line while SCL is HIGH</td>
</tr>
<tr>
<td>STOP</td>
<td>A LOW to HIGH transition on the SDA line while SCL is HIGH</td>
</tr>
<tr>
<td>ACK</td>
<td>The receiver pulls the SDA line LOW and it remains LOW during the HIGH period of the clock pulse, after the transmitter transmits each byte. This indicates to the transmitter that the receiver received the byte properly.</td>
</tr>
<tr>
<td>NACK</td>
<td>The receiver does not pull the SDA line LOW and it remains HIGH during the HIGH period of clock pulse after the transmitter transmits each byte. This indicates to the transmitter that the receiver received the byte properly.</td>
</tr>
<tr>
<td>Repeated START</td>
<td>START condition generated by master at the end of a transfer instead of a STOP condition</td>
</tr>
<tr>
<td>DATA</td>
<td>SDA status change while SCL is LOW (data changing), and no change while SCL is HIGH (data valid)</td>
</tr>
</tbody>
</table>

With all of these modes, there are two types of transfer - read and write. In write transfer, the master sends data to slave; in read transfer, the master receives data from slave.
25.5.4.1 Write Transfer

A typical write transfer begins with the master generating a START condition on the I2C bus. The master then writes a 7-bit I2C slave address and a write indicator ('0') after the START condition. The addressed slave transmits an acknowledgement byte by pulling the data line low during the ninth bit time.

If the slave address does not match any of the slave devices or if the addressed device does not want to acknowledge the request, it transmits a no acknowledgement (NACK) by not pulling the SDA line low. The absence of an acknowledgement, results in an SDA line value of ‘1’ due to the pull-up resistor implementation.

If no acknowledgement is transmitted by the slave, the master may end the write transfer with a STOP event. The master can also generate a repeated START condition for a retry attempt.

The master may transmit data to the bus if it receives an acknowledgement. The addressed slave transmits an acknowledgement to confirm the receipt of every byte of data written. Upon receipt of this acknowledgement, the master may transmit another data byte.

When the transfer is complete, the master generates a STOP condition.

25.5.4.2 Read Transfer

A typical read transfer begins with the master generating a START condition on the I2C bus. The master then writes a 7-bit I2C slave address and a read indicator ('1') after the START condition. The addressed slave transmits an acknowledgement by pulling the data line low during the ninth bit time.

If the slave address does not match with that of the connected slave device or if the addressed device does not want to acknowledge the request, a no acknowledgement (NACK) is transmitted by not pulling the SDA line low. The absence of an acknowledgement, results in an SDA line value of ‘1’ due to the pull-up resistor implementation.

If no acknowledgement is transmitted by the slave, the master may end the read transfer with a STOP event. The master can also generate a repeated START condition for a retry attempt.

If the slave acknowledges the address, it starts transmitting data after the acknowledgement signal. The master transmits an acknowledgement to confirm the receipt of each data byte sent by the slave. Upon receipt
of this acknowledgement, the addressed slave may transmit another data byte.

- The master can send a NACK signal to the slave to stop the slave from sending data bytes. This completes the read transfer.
- When the transfer is complete, the master generates a STOP condition.

25.5.5 I²C Buffer Modes

I²C can operate in three different buffered modes – FIFO, EZ, and CMD_RESP modes. The buffer is used in different ways in each of the modes. The following subsections explain each of these buffered modes in detail.

25.5.5.1 FIFO Mode

The FIFO mode has a Tx FIFO for the data being transmitted and an Rx FIFO for the data being received. Each FIFO is constructed out of the SRAM buffer. The FIFOs are either 64 elements deep with 16-bit data elements or 128 elements deep with 8-bit data elements. The width of the data elements are configured using the CTRL.BYTE_MODE bitfield of the SCB. For I²C, put the FIFO in BYTE mode because all transactions are a byte wide.

The FIFO mode operation is available only in Active and Sleep power modes, not in the Deep Sleep power mode. However, on the Deep Sleep-capable SCB the slave address can be used to wake the device from sleep.

Transmit and receive FIFOs allow write and read accesses. A write access to the transmit FIFO uses register TX_FIFO_WR. A read access from the receive FIFO uses register RX_FIFO_RD.

Transmit and receive FIFO status information is available through status registers TX_FIFO_STATUS and RX_FIFO_STATUS. You can define a programmable threshold that indicates a number of FIFO entries. A trigger/event is generated when the following conditions are met:

- The transmit FIFO has a TX_FIFO_CTRL.TRIGGER_LEVEL. A trigger/event is generated when number of entries in the transmit FIFO is less than TX_FIFO_CTRL.TRIGGER_LEVEL.
- The receive FIFO has an RX_FIFO_CTRL.TRIGGER_LEVEL. A trigger/event is generated when number of receive FIFO entries is greater than the RX_FIFO_CTRL.TRIGGER_LEVEL.

Furthermore, several interrupt status bits are provided as well, which indicate whether the FIFOs are full, empty, and so on.

Deep Sleep to Active Transition

EC_AM = 1, EC_OP = 0, FIFO Mode.

Master Write:

- S_NOT_READY_ADDR_NACK = 0, S_READY_ADDR_ACK = 1. The clock is stretched until the internally-clocked logic takes over, at which point the address is ACK’d and the master can start writing data. Before going to Deep Sleep, clk_scb needs to be disabled. Upon wake up from Deep Sleep clk_scb must be re-enabled; this is when the clock stretch will be released.
- S_NOT_READY_ADDR_NACK = 1, S_READY_ADDR_ACK = 0. The clock is stretched until the internally-clocked logic takes over and the CPU writes either S_ACK, or S_NACK. Before going to Deep Sleep, clk_scb needs to be disabled. Upon wake up from Deep Sleep, clk_scb must be re-enabled; do this before setting S_ACK or S_NACK.

Master Read:

- S_NOT_READY_ADDR_NACK = 0, S_READY_ADDR_ACK = x. The incoming address is stretched until the internally-clocked logic takes over. When the internally clocked logic takes over, there is no guarantee that the internal clock will be at the correct frequency due to PLL/FLL locking times. This may lead to incorrect timing on the I²C bus for the ACK/NACK. To avoid this, disable clk_scb before going to Deep Sleep mode, and then re-enable after the PLL/FLL have stabilized.

Note: When doing a repeated start after a write, wait until the UNDERFLOW interrupt status is asserted before setting the I²C_M_CMD.START bit and writing the new address into the TX_FIFO. Otherwise, the address in the FIFO will be sent as data and not as an address.
25.5.5.2 **EZI2C Mode**

The Easy I²C (EZI2C) protocol is a unique communication scheme built on top of the I²C protocol by Cypress. It uses a meta protocol around the standard I²C protocol to communicate to an I²C slave using indexed memory transfers. This removes the need for CPU intervention.

The EZI2C protocol defines a single memory buffer with an 8-bit address that indexes the buffer (256-entry array of 8-bit per entry is supported) located on the slave device. The EZ address is used to address these 256 locations. The CPU writes and reads to the memory buffer through the EZ_DATA registers. These accesses are word accesses, but only the least significant byte of the word is used.

The slave interface accesses the memory buffer using the current address. At the start of a transfer (I²C START/RESTART), the base address is copied to the current address. A data element write or read operation is to the current address location. After the access, the current address is incremented by 1.

If the current address equals the last memory buffer address (255), the current address is not incremented. Subsequent write accesses will overwrite any previously written value at the last buffer address. Subsequent read accesses will continue to provide the (same) read value at the last buffer address. The bus master should be aware of the memory buffer capacity in EZ mode.

The I²C base and current addresses are provided through I²C_STATUS. At the end of a transfer (I²C), the difference between the base and current addresses indicates how many read or write accesses were performed. The block provides interrupt cause fields to identify the end of a transfer. EZ mode operation is available in Active, Sleep, and Deep Sleep power modes. In PSoC 6 MCUs, only the Deep Sleep-capable SCB block operate in EZI2C mode.

EZI2C distinguishes three operation phases:

- **Address phase**: The master transmits an 8-bit address to the slave. This address is used as the slave base and current address.
- **Write phase**: The master writes 8-bit data element(s) to the slave’s memory buffer. The slave’s current address is set to the slave’s base address. Received data elements are written to the current address memory location. After each memory write, the current address is incremented.
- **Read phase**: The master reads 8-bit data elements from the slave’s memory buffer. The slave’s current address is set to the slave’s base address. Transmitted data elements are read from the current address memory location. After each memory read, the current address is incremented.

Note that a slave’s base address is updated by the master and not by the CPU.
Deep Sleep to Active Transition

EC_AM = 1, EC_OP = 0, EZ Mode.

- S_NOT_READY_ADDR_NACK = 0, S_READY_ADDR_ACK = 1. The clock is stretched until the internally-clocked logic takes over at which point the address is ACK’d and master can start writing data. Before going to Deep Sleep clk_scb must be disabled. Upon wake up from Deep Sleep clk_scb must be re-enabled this is when the clock stretch will be released.

- S_NOT_READY_ADDR_NACK = 1, S_READY_ADDR_ACK = x. The incoming address is NACK’d until the internally-clocked logic takes over. When this happens, there is no guarantee that the internal clock will be at the correct frequency due to PLL/FLL locking times. To avoid this, disable clk_scb before going to Deep Sleep mode, and then re-enable after the PLL/FLL have stabilized.

25.5.5.3 Command-Response Mode

In the PSoC 6 MCU, only the Deep Sleep-capable SCB supports the command-response mode. This mode has a single memory buffer, a base read address, a current read address, a base write address, and a current write address that are used to index the memory buffer. The base addresses are provided by the CPU. The current addresses are used by the slave to index the memory buffer for sequential accesses of the memory buffer. The memory buffer holds 256 8-bit data elements. The base and current addresses are in the range [0 to 255].

The CPU writes and reads to the memory buffer through the SCB_EZ_DATA registers. These are word accesses, but only the least significant byte of the word is used.

The slave interface accesses the memory buffer using the current addresses. At the start of a write transfer (I²C START/RESTART), the base write address is copied to the current write address. A data element write is to the current write address location. After the write access, the current address is incremented by ‘1’. At the start of a read transfer, the base read address is copied to the current read address. A data element read is to the current read address location. After the read data element is transmitted, the current read address is incremented by ‘1’.

If the current addresses equal the last memory buffer address (255), the current addresses are not incremented. Subsequent write accesses will overwrite any previously written value at the last buffer address. Subsequent read accesses will continue to provide the (same) read value at the last buffer address. The bus master should be aware of the memory buffer capacity in command-response mode.
The base addresses are provided through CMD_RESP_CTRL. The current addresses are provided through CMD_RESP_STATUS. At the end of a transfer (I^2C stop), the difference between a base and current address indicates how many read/write accesses were performed. The block provides interrupt cause fields to identify the end of a transfer. Command-response mode operation is available in Active, Sleep, and Deep Sleep power modes. The command-response mode has two phases of operation:

- **Write phase** - The write phase begins with a START/RESTART followed by the slave address with read/write bit set to ‘0’ indicating a write. The slave’s current write address is set to the slave’s base write address. Received data elements are written to the current write address memory location. After each memory write, the current write address is incremented.

- **Read phase** - The read phase begins with a START/RESTART followed by the slave address with read/write bit set to ‘1’ indicating a read. The slave’s current read address is set to the slave’s base read address. Transmitted data elements are read from the current address memory location. After each read data element is transferred, the current read address is incremented.

Note that a slave’s base addresses are updated by the CPU and not by the master.
25.5.6 Clocking and Oversampling

The SCB I^2C supports both internally and externally clocked operation modes. Two bitfields (EC_AM_MODE and EC_OP_MODE) in the SCB_CTRL register determine the SCB clock mode. EC_AM_MODE indicates whether I^2C address matching is internally (0) or externally (1) clocked. I^2C address matching comprises the first part of the I^2C protocol. EC_OP_MODE indicates whether the rest of the protocol operation (besides I^2C address matching) is internally (0) or externally (1) clocked. The externally clocked mode of operation is supported only in the I^2C slave mode.

An internally clocked operation uses the programmable clock dividers. For more information on system clocking, see the Clocking System chapter on page 146. The internally-clocked mode does not support the command-response mode.

Note: In the PSoC 6 MCU, only the Deep Sleep-capable SCB supports externally-clocked mode of operation.

The SCB_CTRL bitfields EC_AM_MODE and EC_OP_MODE can be configured in the following ways.

- **EC_AM_MODE is '0' and EC_OP_MODE is '0':** Use this configuration when only Active mode functionality is required.
  - FIFO mode: Supported.
  - EZ mode: Supported.
  - Command-response mode: Not supported. The slave NACKs every slave address.

- **EC_AM_MODE is '1' and EC_OP_MODE is '0':** Use this configuration when both Active and Deep Sleep functionality are required. An externally-clocked operation uses a clock provided by the serial interface. The externally clocked mode does not support FIFO mode. If EC_OP_MODE is '1', the external interface logic accesses the memory buffer on the external interface clock (I^2C SCL). This allows for EZ and CMD_RESP mode functionality in Active and Deep Sleep power modes.

Table 25-14. Clock Configuration and Mode support

<table>
<thead>
<tr>
<th>Mode</th>
<th>EC_AM_MODE is '0'; EC_OP_MODE is '0'</th>
<th>'EC_AM_MODE is '1'; EC_OP_MODE is '0'</th>
<th>'EC_AM_MODE is '1'; EC_OP_MODE is '1'</th>
</tr>
</thead>
<tbody>
<tr>
<td>FIFO mode</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>EZ mode</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>CMD_RESP mode</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>

An externally-clocked operation uses a clock provided by the serial interface. The externally clocked mode does not support FIFO mode. If EC_OP_MODE is '1', the external interface logic accesses the memory buffer on the external interface clock (I^2C SCL). This allows for EZ and CMD_RESP mode functionality in Active and Deep Sleep power modes.

In Active system power mode, the memory buffer requires arbitration between external interface logic (on I^2C SCL) and the CPU interface logic (on system peripheral clock). This arbitration always gives the highest priority to the external interface logic (host accesses). The external interface logic takes one serial interface clock/bit periods for the I^2C. During this period, the internal logic is denied service to the memory buffer. The PSoC 6 MCU provides two programmable options to address this “denial of service”:

- If the BLOCK bitfield of SCB_CTRL is '1': An internal logic access to the memory buffer is blocked until the memory buffer is granted and the external interface logic has completed access. For a 100-kHz I^2C interface, the maximum blocking period of one serial interface bit period measures 10 µs (approximately 208 clock cycles on a 48 MHz SCB input clock). This option provides normal SCB register functionality, but the blocking time introduces additional internal bus wait states.

- If the BLOCK bitfield of SCB_CTRL is '0': An internal logic access to the memory buffer is not blocked, but fails when it conflicts with an external interface logic
access. A read access returns the value 0xFFFF:FFFF and a write access is ignored. This option does not introduce additional internal bus wait states, but an access to the memory buffer may not take effect. In this case, following failures are detected:

- **Read Failure:** A read failure is easily detected, as the returned value is 0xFFFF:FFFF. This value is unique as non-failing memory buffer read accesses return an unsigned byte value in the range 0x0000:0000-0x0000:00FF.
- **Write Failure:** A write failure is detected by reading back the written memory buffer location, and confirming that the read value is the same as the written value.

For both options, a conflicting internal logic access to the memory buffer sets INTR_TX.BLOCKED field to ‘1’ (for write accesses) and INTR_RX.BLOCKED field to ‘1’ (for read accesses). These fields can be used as either status fields or as interrupt cause fields (when their associated mask fields are enabled).

If a series of read or write accesses is performed and CTRL.BLOCKED is ‘0’, a failure is detected by comparing the logical OR of all read values to 0xFFFF:FFFF and checking the INTR_TX.BLOCKED and INTR_RX.BLOCKED fields to determine whether a failure occurred for a (series of) write or read operation(s).

**Note:** In PSoC 6 MCUs, only one SCB supports externally clocked mode of operation.

### 25.5.6.1 Glitch Filtering

The PSoC 6 MCU SCB I²C has analog and digital glitch filters. Analog glitch filters are applied on the i2c_scl_in and i2c_sda_in input signals (AF_in) to filter glitches of up to 50 ns. An analog glitch filter is also applied on the i2c_sda_out output signal (AF_out). Analog glitch filters are enabled and disabled in the SCB.I2C_CFG register. Do not change the _TRIM bitfields; only change the _SEL bitfields in this register.

Digital glitch filters are applied on the i2c_scl_in and i2c_sda_in input signals (DF_in). The digital glitch filter is enabled in the SCB.RX_CTRL register via the MEDIAN bitfield.

The following table lists the useful combinations of glitch filters.

<table>
<thead>
<tr>
<th>AF_in</th>
<th>AF_out</th>
<th>DF_in</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Used when operating in internally-clocked mode and in master in fast-mode plus (1-MHz speed mode)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Used when operating in internally-clocked mode (EC_OP_MODE is ‘0’)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Used when operating in externally-clocked mode (EC_OP_MODE is ‘1’). Only slave mode.</td>
</tr>
</tbody>
</table>

When operating in EC_OP_MODE = 1, the 100-kHz, 400-kHz, and 1000-kHz modes require the following settings for AF_out:

<table>
<thead>
<tr>
<th>AF_in</th>
<th>AF_out</th>
<th>DF_in</th>
<th>Settings</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>100-kHz: I2C_CFG.SDA_OUT_FILT_SEL = 3, 400-kHz: I2C_CFG.SDA_OUT_FILT_SEL = 3, 1000-kHz: I2C_CFG.SDA_OUT_FILT_SEL = 1</td>
</tr>
</tbody>
</table>
25.5.6.2 Oversampling and Bit Rate

Internally-clocked Master

The PSoC 6 MCU implements the I2C clock as an oversampled multiple of the SCB input clock. In master mode, the block determines the I2C frequency. Routing delays on the PCB, on the chip, and the SCB (including analog and digital glitch filters) all contribute to the signal interface timing. In master mode, the block operates off CLK_SCB and uses programmable oversampling factors for the SCL high (1) and low (0) times.

Table 25-16. I2C Frequency and Oversampling Requirements in I2C Master Mode

<table>
<thead>
<tr>
<th>AF_in</th>
<th>AF_out</th>
<th>DF_in</th>
<th>Mode</th>
<th>Supported Frequency</th>
<th>LOW_PHASE_OVS</th>
<th>HIGH_PHASE_OVS</th>
<th>clk_scb Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>100 kHz</td>
<td>[62, 100] kHz</td>
<td>[9, 15]</td>
<td>[9, 15]</td>
<td>[1.6, 3.2] MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>400 kHz</td>
<td>[264, 400] kHz</td>
<td>[13, 5]</td>
<td>[7, 15]</td>
<td>[6.7, 10] MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1000 kHz</td>
<td>[447, 1000] kHz</td>
<td>[8, 15]</td>
<td>[5, 15]</td>
<td>[12.1, 25.8] MHz</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>100 kHz</td>
<td>[48, 100] kHz</td>
<td>[7, 15]</td>
<td>[7, 15]</td>
<td>[1.3, 3.2] MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>400 kHz</td>
<td>[244, 400] kHz</td>
<td>[12, 15]</td>
<td>[7, 15]</td>
<td>[6.0, 10] MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1000 kHz</td>
<td>Not supported</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 25-16 assumes worst-case conditions on the I2C bus. The following equations can be used to determine the settings for your own system. This will involve measuring the rise and fall times on SCL and SDA lines in your system.

$$t_{\text{CLK\_SCB\(\text{Min}\)}} = \frac{t_{\text{LOW}} + t_{\text{F}}}{\text{LOW\_PHASE\_OVS}}$$

If clk_scb is any faster than this, the tLOW of the I2C specification will be violated. tF needs to be measured in your system.

$$t_{\text{CLK\_SCB\(\text{Max}\)}} = \frac{t_{\text{VD}} - t_{\text{RF}} - 100 \text{ ns}}{3}$$ (When analog filter is enabled and digital disabled)

$$t_{\text{CLK\_SCB\(\text{Max}\)}} = \frac{t_{\text{VD}} - t_{\text{RF}}}{4}$$ (When analog filter is disabled and analog filter is enabled)

tRF is the maximum of either the rise or fall time. If clk_scb is slower than this frequency, tVD will be violated.

Internally-clocked Slave

In slave mode, the I2C frequency is determined by the incoming I2C SCL signal. To ensure proper operation, clk_scb must be significantly higher than the I2C bus frequency. Unlike master mode, this mode does not use programmable oversampling factors.

Table 25-17. SCB Input Clock Requirements in I2C Slave Mode

<table>
<thead>
<tr>
<th>AF_in</th>
<th>AF_out</th>
<th>DF_in</th>
<th>Mode</th>
<th>clk_scb Frequency Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>100 kHz</td>
<td>[1.6, 12.8] MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>400 kHz</td>
<td>[6.7, 17.1] MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1000 kHz</td>
<td>[12.1, 44.8] MHz</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>100 kHz</td>
<td>[1.3, 12.8] MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>400 kHz</td>
<td>[6.0, 16.0] MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1000 kHz</td>
<td>[13.0, 94.1] MHz</td>
</tr>
</tbody>
</table>

$$t_{\text{CLK\_SCB\(\text{Max}\)}} = \frac{t_{\text{VD}} - t_{\text{RF}} - 100 \text{ ns}}{3}$$ (When analog filter is enabled and digital disabled)

$$t_{\text{CLK\_SCB\(\text{Max}\)}} = \frac{t_{\text{VD}} - t_{\text{RF}}}{4}$$ (When analog filter is disabled and analog filter is enabled)

tRF is the maximum of either the rise or fall time. If clk_scb is slower than this frequency, tVD will be violated.
The minimum period of $clk_{scb}$ is determined by one of the following equations:

$$t_{CLK_{SCB} (MIN)} = \left( t_{SU;DAT(min)} + t_{RF} \right) / 16$$

or

$$t_{CLK_{SCB} (MIN)} = (0.6 \times t_F - 50 \text{ ns}) / 2 \quad \text{(When analog filter is enabled and digital disabled)}$$

$$t_{CLK_{SCB} (MIN)} = (0.6 \times t_F) / 3 \quad \text{(When analog filter is disabled and digital enabled)}$$

The result that yields the largest period from the two sets of equations above should be used to set the minimum period of $clk_{scb}$.

**Master-Slave**

In this mode, when the SCB is acting as a master device, the block determines the $I^2C$ frequency. When the SCB is acting as a slave device, the block does not determine the $I^2C$ frequency. Instead, the incoming $I^2C$ SCL signal does.

To guarantee operation in both master and slave modes, choose clock frequencies that work for both master and slave using the tables above.

**25.5.7 Enabling and Initializing the $I^2C$**

The following section describes the method to configure the $I^2C$ block for standard (non-EZ) mode and EZI2C mode.

**25.5.7.1 Configuring for $I^2C$ FIFO Mode**

The $I^2C$ interface must be programmed in the following order.

1. Program protocol specific information using the SCB_I2C_CTRL register. This includes selecting master - slave functionality.
2. Program the generic transmitter and receiver information using the SCB_TX_CTRL and SCB_RX_CTRL registers.
3. Set the SCB_CTRL.BYTE_MODE to ‘1’ to enable the byte mode.
4. Program the SCB_CTRL register to enable the $I^2C$ block and select the $I^2C$ mode. For a complete description of the $I^2C$ registers, see the *PSoC 63 with BLE Registers TRM*.

**25.5.7.2 Configuring for EZ and CMD_RESP Modes**

To configure the $I^2C$ block for EZ and CMD_RESP modes, set the following $I^2C$ register bits

1a. Select the EZI2C mode by writing ‘1’ to the EZ_MODE bit (bit 10) of the SCB_CTRL register.
1b. Select CMD_RESP mode by writing a 1 to the CMD_RESP bit (bit 12) of the SCB_CTRL register.
2. Set the S_READY_ADDR_ACK (bit 12) and S_READY_DATA_ACK (bit 13) bits of the SCB_I2C_CTRL register.
25.5.8 I/O Pad Connections

When configuring the I2C SDA/SCL lines, the following sequence must be followed. If this sequence is not followed, the I2C lines may initially have overshoot and undershoot.

1. Set CTRL.SCB_CTRL_MODE to 0.
2. Set TX_CTRL.OPEN_DRAIN to 1.
3. Configure I2C pins for high-impedance drive mode.
4. Configure SCB for I2C
5. Enable SCB
6. Configure I2C pins for Open Drain Drives Low.

25.5.9 I2C Registers

The I2C interface is controlled by reading and writing a set of configuration, control, and status registers, as listed in Table 25-19.

<table>
<thead>
<tr>
<th>Register</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCB_CTRL</td>
<td>Enables the SCB block and selects the type of serial interface (SPI, UART, I2C). Also used to select internally and externally clocked operation and EZ and non-EZ modes of operation.</td>
</tr>
<tr>
<td>SCB_I2C_CTRL</td>
<td>Selects the mode (master, slave) and sends an ACK or NACK signal based on receiver FIFO status.</td>
</tr>
<tr>
<td>SCB_I2C_STATUS</td>
<td>Indicates bus busy status detection, read/write transfer status of the slave/master, and stores the EZ slave address.</td>
</tr>
<tr>
<td>SCB_I2C_M_CMD</td>
<td>Enables the master to generate START, STOP, and ACK/NACK signals.</td>
</tr>
<tr>
<td>SCB_I2C_S_CMD</td>
<td>Enables the slave to generate ACK/NACK signals.</td>
</tr>
</tbody>
</table>
Table 25-19. \( ^2 \text{C} \) Registers

<table>
<thead>
<tr>
<th>Register</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCB_STATUS</td>
<td>Indicates whether the externally clocked logic is using the EZ memory. This bit can be used by software to determine whether it is safe to issue a software access to the EZ memory.</td>
</tr>
<tr>
<td>SCB_I2C_CFG</td>
<td>Configures filters, which remove glitches from the SDA and SCL lines.</td>
</tr>
<tr>
<td>SCB_TX_CTRL</td>
<td>Specifies the data frame width; also used to specify whether MSb or LSb is the first bit in transmission.</td>
</tr>
<tr>
<td>SCB_TX_FIFO_CTRL</td>
<td>Specifies the trigger level, clearing of the transmitter FIFO and shift registers, and FREEZE operation of the transmitter FIFO.</td>
</tr>
<tr>
<td>SCB_TX_FIFO_STATUS</td>
<td>Indicates the number of bytes stored in the transmitter FIFO, the location from which a data frame is read by the hardware (read pointer), the location from which a new data frame is written (write pointer), and decides if the transmitter FIFO holds the valid data.</td>
</tr>
<tr>
<td>SCB_TX_FIFO_WR</td>
<td>Holds the data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation.</td>
</tr>
<tr>
<td>SCB_RX_CTRL</td>
<td>Performs the same function as that of the SCB_TX_CTRL register, but for the receiver. Also decides whether a median filter is to be used on the input interface lines.</td>
</tr>
<tr>
<td>SCB_RX_FIFO_CTRL</td>
<td>Performs the same function as that of the SCB_TX_FIFO_CTRL register, but for the receiver.</td>
</tr>
<tr>
<td>SCB_RX_FIFO_STATUS</td>
<td>Holds the data read from the receiver FIFO. Reading a data frame removes the data frame from the FIFO; behavior is similar to that of a POP operation. This register has a side effect when read by software: a data frame is removed from the FIFO.</td>
</tr>
<tr>
<td>SCB_RX_FIFO_RD</td>
<td>Holds the data read from the receiver FIFO. Reading a data frame does not remove the data frame from the FIFO; behavior is similar to that of a PEEK operation.</td>
</tr>
<tr>
<td>SCB_RX_FIFO_RD_SILENT</td>
<td>Holds the data read from the receiver FIFO. Reading a data frame does not remove the data frame from the FIFO; behavior is similar to that of a PEEK operation.</td>
</tr>
<tr>
<td>SCB_RX_MATCH</td>
<td>Stores slave device address and is also used as slave device address MASK.</td>
</tr>
<tr>
<td>SCB_EZ_DATA</td>
<td>Holds the data in an EZ memory location.</td>
</tr>
</tbody>
</table>

**Note:** Detailed descriptions of the \( ^2 \text{C} \) register bits are available in the *PSoC 63 with BLE Registers TRM*.

### 25.6 SCB Interrupts

SCB supports interrupt generation on various events. The interrupts generated by the SCB block vary depending on the mode of operation.

Table 25-20. SCB Interrupts

<table>
<thead>
<tr>
<th>Interrupt</th>
<th>Functionality</th>
<th>Active/Deep Sleep</th>
<th>Registers</th>
</tr>
</thead>
<tbody>
<tr>
<td>interrupt_master</td>
<td>( ^2 \text{C} ) master and SPI master functionality</td>
<td>Active</td>
<td>INTR_M, INTR_M_SET, INTR_M_MASK, INTR_M_MASKED</td>
</tr>
<tr>
<td>interrupt_slave</td>
<td>( ^2 \text{C} ) slave and SPI slave functionality</td>
<td>Active</td>
<td>INTR_S, INTR_S_SET, INTR_S_MASK, INTR_S_MASKED</td>
</tr>
</tbody>
</table>
The following sections explain the different interrupt sources for each mode of SCB operation.

**Note:** To avoid being triggered by events from previous transactions, whenever the firmware enables an interrupt mask register bit, it should clear the interrupt request register in advance.

**Note:** If the DMA is used to read data out of RX FIFO, the NOT_EMPTY interrupt may never trigger. This can occur when clk_peri (clocking DMA) is running much faster than the clock to the SCB. As a workaround to this issue, set the RX_FIFO_CTRL.TRIGGER_LEVEL to 1 (not 0); this will allow the interrupt to fire.

<table>
<thead>
<tr>
<th>Interrupt</th>
<th>Functionality</th>
<th>Active/Deep Sleep</th>
<th>Registers</th>
</tr>
</thead>
<tbody>
<tr>
<td>interrupt_tx</td>
<td>UART transmitter and Tx FIFO function</td>
<td>Active</td>
<td>INTR_TX, INTR_TX_SET, INTR_TX_MASK, INTR_TX_MASKED</td>
</tr>
<tr>
<td>interrupt_rx</td>
<td>UART receiver and Rx FIFO function</td>
<td>Active</td>
<td>INTR_RX, INTR_RX_SET, INTR_RX_MASK, INTR_RX_MASKED</td>
</tr>
<tr>
<td>interrupt_i2c_ec</td>
<td>Externally clocked I2C slave function</td>
<td>Deep Sleep</td>
<td>INTR_I2C_EC, INTR_I2C_EC_MASK, INTR_I2C_EC_MASKED</td>
</tr>
<tr>
<td>interrupt_spi_ec</td>
<td>Externally clocked SPI slave function</td>
<td>Deep Sleep</td>
<td>INTR_SPI_EC, INTR_SPI_EC_MASK, INTR_SPI_EC_MASKED</td>
</tr>
</tbody>
</table>
25.6.1 SPI Interrupts

The SPI interrupts can be classified as master interrupts, slave interrupts, Tx interrupts, Rx interrupts, and externally clocked (EC) mode interrupts. Each interrupt output is the logical OR of the group of all possible interrupt sources classified under the section. For example, the Tx interrupt output is the logical OR of the group of all possible Tx interrupt sources. This signal goes high when any of the enabled Tx interrupt sources are true. The SCB also provides an interrupt cause register (SCB_INTR_CAUSE) that can be used to determine interrupt source. The interrupt registers are cleared by writing ‘1’ to the corresponding bitfield. Note that certain interrupt sources are triggered again as long as the condition is met even if the interrupt source was cleared. For example, the TX_FIFO_EMPTY is set as long as the transmit FIFO is empty even if the interrupt source is cleared. For more information on interrupt registers, see the PSoC 63 with BLE Registers TRM. The SPI supports interrupts on the following events:

- SPI master interrupts
  - SPI master transfer done
- SPI slave interrupts
  - SPI Bus Error - Slave deselected at an unexpected time in the SPI transfer. The firmware may decide to clear the Tx and Rx FIFOs for this error.
  - SPI slave deselected after any EZSPI transfer occurred
  - SPI slave deselected after a write EZSPI transfer occurred
- SPI Tx
  - Tx FIFO has less entries than the value specified by TRIGGER_LEVEL in SCB_TX_FIFO_CTRL
  - Tx FIFO is not full
  - Tx FIFO is empty
  - Tx FIFO overflow
  - Tx FIFO underflow
- SPI Rx
  - Rx FIFO has more entries than the value specified by TRIGGER_LEVEL in SCB_RX_FIFO_CTRL
  - Rx FIFO is full
  - Rx FIFO is not empty
  - Rx FIFO overflow
  - Rx FIFO underflow
- SPI Externally clocked
  - Wake up request on slave select
  - SPI STOP detection at the end of each transfer
  - SPI STOP detection at the end of a write transfer
  - SPI STOP detection at the end of a read transfer

25.6.2 UART Interrupts

The UART interrupts can be classified as Tx interrupts and Rx interrupts. Each interrupt output is the logical OR of the group of all possible interrupt sources classified under the section. For example, the Tx interrupt output is the logical OR of the group of all possible Tx interrupt sources. This signal goes high when any of the enabled Tx interrupt sources are true. The SCB also provides an interrupt cause register (SCB_INTR_CAUSE) that can be used to determine interrupt source. The interrupt registers are cleared by writing ‘1’ to the corresponding bitfield. Note that certain interrupt sources are triggered again as long as the condition is met even if the interrupt source was cleared. For example, the TX_FIFO_EMPTY is set as long as the transmit FIFO is empty even if the interrupt source is cleared. For more information on interrupt registers, see the PSoC 63 with BLE Registers TRM. The UART blocks generates interrupts on the following events:

- UART Tx
  - Tx FIFO has fewer entries than the value specified by TRIGGER_LEVEL in SCB_TX_FIFO_CTRL
  - Tx FIFO is not full
  - Tx FIFO is empty
  - Tx FIFO overflow
  - Tx FIFO underflow
  - Tx received a NACK in SmartCard mode

- UART Rx
  - Rx FIFO has more entries than the value specified by TRIGGER_LEVEL in SCB_RX_FIFO_CTRL
  - Rx FIFO is full
  - Rx FIFO is not empty
  - Rx FIFO overflow
  - Rx FIFO underflow
  - Frame error in received data frame
  - Parity error in received data frame
  - LIN baud rate detection is completed
  - LIN break detection is successful
25.6.3 \textit{i}^2\text{C} Interrupts

\textit{i}^2\text{C} interrupts can be classified as master interrupts, slave interrupts, Tx interrupts, Rx interrupts, and externally clocked (EC) mode interrupts. Each interrupt output is the logical OR of the group of all possible interrupt sources classified under the section. For example, the Tx interrupt output is the logical OR of the group of all possible Tx interrupt sources. This signal goes high when any of the enabled Tx interrupt sources are true. The SCB also provides an interrupt cause register (SCB\_INTR\_CAUSE) that can be used to determine interrupt source. The interrupt registers are cleared by writing ‘1’ to the corresponding bitfield. Note that certain interrupt sources are triggered again as long as the condition is met even if the interrupt source was cleared. For example, the TX\_FIFO\_EMPTY is set as long as the transmit FIFO is empty even if the interrupt source is cleared. For more information on interrupt registers, see the \textit{PSoc 63 with BLE Registers TRM}. The \textit{i}^2\text{C} block generates interrupts for the following conditions.

- \textit{i}^2\text{C} Master
  - \textit{i}^2\text{C} master lost arbitration
  - \textit{i}^2\text{C} master received NACK
  - \textit{i}^2\text{C} master received ACK
  - \textit{i}^2\text{C} master sent STOP
  - \textit{i}^2\text{C} bus error (unexpected stop/start condition detected)
- \textit{i}^2\text{C} Slave
  - \textit{i}^2\text{C} slave lost arbitration
  - \textit{i}^2\text{C} slave received NACK
  - \textit{i}^2\text{C} slave received ACK
  - \textit{i}^2\text{C} slave received STOP
  - \textit{i}^2\text{C} slave received START
  - \textit{i}^2\text{C} slave address matched
  - \textit{i}^2\text{C} bus error (unexpected STOP/START condition detected)
- \textit{i}^2\text{C} Tx
  - Tx FIFO has fewer entries than the value specified by TRIGGER\_LEVEL in SCB\_TX\_FIFO\_CTRL
  - Tx FIFO is not full
  - Tx FIFO is empty
  - Tx FIFO overflow
  - Tx FIFO underflow
- \textit{i}^2\text{C} Rx
  - Rx FIFO has more entries than the value specified by TRIGGER\_LEVEL in SCB\_RX\_FIFO\_CTRL
  - Rx FIFO is full
  - Rx FIFO is not empty
  - Rx FIFO overflow
  - Rx FIFO underflow
- \textit{i}^2\text{C} Externally Clocked
  - Wake up request on address match
  - \textit{i}^2\text{C} STOP detection at the end of each transfer
  - \textit{i}^2\text{C} STOP detection at the end of a write transfer
  - \textit{i}^2\text{C} STOP detection at the end of a read transfer
26. Serial Memory Interface (SMIF)

The SMIF block implements a single-SPI, dual-SPI, quad-SPI, or octal-SPI communication to interface with external memory chips. The SMIF block’s primary use case is to set up the external memory and have it mapped to the PSoC 6 MCU memory space using the hardware. This mode of operation, called the XIP mode, allows the bus masters in the PSoC 6 MCU to directly interact with the SMIF for memory access to an external memory location.

26.1 Features

The Serial Memory Interface (SMIF) block provides a master interface to serial memory devices that supports the following functionality.

- Interfacing up to four memory devices (slaves) at a time
- SPI protocol
  - SPI mode 0: clock polarity (CPOL) and clock phase (CPHA) are both ‘0’
  - Support for single, dual, quad, and octal SPI protocols
  - Support for dual-quad SPI mode: the use of two quad SPI memory devices to increase data bandwidth for SPI read and write transfers
  - Support for configurable MISO sampling time and programmable receiver clock
- Support for device capacities in the range of 64 KB to 128 MB
- A memory-mapped mode of operation, eXecute In Place (XIP), which enables mapping the external memory into an internal memory address
- A command mode (MMIO mode), which enables using the SMIF block as a simple communication hardware
- Supports a 4-KB read cache in memory mapped mode
- Supports on-the-fly 128-bit encryption and decryption

26.2 Architecture

Figure 26-1 shows a high-level block diagram of the SMIF hardware in PSoC 6 MCUs. Notice that the block is divided into multiple clock domains. This enables multiple domains to access the SMIF and still enable maintaining an asynchronous clock for the communication interface.

The SMIF block can also generate DMA triggers and interrupt signals. This allows events in the SMIF block to trigger actions in other parts of the system.

The SMIF interface is implemented using eight data lines, four slave select lines, and a clock line.

The access to the SMIF block can be by two modes: MMIO mode or XIP mode. The MMIO mode gives access to the SMIF’s peripheral registers and the internal FIFOs. This mode is used when the user code is responsible for constructing the command structure for the external memory. Typically, this mode is used when the SMIF writes to an external flash memory. The MMIO interface is also used to configure the SMIF hardware block, including configuring the device registers that set up the XIP operation of the SMIF block.

The XIP mode of operation maps the external memory space to a range of addresses in the PSoC 6 MCU’s address space. Refer to the PSoC 63 with BLE Registers TRM for details. When this address range is accessed, the hardware automatically generates the commands required to initiate the associated transfer from the external memory. The typical use case for the XIP mode is to execute code placed in external memory. Here, the memory will be mapped into the internal address space of
the PSoC 6 MCU using the XIP mode. Thus code is execution from external memory is seamless.

The SMIF block has three AHB-Lite interfaces:
- An AHB-Lite interface to access the SMIF’s MMIO registers.
- Two AHB-Lite interfaces to support execute-in-place (XIP).

All interfaces provide access to external memory devices. At any time, either the MMIO AHB-Lite interface or the two XIP AHB-Lite interfaces have access to the memory interface logic and external memory devices. The operation mode is specified by CTL.XIP_MODE. The operation mode should not be modified when the SMIF is busy (STATUS.BUSY is ‘1’).

In the MMIO AHB-Lite interface, access is supported through software writes to transmit (Tx) FIFOs and software
reads from receive (Rx) FIFOs. The FIFOs are mapped on SMIF registers. This interface provides the flexibility to implement any memory device transfer. For example, memory device transfers to setup, program, or erase the external memory devices.

In an XIP AHB-Lite interface, access is supported through XIP: AHB-Lite read and write transfers are automatically (by the hardware) translated in memory device read and write transfers. This interface provides efficient implementation of memory device read and write transfers, but does NOT support other types of memory device transfers. To improve XIP performance, the XIP AHB-Lite interface has a 4-KB read cache.

As mentioned, MMIO mode and XIP mode are mutually exclusive. The operation modes share Tx and Rx FIFOs and memory interface logic. In MMIO mode, the Tx and Rx FIFOs are accessed through the SMIF registers and under software control. In XIP mode, the Tx and Rx FIFOs are under hardware control. The memory interface logic is controlled through the Tx and Rx FIFOs and is agnostic of the operation mode.

26.2.1 Tx and Rx FIFOs

The SMIF block has two Tx FIFOs and one Rx FIFO. These FIFOs provide an asynchronous clock domain transfer between clk_hf logic and clk_if_tx/clk_if_rx memory interface logic. The memory interface logic is completely controlled through the Tx and Rx FIFOs.

- The Tx command FIFO transmits memory commands to the memory interface logic.
- The Tx data FIFO transmits write data to the memory interface transmit logic.
- The Rx data FIFO receives read data from the memory interface receive logic.

26.2.1.1 Tx Command FIFO

The Tx command FIFO consists of four 20-bit entries. Each entry holds a command. A memory transfer consists of a series of commands. In other words, a command specifies a phase of a memory transfer. Four different types of commands are supported:

- Tx command. A memory transfer must start with a Tx command. The Tx command includes a byte that is to be transmitted over the memory interface. The Tx command specifies the width of the data transfer (single, dual, quad, or octal data transfer). The Tx command specifies whether the command is for the last phase of the memory transfer (explicit “last command” indication).
- DUMMY_COUNT command. The DUMMY_COUNT command specifies a number of dummy cycles. Dummy cycles are used to implement a turn-around (TAR) time in which the memory master changes from a transmitter driving the data lines to a receiver receiving on the same data lines. The DUMMY_COUNT command never constitutes the last phase of the memory transfer (implicit NOT “last command” indication - de-asserts the slave select); that is, it must be followed by another command. Note that the DUMMY_COUNT command does not assert the slave select lines. This must be done by a Tx command preceding it.
- RX_COUNT command. The RX_COUNT command specifies the number of bytes to be received from the Rx data FIFO. This command relies on the Rx data FIFO to accept the bytes that are received over the memory interface. The RX_COUNT command does not assert the slave select lines. This must be done by a Tx command preceding it.
- TX_COUNT command. The TX_COUNT command specifies the number of bytes to be transmitted from the Tx data FIFO. This command relies on the Tx data FIFO to provide the bytes that are to be transmitted over the memory interface.

Together, the four command types can be used to construct any SPI transfer. The Tx command FIFO is used by both the memory interface transmit and receive logic. This ensures lockstep operation. The Tx command is a representation of a queue of commands that are to be processed.

The software will write the sequence of commands into the Tx command FIFO to generate a sequence responsible for the communication with slave device. The software can read the number of used Tx command FIFO entries through the TX_CMD_FIFO_STATUS.USED[2:0] register field.

The software can write to the Tx command FIFO through the MMIO TX_CMD_FIFO_WR register. If software attempts to write to a full Tx command FIFO, the MMIO CTL.BLOCK field specifies the behavior:

- If CTL.BLOCK is ‘0’, an AHB-Lite bus error is generated.
- If CTL.BLOCK is ‘1’, the AHB-Lite write transfer is extended until an entry is available. This increases latency.
26.2.1.2 Tx Data FIFO

The Tx data FIFO consists of eight 8-bit entries. A Tx command FIFO TX_COUNT command specifies the number of bytes to be transmitted; that is, specifies the number of Tx data FIFO entries used. The Tx data FIFO is used by the memory interface transmit logic.

Software can read the number of used Tx data FIFO entries through the TX_DATA_FIFO_STATUS.USED[3:0] register field.

Software can write to the Tx data FIFO through the TX_DATA_FIFO_WR1, TX_DATA_FIFO_WR2, and TX_DATA_FIFO_WR4 registers:

- The TX_DATA_FIFO_WR1 register supports a write of a single byte to the FIFO.
- The TX_DATA_FIFO_WR2 register supports a write of two bytes to the FIFO.
- The TX_DATA_FIFO_WR4 register supports a write of four bytes to the FIFO. If software attempts to write more bytes than available entries in the Tx data FIFO, the MMIO CTL.BLOCK field specifies the behavior:
  - If CTL.BLOCK is '0', an AHB-Lite bus error is generated.
  - If CTL.BLOCK is '1', the AHB-Lite write transfer is extended until the required entries are available.

26.2.2 MMIO Mode

If CTL.XIP_MODE is '0', the SMIF is in MMIO mode. Software generates SPI transfers by accessing the Tx FIFOs and Rx FIFO. The Tx command FIFO has formatted commands (Tx, TX_COUNT, RX_COUNT, and DUMMY_COUNT) that are described in the PSoC 63 with BLE Registers TRM.

Software should ensure that it generates correct memory transfers and accesses the FIFOs correctly. For example, if a memory transfer is generated to read four bytes from a memory device, software should read the four bytes from the Rx data FIFO. Similarly, if a memory transfer is generated to write four bytes to a memory device, software should write the four bytes to the Tx command FIFO or Tx data FIFO.

Incorrect software behavior can lock up the memory interface. For example, a memory transfer to read 32 bytes from a memory device, without software reading the Rx data FIFO will lock up the memory transfer as the memory interface cannot provide more than eight bytes to the Rx data FIFO (the Rx data FIFO has eight entries). This will prevent any successive memory transfers from taking place. Hence, the software should make sure that it read the FIFOs to avoid congestion. Note that a locked up memory transfer due to Tx or Rx FIFO states is still compliant to the memory bus protocol (but undesirable): the SPI protocol allows shutting down the interface clock in the middle of a memory transfer.

26.2.3 XIP Mode

If CTL.XIP_MODE is '1', the SMIF is in XIP mode. Hardware automatically (without software intervention) generates memory transfers by accessing the Tx FIFOs and Rx FIFO. Hardware supports only memory read and write transfers. Other functionality such as status reads are not supported. This means operations such as writing into a flash device may not be supported by XIP mode. This is because the writing operation into a flash memory involves not only a write command transfer, but also a status check to verify the status of the operation.

- Hardware generates a memory read transfer for an AHB-Lite read transfer (to be precise: only for AHB-Lite read transfers that miss in the cache).
- Hardware generates a memory write transfer for an AHB-Lite write transfer.

Each slave device slot has a set of associated device configuration registers. To access a memory device in XIP mode, the corresponding device configuration registers should be initialized. The device configuration register sets up the following parameters for memory:

- Write enable: Used to disable writes in XIP mode.
Four-way set associative, with a least recently used (LRU) replacement scheme.

The cache is defined as follows:

- **4 KB capacity.**
- **Read-only cache.** Write transfers bypass the cache. A write to an address, which is prefetched in the cache, invalidates the associated cache subsector. If there is a write to a memory in MMIO mode then you must invalidate the cache while switching back to XIP mode.
- **Four-way set associative, with a least recently used (LRU) replacement scheme.**

Each XIP interface implements a 4-KB cache memory. Any XIP access can be cached if a cache is enabled. There are separate cache registers for the slow cache (in the clk_slow domain) and fast cache (in the clk_fast domain). The cache can be enabled using the SLOW_CA_CTL[ENABLED] or FAST_CA_CTL[ENABLED] registers. Read transfers that “hit” are processed by the cache. Read transfers that “miss” result in a XIP memory read transfer.

If CA_CTL.PREF_EN is ‘1’, prefetching is enabled and if CA_CTL.PREF_EN is ‘0’, prefetching is disabled. If prefetch is enabled, a cache miss results in a 16 B (subsector) refill for the missing data AND a 16 B prefetch for the next sequential data (independent of whether this data is already in the cache or not).

Cache coherency is not supported by the hardware. For example, an XIP interface 0 write to an address in the XIP interface 0 cache invalidates (clears) the associated cache subsector in the XIP interface 0 cache, but not in the XIP interface 1 cache. This means XIP interface 1 cache now has outdated data. The user code can manually invalidate cache by using the SLOW_CA_CMD[INV] or FAST_CA_CMD[INV] register.

### 26.2.4 Cache

To improve XIP performance, the XIP AHB-Lite interface has a cache. The cache is defined as follows:

- **4 KB capacity.**
- **Read-only cache.** Write transfers bypass the cache. A write to an address, which is prefetched in the cache, invalidates the associated cache subsector. If there is a write to a memory in MMIO mode then you must invalidate the cache while switching back to XIP mode.
- **Four-way set associative, with a least recently used (LRU) replacement scheme.**

Each XIP interface implements a 4-KB cache memory. Any XIP access can be cached if a cache is enabled. There are separate cache registers for the slow cache (in the clk_slow domain) and fast cache (in the clk_fast domain). The cache can be enabled using the SLOW_CA_CTL[ENABLED] or FAST_CA_CTL[ENABLED] registers. Read transfers that “hit” are processed by the cache. Read transfers that “miss” result in a XIP memory read transfer.

If CA_CTL.PREF_EN is ‘1’, prefetching is enabled and if CA_CTL.PREF_EN is ‘0’, prefetching is disabled. If prefetch is enabled, a cache miss results in a 16 B (subsector) refill for the missing data AND a 16 B prefetch for the next sequential data (independent of whether this data is already in the cache or not).

Cache coherency is not supported by the hardware. For example, an XIP interface 0 write to an address in the XIP interface 0 cache invalidates (clears) the associated cache subsector in the XIP interface 0 cache, but not in the XIP interface 1 cache. This means XIP interface 1 cache now has outdated data. The user code can manually invalidate cache by using the SLOW_CA_CMD[INV] or FAST_CA_CMD[INV] register.
hardware, by applying AES-128 with KEY[127:0] on a plaintext PT[127:0], we get a ciphertext CT[127:0].

In XIP mode, the XIP address is used as the plaintext PT[]. The resulting ciphertext CT[] is used on-the-fly and not software accessible. The XIP address is extended with the CRYPTO_INPUT3, ..., CRYPTO_INPUT0 registers.

In MMIO mode, the MMIO CRYPTO_INPUT3, ..., CRYPTO_INPUT0 registers provide the plaintext PT[]. The resulting ciphertext CT[] is provided through the MMIO CRYPTO_OUTPUT3, ..., CRYPTO_OUTPUT0 registers.

Figure 26-2 illustrates the functionality in XIP and MMIO modes.

In XIP mode, the resulting ciphertext CT[] (of the encrypted address) is XOR'd with the memory transfer’s read data or write data. Note that the AES-128 block cipher is on the address of the data and not on the data itself. For memory read transfers, this means that as long as the latency of the memory transfer’s read data is longer than the AES-128 block cipher latency, the on-the-fly decryption does not add any delay. Figure 26-3 illustrates the complete XIP mode functionality.

The XIP mode only encrypts the address and XORs with the data; to implement the same in MMIO, you must provide the address as the PT[] into the crypto_INPUTx registers.

Figure 26-3. XIP Mode Functionality
26.3 Memory Device Signal Interface

The SMIF acts as a master for SPI applications. SPI requires the definition of clock polarity and phase. In SPI mode, the SMIF supports a single clock polarity and phase configuration:

- Clock polarity (CPOL) is '0': the base value of the clock is 0.
- Clock phase (CPHA) is '0': driving of data is on the falling edge of the clock; capturing of data is specified by CTL.CLOCK_IF_RX_SEL.

The above configuration is also known as SPI configuration 0 and is supported by SPI memory devices.

26.3.1 Specifying Memory Devices

The SMIF requires that the memory devices are defined for their operation in XIP mode. The SMIF supports up to four memory devices. Each memory device is defined by a set of registers. The memory device specific register structure includes:

- The device base address and capacity. The ADDR register specifies the memory device’s base address in the PSoC 6 MCU address space and the MASK register specifies the memory device's size/capacity. If a memory device is not present or is disabled, the ADDR and MASK registers specify a memory device with 0 B capacity. Typically, the devices’ address regions in the PSoC 6 MCU address space are non-overlapping (except for dual-quad SPI mode) to ensure that the activation of select signals is mutually exclusive.

- The device data signal connections (as described in Connecting SPI Memory Devices on page 263).

- The definition of a read transfer to support XIP mode.

- The definition of a write transfer to support XIP mode.

Each memory device uses a dedicated device select signal: memory device 0 uses select[0], memory device 1 uses select[1], and so on. In other words, there is a fixed, one-to-one connection between memory device, register set, and select signal connection.

In XIP mode, the XIP AHB-Lite bus transfer address is compared with the device region. If the address is within the device region, the device select signal is activated. If an XIP AHB-Lite bus transfer address is within multiple regions (this is possible if the device regions overlap), all associated device select signals are activated. This overlap enables XIP in dual-quad SPI mode: the command, address, and mode bytes can be driven to two quad SPI devices simultaneously.

In XIP mode, dual quad SPI mode requires the ADDR_CTL.DIV2 field of the selected memory devices to be set to ‘1’. When this field is ‘1’, the transfer address is divided by 2 and the divided by 2 address is provided to the memory devices.

In dual quad SPI mode, each memory device contributes a 4-bit nibble for each 8-bit byte. However, both memory devices are quad SPI memories with a byte interface. Therefore, the transfer size must be a multiple of 2.

The XIP_ALIGMENT_ERROR interrupt cause is set under the following conditions (in XIP mode and when ADDR_CTL.DIV2 is ‘1’):

- The transfer address is not a multiple of 2. In this case the divided by 2 address for the memory devices is incorrect.
- The transfer size is not a multiple of 2. In this case, the memory devices contribute only a nibble of a byte. This is not supported as the memory devices have a byte interface.

26.3.2 Connecting SPI Memory Devices

Memory device I/O signals (SCK, S, SI/IO0, SO/IO1, IO2, IO3, IO4, IO5, IO6, IO7) are connected to the SMIF I/O signals (clk, select[3:0], and spi_data[7:0]). Not all memory devices provide the same number of I/O signals.

<table>
<thead>
<tr>
<th>Memory Device</th>
<th>IO Signals</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single SPI memory</td>
<td>SCK, S, SI, SO. This memory device has two data signals (SI and SO).</td>
</tr>
<tr>
<td>Dual SPI memory</td>
<td>SCK, S, IO0, IO1. This memory device has two data signals (IO0, IO1).</td>
</tr>
<tr>
<td>Quad SPI memory</td>
<td>SCK, S, IO0, IO1, IO2, IO3. This memory device has four data signals (IO0, IO1, IO2, IO3).</td>
</tr>
<tr>
<td>Octal SPI memory</td>
<td>SCK, S, IO0, IO1, IO2, IO3, IO4, IO5, IO6, IO7. This memory device has eight data signals (IO0, IO1, IO2, IO3, IO4, IO5, IO6, IO7).</td>
</tr>
</tbody>
</table>

Table 26-1 illustrates that each memory has a single clock signal SCK, a single (low active) select signal (S), and multiple data signals (IO0, IO1, ...).

Each memory device has a fixed select signal connection (to select[3:0]).
Each memory device has programmable data signal connections (to data[7:0]): the CTL.DATA_SEL[1:0] field specifies how a device’s data signals are connected. The CTL.DATA_SEL[1:0] is responsible for configuring the selection of data lines to be used by a slave. This is not to be confused with the select lines that are used for addressing the four slaves of the SMIF master. This information is used by the SMIF interface to drive out data on the correct spi_data[] outputs and capture data from the correct spi_data[] inputs. If multiple device select signals are activated, the same data is driven to all selected devices simultaneously.

Not all data signal connections are legal/supported. Supported connections are dependent on the type of memory device.

<table>
<thead>
<tr>
<th>DATA_SEL[1:0]</th>
<th>Single SPI Device</th>
<th>Dual SPI Device</th>
<th>Quad SPI Device</th>
<th>Octal SPI Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>spi_data[0] = SI</td>
<td>spi_data[0] = IO0</td>
<td>spi_data[0] = IO0</td>
<td>spi_data[0] = IO0</td>
</tr>
</tbody>
</table>

Memory devices can:
- Use shared data signal connections.
- Use dedicated data signal connections. This reduces the load on the data lines allowing faster signal level changes, which in turn allows for a faster I/O interface.

Note that dual-quad SPI mode requires dedicated data signals to enable read and/or write data transfer from and to two quad SPI devices simultaneously.

Figure 26-4 illustrates memory device 0, which is a single SPI memory with data signals connections to spi_data[1:0].

Figure 26-4. Single SPI Memory Device 0 Connected to spi_data[1:0]
Because of the pin layout, you might want to connect a memory device to specific data lines. Figure 26-5 illustrates memory device 0, which is a single SPI memory with data signals connections to spi_data[7:6].

**Figure 26-5. Single SPI Memory Device 0 Connected to spi_data[7:6]**

![Diagram of SPI Memory Device 0](image)

Figure 26-6 illustrates memory devices 0 and 1, both of which are single SPI memories. Each device uses dedicated data signal connections. The device address regions in the PSoC 6 MCU address space must be non-overlapping to ensure that the activation of select[0] and select[1] are mutually exclusive.

**Figure 26-6. Single SPI Memory Devices 0 and 1 - Dedicated Data Signal**

![Diagram of SPI Memory Devices 0 and 1](image)

Figure 26-7 illustrates memory devices 0 and 1, both of which are single SPI memories. Both devices use shared data signal connections. The devices’ address regions in the PSoC 6 MCU address space must be non-overlapping to ensure that the activation of select[0] and select[1] are mutually exclusive. Note that this solution increases the load on the data lines, which may result in a slower I/O interface.

**Figure 26-7. Single SPI Memory Devices 0 and 1 - Shared Data Signal**

![Diagram of SPI Memory Devices 0 and 1](image)
Figure 26-7. Single SPI Memory Devices 0 and 1 - Shared Data Signal

Figure 26-8 illustrates memory device 0, which is a quad SPI memory with data signals connections to spi_data[7:4].

Figure 26-9 illustrates memory devices 0 and 1, device 0 is a single SPI memory and device 1 is a quad SPI memory. Each device uses dedicated data signal connections. The device address regions in the PSoC 6 MCU address space must be non-overlapping to ensure that the activation of select[0] and select[1] are mutually exclusive.
Figure 26-9. Single SPI Memory 0 and Quad SPI Memory 1 - Dedicated Data Signal

Figure 26-9 illustrates memory devices 0 and 1, device 0 is a single SPI memory and device 1 is a quad SPI memory. Both devices use shared data signal connections. The device address regions in the PSoC 6 MCU address space must be non-overlapping to ensure that the activation of select[0] and select[1] are mutually exclusive.

Figure 26-10. Single SPI Memory Device 0 and Quad SPI Memory Device 1 - Shared Data Signal

Figure 26-10 illustrates memory devices 0 and 1, device 0 is a single SPI memory and device 1 is a quad SPI memory. Both devices use shared data signal connections. The device address regions in the PSoC 6 MCU address space must be non-overlapping to ensure that the activation of select[0] and select[1] are mutually exclusive.

Figure 26-11. Single SPI Memory Device 0 and Quad SPI Memory Device 1 - Shared Data Signal

Figure 26-11 illustrates memory devices 0 and 1, both of which are quad SPI memories. Each device uses dedicated data signal connections. The device address regions in the PSoC 6 MCU address space are the same to ensure that the activation of select[0] and select[1] are the same (in XIP mode). This is known as a dual-quad configuration: during SPI read and write transfers, each device provides a nibble of a byte.
26.3.3 SPI Data Transfer

SPI data transfer uses most-significant-bit (MSb) for the first data transfer. This means that for a byte B, consisting of bits b7, b6, ..., b0, bit b7 is transferred first, followed by bit b6, and so on. For dual, quad, dual quad, and octal SPI transfers, multiple bits are transferred per cycle. For a single SPI device and device data signal connections to spi_data[1:0] (DATA_SEL is "0"), Table 26-3 summarizes the transfer of byte B.
Serial Memory Interface (SMIF)

Table 26-3. Single Data Transfer

<table>
<thead>
<tr>
<th>Cycle</th>
<th>Data Transfer</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>For a write transfer: b7 is transferred on data[0] and SI/IO0. For a read transfer: b7 is transferred on data[1] and SO/IO1.</td>
</tr>
<tr>
<td>1</td>
<td>For a write transfer: b6 is transferred on data[0] and SI/IO0. For a read transfer: b6 is transferred on data[1] and SO/IO1.</td>
</tr>
<tr>
<td>2</td>
<td>For a write transfer: b5 is transferred on data[0] and SI/IO0. For a read transfer: b5 is transferred on data[1] and SO/IO1.</td>
</tr>
<tr>
<td>3</td>
<td>For a write transfer: b4 is transferred on data[0] and SI/IO0. For a read transfer: b4 is transferred on data[1] and SO/IO1.</td>
</tr>
<tr>
<td>4</td>
<td>For a write transfer: b3 is transferred on data[0] and SI/IO0. For a read transfer: b3 is transferred on data[1] and SO/IO1.</td>
</tr>
<tr>
<td>5</td>
<td>For a write transfer: b2 is transferred on data[0] and SI/IO0. For a read transfer: b2 is transferred on data[1] and SO/IO1.</td>
</tr>
<tr>
<td>6</td>
<td>For a write transfer: b1 is transferred on data[0] and SI/IO0. For a read transfer: b1 is transferred on data[1] and SO/IO1.</td>
</tr>
<tr>
<td>7</td>
<td>For a write transfer: b0 is transferred on data[0] and SI/IO0. For a read transfer: b0 is transferred on data[1] and SO/IO1.</td>
</tr>
</tbody>
</table>

Note that in single SPI data transfer, the data signals are uni-directional: in the table, data[0] is exclusively used for write data connected to the device SI input signal and data[1] is exclusively used for read data connected to the device SO output signal.

For a dual SPI device and device data signal connections to data[1:0] (DATA_SEL is “0”), Table 26-4 summarizes the transfer of byte B.

Table 26-4. Dual Data Transfer

<table>
<thead>
<tr>
<th>Cycle</th>
<th>Data Transfer</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>b7, b6 are transferred on data[1:0] and IO1, IO0.</td>
</tr>
<tr>
<td>1</td>
<td>b5, b4 are transferred on data[1:0] and IO1, IO0.</td>
</tr>
<tr>
<td>2</td>
<td>b3, b2 are transferred on data[1:0] and IO1, IO0.</td>
</tr>
<tr>
<td>3</td>
<td>b1, b0 are transferred on data[1:0] and IO1, IO0.</td>
</tr>
</tbody>
</table>

For a quad SPI device and device data signal connections to data[3:0] (DATA_SEL is “0”), Table 26-5 summarizes the transfer of byte B.

Table 26-5. Quad Data Transfer

<table>
<thead>
<tr>
<th>Cycle</th>
<th>Data Transfer</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>b7, b6, b5, b4 are transferred on data[3:0] and IO3, IO2, IO1, IO0.</td>
</tr>
<tr>
<td>1</td>
<td>b3, b2, b1, b0 are transferred on data[3:0] and IO3, IO2, IO1, IO0.</td>
</tr>
</tbody>
</table>

For a octal SPI device and device data signal connections to data[7:0] (DATA_SEL is “0”), Table 26-6 summarizes the transfer of byte B.

Table 26-6. Octal Data Transfer

<table>
<thead>
<tr>
<th>Cycle</th>
<th>Data Transfer</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>b7, b6, b5, b4, b3, b2, b1, b0 are transferred on data[7:0] and IO7, IO6, IO5, IO4, IO3, IO2, IO1, IO0.</td>
</tr>
</tbody>
</table>
In dual-quad SPI mode, two quad SPI devices are used.

- The first device (the device with the lower device structure index) should have device data signal connections to data[3:0] (DATA_SEL is 0).
- The second device (the device with the higher device structure index) should have device data signal connection to data[7:4] (DATA_SEL is 2).

The command and data phases of the SPI transfer use different width data transfers:

- The command, address, and mode bytes use quad SPI data transfer.
- The read data and write data use octal data transfer. Each device provides a nibble of each data byte: the first device provides the lower nibble and the second device provides the higher nibble.

Table 26-7 summarizes the transfer of a read data and write data byte B.

Table 26-7. Dual-quad SPI Mode, Octal Data Transfer

<table>
<thead>
<tr>
<th>Cycle</th>
<th>Data transfer</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>b7, b6, b5, b4 are transferred on data[7:4] and second device IO3, IO2, IO1, IO0. b3, b2, b1, b0 are transferred on data[3:0] and first device IO3, IO2, IO1, IO0.</td>
</tr>
</tbody>
</table>

26.3.4 Example of Setting up SMIF

Devices 0 and 1 are used to implement the dual-quad SPI mode. Both devices are 1 MB / 8 Mb; the address requires 3 bytes. Device 0 has device data signal connections to data[3:0] and device 1 has device data signal connections to data[7:4].

Figure 26-13. Setting up SMIF

For dual quad SPI mode, the AHB-Lite bus transfer address is divided by two. Cryptography and write functionality are disabled in the following example.

```c
#define MASK_1MB 0xfff00000;
DEV0_ADDR  = CPUSS_SMIF_BASE;
DEV0_MASK  = MASK_1MB    // MASK: 1 MB region
DEV0_CTL   = (0 << SMIF_DEVICE_CTL_DATA_SEL_Pos)     // DATA_SEL: data[3:0]
            | (0 << SMIF_DEVICE_CTL_CRYPTO_EN_Pos)       // CRYPTO_EN
            | (0 << SMIF_DEVICE_CTL_WR_EN_Pos));       // WR_EN
DEV_ADDR_CTL = (1 << SMIF_DEVICE_ADDR_CTL_DIV2_Pos)   // DIV2: enabled
            | ((3-1) << SMIF_DEVICE_ADDR_CTL_SIZE2_Pos)); // SIZE: 3 B address
```
For XIP read transfers, the 0xEB command/instruction is used (Figure 26-14 illustrates a two-byte transfer from devices 0 and 1 in dual quad SPI mode).

**Figure 26-14. Two-Byte Transfer in Dual Quad SPI Mode**

<table>
<thead>
<tr>
<th>0xEB instruction, instruction 1 bit/cycle; address, mode, data 4 bits/cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td>spi_select[0]</td>
</tr>
<tr>
<td>spi_select[1]</td>
</tr>
<tr>
<td>spi_clk</td>
</tr>
<tr>
<td>instruction (0xeb)</td>
</tr>
<tr>
<td>24 bit address</td>
</tr>
<tr>
<td>mode</td>
</tr>
<tr>
<td>4 dummy cycles</td>
</tr>
<tr>
<td>8-bit data</td>
</tr>
<tr>
<td>spi_data[0]</td>
</tr>
<tr>
<td>spi_data[1]</td>
</tr>
<tr>
<td>spi_data[2]</td>
</tr>
<tr>
<td>spi_data[3]</td>
</tr>
<tr>
<td>spi_data[4]</td>
</tr>
<tr>
<td>spi_data[5]</td>
</tr>
<tr>
<td>spi_data[6]</td>
</tr>
<tr>
<td>spi_data[7]</td>
</tr>
<tr>
<td>single</td>
</tr>
<tr>
<td>quad</td>
</tr>
<tr>
<td>octal</td>
</tr>
</tbody>
</table>

The definition of a read transfer is as follows:

```c
DEV0_RD_CMD_CTL = (1UL << SMIF_DEVICE_RD_CMD_CTL_PRESENT_Pos) // PRESENT
| (0 << SMIF_DEVICE_RD_CMD_CTL_WIDTH_Pos) // WIDTH: single data transfer
| 0xeb);                                   // CODE

DEV0_RD_ADDR_CTL = (2 << SMIF_DEVICE_RD_ADDR_CTL_WIDTH_Pos)); // WIDTH: quad data transfer

DEV0_RD_MODE_CTL = (1UL << SMIF_DEVICE_RD_MODE_CTL_PRESENT_Pos) // PRESENT
| (2 << SMIF_DEVICE_RD_MODE_CTL_WIDTH_Pos) // WIDTH: quad data transfer
| 0x00);                                   // CODE

DEV0_RD_DUMMY_CTL= (1UL << SMIF_DEVICE_RD_DUMMY_CTL_PRESENT_Pos) // PRESENT
| ((4-1) << SMIF_DEVICE_RD_DUMMY_CTL_SIZE5_Pos)); // SIZE: 4 dummy cycles

DEV0_RD_DATA_CTL = (3 << SMIF_DEVICE_RD_DATA_CTL_WIDTH_Pos)); // WIDTH: octal data transfer
```

Note that the command uses single data transfer, the address and mode byte use quad data transfer, and the read data byte uses octal data transfer.
26.4 Triggers

The SMIF has two level-sensitive triggers:
- tr_tx_req is associated with the Tx data FIFO.
- tr_rx_req is associated with the Rx data FIFO.

If the SMIF is enabled (CTL.ENABLED is ‘1’) and MMIO operation mode is selected (CTL.XIP_MODE is ‘0’), the trigger functionality is enabled. If the SMIF is disabled (CTL.ENABLED is ‘0’) or the XIP operation mode is selected (CTL.XIP_MODE is ‘1’), the triggers functionality is disabled. The trigger functionality is defined as follows:

- The MMIO TX_DATA_FIFO_CTL.TRIGGER_LEVEL field specifies a number of FIFO entries. The tr_tx_req trigger is active when the number of used Tx data FIFO entries is smaller or equal than the specified number; that is, TX_DATA_FIFO_STATUS.USED ≤ TRIGGER_LEVEL.

- The MMIO RX_DATA_FIFO_CTL.TRIGGER_LEVEL field specifies a number of FIFO entries. The tr_rx_req trigger is active when the number of used Rx data FIFO entries is greater than the specified number; that is, RX_DATA_FIFO_STATUS.USED > TRIGGER_LEVEL.

26.5 Interrupts

The SMIF has a single interrupt output with six interrupt causes:

- INTR.TR_TX_REQ. This interrupt cause is activated in MMIO mode when the tr_tx_req trigger is activated.
- INTR.TR_RX_REQ. This interrupt cause is activated in MMIO mode when the tr_rx_req trigger is activated.
- INTR.XIP_ALIGNMENT_ERROR. This interrupt cause is activated in XIP mode when the selected device’s ADDR_CTL.DIV2 field is ‘1’ and the AHB-Lite bus address is not a multiple of 2, or the requested transfer size is not a multiple of 2. This interrupt cause identifies erroneous behavior in dual-quad SPI mode (the selected device ADDR_CTL.DIV2 field is set to ‘1’).
- INTR.TX_CMD_FIFO_OVERFLOW. This interrupt cause is activated in MMIO mode, on an AHB-Lite write transfer to the Tx command FIFO (TX_CMD_FIFO_WR) with insufficient free entries.
- INTR.TX_DATA_FIFO_OVERFLOW. This interrupt cause is activated in MMIO mode, on an AHB-Lite write transfer to the Tx data FIFO (TX_DATA_FIFO_WR1, TX_DATA_FIFO_WR2, and TX_DATA_FIFO_WR4) with insufficient free entries.
- INTR.RX_DATA_FIFO_OVERFLOW. This interrupt cause is activated in MMIO mode, on an AHB-Lite read transfer from the Rx data FIFO (RX_DATA_FIFO_RD1, RX_DATA_FIFO_RD2, and RX_DATA_FIFO_RD4) with insufficient free entries.
27. Timer, Counter, and PWM

The Timer, Counter, and Pulse Width Modulator (TCPWM) block in the PSoC 6 MCU implements a 16- or 32-bit timer, counter, pulse width modulator (PWM), or quadrature decoder functionality. The block can be used to measure the period and pulse width of an input signal (timer), find the number of times a particular event occurs (counter), generate PWM signals, or decode quadrature signals. This chapter explains the features, implementation, and operational modes of the TCPWM block.

27.1 Features

- The TCPWM block supports the following operational modes:
  - Timer-counter with compare
  - Timer-counter with capture
  - Quadrature decoding
  - Pulse width modulation
  - Pseudo-random PWM
  - PWM with dead time
- Up, Down, and Up/Down counting modes.
- Clock prescaling (division by 1, 2, 4, ... 64, 128)
- Double buffering of compare/capture and period values
- Underflow, overflow, and capture/compare output signals
- Supports interrupt on:
  - Terminal count – Depends on the mode; typically occurs on overflow or underflow
  - Capture/compare – The count is captured to the capture register or the counter value equals the value in the compare register
- Complementary output for PWMs
- Selectable start, reload, stop, count, and capture event signals for each TCPWM with rising edge, falling edge, both edges, and level trigger options
27.2 Architecture

Figure 27-1. TCPWM Block Diagram

In the PSoC 6 MCU, there are two blocks of TCPWMs. Block 0 has eight 32-bit counters. Block 1 has 24 16-bit counters. In this chapter, a TCPWM refers to the entire block and all the counters inside. A counter refers to the individual counter inside the TCPWM. TCPWM has these interfaces:

- **Bus interface**: Connects the counter to the CPU subsystem.
- **I/O signal interface**: Consists of input triggers (such as reload, start, stop, count, and capture) and output signals (such as pwm, pwm_n, overflow (OV), underflow (UN), and capture/compare (CC)).
- **Interrupts**: Provides interrupt request signals from each counter, based on TC or CC conditions.
- **System interface**: Consists of control signals such as clock and reset from the system resources subsystem.

This TCPWM block can be configured by writing to the TCPWM registers. See “TCPWM Registers” on page 306 for more information on all registers required for this block.

27.2.1 Enabling and Disabling Counters in TCPWM Block

A counter can be enabled by setting the corresponding bit of the TCPWM_CTRL_SET register. It can be disabled by setting the bit in the TCPWM_CTRL_CLR register. These registers are used to avoid race-conditions on read-modify-write attempts to the TCPWM_CTRL register, which controls the enable/disable fields of the counters.

**Note**: The counter must be configured before enabling it. Disabling the counter retains the values in the registers.

27.2.2 Clocking

Each TCPWM counter can have its own clock source. The only source for the clock is from the configurable peripheral clock dividers generated by the clocking system; see the Clocking System chapter on page 146 for details. To select a clock divider for a particular counter inside a TCPWM, use the CLOCK_CTL register from the PERI register space. In this section the clock to the counter will be called clk_counter. Event generation is performed on the clk_counter. Another clock, clk_sys is used for the pulse width of the output triggers. clk_sys is synchronous to PERI clock, clk_peri (see “CLK_PERI” on page 157), but can be divided using CLOCK_CTL from the PERI_GROUP_STRUCT register space.

27.2.2.1 Clock Prescaling

clk_counter can be further divided inside each counter, with values of 1, 2, 4, 8...64, 128. This division is called prescaling. The prescaling is set in the GENERIC field of the TCPWM_CNT_CNTL register.

**Note**: Clock prescaling is not available in quadrature mode and pulse width modulation mode with dead time.

27.2.2.2 Count Event

The counter functionality is performed on an “active count” prescaled clock, which is gated by a “count event” signal. For example, a counter increments or decrements by ‘1’ every counter clock cycle in which a count event is detected.

**Note**: Count events are not supported in quadrature and pulse-width modulation pseudo-random modes; the clk_counter is used in these cases instead of the active count prescaled clock.
27.2.3 Trigger Inputs

Each TCPWM block has 14 Trigger_In signals, which come from other on-chip resources such as other TCPWMs, SCBs, and DMA. The Trigger_In signals are shared with all counters inside of one TCPWM block. Use the Trigger Mux registers to configure which signals get routed to the Trigger_In for each TCPWM block. See the Trigger Multiplexer Block chapter on page 197 for more details. Two constant trigger inputs ‘0’ are ‘1’ are available in addition to the 14 Trigger_In. The trigger input source is selected using the TCPWM_CNT_TR_CTRL0 register.

Each counter can select any of the 16 trigger signals to be the source for any of the following events:

■ Reload
■ Start
■ Stop/Kill
■ Count
■ Capture/swap

Note: TCPWM_CMD_RELOAD, TCPWM_CMD_STOP, TCPWM_CMD_START, and TCPWM_CMD_CAPTURE can be used to trigger the reload, stop, start, and capture respectively from software.

The sections describing each TCPWM mode will describe the function of each input event in detail.

Typical operation uses the reload event once to initialize and start the counter and the stop event to stop the counter.

When the counter is stopped, the start event can be used to start the counter with its counter value unmodified from when it was stopped.

If stop, reload, and start events coincide, the following precedence relationship holds:

■ A stop event has higher priority than a reload event.
■ A reload event has higher priority that a start event.

As a result, when a reload or start event coincides with a stop event, the reload or start event has no effect.

Before going to the counter each Trigger_IN can pass through a positive edge detector, negative edge detector, both edge detector, or pass straight through to the counter. This is controlled using TCPWM_CNT_TR_CTRL1. In the quadrature mode, edge detection is performed on clk_counter. For all other modes, edge detection is on the clk_peri.

Multiple detected events are treated as follows:

■ In the rising edge and falling edge modes, multiple events are effectively reduced to a single event. As a result, events may be lost.
■ In the rising/falling edge mode, an even number of events are not detected and an odd number of events are reduced to a single event. This is because the rising/falling edge mode is typically used for capture events to determine the width of a pulse. The current functionality will ensure that the alternating pattern of rising and falling is maintained.

Notes:

■ All trigger inputs are synchronized to clk_peri.
■ When more than one event occurs in the same clk_counter period, one or more events may be missed. This can happen for high-frequency events (frequencies close to the counter frequency) and a timer configuration in which a pre-scaled (divided) clk_counter is used.
27.2.4 Trigger Outputs

Each counter can generate three trigger output events. These trigger output events can be routed through the trigger mux to other peripherals on the device. The three trigger outputs are:

- Overflow (OV): An overflow event indicates that in up-counting mode, COUNTER equals the PERIOD register, and is changed to a different value.
- Underflow (UN): An underflow event indicates that in a down-counting mode, COUNTER equals 0, and is changed to a different value.
- Compare/Capture (CC): This event is generated when the counter is running and one of the following conditions occur:
  - Counter equals the compare value. This event is either generated when the match is about to occur (COUNTER does not equal CC and is changed to CC) or when the match is not about to occur (COUNTER equals CC and is changed to a different value).
  - A capture event has occurred and the CC/CC_BUFF registers are updated.

Note: These signals remain high only for two cycles of clk_sys. For reliable operation, the condition that causes this trigger should be at the most a quarter of the clk_sys. For example, if the clk_sys is running at 24 MHz, the condition causing the trigger should occur at a frequency equal to or less than 6 MHz.

27.2.5 Interrupts

The TCPWM block provides a dedicated interrupt output for each counter. This interrupt can be generated for a TC or CC event. A TC is the logical OR of the OV and UN events. Four registers are used to handle interrupts in this block, as shown in Table 27-1.

Table 27-1. Interrupt Register

<table>
<thead>
<tr>
<th>Interrupt Registers</th>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCPWM_CNT_INTR</td>
<td>0</td>
<td>TC</td>
<td>This bit is set to ‘1’, when a terminal count is detected. Write ‘1’ to clear this bit.</td>
</tr>
<tr>
<td>(Interrupt request register)</td>
<td>1</td>
<td>CC_MATCH</td>
<td>This bit is set to ‘1’ when the counter value matches capture/compare register value. Write ‘1’ to clear this bit.</td>
</tr>
<tr>
<td>TCPWM_CNT_INTR_SET</td>
<td>0</td>
<td>TC</td>
<td>Write ‘1’ to set the corresponding bit in the interrupt request register. When read, this register reflects the interrupt request register status.</td>
</tr>
<tr>
<td>(Interrupt set request register)</td>
<td>1</td>
<td>CC_MATCH</td>
<td>Write ‘1’ to set the corresponding bit in the interrupt request register. When read, this register reflects the interrupt request register status.</td>
</tr>
<tr>
<td>TCPWM_CNT_INTR_MASK</td>
<td>0</td>
<td>TC</td>
<td>Mask bit for the corresponding TC bit in the interrupt request register.</td>
</tr>
<tr>
<td>(Interrupt mask register)</td>
<td>1</td>
<td>CC_MATCH</td>
<td>Mask bit for the corresponding CC_MATCH bit in the interrupt request register.</td>
</tr>
<tr>
<td>TCPWM_CNT_INTR_MASKED</td>
<td>0</td>
<td>TC</td>
<td>Logical AND of the corresponding TC request and mask bits.</td>
</tr>
<tr>
<td>(Interrupt masked request register)</td>
<td>1</td>
<td>CC_MATCH</td>
<td>Logical AND of the corresponding CC_MATCH request and mask bits.</td>
</tr>
</tbody>
</table>

27.2.6 PWM Outputs

The TCPWM has two outputs, pwm and pwm_n (complementary of pwm). Note that the OV, UN, and CC conditions are used to drive pwm and pwm_n, by configuring the TCPWM_CNT_TR_CTRL2 register (Table 27-2).

Table 27-2. Configuring Output for OV, UN, and CC Conditions

<table>
<thead>
<tr>
<th>Field</th>
<th>Bit</th>
<th>Value</th>
<th>Event</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CC_MATCH_MODE</td>
<td>1:0</td>
<td>0</td>
<td>Set pwm to ‘1’</td>
<td>Configures output line on a compare match (CC) event</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>Clear pwm to ‘0’</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2</td>
<td>Invert pwm</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3</td>
<td>No change</td>
<td></td>
</tr>
<tr>
<td>OVERFLOW_MODE</td>
<td>3:2</td>
<td>0</td>
<td>Set pwm to ‘1’</td>
<td>Configures output line on an overflow (OV) event</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>Clear pwm to ‘0’</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2</td>
<td>Invert pwm</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3</td>
<td>No change</td>
<td></td>
</tr>
<tr>
<td>UNDERFLOW_MODE</td>
<td>5:4</td>
<td>0</td>
<td>Set pwm to ‘1’</td>
<td>Configures output line on a underflow (UN) event</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>Clear pwm to ‘0’</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2</td>
<td>Invert pwm</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3</td>
<td>No change</td>
<td></td>
</tr>
</tbody>
</table>
27.2.7 Power Modes

The TCPWM block works in Active and Sleep modes. The TCPWM block is powered from V\textsubscript{CCD}. The configuration registers and other logic are powered in Deep Sleep mode to keep the states of configuration registers. See Table 27-3 for details.

Table 27-3. Power Modes in TCPWM Block

<table>
<thead>
<tr>
<th>Power Mode</th>
<th>Block Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active</td>
<td>This block is fully operational in this mode with clock running and power switched on.</td>
</tr>
<tr>
<td>Sleep</td>
<td>The CPU is in sleep but the block is still functional in this mode. All counter clocks are on.</td>
</tr>
<tr>
<td>Deep Sleep</td>
<td>Both power and clocks to the block are turned off, but configuration registers retain their states.</td>
</tr>
<tr>
<td>Hibernate</td>
<td>In this mode, the power to this block is switched off. Configuration registers will lose their state.</td>
</tr>
</tbody>
</table>

27.3 Operation Modes

The counter block can function in six operational modes, as shown in Table 27-4. The MODE [26:24] field of the counter control register (TCPWM_CNTx_CTRL) configures the counter in the specific operational mode.

Table 27-4. Operational Mode Configuration

<table>
<thead>
<tr>
<th>Mode</th>
<th>MODE Field [26:24]</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>000</td>
<td>The counter increments or decrements by ‘1’ at every counter clock cycle in which a count event is detected. The Compare/Capture register is used to compare the count.</td>
</tr>
<tr>
<td>Capture</td>
<td>010</td>
<td>The counter increments or decrements by ‘1’ at every counter clock cycle in which a count event is detected. A capture event copies the counter value into the capture register.</td>
</tr>
<tr>
<td>Quadrature</td>
<td>011</td>
<td>Quadrature decoding. The counter is decremented or incremented based on two phase inputs according to an X1, X2, or X4 decoding scheme.</td>
</tr>
<tr>
<td>PWM</td>
<td>100</td>
<td>Pulse width modulation.</td>
</tr>
<tr>
<td>PWM_DT</td>
<td>101</td>
<td>Pulse width modulation with dead time insertion.</td>
</tr>
<tr>
<td>PWM_PR</td>
<td>110</td>
<td>Pseudo-random PWM using a 16- or 32-bit linear feedback shift register (LFSR) to generate pseudo-random noise.</td>
</tr>
</tbody>
</table>

The counter can be configured to count up, down, and up/down by setting the UP\_DOWN\_MODE[17:16] field in the TCPWM_CNTx_CTRL register, as shown in Table 27-5.

Table 27-5. Counting Mode Configuration

<table>
<thead>
<tr>
<th>Counting Modes</th>
<th>UP_DOWN_MODE[17:16]</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>UP Counting Mode</td>
<td>00</td>
<td>Increments the counter until the period value is reached. A Terminal Count (TC) condition is generated when the counter changes from the period value.</td>
</tr>
<tr>
<td>DOWN Counting Mode</td>
<td>01</td>
<td>Decrements the counter from the period value until 0 is reached. A TC condition is generated when the counter changes from a value of ‘0’.</td>
</tr>
<tr>
<td>UP/DOWN Counting Mode 1</td>
<td>10</td>
<td>Increments the counter until the period value is reached, and then decrements the counter until ‘0’ is reached. A TC condition is generated only when the counter changes from a value of ‘0’.</td>
</tr>
<tr>
<td>UP/DOWN Counting Mode 2</td>
<td>11</td>
<td>Similar to up/down counting mode 1 but a TC condition is generated when the counter changes from ‘0’ and when the counter value changes from the period value.</td>
</tr>
</tbody>
</table>
27.3.1 Timer Mode

The timer mode is commonly used to measure the time of occurrence of an event or to measure the time difference between two events. The timer functionality increments/decrements a counter between 0 and the value stored in the PERIOD register. When the counter is running, the count value stored in the COUNTER register is compared with the compare/capture register (CC). When COUNTER equals CC, the cc_match event is generated.

Timer functionality is typically used for one of the following:
- Timing a specific delay – the count event is a constant ‘1’.
- Counting the occurrence of a specific event – the event should be connected as an input trigger and selected for the count event.

**Table 27-6. Timer Mode Trigger Input Description**

<table>
<thead>
<tr>
<th>Trigger Inputs</th>
<th>Usage</th>
</tr>
</thead>
</table>
| Reload         | Sets the counter value and starts the counter. Behavior is dependent on UP_DOWN_MODE:  
|                | ■ COUNT_UP: The counter is set to “0” and count direction is set to “up”.  
|                | ■ COUNT_DOWN: The counter is set to PERIOD and count direction is set to “down”.  
|                | ■ COUNT_UPDN1/2: The counter is set to “1” and count direction is set to “up”.  
|                | Can be used when the counter is running or not running. |
| Start          | Starts the counter. The counter is not initialized by hardware. The current counter value is used. Behavior is dependent on UP_DOWN_MODE. When the counter is not running:  
|                | ■ COUNT_UP: The count direction is set to “up”.  
|                | ■ COUNT_DOWN: The count direction is set to “down”.  
|                | ■ COUNT_UPDN1/2: The count direction is not modified.  
|                | Note that when the counter is running, the start event has no effect.  
|                | Can be used when the counter is running or not running. |
| Stop           | Stops the counter. |
| Count          | Count event increments/decrements the counter. |
| Capture        | Not used. |

Incrementing and decrementsing the counter is controlled by the count event and the counter clock clk_counter. Typical operation will use a constant ‘1’ count event and clk_counter without pre-scaling. Advanced operations are also possible; for example, the counter event configuration can decide to count the rising edges of a synchronized input trigger.

**Table 27-7. Timer Mode Supported Features**

<table>
<thead>
<tr>
<th>Supported Features</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock pre-scaling</td>
<td>Pre-scales the counter clock clk_counter.</td>
</tr>
</tbody>
</table>
| One-shot           | Counter is stopped by hardware, after a single period of the counter:  
|                    | ■ COUNT_UP: on an overflow event.  
|                    | ■ COUNT_DOWN, COUNT_UPDN1/2: on an underflow event. |
| Auto reload CC      | CC and CC_BUFF are exchanged on a cc_match event (when specified by CTRL.AUTO_RELOAD_CC) |
| Up/down modes       | Specified by UP_DOWN_MODE:  
|                    | ■ COUNT_UP: The counter counts from 0 to PERIOD.  
|                    | ■ COUNT_DOWN: The counter counts from PERIOD to 0.  
|                    | ■ COUNT_UPDN1/2: The counter counts from 1 to PERIOD and back to 0. |

Table 27-6 lists the trigger outputs and the conditions when they are triggered.
Table 27-8. Timer Mode Trigger Outputs

<table>
<thead>
<tr>
<th>Trigger Outputs</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>cc_match (CC)</td>
<td>Counter changes from a state in which COUNTER equals CC.</td>
</tr>
<tr>
<td>Underflow (UN)</td>
<td>Counter is decrementing and changes from a state in which COUNTER equals “0”.</td>
</tr>
<tr>
<td>Overflow (OV)</td>
<td>Counter is incrementing and changes from a state in which COUNTER equals PERIOD.</td>
</tr>
</tbody>
</table>

Note: Each output is only two clk_sys wide and is represented by an arrow in the timing diagrams in this chapter, for example see Figure 27-5.

Table 27-9. Timer Mode Interrupt Outputs

<table>
<thead>
<tr>
<th>Interrupt Outputs</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>tc</td>
<td>Specified by UP_DOWN_MODE:</td>
</tr>
<tr>
<td></td>
<td>- COUNT_UP: The tc event is the same as the overflow event.</td>
</tr>
<tr>
<td></td>
<td>- COUNT_DOWN: The tc event is the same as the underflow event.</td>
</tr>
<tr>
<td></td>
<td>- COUNT_UPDN1: The tc event is the same as the underflow event.</td>
</tr>
<tr>
<td></td>
<td>- COUNT_UPDN2: The tc event is the same as the logical OR of the overflow and underflow events.</td>
</tr>
<tr>
<td>cc_match (CC)</td>
<td>Counter changes from a state in which COUNTER equals CC.</td>
</tr>
</tbody>
</table>

Table 27-10. Timer Mode PWM Outputs

<table>
<thead>
<tr>
<th>PWM Outputs</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>pwm</td>
<td>Not used.</td>
</tr>
<tr>
<td>pwm_n</td>
<td>Not used.</td>
</tr>
</tbody>
</table>

Notes:

- The timer functionality uses only PERIOD (and not PERIOD_BUFF).
- Do not write to COUNTER when the counter is running.

Figure 27-5 illustrates a timer in up-counting mode. The counter is initialized (to 0) and started with a software-based reload event.

Notes:

- PERIOD is 4, resulting in an effective repeating counter pattern of 4+1 = 5 counter clock periods. The CC register is 2, and sets the condition for a cc_match event.
- When the counter changes from a state in which COUNTER is 4, an overflow and tc event are generated.
- When the counter changes from a state in which COUNTER is 2, a cc_match event is generated.
- A constant count event of ‘1’ and clk_counter without prescaling is used in the following scenarios. If the count event is ‘0’ and a reload event is triggered, the reload will be registered only on the first clock edge when the count event is ‘1’.
Figure 27-5. Timer in Up-counting Mode

Figure 27-6 illustrates a timer in “one-shot” operation mode. Note that the counter is stopped on a tc event.

Figure 27-6. Timer in One-shot Mode

Figure 27-7 illustrates clock pre-scaling. Note that the counter is only incremented every other counter cycle.

Figure 27-7. Timer Clock Pre-scaling

Figure 27-8 illustrates a counter that is initialized and started (reload event), stopped (stop event), and continued/started (start event). Note that the counter does not change value when it is not running (STATUS.RUNNING).
Figure 27-8. Counter Start/Stopped/Continued

Figure 27-9 illustrates a timer that uses both CC and CC_BUFF registers. Note that CC and CC_BUFF are exchanged on a cc_match event.

Figure 27-9. Use of CC and CC_BUFF Register Bits

Figure 27-10 illustrates a timer in down counting mode. The counter is initialized (to PERIOD) and started with a software-based reload event.

Notes:
- When the counter changes from a state in which COUNTER is 0, a UN and TC events are generated.
- When the counter changes from a state in which COUNTER is 2, a cc_match event is generated.
- PERIOD is 4, resulting in an effective repeating counter pattern of $4+1 = 5$ counter clock periods.
Figure 27-10. Timer in Down-counting Mode

Figure 27-11 illustrates a timer in up/down counting mode 1. The counter is initialized (to 1) and started with a software-based reload event.

Notes:
- When the counter changes from a state in which COUNTER is 4, an overflow is generated.
- When the counter changes from a state in which COUNTER is 0, an underflow and tc event are generated.
- When the counter changes from a state in which COUNTER is 2, a cc_match event is generated.
- PERIOD is 4, resulting in an effective repeating counter pattern of $2 \times 4 = 8$ counter clock periods.

Figure 27-11. Timer in Up/Down Counting Mode 1

Figure 27-12 illustrates a timer in up/down counting mode 1, with different CC values.

Notes:
- When CC is 0, the cc_match event is generated at the start of the period (when the counter changes from a state in which COUNTER is 0).
- When CC is PERIOD, the cc_match event is generated at the middle of the period (when the counter changes from a state in which COUNTER is PERIOD).
27.3.1.1 Configuring Counter for Timer Mode

The steps to configure the counter for Timer mode of operation and the affected register bits are as follows.

1. Disable the counter by writing ‘1’ to the TCPWM_CTRL_CLR register.
2. Select Timer mode by writing ‘000’ to the MODE[26:24] field of the TCPWM_CNT_CTRL register.
3. Set the required 16- or 32-bit period in the TCPWM_CNT_PERIOD register.
4. Set the 16- or 32-bit compare value in the TCPWM_CNT_CC register and the buffer compare value in the TCPWM_CNT_CC_BUFF register.
5. Set AUTO_RELOAD_CC field of the TCPWM_CNT_CTRL register, if required to swap values at every CC condition.
7. Set the direction of counting by writing to the UP_DOWN_MODE[17:16] field of the TCPWM_CNT_CTRL register.
8. The timer can be configured to run either in continuous mode or one-shot mode by writing 0 or 1, respectively to the ONE_SHOT[18] field of the TCPWM_CNT_CTRL register.
9. Set the TCPWM_CNT_TR_CTRL0 register to select the trigger that causes the event (reload, start, stop, capture, and count).
10. Set the TCPWM_CNT_TR_CTRL1 register to select the edge of the trigger that causes the event (reload, start, stop, capture, and count).
11. If required, set the interrupt upon TC or CC condition.
12. Enable the counter by writing ‘1’ to the TCPWM_CTRL_SET register. A start trigger must be provided through firmware (TCPWM_CMD_START register) to start the counter if the hardware start signal is not enabled.
27.3.2 Capture Mode

The capture functionality increments and decrements a counter between 0 and PERIOD. When the capture event is activated the counter value COUNTER is copied to CC (and CC is copied to CC_BUFF).

The capture functionality can be used to measure the width of a pulse (connected as one of the input triggers and used as capture event).

The capture event can be triggered through the capture trigger input or through a firmware write to command register (TCPWM_CMD_CAPTURE).

Table 27-11. Capture Mode Trigger Input Description

<table>
<thead>
<tr>
<th>Trigger Inputs</th>
<th>Usage</th>
</tr>
</thead>
</table>
| reload         | Sets the counter value and starts the counter. Behavior is dependent on UP_DOWN_MODE:  
  ■ COUNT_UP: The counter is set to “0” and count direction is set to “up”.  
  ■ COUNT_DOWN: The counter is set to PERIOD and count direction is set to “down”.  
  ■ COUNT_UPDN1/2: The counter is set to “1” and count direction is set to “up”.  
  Can be used only when the counter is not running. |
| start          | Starts the counter. The counter is not initialized by hardware. The current counter value is used. Behavior is dependent on UP_DOWN_MODE:  
  ■ COUNT_UP: The count direction is set to “up”.  
  ■ COUNT_DOWN: The count direction is set to “down”.  
  ■ COUNT_UPDN1/2: The count direction is not modified.  
  Can be used only when the counter is not running. |
| stop           | Stops the counter. |
| count          | Count event increments/decrements the counter. |
| capture        | Copies the counter value to CC and copies CC to CC_BUFF. |

Table 27-12. Capture Mode Supported Features

<table>
<thead>
<tr>
<th>Supported Features</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock pre-scaling</td>
<td>Pre-scales the counter clock clk_counter.</td>
</tr>
</tbody>
</table>
| One-shot           | Counter is stopped by hardware, after a single period of the counter:  
  ■ COUNT_UP: on an overflow event.  
  ■ COUNT_DOWN, COUNT_UPDN1/2: on an underflow event. |
| Up/down modes      | Specified by UP_DOWN_MODE:  
  ■ COUNT_UP: The counter counts from 0 to PERIOD.  
  ■ COUNT_DOWN: The counter counts from PERIOD to 0.  
  ■ COUNT_UPDN1/2: The counter counts from 1 to PERIOD and back to 0. |

Table 27-13. Capture Mode Trigger Output Description

<table>
<thead>
<tr>
<th>Trigger Outputs</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>cc_match (CC)</td>
<td>CC is copied to CC_BUFF and counter value is copied to CC (cc_match equals capture event).</td>
</tr>
<tr>
<td>Underflow (UN)</td>
<td>Counter is decrementing and changes from a state in which COUNTER equals “0”.</td>
</tr>
<tr>
<td>Overflow (OV)</td>
<td>Counter is incrementing and changes from a state in which COUNTER equals PERIOD.</td>
</tr>
</tbody>
</table>
Table 27-14. Capture Mode Interrupt Outputs

<table>
<thead>
<tr>
<th>Interrupt Outputs</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>tc</td>
<td>Specified by UP_DOWN_MODE:</td>
</tr>
<tr>
<td></td>
<td>■ COUNT_UP: tc event is the same as the overflow event.</td>
</tr>
<tr>
<td></td>
<td>■ COUNT_DOWN: tc event is the same as the underflow event.</td>
</tr>
<tr>
<td></td>
<td>■ COUNT_UPDN1: tc event is the same as the underflow event.</td>
</tr>
<tr>
<td></td>
<td>■ COUNT_UPDN2: tc event is the same as the logical OR of the overflow and underflow events.</td>
</tr>
<tr>
<td>cc_match (CC)</td>
<td>CC is copied to CC_BUFF and counter value is copied to CC (cc_match equals capture event).</td>
</tr>
</tbody>
</table>

Table 27-15. Capture Mode PWM Outputs

<table>
<thead>
<tr>
<th>PWM Outputs</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>pwm</td>
<td>Not used.</td>
</tr>
<tr>
<td>pwm_n</td>
<td>Not used.</td>
</tr>
</tbody>
</table>

Figure 27-14. Capture Functionality

Notes:

- The capture event detection uses rising edge detection. As a result, the capture event is remembered until the next "active count" pre-scaled counter clock.
- When a capture event occurs, COUNTER is copied into CC. CC is copied to CC_BUFF.
- A cc_match event is generated when the counter value is captured.

Figure 27-15 illustrates capture behavior in the up counting mode.
When multiple capture events are detected before the next “active count” pre-scaled counter clock, capture events are treated as follows:

- In the rising edge and falling edge modes, multiple events are effectively reduced to a single event.
- In the rising/falling edge mode, an even number of events is not detected and an odd number of events is reduced to a single event.

This behavior is illustrated by Figure 27-16, in which a pre-scaler by a factor of 4 is used.

![Figure 27-16. Multiple Events Detected before Active-Count](image)

27.3.2.1 Configuring Counter for Capture Mode

The steps to configure the counter for Capture mode operation and the affected register bits are as follows.

1. Disable the counter by writing ‘1’ to the TCPWM_CTRL_CLR register.
2. Select Capture mode by writing ‘010’ to the MODE[26:24] field of the TCPWM_CNT_CTRL register.
3. Set the required 16-bit period in the TCPWM_CNT_PERIOD register.
5. Set the direction of counting by writing to the UP_DOWN_MODE[17:16] field of the TCPWM_CNT_CTRL register.
6. Counter can be configured to run either in continuous mode or one-shot mode by writing 0 or 1, respectively to the ONE_SHOT[18] field of the TCPWM_CNT_CTRL register.
7. Set the TCPWM_CNT_TR_CTRL0 register to select the trigger that causes the event (reload, start, stop, capture, and count).
8. Set the TCPWM_CNT_TR_CTRL1 register to select the edge that causes the event (reload, start, stop, capture, and count).
9. If required, set the interrupt upon TC or CC condition.
10. Enable the counter by writing ‘1’ to the TCPWM_CTRL_SET register. A start trigger must be provided through firmware (TCPWM_CMD_START register) to start the counter if the hardware start signal is not enabled.
27.3.3 Quadrature Decoder Mode

Quadrature functionality increments and decrements a counter between 0 and 0xFFFF or 0xFFFFFFFF (32-bit mode). Counter updates are under control of quadrature signal inputs: index, phiA, and phiB. The index input is used to indicate an absolute position. The phiA and phiB inputs are used to determine a change in position (the rate of change in position can be used to derive speed). The quadrature inputs are mapped onto triggers (as described in Table 27-16).

Table 27-16. Quadrature Mode Trigger Input Description

<table>
<thead>
<tr>
<th>Trigger Input</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>reload/index</td>
<td>This event acts as a quadrature index input. It initializes the counter to the counter midpoint 0x8000 (16-bit) or 0x8000000 (32-bit mode) and starts the quadrature functionality. Rising edge event detection or falling edge detection mode should be used.</td>
</tr>
<tr>
<td>start/phiB</td>
<td>This event acts as a quadrature phiB input. Pass through (no edge detection) event detection mode should be used.</td>
</tr>
<tr>
<td>stop</td>
<td>Stops the quadrature functionality.</td>
</tr>
<tr>
<td>count/phiA</td>
<td>This event acts as a quadrature phiA input. Pass through (no edge detection) event detection mode should be used.</td>
</tr>
<tr>
<td>capture</td>
<td>Not used.</td>
</tr>
</tbody>
</table>

Table 27-17. Quadrature Mode Supported Features

<table>
<thead>
<tr>
<th>Supported Features</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quadrature encoding</td>
<td>Three encoding schemes for the phiA and phiB inputs are supported (as specified by CTRL QUADRATURE_MODE): X1 encoding, X2 encoding, X4 encoding.</td>
</tr>
</tbody>
</table>

Note: Clock pre-scaling is not supported and the count event is used as a quadrature input phiA. As a result, the quadrature functionality operates on the counter clock (clk_counter), rather than on an "active count" prescaled counter clock.

Table 27-18. Quadrature Mode Trigger Output Description

<table>
<thead>
<tr>
<th>Trigger Outputs</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>cc_match (CC)</td>
<td>Counter value COUNTER equals 0 or 0xFFFF or 0xFFFFFFFF (32-bit mode) or a reload/index event.</td>
</tr>
<tr>
<td>Underflow (UN)</td>
<td>Not used.</td>
</tr>
<tr>
<td>Overflow (OV)</td>
<td>Not used.</td>
</tr>
</tbody>
</table>

Table 27-19. Quadrature Mode Interrupt Outputs

<table>
<thead>
<tr>
<th>Interrupt Outputs</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>cc_match (CC)</td>
<td>Counter value COUNTER equals 0 or 0xFFFF or 0xFFFFFFFF (32-bit mode) or a reload/index event.</td>
</tr>
<tr>
<td>tc</td>
<td>Reload/index event.</td>
</tr>
</tbody>
</table>

Table 27-20. Quadrature Mode PWM Outputs

<table>
<thead>
<tr>
<th>PWM Outputs</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>pwm</td>
<td>Not used.</td>
</tr>
<tr>
<td>pwm_n</td>
<td>Not used.</td>
</tr>
</tbody>
</table>
Quadrature functionality is described as follows:

- A software-generated reload event starts quadrature operation. As a result, COUNTER is set to 0x8000 or 0x80000000, which is the counter midpoint (the COUNTER is set to 0x7FFF if the reload event coincides with a decrement event; the COUNTER is set to 0x8001 if the reload event coincides with an increment event). Note that a software-generated reload event is generated only once, when the counter is not running. All other reload/index events are hardware-generated reload events as a result of the quadrature index signal.

- During quadrature operation:
  - The counter value COUNTER is incremented or decremented based on the specified quadrature encoding scheme.
  - On a reload/index event, CC is copied to CC_BUFF, COUNTER is copied to CC, and COUNTER is set to 0x8000. In addition, the tc and cc_match events are generated.
  - When the counter value COUNTER is 0x0000, CC is copied to CC_BUFF, COUNTER (0x0000) is copied to CC, and COUNTER is set to 0x8000. In addition, the cc_match event is generated.
  - When the counter value COUNTER is 0xFFFF, CC is copied to CC_BUFF, COUNTER (0xFFFF) is copied to CC, and COUNTER is set to 0x8000. In addition, the cc_match event is generated.

The software interrupt handler uses the tc and cc_match interrupt cause fields to distinguish between a reload/index event and a situation in which a minimum/maximum counter value was reached (about to wrap around). The CC and CC_BUFF registers are used to determine when the interrupt causing event occurred.

Note that a counter increment/decrement can coincide with a reload/index/tc event or with a situation cc_match event. Under these circumstances, the counter value set to either 0x8000+1 (increment) or 0x8000-1 (decrement).

Counter increments (incr1 event) and decrements (decr1 event) are determined by the quadrature encoding scheme as illustrated by Figure 27-18.
Figure 27-19 illustrates quadrature functionality as a function of the reload/index, incr1, and decr1 events. Note that the first reload/index event copies the counter value COUNTER to CC.

Figure 27-19. Quadrature Mode Reload/Index Timing

Figure 27-20 illustrate quadrature functionality for different event scenarios (including scenarios with coinciding events). In all scenarios, the first reload/index event is generated by software when the counter is not yet running.

Figure 27-20
Figure 27-20. Quadrature Mode Timing Cases

**Quadrature decoding, no coinciding reload and decrement events**

Counter cycle

- Underflow with decre 1-event
- Underflow without decre 1-event

**Quadrature decoding, no coinciding reload events**

Counter cycle

- Underflow with incr 1-event
- Overflow with decre 1-event

**Quadrature decoding, decrement/increment behavior, no coinciding reload events**

Counter cycle

- Reload event and underflow with decre 1-event
- Reload event and overflow with incr 1-event

**Quadrature decoding, decrement/increment behavior, coinciding reload events**

Counter cycle

- Reload event and underflow with decre 1-event
- Reload event and overflow with incr 1-event

**Quadrature decoding, decrement behavior and reload events**

Counter cycle

- Reload event and decre 1-event coincide
27.3.3 Configuring Counter for Quadrature Mode

The steps to configure the counter for quadrature mode of operation and the affected register bits are as follows.

1. Disable the counter by writing ‘1’ to the TCPWM_CTRL_CLR register.
4. Set the TCPWM_CNT_TR_CTRL0 register to select the trigger that causes the event (Index and Stop).
5. Set the TCPWM_CNT_TR_CTRL1 register to select the edge that causes the event (Index and Stop).
6. If required, set the interrupt upon TC or CC condition.
7. Enable the counter by writing ‘1’ to the TCPWM_CTRL_SET register. A start trigger must be provided through firmware (TCPWM_CMD_START register) to start the counter if the hardware start signal is not enabled.

27.3.4 Pulse Width Modulation Mode

PWM functionality increments/decrements a counter between 0 and PERIOD. When the counter is running, the counter value COUNTER is compared with CC. When COUNTER equals CC, the cc_match event is generated. Additionally, on a counter overflow and counter underflow, the overflow and underflow events are generated. Combined, the cc_match, overflow and underflow events are used to generate a pulse-width modulated signal on the PWM “pwm” and “pwm_n” output signals. Left-aligned, right-aligned, and center-aligned PWM signals can be generated. Asymmetric PWM signals can be generated using the COUNT_UPDN2 mode.

<table>
<thead>
<tr>
<th>Trigger Inputs</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>reload</td>
<td>Sets the counter value and starts the counter. Behavior is dependent on UP_DOWN_MODE:</td>
</tr>
<tr>
<td></td>
<td>▪ COUNT_UP: The counter is set to “0” and count direction is set to “up”.</td>
</tr>
<tr>
<td></td>
<td>▪ COUNT_DOWN: The counter is set to PERIOD and count direction is set to “down”.</td>
</tr>
<tr>
<td></td>
<td>▪ COUNT_UPDN1/2: The counter is set to “1” and count direction is set to “up”.</td>
</tr>
<tr>
<td></td>
<td>Can be used only when the counter is not running.</td>
</tr>
<tr>
<td>start</td>
<td>Starts the counter. The counter is not initialized by hardware. The current counter value is used. Behavior is dependent on UP_DOWN_MODE:</td>
</tr>
<tr>
<td></td>
<td>▪ COUNT_UP: The count direction is set to “up”.</td>
</tr>
<tr>
<td></td>
<td>▪ COUNT_DOWN: The count direction is set to “down”.</td>
</tr>
<tr>
<td></td>
<td>▪ COUNT_UPDN1/2: The count direction is set to “up”.</td>
</tr>
<tr>
<td></td>
<td>Can be used only when the counter is not running.</td>
</tr>
<tr>
<td>stop/kill</td>
<td>Stops the counter. Different stop/kill modes exist.</td>
</tr>
<tr>
<td>count</td>
<td>Count event increments/decrements the counter.</td>
</tr>
<tr>
<td>capture/swap</td>
<td>This event acts as a swap event. When this event is active, the CC/CC_BUFF and PERIOD/PERIOD_BUFF registers are exchanged on a tc event (when specified by CTRL.AUTO_RELOAD_CC and CTRL.AUTO_RELOAD_PERIOD).</td>
</tr>
<tr>
<td></td>
<td>A swap event requires rising, falling, or rising/falling edge event detection mode. Pass-through mode is not supported, unless the selected event is a constant ‘0’ or ‘1’.</td>
</tr>
<tr>
<td></td>
<td>When a swap event is detected and the counter is running, the event is kept pending until the next tc event. When a swap event is detected and the counter is not running, the event is cleared by hardware.</td>
</tr>
</tbody>
</table>
Table 27-22. PWM Mode Supported Features

<table>
<thead>
<tr>
<th>Supported Features</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock pre-scaling</td>
<td>Pre-scales the counter clock “clk_counter”.</td>
</tr>
<tr>
<td>One-shot</td>
<td>Counter is stopped by hardware, after a single period of the counter:</td>
</tr>
<tr>
<td></td>
<td>■ COUNT_UP: on an overflow event.</td>
</tr>
<tr>
<td></td>
<td>■ COUNT_DOWN and COUNT_UPDN1/2: on an underflow event.</td>
</tr>
<tr>
<td>Compare Swap</td>
<td>CC and CC_BUFF are exchanged on a swap event and tc event (when specified by CTRL.AUTO_RELOAD_CC).</td>
</tr>
<tr>
<td>Period Swap</td>
<td>PERIOD and PERIOD_BUFF are exchanged on a swap event and tc event (when specified by CTRL.AUTO_RELOAD_PERIOD). <strong>Note:</strong> When COUNT_UPDN2 mode exchanges PERIOD and PERIOD_BUFF at a tc event that coincides with an overflow event, software should ensure that the PERIOD and PERIOD_BUFF values are the same.</td>
</tr>
<tr>
<td>Alignment (Up/Down modes)</td>
<td>Specified by UP_DOWN_MODE:</td>
</tr>
<tr>
<td></td>
<td>■ COUNT_UP: The counter counts from 0 to PERIOD. Generates a left-aligned PWM output.</td>
</tr>
<tr>
<td></td>
<td>■ COUNT_DOWN: The counter counts from PERIOD to 0. Generates a right-aligned PWM output.</td>
</tr>
<tr>
<td></td>
<td>■ COUNT_UPDN1/2: The counter counts from 1 to PERIOD and back to 0. Generates a center-aligned/ asymmetric PWM output.</td>
</tr>
<tr>
<td>Kill modes</td>
<td>Specified by PWM_SYNC_KILL and PWM_STOP_ON_KILL.</td>
</tr>
</tbody>
</table>

Note that the PWM mode does not support dead time insertion. This functionality is supported by the separate PWM_DT mode.

Table 27-23. PWM Mode Trigger Output Description

<table>
<thead>
<tr>
<th>Trigger Output</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>cc_match (CC)</td>
<td>Specified by UP_DOWN_MODE:</td>
</tr>
<tr>
<td></td>
<td>■ COUNT_UP and COUNT_DOWN: The counter changes to a state in which COUNTER equals CC.</td>
</tr>
<tr>
<td></td>
<td>■ COUNT_UPDN1/2: counter changes from a state in which COUNTER equals CC.</td>
</tr>
<tr>
<td>Underflow (UN)</td>
<td>Counter is decrementing and changes from a state in which COUNTER equals “0”.</td>
</tr>
<tr>
<td>Overflow (OV)</td>
<td>Counter is incrementing and changes from a state in which COUNTER equals PERIOD.</td>
</tr>
</tbody>
</table>

Table 27-24. PWM Mode Interrupt Output Description

<table>
<thead>
<tr>
<th>Interrupt Outputs</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>tc</td>
<td>Specified by UP_DOWN_MODE:</td>
</tr>
<tr>
<td></td>
<td>■ COUNT_UP: tc event is the same as the overflow event.</td>
</tr>
<tr>
<td></td>
<td>■ COUNT_DOWN: tc event is the same as the underflow event.</td>
</tr>
<tr>
<td></td>
<td>■ COUNT_UPDN1: tc event is the same as the underflow event.</td>
</tr>
<tr>
<td></td>
<td>■ COUNT_UPDN2: tc event is the same as the logical OR of the overflow and underflow events.</td>
</tr>
<tr>
<td>cc_match (CC)</td>
<td>Specified by UP_DOWN_MODE:</td>
</tr>
<tr>
<td></td>
<td>■ COUNT_UP and COUNT_DOWN: The counter changes to a state in which COUNTER equals CC.</td>
</tr>
<tr>
<td></td>
<td>■ COUNT_UPDN1/2: counter changes from a state in which COUNTER equals CC.</td>
</tr>
</tbody>
</table>

Table 27-25. PWM Mode PWM Outputs

<table>
<thead>
<tr>
<th>PWM Outputs</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>pwm</td>
<td>PWM output.</td>
</tr>
<tr>
<td>pwm_n</td>
<td>Complementary PWM output.</td>
</tr>
</tbody>
</table>
Note that the cc_match event generation in COUNT_UP and COUNT_DOWN modes are different from the generation in other functional modes or counting modes. This is to ensure that 0 percent and 100 percent duty cycles can be generated.

**Figure 27-21. PWM Mode Functionality**

PWM behavior depends on the PERIOD and CC registers. The software can update the PERIOD_BUFF and CC_BUFF registers, without affecting the PWM behavior. This is the main rationale for double buffering these registers.

A potential problem arises when software updates are not completed before the next tc event with an active pending swap event. For example, if software updates PERIOD_BUFF before the tc event and CC_BUFF after the tc event, swapping does not reflect the CC_BUFF register update. To prevent this from happening, the swap event should be generated by software through a register write after both the PERIOD_BUFF and CC_BUFF registers are updated. The swap event is kept pending by the hardware until the next tc event occurs.

The previous section addressed synchronized updates of the CC/CC_BUFF and PERIOD/PERIOD_BUFF registers of a single PWM using a software-generated swap event. During motor control, three PWMs work in unison and updates to all period and compare register pairs should be synchronized. All three PWMs have synchronized periods and as a result have synchronized tc events. The swap event for all three PWMs is generated by software through a single register write. The software should generate the swap events after the PERIOD_BUFF and CC_BUFF registers of all three PWMs are updated.

**Figure 27-22** illustrates a PWM in up counting mode. The counter is initialized (to 0) and started with a software-based reload event.

**Notes:**
- When the counter changes from a state in which COUNTER is 4, an overflow and tc event are generated.
- When the counter changes to a state in which COUNTER is 2, a cc_match event is generated.
- PERIOD is 4, resulting in an effective repeating counter pattern of 4+1 = 5 counter clock periods.
Figure 27-23 illustrates a PWM in up counting mode with different CC values. The figure also illustrates how a left-aligned and right-aligned PWM can be creating using the PWM in up counting mode. Note that CC is changed (to CC_BUFF, which is not depicted) on a tc event.

![Figure 27-23. PWM Left- and Right-Aligned Outputs](image)

Notes:
- When the counter changes from a state in which COUNTER is 0, an underflow and tc event are generated.
- When the counter changes to a state in which COUNTER is 2, a cc_match event is generated.
- PERIOD is 4, resulting in an effective repeating counter pattern of 4+1 = 5 counter clock periods.

Figure 27-24 illustrates a PWM in down counting mode. The counter is initialized (to PERIOD) and started with a software-based reload event.

![Figure 27-24. PWM in Down Counting Mode](image)

Notes:
- When the counter changes from a state in which COUNTER is 0, an underflow and tc event are generated.
- When the counter changes to a state in which COUNTER is 2, a cc_match event is generated.
- PERIOD is 4, resulting in an effective repeating counter pattern of 4+1 = 5 counter clock periods.

Figure 27-25 illustrates a PWM in down counting mode with different CC values. The figure also illustrates how a right-aligned PWM can be creating using the PWM in down counting mode. Note that the CC is changed (to CC_BUFF, which is not depicted) on a tc event.
Figure 27-25. Right-Aligned Down Counting PWM

Figure 27-26 illustrates a PWM in up/down counting mode. The counter is initialized (to 1) and started with a software-based reload event.

Notes:
- When the counter changes from a state in which COUNTER is 4, an overflow is generated.
- When the counter changes from a state in which COUNTER is 0, an underflow and tc event are generated.
- When the counter changes from a state in which COUNTER is 2, a cc_match event is generated. Note that the actual counter value COUNTER from before the reload event is NOT used, instead the counter value before the reload event is considered to be 0.
- PERIOD is 4, resulting in an effective repeating counter pattern of $2^4 = 8$ counter clock periods.

Figure 27-26. Up/Down Counting PWM

Figure 27-27 illustrates a PWM in up/down counting mode with different CC values. The figure also illustrates how a center-aligned PWM can be creating using the PWM in up/down counting mode.

Note:
- The actual counter value COUNTER from before the reload event is NOT used. Instead the counter value before the reload event is considered to be 0. As a result, when the first CC value at the reload event is 0, a cc_match event is generated.
- CC is changed (to CC_BUFF, which is not depicted) on a tc event.
As mentioned, different stop/kill modes exist. The mode is specified by PWM_STOP_ON_KILL and PWM_SYNC_KILL. The following three modes are supported:

- **PWM_STOP_ON_KILL is ‘1’ (PWM_SYNC_KILL is don’t care).** This mode stops the counter on a stop/kill event.
- **PWM_STOP_ON_KILL is ‘0’ and PWM_SYNC_KILL is ‘0’**. This mode keeps the counter running, but suppresses the PWM output signals synchronously with the next count clock (“active count” pre-scaled clk_counter) and continues to do so for the duration of the stop/kill event.
- **PWM_STOP_ON_KILL is ‘0’ and PWM_SYNC_KILL is ‘1’**. This mode keeps the counter running, but suppresses the PWM output signals synchronously with the next count clock (“active count” pre-scaled clk_counter) and continues to do so until the next tc event without a stop/kill event.

Figure 27-28, Figure 27-29. and Figure 27-30 illustrate the above three modes.
Figure 27-29. PWM Async Kill

- **Dead time**
- **Pwm polarity**
- **Pwm_n polarity**

Figure 27-30. PWM Sync Kill

- **Dead time**
- **Pwm polarity**
- **Pwm_n polarity**

Figure 27-31 illustrates center-aligned PWM with PERIOD/PERIOD_BUFF and CC/CC_BUFF registers (up/down counting mode 1). At the TC condition, the PERIOD and CC registers are automatically exchanged with the PERIOD_BUFF and CC_BUFF registers. The swap event is generated by hardware trigger 1, which is a constant ‘1’ and therefore always active at the TC condition. After the hardware exchange, the software handler on the tc interrupt cause updates PERIOD_BUFF and CC_BUFF.
The generation of the PWM output signals is a multi-step process and is illustrated as follows:

**Figure 27-32. PWM Output Generation**

**Figure 27-33. PWM Outputs When Killed**

*Note:* When the counter is not enabled or not running ((temporarily) stopped or killed), the PWM output signals values are determined by their respective polarity settings.
27.3.4.1 Asymmetric PWM

The PWM mode supports the generation of an asymmetric PWM. For an asymmetric PWM, the `pwm_dt_input` pulse is not necessarily centered in the middle of the period. This functionality is realized by having a different CC value when counting up and when counting down. The CC and CC_BUFF values are exchanged on an overflow event. Note that this restricts the asymmetry of the generated `pwm_dt_input` pulse.

The COUNT_UPDN2 mode should use the same period value when counting up and counting down. When PERIOD and PERIOD_BUFF are swapped on a tc event (overflow or underflow event), care should be taken to ensure that:

- Within a PWM period (tc event coincides with an overflow event), the period values are the same (an overflow swap of PERIOD and PERIOD_BUFF should not change the period value; that is, PERIOD_BUFF should be PERIOD)
- Between PWM periods (tc event coincides with an underflow event), the period value can change (an underflow swap of PERIOD and PERIOD_BUFF may change the period value; that is, PERIOD_BUFF may be different from PERIOD).

Figure 27-34 illustrates how the COUNT_UPDN2 mode is used to generate an asymmetric PWM.

Notes:
- When up counting, when CC value at the underflow event is 0, a cc_match event is generated.
- When down counting, when CC value at the overflow event is PERIOD, a cc_match event is generated.
- A tc event is generated for both an underflow and overflow event. The tc event is used to exchange the CC and CC_BUFF values.

The previous waveform illustrated functionality when the CC values are neither “0” nor PERIOD. Corner case conditions in which the CC values equal “0” or PERIOD are illustrated as follows.

Figure 27-35 illustrates how the COUNT_UPDN2 mode is used to generate an asymmetric PWM.

Notes:
- When up counting, when CC value at the underflow event is 0, a cc_match event is generated.
- When down counting, when CC value at the overflow event is PERIOD, a cc_match event is generated.
- A tc event is generated for both an underflow and overflow event. The tc event is used to exchange the CC and CC_BUFF values.
- Software updates CC_BUFF and PERIOD_BUFF in an interrupt handler on the tc event (and overwrites the hardware updated values from the CC/CC_BUFF and PERIOD/PERIOD_BUFF exchanges).
### 27.3.4.2 Configuring Counter for PWM Mode

The steps to configure the counter for the PWM mode of operation and the affected register bits are as follows.

1. Disable the counter by writing ‘1’ to the TCPWM_CTRL_CLR register.
2. Select PWM mode by writing ‘100b’ to the MODE[26:24] field of the TCPWM_CNT_CTRL register.
4. Set the required 16-bit period in the TCPWM_CNT_PERIOD register and the buffer period value in the TCPWM_CNT_PERIOD_BUFF register to swap values, if required.
5. Set the 16-bit compare value in the TCPWM_CNT_CC register and buffer compare value in the TCPWM_CNT_CC_BUFF register to swap values, if required.
6. Set the direction of counting by writing to the UP_DOWN_MODE[17:16] field of the TCPWM_CNT_CTRL register to configure left-aligned, right-aligned, or center-aligned PWM.
7. Set the PWM_STOP_ON_KILL and PWM_SYNC_KILL fields of the TCPWM_CNT_CTRL register as required.
8. Set the TCPWM_CNT_TR_CTRL0 register to select the trigger that causes the event (reload, start, kill, swap, and count).
9. Set the TCPWM_CNT_TR_CTRL1 register to select the edge that causes the event (reload, start, kill, swap, and count).
10. pwm and pwm_n can be controlled by the TCPWM_CNT_TR_CTRL2 register to set, reset, or invert upon CC, OV, and UN conditions.
11. If required, set the interrupt upon TC or CC condition.
12. Enable the counter by writing ‘1’ to the TCPWM_CTRL_SET register. A start trigger must be provided through firmware (TCPWM_CMD_START register) to start the counter if the hardware start signal is not enabled.
27.3.5 Pulse Width Modulation with Dead Time Mode

The PWM-DT functionality is the same as PWM functionality, except for the following differences:

- PWM_DT supports dead time insertion; PWM does not support dead time insertion.
- PWM_DT does not support clock pre-scaling; PWM supports clock pre-scaling.

Dead time insertion is a step that operates on a preliminary PWM output signal pwm_dt_input, as illustrated in Figure 27-32. Figure 27-37 illustrates dead time insertion for different dead times and different output signal polarity settings.
Figure 27-38 illustrates how the polarity settings and stop/kill functionality combined control the PWM output signals “pwm” and “pwm_n”.

27.3.5.1 Configuring Counter for PWM with Dead Time Mode

The steps to configure the counter for PWM with Dead Time mode of operation and the affected register bits are as follows:

1. Disable the counter by writing ‘1’ to the TCPWM_CTRL_CLR register.
2. Select PWM with Dead Time mode by writing ‘101’ to the MODE[26:24] field of the TCPWM_CNT_CTRL register.
3. Set the required dead time by writing to the GENERIC[15:8] field of the TCPWM_CNT_CTRL register.
4. Set the required 16-bit period in the TCPWM_CNT_PERIOD register and the buffer period value in the TCPWM_CNT_PERIOD_BUFF register to swap values, if required.
5. Set the 16-bit compare value in the TCPWM_CNT_CC register and the buffer compare value in the TCPWM_CNT_CC_BUFF register to swap values, if required.
6. Set the direction of counting by writing to the UP_DOWN_MODE[17:16] field of the TCPWM_CNT_CTRL register to configure left-aligned, right-aligned, or center-aligned PWM.
7. Set the PWM_STOP_ON_KILL and PWM_SYNC_KILL fields of the TCPWM_CNT_CTRL register as required.
8. Set the TCPWM_CNT_TR_CTRL0 register to select the trigger that causes the event (reload, start, kill, swap, and count).
9. Set the TCPWM_CNT_TR_CTRL1 register to select the edge that causes the event (reload, start, kill, swap, and count).
10. pwm and pwm_n can be controlled by the TCPWM_CNT_TR_CTRL2 register to set, reset, or invert upon CC, OV, and UN conditions.
11. If required, set the interrupt upon TC or CC condition.
12. Enable the counter by writing ‘1’ to the TCPWM_CTRL_SET register. A start trigger must be provided through firmware (TCPWM_CMD_START register) to start the counter if the hardware start signal is not enabled.
27.3.6 Pulse Width Modulation Pseudo-Random Mode (PWM_PR)

The PWM_PR functionality changes the counter value using the linear feedback shift register (LFSR). This results in a pseudo random number sequence. A signal similar to PWM signal is created by comparing the counter value COUNTER with CC. The generated signal has different frequency/noise characteristics than a regular PWM signal.

<table>
<thead>
<tr>
<th>Trigger Inputs</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>reload</td>
<td>Same behavior as start event. Can be used only when the counter is not running.</td>
</tr>
<tr>
<td>start</td>
<td>Starts the counter. The counter is not initialized by hardware. The current counter value is used. Behavior is independent on UP_DOWN_MODE. Can be used only when the counter is not running.</td>
</tr>
<tr>
<td>stop/kill</td>
<td>Stops the counter. Different stop/kill modes exist.</td>
</tr>
<tr>
<td>count</td>
<td>Not used.</td>
</tr>
<tr>
<td>capture</td>
<td>This event acts as a swap event. When this event is active, the CC/CC_BUFF and PERIOD/PERIOD_BUFF registers are exchanged on a tc event (when specified by CTRL.AUTO_RELOAD_CC and CTRL.AUTO_RELOAD_PERIOD). A swap event requires rising, falling, or rising/falling edge event detection mode. Pass-through mode is not supported, unless the selected event is a constant '0' or '1'. When a swap event is detected and the counter is running, the event is kept pending until the next tc event. When a swap event is detected and the counter is not running, the event is cleared by hardware.</td>
</tr>
</tbody>
</table>

**Note:** Event detection is on the peripheral clock, clk_peri.

Table 27-27. PWM_PR Supported Features

<table>
<thead>
<tr>
<th>Supported Features</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock pre-scaling</td>
<td>Pre-scales the counter clock, clk_counter.</td>
</tr>
<tr>
<td>One-shot</td>
<td>Counter is stopped by hardware, after a single period of the counter (counter value equals period value PERIOD).</td>
</tr>
<tr>
<td>Auto reload CC</td>
<td>CC and CC_BUFF are exchanged on a swap event AND tc event (when specified by CTRL.AUTO_RELOAD_CC).</td>
</tr>
<tr>
<td>Auto reload PERIOD</td>
<td>PERIOD and PERIOD_BUFF are exchanged on a swap event and tc event (when specified by CTRL.AUTO_RELOAD_PERIOD).</td>
</tr>
<tr>
<td>Kill modes</td>
<td>Specified by PWM_STOP_ON_KILL. See memory map for further details.</td>
</tr>
</tbody>
</table>

**Note:** The count event is not used. As a result, the PWM_PR functionality operates on the pre-scaled counter clock (clk_counter), rather than on an *active count* pre-scaled counter clock.

Table 27-28. PWM_PR Trigger Outputs

<table>
<thead>
<tr>
<th>Trigger Outputs</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>cc_match (CC)</td>
<td>Counter changes from a state in which COUNTER equals CC.</td>
</tr>
<tr>
<td>Underflow (UN)</td>
<td>Not used.</td>
</tr>
<tr>
<td>Overflow (OV)</td>
<td>Not used.</td>
</tr>
</tbody>
</table>

Table 27-29. PWM_PR Interrupt Outputs

<table>
<thead>
<tr>
<th>Interrupt Outputs</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>cc_match (CC)</td>
<td>Counter changes from a state in which COUNTER equals CC.</td>
</tr>
<tr>
<td>tc</td>
<td>Counter changes from a state in which COUNTER equals PERIOD.</td>
</tr>
</tbody>
</table>
The PWM_PR functionality is described as follows:

- The counter value COUNTER is initialized by software (to a value different from 0).
- A reload or start event starts PWM_PR operation.
- During PWM_PR operation:
  - The counter value COUNTER is changed based on the LFSR polynomial: \(x^{16} + x^{14} + x^{13} + x^{11} + 1\) (en.wikipedia.org/wiki/Linear_feedback_shift_register).
  
  
  \[
  \text{temp} = \text{COUNTER}[16-16] ^ \text{COUNTER}[16-14] ^ \text{COUNTER}[16-13] ^ \text{COUNTER}[16-11] \text{ or } \\
  \text{temp} = \text{COUNTER}[0] ^ \text{COUNTER}[2] ^ \text{COUNTER}[3] ^ \text{COUNTER}[5];
  \]
  
  \[
  \text{COUNTER} = (\text{temp} << 15) | (\text{COUNTER} >> 1)
  \]
  This will result in a pseudo random number sequence for COUNTER. For example, when COUNTER is initialized to 0xACE1, the number sequence is: 0xACE1, 0x5670, 0xAB38, 0x559C, 0x2ACE, 0x1567, 0x8AB3... This sequence will repeat itself after \(2^{16} - 1\) or 65535 counter clock cycles.
  - A 32-bit counter uses the LFSR polynomial: \(x^{32} + x^{30} + x^{26} + x^{25} + 1\)
  - When the counter value COUNTER equals CC, a cc_match event is generated.
  - When the counter value COUNTER equals PERIOD, a tc event is generated.
  - On a tc event, the CC/CC_BUFF and PERIOD/PERIOD_BUFF can be conditionally ex-changed under control of the capture/swap event and the CTRL.AUTO_RELOAD_CC and CTRL.AUTO_RELOAD_PERIOD field (see PWM functionality).
  - The output pwm_dt_input reflects: COUNTER[14:0] < CC[15:0]. Note that only the lower 15 bits of COUNTER are used for comparison, while the COUNTER itself can run up to 16- or 32-bit values. As a result, for CC greater or equal to 0x8000, pwm_dt_input is always 1. The pwm polarity can be inverted (as specified by CTRL QUADRATURE_MODE[0]).

As mentioned, different stop/kill modes exist. The mode is specified by PWM_STOP_ON_KILL (PWM_SYNC_KILL should be ‘0’ – asynchronous kill mode). The memory map describes the modes and the desired settings for the stop/kill event. The following two modes are supported:

- PWM_STOP_ON_KILL is ‘1’. This mode stops the counter on a stop/kill event.
- PWM_STOP_ON_KILL is ‘0’. This mode keeps the counter running, but suppresses the PWM output signals immediately and continues to do so for the duration of the stop/kill event.

<table>
<thead>
<tr>
<th>PWM PR PWM Outputs</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>pwm</td>
<td>PWM output.</td>
</tr>
<tr>
<td>pwm_n</td>
<td>Complementary PWM output.</td>
</tr>
</tbody>
</table>

**Figure 27-39. PWM_PR Functionality**

<table>
<thead>
<tr>
<th>PWM Outputs</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>pwm</td>
<td>PWM output.</td>
</tr>
<tr>
<td>pwm_n</td>
<td>Complementary PWM output.</td>
</tr>
</tbody>
</table>
Note that the LFSR produces a deterministic number sequence (given a specific counter initialization value). Therefore, it is possible to calculate the COUNTER value after a certain number of LFSR iterations, n. This calculated COUNTER value can be used as PERIOD value, and the tc event will be generated after precisely n counter clocks.

Figure 27-40 illustrates PWM_PR functionality.

Notes:

- The grey shaded areas represent the counter region in which the pwm_dt_input value is ‘1’, for a CC value of 0x4000. There are two areas, because only the lower 15 bits of the counter value are used.
- When CC is set to 0x4000, roughly one-half of the counter clocks will result in a pwm_dt_input value of ‘1’.

27.3.6.1 Configuring Counter for Pseudo-Random PWM Mode

The steps to configure the counter for pseudo-random PWM mode of operation and the affected register bits are as follows.

1. Disable the counter by writing ‘1’ to the TCPWM_CTRL_CLR register.
3. Set the required period (16 bit) in the TCPWM_CNT_PERIOD register and buffer period value in the TCPWM_CNT_PERIOD_BUFF register to swap values, if required.
4. Set the 16-bit compare value in the TCPWM_CNT_CC register and the buffer compare value in the TCPWM_CNT_CC_BUFF register to swap values.
5. Set the PWM_STOP_ON_KILL and PWM_SYNC_KILL fields of the TCPWM_CNT_CTRL register as required.
6. Set the TCPWM_CNT_TR_CTRL0 register to select the trigger that causes the event (reload, start, kill, and swap).
7. Set the TCPWM_CNT_TR_CTRL1 register to select the edge that causes the event (reload, start, kill, and swap).
8. pwm and pwm_n can be controlled by the TCPWM_CNT_TR_CTRL2 register to set, reset, or invert upon CC, OV, and UN conditions.
9. If required, set the interrupt upon TC or CC condition.
10. Enable the counter by writing ‘1’ to the TCPWM_CTRL_SET register. A start trigger must be provided through firmware (TCPWM_CMD_START register) to start the counter if the hardware start signal is not enabled.
### 27.4 TCPWM Registers

<table>
<thead>
<tr>
<th>Register</th>
<th>Comment</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCPWM_CTRL</td>
<td>TCPWM control register</td>
<td>Enables the counter block</td>
</tr>
<tr>
<td>TCPWM_CTRL_CLR</td>
<td>TCPWM control clear register</td>
<td>Used to avoid race-conditions on read-modify-write attempt to the CTRL register</td>
</tr>
<tr>
<td>TCPWM_CTRL_SET</td>
<td>TCPWM control set register</td>
<td>Used to avoid race-conditions on read-modify-write attempt to the CTRL register</td>
</tr>
<tr>
<td>TCPWM_CMD_CAPTURE</td>
<td>TCPWM capture command register</td>
<td>Generate a capture trigger input from software</td>
</tr>
<tr>
<td>TCPWM_CMD_RELOAD</td>
<td>TCPWM reload command register</td>
<td>Generate a reload trigger input from software</td>
</tr>
<tr>
<td>TCPWM_CMD_STOP</td>
<td>TCPWM stop command register</td>
<td>Generate a stop trigger input from software</td>
</tr>
<tr>
<td>TCPWM_CMD_START</td>
<td>TCPWM start command register</td>
<td>Generate a start trigger input from software</td>
</tr>
<tr>
<td>TCPWM_INTR_CAUSE</td>
<td>TCPWM counter interrupt cause</td>
<td>Determines the source of the combined interrupt signal</td>
</tr>
<tr>
<td>TCPWM_CNT_CTRL</td>
<td>Counter control register</td>
<td>Configures counter mode, encoding modes, one-shot mode, swap mode, kill mode, dead time, clock pre-scaling, and counting direction</td>
</tr>
<tr>
<td>TCPWM_CNT_STATUS</td>
<td>Counter status register</td>
<td>Reads the direction of counting, dead time duration, and clock pre-scaling; checks whether the counter is running</td>
</tr>
<tr>
<td>TCPWM_CNT_COUNTER</td>
<td>Count register</td>
<td>Contains the 16- or 32-bit counter value</td>
</tr>
<tr>
<td>TCPWM_CNT_CC</td>
<td>Counter compare/capture register</td>
<td>Captures the counter value or compares the value with counter value</td>
</tr>
<tr>
<td>TCPWM_CNT_CC_BUFF</td>
<td>Counter buffered compare/capture</td>
<td>Buffer register for counter CC register; swaps period value</td>
</tr>
<tr>
<td>TCPWM_CNT_PERIOD</td>
<td>Counter period register</td>
<td>Contains upper value of the counter</td>
</tr>
<tr>
<td>TCPWM_CNT_PERIOD_BUFF</td>
<td>Counter buffered period register</td>
<td>Buffer register for counter period register; swaps compare value</td>
</tr>
<tr>
<td>TCPWM_CNT_TR_CTRL0</td>
<td>Counter trigger control register 0</td>
<td>Selects trigger for specific counter events</td>
</tr>
<tr>
<td>TCPWM_CNT_TR_CTRL1</td>
<td>Counter trigger control register 1</td>
<td>Determine edge detection for specific counter input signals</td>
</tr>
<tr>
<td>TCPWM_CNT_TR_CTRL2</td>
<td>Counter trigger control register 2</td>
<td>Controls counter output lines upon CC, OV, and UN conditions</td>
</tr>
<tr>
<td>TCPWM_CNT_INTR</td>
<td>Interrupt request register</td>
<td>Sets the register bit when TC or CC condition is detected</td>
</tr>
<tr>
<td>TCPWM_CNT_INTR_SET</td>
<td>Interrupt set request register</td>
<td>Sets the corresponding bits in interrupt request register</td>
</tr>
<tr>
<td>TCPWM_CNT_INTR_MASK</td>
<td>Interrupt mask register</td>
<td>Mask for interrupt request register</td>
</tr>
<tr>
<td>TCPWM_CNT_INTR_MASKED</td>
<td>Interrupt masked request register</td>
<td>Bitwise AND of interrupt request and mask registers</td>
</tr>
</tbody>
</table>
28. Inter-IC Sound Bus

The Inter-IC Sound Bus (I²S) is a serial bus interface standard used to connect digital audio devices together. The specification is from Philips® Semiconductor (I²S bus specification: February 1986, revised June 5, 1996). In addition to the standard I²S format, the I²S block also supports the Left Justified (LJ) format and the Time Division Multiplexed (TDM) format.

28.1 Features

- Supports standard Philips I²S, LJ, and eight-channel TDM digital audio interface formats
- Supports both master and slave mode operation in all the digital audio formats
- Supports independent operation of Receive (Rx) and Transmit (Tx) directions
- Supports operating from an external master clock provided through an external IC such as audio codec
- Provides configurable clock divider registers to generate the required sample rates
- Supports data word length of 8-bit, 16-bit, 18-bit, 20-bit, 24-bit, and 32-bit per channel
- Supports channel length of 8-bit, 16-bit, 18-bit, 20-bit, 24-bit, and 32-bit per channel (channel length fixed at 32-bit in TDM format)
- Provides two hardware FIFO buffers, one each for the Tx block and Rx block, respectively
- Supports both DMA- and CPU-based data transfers

28.2 Architecture

Figure 28-1. I²S Block Diagram
Figure 28-1 shows the high-level block diagram of the I²S block, which consists of two sub-blocks – I²S Transmitter (Tx) and I²S Receiver (Rx). The digital audio interface format and master/slave mode configuration can be done independently for the Tx and Rx blocks. In the master mode, the word select (ws) and serial data clock (sck) are generated by the I²S block in the PSoC 6 MCU. In the slave mode, the ws and sck signals are inputs signals to the PSoC 6 MCU, and are generated by the external master device. The I²S block configuration, control, and status registers, along with the FIFO data buffers are accessible through the AHB bus. AHB bus masters such as CPU and DMA can access the I²S registers through the AHB interface. Refer to the device datasheet for information on port pin assignments of the I²S block signals and AC/DC electrical specifications.

### 28.3 Digital Audio Interface Formats

The I²S block supports the following digital audio interface formats:

- Standard I²S format
- Left Justified format
- Time Division Multiplexed (TDM) format

The Tx and Rx sub-blocks can be independently configured to support one of the above formats in either master or slave mode. The I2S_MODE bits in the I2S_TX_CTL and I2S_RX_CTL registers are used to configure the digital audio interface format for the Tx and Rx blocks respectively. The MS (Master/Slave) bit in the I2S_TX_CTL and I2S_RX_CTL registers is used to configure the blocks in master or slave mode.

#### 28.3.1 Standard I²S Format

Figure 28-2 shows the timing diagrams for the different word length and channel length combinations in the standard I²S digital audio format. In the standard I²S format, the word select signal (ws) is low for left channel data, and high for right channel data. The ws signal transitions one bit-clock (sck) early relative to the start of the left/right channel data. All the serial data (sd), ws signal transitions on the falling edge of the sck signal, and the read operations on the ws and sd lines are usually done on the rising edge of sck. Therefore, the I²S Tx block writes to the serial data (tx_sdo) line on the falling edge of tx_sck, and the I²S Rx block reads the data (rx_sdi) on the rising edge of rx_sck. The serial data is transmitted most significant bit (MSb) first. Depending on whether the block is in master or slave mode, the ws/sck signals are either generated by the block (master mode) or input signals to the block (slave mode).

The I²S block supports configurable word length and channel length selection options. The word length for the Tx and Rx blocks can be configured using the WORD_LEN bits in the I2S_TX_CTL and I2S_RX_CTL registers, respectively. The channel length for the Tx and Rx blocks can be configured using the CH_LEN bits in the I2S_TX_CTL and I2S_RX_CTL registers respectively. The channel length configuration should always be greater than or equal to the word length configuration. Ensure that when the I²S Rx block is operated in slave mode, the master Tx device ensures that its channel length configuration aligns with the I²S Rx block channel length setting. If there is channel length mismatch, the PSoC I²S Rx block in slave mode will not operate correctly.

In the Tx block, when the channel length is greater than the word length, the unused bits can be transmitted either as ‘0’ or ‘1’. This selection is made using the OVHDATA bit in the I2S_TX_CTL register. In the Rx block, when the word length is less than 32 bits, the unused most significant bits written to the 32-bit Rx FIFO register can either be set to ’0’ or sign bit extended. This selection is made using the BIT_EXTENSION bit in the I2S_RX_CTL register.
Table 28-1 lists the supported word length and channel length combinations.
28.3.2 Left Justified (LJ) Format

Figure 28-3 shows the timing diagrams for the Left Justified interface format using the 32-bit channel length and 32-bit word length configuration as an example. The only differences between the standard I2S and LJ formats are:

- In the standard I2S format, WS signal is low for left channel data and high for right channel data. In the LJ format, WS signal is high for left channel data and low for right channel data.

- In the standard I2S format, WS signal transitions one bit-clock (sck) early relative to the start of the channel data (coincides with LSB of the previous channel). In the LJ format, there is no early transition, and the WS signal transitions coincide with the start of the channel data.

Apart from these differences, all the features explained in the standard I2S format section apply to the LJ format as well.

28.3.3 Time Division Multiplexed (TDM) Format

Figure 28-4 shows the timing diagrams for the two types of Time Division Multiplexed (TDM) formats supported by the I2S block. The differences between the standard I2S/LJ formats and the TDM format are as follows:

- Standard I2S/LJ formats support only two channels (left/right) per frame, while TDM format supports up to eight channels per frame.

- In the TDM format, channel length for all eight channels is fixed at 32 bits. In the standard I2S/LJ formats, the channel length is configurable. The word length per channel is configurable similar to the standard I2S and the data is also transmitted most significant bit first. Similar to I2S, when the word length per channel is less than the 32-bit channel length for Tx block, the OVHDATA bit in the I2S_TX_CTL register is used to fill the unused least significant channel data bits with either all zeros or all ones.

- In the TDM format, all eight channels of data are always present in a frame, and thus the frame width is fixed at 256 bits. You have the option to configure the number of active channels in a frame by configuring the CH_NR bits in the I2S_TX_CTL and I2S_RX_CTL registers. In the standard I2S/LJ format, the CH_NR should always be configured for two channels. The number of active channels in the TDM format can be less than or equal to eight channels. The unused (inactive) channels always follow the active channels in a frame. As an example, if CH_NR is set for four channels, CH0 to CH3 are the active channels and CH4 to CH7 are the unused channels. The OVHDATA bit in the I2S_TX_CTL register is used to fill the unused channels with either all zeros or all ones.

### Table 28-1. Word Length and Channel Length Combinations

<table>
<thead>
<tr>
<th>Word Length</th>
<th>8-bit</th>
<th>16-bit</th>
<th>18-bit</th>
<th>20-bit</th>
<th>24-bit</th>
<th>32-bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel Length</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>32-bit</td>
<td>Valid</td>
<td>Valid</td>
<td>Valid</td>
<td>Valid</td>
<td>Valid</td>
<td>Valid</td>
</tr>
<tr>
<td>24-bit</td>
<td>Valid</td>
<td>Valid</td>
<td>Valid</td>
<td>Valid</td>
<td>Valid</td>
<td>Invalid</td>
</tr>
<tr>
<td>30-bit</td>
<td>Valid</td>
<td>Valid</td>
<td>Valid</td>
<td>Valid</td>
<td>Invalid</td>
<td>Invalid</td>
</tr>
<tr>
<td>18-bit</td>
<td>Valid</td>
<td>Valid</td>
<td>Invalid</td>
<td>Invalid</td>
<td>Invalid</td>
<td>Invalid</td>
</tr>
<tr>
<td>16-bit</td>
<td>Valid</td>
<td>Invalid</td>
<td>Invalid</td>
<td>Invalid</td>
<td>Invalid</td>
<td>Invalid</td>
</tr>
<tr>
<td>8-bit</td>
<td>Valid</td>
<td>Invalid</td>
<td>Invalid</td>
<td>Invalid</td>
<td>Invalid</td>
<td>Invalid</td>
</tr>
</tbody>
</table>
The pulse width of the word select (WS) signal in the TDM format can be configured to be either one bit clock (sck) wide or one channel wide. The selection is made using the WS_PULSE bit in the I2S_TX_CTL and I2S_RX_CTL registers. The pulse width is fixed to one channel width in the I2S/LJ format.

Two types of TDM formats are supported. In TDM mode A, the WS rising edge signal to signify the start of frame coincides with the start of CH0 data. In TDM mode B, the WS rising edge signal to signify the start of frame is one bit clock (sck) early, relative to the start of CH0 data (coincides with the last bit of the previous frame). The selection between the two TDM formats is made using the I2S_MODE bits in the I2S_TX_CTL and I2S_RX_CTL registers.

Figure 28-4. TDM Digital Audio Interface Format

28.4 Clocking Polarity and Delay Options

The I²S block supports configurable clock polarity and delay options to alleviate any timing issues in the system involving PCB signal propagation delays, and delays associated with internal device signal routing.

When the I²S Tx block operates in the slave mode, the tx_sck and tx_ws signals are input signals to the PSoC 6 MCU, and the tx_sdo output signal is transmitted off the tx_sck falling edge. The tx_sdo signal is sampled by the external master device Rx block on the subsequent tx_sck rising edge. Timing issues arise if the tx_sdo signal reaching the master side Rx block does not meet the setup and hold time requirements for input data on the master side. The I²S Tx block in the PSoC 6 MCU has an option to advance the serial data transmission by 0.5 SCK cycles when the B_CLOCK_INV bit in the I2S_TX_CTL register is set. This feature can be used if there are timing issues while operating the I²S Tx block in slave mode.

Similarly, when the I²S Rx block operates in the master mode, the rx_sck and rx_ws signals are output signals from the PSoC 6 MCU, and the rx_sdi signal is transmitted by the external master device on the falling edge of rx_sck. The PSoC I²S Rx block samples the rx_sdi signal on the subsequent rx_sck rising edge. Timing issues arise if the rx_sdi signal reaching the PSoC block does not meet the setup and hold time requirements for input data. The I²S Rx block has an option to delay the serial data capture by 0.5 SCK cycles when the B_CLOCK_INV bit in the I2S_RX_CTL register is set. This feature can be used if there are timing issues while operating the I²S Rx block in master mode.

In addition to these clock delay options, there is also an option to invert the outgoing bit clock (sck) in master mode by setting the SCKO_POL bit in the I2S_TX_CTL and I2S_RX_CTL registers. Similarly, in the slave mode, there is an option to invert the incoming bit clock (sck) by setting the SCKI_POL bit in the I2S_TX_CTL and I2S_RX_CTL registers.

Refer to the PSoC 63 with BLE Registers TRM for detailed description of the B_CLOCK_INV, SCKI_POL, and SCKO_POL register configurations.
28.5 Interfacing with Audio Codecs

The I²S block in the PSoC 6 MCU interfaces with an audio codec device based on the choice of codec device and the end application requirements. Some scenarios and the connection diagrams are as follows:

- Codecs with separate ws and sck signals for the Rx and Tx directions: To interface with these codecs, the connections between the PSoC I²S block and the codec device will be as shown in Figure 28-1 where the PSoC I²S Tx signals (tx_sck, tx_ws, tx_sdo) connect to the codec Rx signals, and the PSoC I²S Rx signals (rx_sck, rx_ws, rx_sdi) connect to the codec Tx signals. The direction of sck (tx_sck, rx_sck) and ws (tx_ws, rx_ws) signals depends on which device is the master and which device is the slave.

- Codecs with common ws and sck signals for both Rx and Tx directions: There are two possible configurations to interface these codecs with the PSoC 6 MCU as shown in Figure 28-5. In both configurations, the sck signals (tx_sck, rx_sck, codec_sck) are shorted externally. The same goes for the ws signal connections as well (tx_ws, rx_ws, codec_ws). Ensure that only one block is driving the sck and ws lines. So when the codec acts as the slave device, the PSoC I²S Rx block should be in the master mode, and the PSoC I²S Tx block should be in the slave mode (or PSoC I²S Rx as slave and PSoC I²S Tx as master). When the codec acts as the master device, both the PSoC I²S Rx and PSoC I²S Tx blocks should be in slave mode.

28.6 Clocking Features

The I²S unit has three clock inputs.

Table 28-2. Clock Inputs

<table>
<thead>
<tr>
<th>Signal</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk_sys_i2s</td>
<td>System clock. This clock is used for the AHB slave Interface, control, status, and interrupt registers, and also clocks the DMA trigger control logic.</td>
</tr>
<tr>
<td>clk_audio_i2s</td>
<td>I²S internal clock. This clock is used for I²S transmitter (Tx)/receiver (Rx) blocks; it is asynchronous with the clk_sys_i2s. This clock is connected to the CLK_HF[1] high-frequency clock in the device. Refer to the Clocking System chapter on page 146 for more details on high frequency clocks.</td>
</tr>
<tr>
<td>clk_i2s_if</td>
<td>I²S external clock. This clock is provided from an external I²S bus host through a port pin. It is used in place of the clk_audio_i2s clock to synchronize I²S data to the clock used by the external I²S bus host.</td>
</tr>
</tbody>
</table>

Figure 28-6 shows the clocking divider structure in the I²S block. In the master mode, the sck and ws signals are generated either using the clk_audio_i2s internal clock or the clk_i2s_if external clock. Refer to the device datasheet for the port pin assignment of clk_i2s_if clock. The CLOCK_SEL bit in the I2S_CLOCK_CTL register controls the selection between internal and external clocks.
There are two stages of clock dividers in the I²S block as follows.

- The first stage clock divider is used to generate the internal I²S master clock (MCLK_SOC). The input clock to the first stage divider is either clk_audio_i2s or clk_i2s_if. The first stage clock divider is configured using the CLOCK_DIV bits in I2S_CLOCK_CTL register. Divider values from 1 to 64 are supported.

- The second stage clock divider is used to generate the sck signals. The input clock is the output from the first stage clock divider. This divider value is fixed at '8' (FTX_SCK = FRX_SCK = FMCLK_SOC/8). The word select (ws) signal frequency depends on the sck frequency, and the configured channel length value.

When in slave mode, the internal clock (MCLK_SOC) frequency should still be eight times the frequency of the input serial clock. You must choose the appropriate clock source and the CLOCK_DIV divider value to guarantee this condition is met in the slave mode of operation. Usually, when the PSoC I²S block operates in the slave mode, the host sends a master clock which is an integral multiple of the sampling rate. This master clock can be routed to the clk_i2s_if port pin. The CLOCK_DIV divider value can then be adjusted to ensure that the MCLK_SOC is eight times the input SCK frequency.

Table 28-3 gives an example of the clock divider settings for operating the I²S block at the standard sampling rates in the standard I²S format. Note that the first stage divider values in the table are the register field values – the actual divider values are one more than the configured register values as explained in the clock divider section. Refer to the device datasheet for details on maximum values of SCK frequency, and the output sampling rates.

<table>
<thead>
<tr>
<th>Sampling Rate (SR) (kHz)</th>
<th>WORD_LEN (bits)</th>
<th>SCK (2<em>WORD_LEN</em>SR) (MHz)</th>
<th>CLK_HF1 (or clk_i2s_if) (MHz)</th>
<th>(CLK_HF1) / SCK (Total Divider Ratio)</th>
<th>CLK_CLOCK_DIV (First Divider)</th>
<th>Second Stage Divider (Fixed at 8)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>32</td>
<td>0.512</td>
<td></td>
<td>96</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>32</td>
<td>1.024</td>
<td></td>
<td>48</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>32</td>
<td>2.048</td>
<td>49.152</td>
<td>24</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>48</td>
<td>32</td>
<td>3.072</td>
<td></td>
<td>16</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>44.1</td>
<td>32</td>
<td>2.8224</td>
<td>45.1584</td>
<td>32</td>
<td>3</td>
<td>8</td>
</tr>
</tbody>
</table>
28.7 FIFO Buffer and DMA Support

The i²S block has two FIFO buffers - one each for the Tx block and Rx block, respectively. The ordering format of the channel data in both Tx and Rx FIFOs depends on the configured digital audio format. This ordering format should be considered when writing to the Tx FIFO or reading from the Rx FIFO. In the standard i²S and LJ digital audio formats, the ordering of the data is (L, R, L, R, ...) where L refers to the left channel data and R refers to the right channel data. In the TDM format with the number of active channels set to four, the data order will be (CH0, CH1, CH2, CH3, CH0, CH1, CH2, CH3, CH0, ...). If the number of active channels is set to eight, the cycle will repeat after CH0–CH7 data.

i²S Tx FIFO: The i²S Tx block has a hardware FIFO of depth 256 elements where each element is 32-bit wide. In addition to this 256-element FIFO, the i²S block has an internal transmit buffer that can store four 32-bit data to be transmitted. This four-element buffer is used as an intermediary to hold data to be transferred on the i²S bus, and is not exposed to the AHB BUS interface.

The I2S_TX_FIFO_CTL register is used for FIFO control operations. The TRIGGER_LEVEL bits in the I2S_TX_FIFO_CTL register can be used to generate a transmit trigger event when the Tx FIFO has less entries than the value configured in the TRIGGER_LEVEL bits.

The FIFO freeze operation can be enabled by setting the FREEZE bit in the I2S_TX_FIFO_CTL register. When the FREEZE bit is set and the Tx block is operational (TX_START bit in I2S_CMD is set), hardware reads from the Tx FIFO do not remove the FIFO entries. Also, the Tx FIFO read pointer will not be advanced. Any writes to the I2S_TX_FIF0 register will increment the Tx FIFO write pointer; when the Tx FIFO becomes full, the internal write pointer stops incrementing. The freeze operation may be used for firmware debug purposes. This operation is not intended for normal operation. To return to normal operation after using the freeze operation, the i²S must be reset by clearing the TX_ENABLED bit in the I2S_CTL register, and then setting the bit again.

The CLEAR bit in the I2S_TX_FIFO_CTL register is used to clear the Tx FIFO by resetting the read/write pointers associated with the FIFO. Write accesses to the Tx FIFO using the I2S_TX_FIFO_WR or I2S_TX_FIFO_WR_SILENT registers are not allowed while the CLEAR bit is set.

The I2S_TX_FIFO_STATUS register provides FIFO status information. This includes number of used entries in the Tx FIFO and the current values of the Tx FIFO read/write pointers. This register can be used for debug purposes. The i²S Tx FIFO read pointer is updated whenever the data is transferred from the Tx FIFO to the internal transmit buffer. Tx FIFO write pointer is updated whenever the data is written to the I2S_TX_FIFO_WR register, either through the CPU or the DMA controller.

For Tx FIFO data writes using the CPU, the hardware can be used to trigger an interrupt event for any of the FIFO conditions such as TX_TRIGGER, TX_NOT_FULL, and TX_EMPTY. As part of the interrupt handler, the CPU can write to the I2S_TX_FIFO_WR register. The recommended method is to write (256 - TRIGGER_LEVEL) words to the I2S_TX_FIFO_WR register every time the TX_TRIGGER interrupt event is triggered. In addition, interrupt events can be generated for FIFO overflow/underflow conditions.

For DMA-based Tx data transfers, the i²S Tx DMA trigger signal (tr_i2s_tx_req) can be enabled by writing ‘1’ to the TX_REQ_EN bit in I2S_TR_CTL register. The trigger signal output will become high whenever the Tx FIFO has less entries than that configured in the TRIGGER_LEVEL field. The DMA channel can be configured to transfer up to (256 - TRIGGER_LEVEL) words from the applicable source address (such as Flash and SRAM regions). The destination address of the DMA should always be the I2S_TX_FIFO_WR register address, with the destination address increment feature disabled in the DMA channel configuration. This FIFO address increment logic is handled internally to adjust the write pointer, and the DMA should not increment the destination address. For more details on DMA channel configuration, refer to the DMA Controller chapter on page 72.

The data in the I2S_TX_FIFO is always right-aligned. The I2S_TX_FIFO_WR format for different word length configurations is provided in Figure 28-7.

<table>
<thead>
<tr>
<th>Word Length = 24-bit mode</th>
<th>Word Length = 20-bit mode</th>
<th>Word Length = 18-bit mode</th>
<th>Word Length = 16-bit mode</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>fixed “0”</td>
<td>fixed “0”</td>
<td>fixed “0”</td>
</tr>
<tr>
<td>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
<td>19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
<td>15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
<td>15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
</tr>
<tr>
<td></td>
<td>MSb</td>
<td>MSb</td>
<td>MSb</td>
</tr>
<tr>
<td></td>
<td>LSb</td>
<td>LSb</td>
<td>LSb</td>
</tr>
</tbody>
</table>

Figure 28-7. I2S_TX_FIFO_WR Register Format for Different Word Lengths
I²S Rx FIFO: The I²S Rx block has a hardware FIFO of depth 256 elements where each element is 32-bit wide. In addition to this 256-element FIFO, the I²S block has an internal receive buffer that can store four 32-bit data to be received. This four-element buffer is used as an intermediary to hold data received on the I²S bus, and is not exposed to the AHB BUS interface.

The I2S_RX_FIFO_CTL register is used for FIFO control operations. The TRIGGER_LEVEL bits in the I2S_RX_FIFO_CTL register is used to generate a receive trigger event when the Rx FIFO has more entries than the value configured in the TRIGGER_LEVEL bits. In the standard I²S/LJ format, the TRIGGER_LEVEL bits can be configured up to the allowed maximum value of 253. In the TDM format, the maximum value of TRIGGER_LEVEL is (254−CH_NR) where CH_NR is the number of active channels in the TDM frame.

The FIFO freeze operation can be enabled by setting the FREEZE bit in the I2S_RX_FIFO_CTL register. When the FREEZE bit is set and the Rx block is operational (RX_START bit in the I2S_CMD register is set), hardware will not write to the Rx FIFO. Also, the Rx FIFO write pointer will not be advanced. Any reads from the I2S_RX_FIFO register will increment the Rx FIFO read pointer; when the Rx FIFO becomes empty, the internal read pointer stops incrementing. The freeze operation may be used for firmware debug purposes. This operation is not intended for normal operation. To return to normal operation after using the freeze operation, the I²S must be reset by clearing the RX_ENABLED bit in the I2S_CTL register and then setting the bit again.

The CLEAR bit in I2S_RX_FIFO_CTL register is used to clear the Rx FIFO by resetting the read/write pointers associated with the FIFO. Read accesses from the Rx FIFO using the I2S_RX_FIFO_RD or I2S_RX_FIFO_RD_SILENT registers are not allowed while the CLEAR bit is set.

The I2S_RX_FIFO_STATUS register provides FIFO status information. This includes number of used entries in the Rx FIFO and the current values of the Rx FIFO read/write pointers. This register can be used for debug purposes. The I²S Rx FIFO write pointer is updated whenever the data is transferred to the Rx FIFO from the internal receive buffer. Rx FIFO read pointer is updated whenever the data is read from the I2S_RX_FIFO_RD register, either through the CPU or the DMA controller. For debug purposes, the I2S_RX_FIFO_RD_SILENT register is available, which always returns the top element of the Rx FIFO without updating the read pointer.

For Rx FIFO data reads using the CPU, the hardware can be used to trigger an interrupt event for any of the FIFO conditions such as RX_TRIGGER, RX_NOT_EMPTY, and RX_FULL. As part of the interrupt handler, the CPU can read from the I2S_RX_FIFO_RD register. The recommended method is to read (TRIGGER_LEVEL + 1) words from the I2S_RX_FIFO_RD register every time the RX_TRIGGER interrupt event is triggered. In addition, interrupt events can be generated for FIFO overflow/underflow conditions.

For DMA-based Rx data transfers, the I²S Rx DMA trigger signal (tr_i2s_rx_req) can be enabled by writing ‘1’ to the RX_REQ_EN bit in the I2S_TR_CTL register. The trigger signal output will become high whenever the Rx FIFO has more entries than that configured in the TRIGGER_LEVEL field. The DMA channel can be configured to transfer up to (TRIGGER_LEVEL + 1) words to the applicable destination address (such as SRAM regions). The source address of the DMA should always be the I2S_RX_FIFO_RD register address, with the source address increment feature disabled in the DMA channel configuration. This FIFO address increment logic is handled internally to adjust the read pointer, and the DMA should not increment the source address. For more details on DMA channel configuration, refer to the DMA Controller chapter on page 72.

The data in the I2S_RX_FIFO is always right aligned. The I2S_RX_FIFO_RD format for different word length configurations is provided in Figure 28-8. Note that the unused most significant bits are either set as ‘0’ or sign-bit extended depending on the BIT_EXTENSION bit in the I2S_RX_CTL register.
28.8 Interrupt Support

The I2S block has one interrupt output signal that goes to the interrupt controller in the CPU. Refer to the Interrupts chapter on page 47 for details on the vector number of the I2S interrupt and the procedure to configure the interrupt priority, vector address, and enabling/disabling. The I2S interrupt can be triggered under any of the following events - TX_TRIGGER, TX_NOT_FULL, TXEMPTY, TX_OVERFLOW, TX_UNDERFLOW, TX_UD, RX_TRIGGER, RX_NOT_EMPTY, RX_FULL, RX_OVERFLOW, RX_UNDERFLOW, or RX_WD. Each of the interrupt events can be individually enabled/disabled to generate an interrupt condition. The I2S_INTR_MASK register is used to enable the required events by writing '1' to the corresponding bit. Irrespective of the INTR_MASK settings, if any of the events occur, the corresponding event status bit will be set by the hardware in the I2S_INTR register. The I2S_INTR_MASKED register is the bitwise AND of the I2S_INTR_MASK and I2S_INTR registers. The final I2S interrupt signal is the logical OR of all the bits in the I2S_INTR_MASKED register. So only those events that are enabled in the I2S_INTR_MASK register are propagated as interrupt events to the interrupt controller. Interrupts can also be triggered in software by writing to the corresponding bits in I2S_INTR_SET register. Figure 28-9 illustrates the interrupt signal generation.
In the interrupt service routine (ISR), the I2S_INTR_MASKED register should be read to know the events that triggered the interrupt event. Multiple events can trigger the interrupt because the final interrupt signal is the logical OR output of the events. The ISR should do the tasks corresponding to each interrupt event that was triggered. At the end of the ISR, the value read in the I2S_INTR_MASKED register earlier should be written to the I2S_INTR register to clear the bits whose interrupt events were processed in the ISR. Unless the bits are not cleared by writing ‘1’ to the I2S_INTR register, the interrupt signal will always be high. A dummy read of the I2S_INTR register should be done for the earlier register write to take effect.

### 28.9 Watchdog Timer

The Tx and Rx blocks have independent watchdog timers, which can be used to generate an interrupt event if the Word Select (WS) input is idle for more than the configured time period. This feature is available only in the slave mode of operation where the external master drives the WS input lines (tx_ws, rx_ws). This feature can be used to detect any signal transmission issues, master device issues, or if the master has halted communication. If the master drives the same word select signal to both the tx_ws and rx_ws lines, then only one of the watchdog timers can be enabled to cause the interrupt event. Although the following explanation covers Tx watchdog, the same explanation applies to Rx watchdog as well.

To enable the Tx watchdog timer feature, WD_EN bit in the I2S_TX_CTL register should be set. The watchdog timer reload value (32-bit timer) is configured by writing to the I2S_TX_WATCHDOG register. A value of zero written to the I2S_TX_WATCHDOG register will also disable the watchdog timer. Figure 28-10 illustrates the watchdog behavior when the timer is enabled. The timer runs off the CLK_PERI system clock. Refer to the Clocking System chapter on page 146 for details on generation of CLK_PERI. The timer starts running when WD_EN and TX_START bits are set. The timer reload happens either on a rising edge event on tx_ws input signal, or when the timer values reaches zero. When the timer value reaches zero, the TX_WD interrupt event is generated. The TX_WD bit in the I2S_INTR register should be set to enable interrupt generation by the watchdog timer interrupt event. The interrupt event can be cleared by writing ‘1’ to the TX_WD bit in the I2S_INTR register.

![Watchdog Timer Working](image)
29. PDM-PCM Converter

The PDM-PCM unit accepts a stereo or mono serial data stream (pulse modulated 1-bit stream) coming from external digital PDM microphones. The PDM-PCM converter consists of a fifth order cascaded integrator comb (CIC) filter followed by a decimator, and a final stage high-pass filter. This block simplifies the conversion process by exposing the different configuration settings as registers, which you can program to meet the application needs. The entire PDM-PCM conversion process is handled in hardware; the PCM output data streaming can be done using the DMA controller thus freeing up the CPU bandwidth from performing periodic audio streaming activities.

29.1 Features

- Supports Mono/Stereo mode pulse density modulation (PDM) to pulse code modulation (PCM) conversion
- Accepts 1-bit PDM input and can generate 16-, 18-, 20-, or 24-bit PCM digital data output
- Configurable PDM microphone clock frequency
- Ability to generate standard audio sampling rates by adjusting the decimation rate and clock divider values
- Digital volume control: Programmable gain amplifier (PGA) control from −12 dB to +10.5 dB in 1.5-dB steps
- Smooth PGA and soft-mute control
- Hardware receive buffer: 24-bit wide, 255-element FIFO with support for DMA controller-based data transfer
- Optional high-pass filter to remove DC and low-frequency noise

29.2 Architecture

Figure 29-1 shows the block diagram of the PDM-PCM converter. Refer to the device datasheet for information on port pin assignments of the PDM block signals, electrical specifications, and the interrupt vector number.
29.2.1 Enable/Disable Converter

The PDM-PCM converter can be powered ON or OFF by using the ENABLED bit in the PDM_CTL register. The block can be turned OFF when not used to save power. When the block is powered off by writing ‘0’ to the ENABLED bit, the non-retention registers lose their current values. Refer to the PSoC 63 with BLE Registers TRM to know which registers are retention and non-retention type. When the block is enabled again, the non-retention registers are reset to their default values. User firmware should ensure that all non-retention registers are configured as required after the ENABLED bit is set, and before the PDM-PCM conversion is started by setting the STREAM_EN bit in the PDM_CMD register. See Operating Procedure on page 324 for the recommended procedure to configure this PDM-PCM converter before starting the PDM-PCM conversion.

29.2.2 Clocking Features

The block uses the CLK_HF[1] root high-frequency clock for performing the PDM-PCM conversion process. Refer to the Clocking System chapter on page 146 for details on selecting the clock source for CLK_HF[1], and configuring the divider registers to generate CLK_HF[1].

Figure 29-2 shows the clock divider structure in the block. The block has three stages of clock dividers to generate the clock (PDM_CKO), which goes to the external PDM microphone clock input.

1. The first stage clock divider (CLK_CLOCK_DIV field in the PDM_CLOCK_CTL register) is used to generate the actual clock signal (PDM_CLK) that goes to the PDM-PCM converter. The input is CLK_HF[1]; the CLK_CLOCK_DIV can be a value between 0 and 3 (divider value between 1 and 4).

   \[ f_{PDM\_CLK} = \frac{f_{CLK\_HF[1]}}{(CLK\_CLOCK\_DIV + 1)} \]

2. The second stage clock divider (MCLKQ_CLOCK_DIV field in the PDM_CLOCK_CTL register) is used to generate the internal master clock and can take a value between 0 and 3 (divider value between 1 and 4). The input clock is pdm_clk and the output of the divider is MCLKQ.

   \[ f_{MCLKQ} = \frac{f_{PDM\_CLK}}{(MCLKQ\_CLOCK\_DIV + 1)} \]

3. The third stage clock divider (CKO_CLOCK_DIV field in the PDM_CLOCK_CTL register) is used to generate the clock that goes to the PDM microphone clock (PDM_CKO) through the output pin of the PSoC 6 MCU. The input clock is MCLKQ. The divider register can be between 1 and 15 (divider value between 2 and 16).

   \[ f_{PDM\_CKO} = \begin{cases} f_{MCLKQ} / (CKO\_CLOCK\_DIV + 1), & \text{if } CKO\_CLOCK\_DIV \geq 1 \\ f_{MCLKQ} / 2, & \text{if } CKO\_CLOCK\_DIV = 0 \end{cases} \]

29.2.3 Over-Sampling Ratio

Over-sampling ratio (OSR) is the ratio between the frequency of the PDM microphone clock \( f_{PDM\_CKO} \) and the output PCM sampling rate frequency \( f_S \). The OSR is determined by the SINC_RATE bits in the PDM_CLOCK_CTL register. The relation is as follows.

\[ \text{OSR} = \frac{f_{PDM\_CKO}}{f_S} = 2 \times \text{SINC\_RATE} \]

Table 29-1 gives an example of the PDM clock divider and SINC_RATE register configurations to generate the PCM output at standard sampling rates. Note that the PDM divider values in the table are the register field values – the actual divider values are one more than the configured register values as explained in the clock divider section. Refer to the device datasheet for details on maximum values of PDM_CKO frequency, PDM_CLK frequency, and the output sampling rates.
There are various methods to generate the \( \text{CLK}_{\text{HF}[1]} \) frequencies listed in the table depending on the clocking options available on the device. Refer to the Clocking System chapter on page 146 for details on the clocking options available in the device, including the clock sources and PLL/FLL circuitry. For example, an external crystal oscillator (ECO) can be used in conjunction with a phase-locked loop (PLL) to generate the \( \text{CLK}_{\text{HF}[1]} \) at the desired frequency of 49.152 MHz or 45.1584 MHz.

One possible combination of PLL divider values to generate the 49.152 MHz frequency from a 17.2032 MHz ECO are: \( \text{REFERENCE\_DIV} = 7, \text{FEEDBACK\_DIV} = 100, \text{OUTPUT\_DIV} = 5 \). One possible combination of PLL divider values to generate the 45.1584 MHz frequency from a 17.2032 MHz ECO are: \( \text{REFERENCE\_DIV} = 8, \text{FEEDBACK\_DIV} = 105, \text{OUTPUT\_DIV} = 5 \).

### 29.2.4 Mono/Stereo Microphone Support

The PDM-PCM converter supports mono-left, mono-right, stereo, and swapped stereo modes of operation. The operation mode is controlled by the \text{PCM\_CH\_SET} and \text{SWAP\_LR} bits in the \text{PDM\_MODE\_CTL} register. The register settings for the different operation modes are given in Table 29-2. The table also lists the invalid register settings, which you must not use in the firmware.

### Table 29-1. PDM Clock Divider Values for Standard Audio Sampling Rates

<table>
<thead>
<tr>
<th>Sampling Rate (SR) (kHz)</th>
<th>SINC_RATE (= OSR/2)</th>
<th>PDM_CKO (=2*SINC_RATE*SR) (MHz)</th>
<th>CLK_HF1 (MHz)</th>
<th>( \frac{(\text{CLK}_\text{HF}[1])/(\text{PDM}_\text{CKO})}{(\text{Total Divider Ratio})} )</th>
<th>( \text{CLK_CLOCK_DIV} ) (First Divider)</th>
<th>( \text{MCLKQ_CLOCK_DIV} ) (Second Divider)</th>
<th>( \text{CKO_CLOCK_DIV} ) (Third Divider)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>32</td>
<td>0.512</td>
<td>49.152</td>
<td>96</td>
<td>1</td>
<td>3</td>
<td>11</td>
</tr>
<tr>
<td>16</td>
<td>32</td>
<td>1.024</td>
<td></td>
<td>48</td>
<td>1</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>32</td>
<td>32</td>
<td>2.048</td>
<td></td>
<td>24</td>
<td>0</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>48</td>
<td>32</td>
<td>3.072</td>
<td></td>
<td>16</td>
<td>0</td>
<td>1</td>
<td>7</td>
</tr>
<tr>
<td>44.1</td>
<td>32</td>
<td>2.8224</td>
<td>45.1584</td>
<td>32</td>
<td>0</td>
<td>1</td>
<td>7</td>
</tr>
</tbody>
</table>

There are various methods to generate the \( \text{CLK}_{\text{HF}[1]} \) frequencies listed in the table depending on the clocking options available on the device. Refer to the Clocking System chapter on page 146 for details on the clocking options available in the device, including the clock sources and PLL/FLL circuitry. For example, an external crystal oscillator (ECO) can be used in conjunction with a phase-locked loop (PLL) to generate the \( \text{CLK}_{\text{HF}[1]} \) at the desired frequency of 49.152 MHz or 45.1584 MHz.

One possible combination of PLL divider values to generate the 49.152 MHz frequency from a 17.2032 MHz ECO are: \( \text{REFERENCE\_DIV} = 7, \text{FEEDBACK\_DIV} = 100, \text{OUTPUT\_DIV} = 5 \). One possible combination of PLL divider values to generate the 45.1584 MHz frequency from a 17.2032 MHz ECO are: \( \text{REFERENCE\_DIV} = 8, \text{FEEDBACK\_DIV} = 105, \text{OUTPUT\_DIV} = 5 \).

### Table 29-2. Operation Mode Register Settings

<table>
<thead>
<tr>
<th>Register Setting</th>
<th>Operation Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>\text{PCM_CH_SET} = 0, SWAP_LR = 0 or 1</td>
<td>Recording OFF</td>
</tr>
<tr>
<td>\text{PCM_CH_SET} = 1, SWAP_LR = 0</td>
<td>Mono-Left recording mode. Only the left microphone channel is sampled on the rising edge of PDM_CKO. FIFO buffer contains only left channel data.</td>
</tr>
<tr>
<td>\text{PCM_CH_SET} = 2, SWAP_LR = 1</td>
<td>Mono-Right recording mode. Only the right microphone channel is sampled on the falling edge of PDM_CKO. FIFO buffer contains only right channel data.</td>
</tr>
<tr>
<td>\text{PCM_CH_SET} = 3, SWAP_LR = 0</td>
<td>Stereo recording mode. The right microphone channel is sampled on the falling edge of PDM_CKO and left channel on rising edge. FIFO buffer contains data in L/R format (left channel followed by right channel)</td>
</tr>
<tr>
<td>\text{PCM_CH_SET} = 3, SWAP_LR = 1</td>
<td>Swapped Stereo recording mode. The right microphone channel is sampled on the rising edge of PDM_CKO and left channel on falling edge. FIFO buffer contains data in L/R format (left channel followed by right channel)</td>
</tr>
<tr>
<td>\text{PCM_CH_SET} = 1, SWAP_LR = 1 or \text{PCM_CH_SET} = 2, SWAP_LR = 0</td>
<td>Invalid setting (not supported). Do not operate the PDM-PCM converter in these configuration settings.</td>
</tr>
</tbody>
</table>

Figure 29-3 shows the timing diagrams for the different operating modes.
To alleviate uncertain board delay impact on PDM_IN setup and hold timing constraints, the PDM-PCM provides CKO_DELAY bits in the PDM_MODE_CTL register to add extra delay for the PDM_CKO path to internal sampler. CKO_DELAY can be a value between 0 and 7. A value of ‘0’ implies that internal sampling of PDM data is advanced by three PDM_CLK clock cycles for the PDM_CKO transition. A value of ‘7’ implies that internal sampling of PDM data is delayed by four PDM_CLK clock cycles for the PDM_CKO transition. Refer to the PSoC 63 with BLE Registers TRM for details on the meaning of different CKO_DELAY values.

Note: Variations have been observed in the recommendation for left/right sampling logic among the different PDM microphone manufacturers. The SWAP_LR bit in the PDM-PCM converter ensures that you can adjust the sampling logic according to the microphone datasheet recommendations. Refer to the PDM microphone manufacturer datasheet for the exact timing details. Also, in stereo mode, use the same manufacturer for both the left/right PDM microphones to ensure the timing behavior is uniform for both channels.

29.2.5 Hardware FIFO Buffers and DMA Controller Support

The PDM-PCM converter has a hardware FIFO depth of 255 elements where each element is 24-bit wide.

The PDM_RX_FIFO_CTL register is used for FIFO control operations. Refer to the register description in the PSoC 63 with BLE Registers TRM for more details. The TRIGGER_LEVEL field in the PDM_RX_FIFO_CTL register is used to generate a receive trigger event (interrupt event, DMA trigger signal) when the Rx FIFO has more entries than the value configured in the TRIGGER_LEVEL field. The TRIGGER_LEVEL field can be configured up to 254 in the mono microphone recording mode and up to 253 in the stereo microphone recording mode.

The FIFO freeze operation can be enabled by setting the FREEZE bit in the PDM_RX_FIFO_CTL register. When the FREEZE bit is set and the Rx block is operational (STREAM_EN bit in the PDM_CMD register is set), hardware will not write to the Rx FIFO. Also, the Rx FIFO write pointer will not be advanced. Any reads from the PDM_RX_FIFO_RD register will increment the Rx FIFO read pointer; when the Rx FIFO becomes empty, the internal read pointer stops incrementing. The freeze operation may be used for firmware debug purposes. This operation is not intended for normal operation. To return to normal operation after using the freeze operation, the PDM-PCM must be reset by clearing the ENABLED bit in PDM_CTL register, and then setting the bit again.

The CLEAR bit in the PDM_RX_FIFO_CTL register is used to clear the Rx FIFO by resetting the read/write pointers associated with the FIFO. Read accesses from the Rx FIFO using PDM_RX_FIFO_RD or PDM_RX_FIFO_RD_SILENT registers are not allowed while the CLEAR bit is set.

The PDM_RX_FIFO_STATUS register provides FIFO status information. This includes number of used entries in the Rx FIFO and the current values of the Rx FIFO read/write pointers. This register can be used for debug purposes. The Rx FIFO write pointer is updated whenever the data is transferred to the Rx FIFO from the internal receive buffer. Rx FIFO read pointer is updated whenever the data is read from the PDM_RX_FIFO_RD register, either through the CPU or the DMA controller. For debug purposes, the PDM_RX_FIFO_RD_SILENT register is available, which
always returns the top element of the Rx FIFO without updating the read pointer.

For Rx FIFO data reads using the CPU, the hardware can be used to trigger an interrupt event for any of the FIFO conditions such as RX_TRIGGER and RX_NOT_EMPTY. As part of the interrupt handler, the CPU can read from the PDM_RX_FIFO_RD register. The recommended method is to read \((\text{TRIGGER\_LEVEL} + 1)\) words from the PDM_RX_FIFO_RD register every time the RX_TRIGGER interrupt event is triggered. In addition, interrupt events can be generated for FIFO overflow and underflow conditions.

For DMA-based data transfers, the DMA trigger signal \((\text{tr\_pdm\_rx\_req})\) can be enabled by writing ‘1’ to the RX_REQ_EN bit in the PDM_TR_CTL register. The trigger signal output will become high whenever the Rx FIFO has more entries than that configured in the TRIGGER_LEVEL field. Refer to the Trigger Multiplexer Block chapter on page 197 for details on how to connect the DMA trigger signal to a particular DMA channel. The DMA channel can be configured to transfer up to \((\text{TRIGGER\_LEVEL} + 1)\) words to the applicable destination address (such as SRAM regions). The source address of the DMA should always be the PDM_RX_FIFO_RD register address, with the source address increment feature disabled in the DMA channel configuration. This FIFO address increment logic is handled internally to adjust the read pointer, and the DMA should not increment the source address. For more details on DMA channel configuration, refer to the DMA Controller chapter on page 72.

The successive data read from the PDM_RX_FIFO_RD follows the Left 1/Right 1/Left 2/Right 2/… format in stereo and swapped stereo modes of operation. For mono left and mono right recording modes, the data read from FIFO contains either the left channel data (mono left mode) or the right channel data (mono right mode).

The data in the PDM_RX_FIFO_RD is always right-aligned. The PDM_TX_FIFO_RD format for different word length configurations is provided in Figure 29-4. Note that the unused most significant bits are either set as ‘0’ or sign-bit extended depending on the BIT_EXTENSION field setting in the PDM_DATA_CTL register.


data format of PDM_RX_FIFO

<table>
<thead>
<tr>
<th>WORD_LEN = 24-bit mode</th>
<th>bit_extension = 0</th>
<th>bit_extension = 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>fixed &quot;0&quot;</td>
<td>23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
<td></td>
</tr>
<tr>
<td>bit_extension = 1 (sign bit extension)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>&quot;1&quot; &quot;1&quot; &quot;1&quot; &quot;1&quot; &quot;1&quot; &quot;1&quot; &quot;1&quot; &quot;1&quot; &quot;1&quot; &quot;1&quot; &quot;1&quot; &quot;1&quot; &quot;1&quot; &quot;1&quot; &quot;1&quot; &quot;1&quot;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>&quot;0&quot; &quot;0&quot; &quot;0&quot; &quot;0&quot; &quot;0&quot; &quot;0&quot; &quot;0&quot; &quot;0&quot; &quot;0&quot; &quot;0&quot; &quot;0&quot; &quot;0&quot; &quot;0&quot; &quot;0&quot; &quot;0&quot; &quot;0&quot;</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>WORD_LEN = 20-bit mode</th>
<th>bit_extension = 0</th>
<th>bit_extension = 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>fixed &quot;0&quot;</td>
<td>19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
<td></td>
</tr>
<tr>
<td>bit_extension = 1 (sign bit extension)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>&quot;1&quot; &quot;1&quot; &quot;1&quot; &quot;1&quot; &quot;1&quot; &quot;1&quot; &quot;1&quot; &quot;1&quot; &quot;1&quot; &quot;1&quot; &quot;1&quot; &quot;1&quot; &quot;1&quot; &quot;1&quot; &quot;1&quot; &quot;1&quot;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>&quot;0&quot; &quot;0&quot; &quot;0&quot; &quot;0&quot; &quot;0&quot; &quot;0&quot; &quot;0&quot; &quot;0&quot; &quot;0&quot; &quot;0&quot; &quot;0&quot; &quot;0&quot; &quot;0&quot; &quot;0&quot; &quot;0&quot; &quot;0&quot;</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

29.2.6 Interrupt Support

The block has one output signal (interrupt_pdm) that goes to the interrupt controller in the CPU. Refer to the device datasheet for details on the vector number of the PDM-PCM interrupt. Refer to the Interrupts chapter on page 47 for the procedure to configure the interrupt priority, vector address, and enabling/disabling.

The PDM interrupt can be triggered under any of the following events – RX_TRIGGER, RX_NOT_EMPTY, RX_OVERFLOW, or RX_UNDERFLOW. Table 29-3 lists the trigger conditions and details of these events.
Each of the interrupt events can be individually enabled or disabled to generate the interrupt condition. The PDM_INTR_MASK register is used to enable the required events by writing ‘1’ to the corresponding bit.

Irrespective of the INTR_MASK settings, if any event occurs, the corresponding event status bit will be set by the hardware in the PDM_INTR register. The PDM_INTR_MASKED register is the bitwise AND of the PDM_INTR_MASK and PDM_INTR registers. The final PDM interrupt signal is the logical OR of all the bits in the PDM_INTR_MASKED register. So only those events that are enabled in the PDM_INTR_MASK register are propagated as interrupt events to the interrupt controller.

Interrupt events can also be triggered in software by writing to the corresponding bits in PDM_INTR_SET register.

Figure 29-5 illustrates the interrupt signal generation from the PDM-PCM block as explained above. Only the RX_TRIGGER interrupt generation is highlighted in the figure; the remaining interrupt events also follow the same generation logic.

### Table 29-3. Interrupt Event Trigger Condition

<table>
<thead>
<tr>
<th>Interrupt Event</th>
<th>Trigger Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>RX_TRIGGER</td>
<td>The PDM Rx FIFO has more entries than the value specified in the TRIGGER_LEVEL field in the PDM_RX_FIFO_CTL register. At least (TRIGGER_LEVEL + 1) words can be read from the PDM_RX_FIFO_RD register in the interrupt service routine.</td>
</tr>
<tr>
<td>RX_NOT_EMPTY</td>
<td>The PDM Rx FIFO has at least one word that can be read from the PDM_RX_FIFO_RD register.</td>
</tr>
<tr>
<td>RX_OVERFLOW</td>
<td>The PDM Rx FIFO content is overwritten by the PDM-PCM converter due to the number of unread words exceeding the 256 word buffer capacity. The output PCM data after the overflow condition is discarded and not transferred to the FIFO. This event can be used to detect bandwidth constraints in the end application due to DMA or the interrupt used for data transfer not getting the required priority for executing the data transfers.</td>
</tr>
<tr>
<td>RX_UNDERFLOW</td>
<td>Attempt to read from an empty PDM Rx FIFO. This can happen due to incorrect configuration of the DMA or the interrupt service routine code used to do the data transfer.</td>
</tr>
</tbody>
</table>

In the interrupt service routine (ISR) corresponding to the interrupt vector number of interrupt_pdm, the PDM_INTR_MASKED register should be read to know the events that triggered the interrupt event. Multiple events can trigger the interrupt because the final interrupt signal is the logical OR output of the events. The ISR should do the tasks corresponding to each interrupt event that was triggered. At the end of the ISR, the value read in the PDM_INTR_MASKED register earlier should be written to the PDM_INTR register to clear the bits whose interrupt events were processed in the ISR. A dummy read of the PDM_INTR register should be done for the earlier register write to PDM_INTR to take effect.

All of the interrupt event bits in PDM_INTR register will continue to indicate the event condition regardless of the true state until that bit is cleared (for example, when set, the RX_OVERFLOW bit will continue to indicate an OVERFLOW state until the RX_OVERFLOW bit is cleared regardless of the true state of the FIFO. A mere FIFO read of the FIFO will not clear the RX_OVERFLOW bit.). Unless the PDM_INTR bits that are used to generate the interrupt are not cleared by writing ‘1’ to the PDM_INTR bits, the interrupt signal will always be high.

#### 29.2.7 Digital Volume Gain

The PDM-PCM converter supports independent digital volume control on the left/right channels with a range from –12.5 dB to +10.5 dB in steps of 1.5 dB. It is programmed by configuring the PGA_R and PGA_L bits in the PDM_CTL register. PGA gain may be changed on the fly during normal operation, or as a one-time setting before starting the PDM-PCM conversion process.
29.2.8 Smooth Gain Transition

To reduce zipper or clip noise during on-the-fly gain transition or during soft mute operation, a built-in volume smoother is implemented with fine gain steps and fine time steps that enable soft ramp up or ramp down of the volume levels. Two fine gain options of 0.13 dB and 0.26 dB step sizes are available. The fine gain is set by the STEP_SEL bit in the PDM_CTL register. In addition to the fine gain steps, a time step is available for the fine gain change in terms of the number of sample cycles. The time step can be configured to a value between 64 sample periods and 512 sample periods using the S_CYCLES bits in the PDM_MODE_CTL register. So the STEP_SEL and S_CYCLES bit settings together determine the rate at which PGA gain or the soft mute transitions take effect.

29.2.9 Soft Mute

The PDM-PCM contains a built-in software-controlled mute function that digitally attenuates signals to imperceptible levels or zero. When mute function is enabled by setting the SOFT_MUTE bit in the PDM_CTL register, the corresponding PCM output is decreased from current level to mute state through predefined granular gain step per time constant transition. The STEP_SEL bit setting determines the gain step and the S_CYCLES bits determine the time constant. During soft-mute, the block is still ON and the PCM data streaming is operational; the DMA or CPU-based data transfer also happens as usual. Only the PCM output level is muted. When mute function is disabled by setting SOFT_MUTE = 0, the mute function is OFF and the PDM-PCM returns to normal operation where output signal level goes up to normal with current PGA gain.

29.2.10 Word Length and Sign Bit Extension

The PCM output word length can be configured for either 16-bits, 18-bits, 20-bits, or 24-bits using WORD_LEN bits in the PDM_DATA_CTL register. Irrespective of the word length setting, the PCM output is always read from the FIFO data buffer register (PDM_RX_FIFO_RD) as a 32-bit value. The unused most significant bits in the 32-bit value can either be sign extended or extended by ‘0’ by using the BIT_EXTENSION bit in the PDM_DATA_CTL register.

29.2.11 High-Pass Filter

The PDM-PCM converter has a final stage high-pass filter (HPF) that blocks DC offset and low-frequency noise in signal band. The HPF is enabled when the HPF_EN_N bit in the PDM_MODE_CTL register is zero, and disabled when the HPF_EN_N bit is 1.

The filter response for HPF is characterized as:

$$ H(z) = \frac{1 - z^{-1}}{1 - (1 - z^{-\text{HPF\_GAIN}})z^{-1}} $$

The HPF operates at the final PCM output sampling rate. HPF\_GAIN is a 4-bit gain configuration setting in the PDM_MODE_CTL register. In default mode, HPF\_GAIN = 0xB, so the HPF can be formulated by polynomial:

$$ H(z) = \frac{1 - z^{-1}}{1 - 0.99951z^{-1}} $$

The HPF\_GAIN setting can be tuned to adjust HPF cutoff corner frequency for better system configuration.

29.2.12 Enable/Disable Streaming

The PDM-PCM conversion process can be dynamically enabled/disabled by using the STREAM_EN bit in the PDM_CMD register.

29.2.13 Power Modes

The PDM-PCM can operate in Active, LPACTIVE, Sleep, and LPSLEEP modes. It is not operational in Deep Sleep or Hibernate power modes. When the device transitions from Deep Sleep/Hibernate power modes to the Active/Sleep power modes, the non-retention registers lose their previous configuration values. So the non-retention registers must be appropriately configured before enabling the PDM-PCM again for Active/Sleep mode operation. One option is to store the non-retention register values in SRAM before entering Deep Sleep/Hibernate modes. When returning to the Sleep/Active modes, the SRAM values can be copied to the registers after enabling the PDM-PCM by setting the ENABLED bit in the PDM_CTL register. Refer to the PSoC 6 with BLE Architecture TRM to identify the non-retention registers for the PDM.

29.3 Operating Procedure

29.3.1 Initial Configuration

The sequence of steps for initial configuration of the PDM-PCM converter before starting the conversion process is as follows:

1. Configure the clock dividers and decimation rate in the PDM_CLOCK_CTL register. This register configuration should be done before enabling the PDM-PCM converter. If the ENABLED bit in the PDM_CTL register is set, it should be cleared before changing the clock configuration.
2. Enable the block; set the PGA gain and fine gain step setting as required by writing to the PDM_CTL register.
3. Configure the PDM_MODE_CTL and PDM_DATA_CTL registers as required.
4. Configure the Rx FIFO trigger level setting by writing to the TRIGGER_LEVEL bits in the PDM_RX_FIFO_CTL register. The CLEAR and FREEZE bits in PDM_RX_FIFO_CTL are not set for normal operation.

5. Configure the events that must generate the interrupt by setting the corresponding bits in the PDM_INTR_MASK register, and clearing the remaining bits.

6. Configure the interrupt PDM interrupt vector and enable the interrupt vector. See the Interrupts chapter on page 47 for details.

7. If a DMA-based data transfer is required, connect the PDM DMA trigger signal (tr_pdm_rx_req) to the trigger input of the required DMA channel. See the Trigger Multiplexer Block chapter on page 197 for details on how to connect to the DMA channel trigger input. Configure the DMA channel as required - the source address of the DMA descriptor is PDM_RX_FIFO_RD register with the source address increment feature disabled and the source data length is word type (32-bits). The DMA channel can be used to transfer (TRIGGER_LEVEL + 1) words from the PDM_RX_FIFO_RD register whenever the trigger signal becomes high. The destination address configuration depends on the application requirements. See the DMA Controller chapter on page 72 for details on DMA channel configuration.

8. Enable the DMA trigger signal generation by setting the RX_REQ_EN bit in the PDM_TR_CTL register.

29.3.2 Interrupt Service Routine (ISR) Configuration

The code for the PDM interrupt service routine should have the following flow:

1. The events that triggered the interrupt can be found by reading the PDM_INTR_MASKED register in the ISR. All the bits that are set causes the interrupt event. The register value should also be in a variable “var”.

2. For each of the event bits that are set in PDM_INTR_MASKED, appropriate application level tasks can be executed. For example, the RX_TRIGGER event can be used for CPU-based data transfers if a DMA-based data transfer is not used. DMA transfers should use the tr_pdm_rx_req trigger signal (by setting the RX_REQ_EN bit in the PDM_TR_CTL register). The DMA trigger should not use the RX_TRIGGER interrupt event to reduce CPU usage for data transfer. The RX_OVERFLOW event can be used to take appropriate counter measures such as giving higher priority to PDM-PCM DMA channel. The RX_UNDERFLOW event typically indicates wrong data transfer logic in the application – either in the CPU-based data transfer code or in the DMA channel configuration used to transfer data.

3. After the event conditions have been processed, the “var” value read from PDM_INTR_MASKED should be written to the PDM_INTR register to clear the events that are set in the register. Due to the buffered write logic, the

PDM_INTR register should also be read after the write process to ensure the write process is completed in the slower peripheral clock domain.

29.3.3 Enabling / Disabling Streaming

The PDM-PCM conversion process starts after the STREAM_EN bit is set in the PDM_CMD register. Depending on the application needs, the streaming can be dynamically started and stopped using the STREAM_EN bit. Clear the Rx FIFO before starting the streaming process to reset the read/write pointers and FIFO state. The procedure to clear the FIFO is to write a ‘1’ to the CLEAR bit in PDM_RX_FIFO_CTL followed by writing a ‘0’ to the CLEAR bit. When the CLEAR bit is set, all the data entries in the Rx FIFO are cleared by resetting the internal read/write pointers. Read accesses to the PDM_RX_FIFO_RD and PDM_RX_FIFO_RD_SILENT registers are prohibited when the CLEAR bit is 1. Therefore, the CLEAR bit should be cleared before starting the streaming operation.
30. **Universal Serial Bus (USB) Device Mode**

The PSoC 6 MCU USB block can act as a USB device that communicates with a USB host. The USB block is available as a fixed-function digital block in the PSoC 6 MCU. It supports full-speed communication (12 Mbps) and is designed to be compliant with the USB Specification Revision 2.0. USB devices can be designed for plug-and-play applications with the host and also support hot swapping. This chapter details the PSoC 6 MCU USB block and transfer modes. For details about the USB specification, see the USB Implementers Forum website.

### 30.1 Features

The USB in the PSoC 6 MCU has the following features:

- Complies with USB Specification 2.0
- Supports full-speed peripheral device operation with a signaling bit rate of 12 Mbps
- Supports eight data endpoints and one control endpoint
- Provides shared 512-byte buffer for data endpoints
- Provides dedicated 8-byte memory for control endpoint (EP0)
- Supports four types of transfers – bulk, interrupt, isochronous, and control
- Supports bus- and self-powered configurations
- Enables USB suspend mode for low power
- Supports three types of logical transfer modes:
  - No DMA mode (Mode 1)
  - Manual DMA mode (Mode 2)
  - Automatic DMA mode (Mode 3)
- Supports maximum packet size of 512 bytes using Mode 1 and Mode 2, and maximum packet size of 1023 bytes for isochronous transfer using Mode 3
- Provides integrated 22-Ω USB termination resistors on D+ and D− lines, and 1.5-kΩ pull-up resistor on the D+ line
- Supports USB 2.0 Link Power Management (LPM)
30.2 Architecture

Figure 30-1 illustrates the device architecture of the USB block in PSoC 6 MCUs. It consists of the USB Physical Layer (USB PHY), Serial Interface Engine (SIE), and the local 512-byte memory buffer.

Figure 30-1. USB Device Block Diagram

![USB Device Block Diagram](image)

30.2.1 USB Physical Layer (USB PHY)

The USB PHY allows physical layer communication with the USB host through the D±, D–, and VBUS pins. It handles the differential mode communication with the host, VBUS detection, and monitoring events such as SE0 on the USB bus.

30.2.2 Serial Interface Engine (SIE)

The SIE handles the decoding and creating of data and control packets during transmit and receive. It decodes the USB bit streams into USB packets during receive, and creates USB bit streams during transmit. The following are the features of the SIE:

- Conforms to USB Specification 2.0
- Supports one device address
- Supports eight data endpoints and one control endpoint
- Supports interrupt trigger events for each endpoint
- Integrates an 8-byte buffer in the control endpoint

The registers for the SIE are mainly used to configure the data endpoint operations and the control endpoint data buffers. This block also controls the interrupt events available for each endpoint.

30.2.3 Arbiter

The Arbiter handles access of the SRAM memory by the endpoints. The SRAM memory can be accessed by the CPU, DMA, or SIE. The arbiter handles the arbitration between the CPU, DMA, and SIE. The arbiter consists of the following blocks:

- SIE Interface Module
- CPU/DMA Interface
- Memory Interface
- Arbiter Logic

The arbiter registers are used to handle the endpoint configurations, read address, and write address for the endpoints. It also configures the logical transfer type required for each endpoint.

30.2.3.1 SIE Interface Module

This module handles all the transactions with the SIE. The SIE reads data from the SRAM memory and transmits to the host. Similarly, it writes the data received from the host to the SRAM memory. These requests are registered in the SIE Interface module and are handled by this module.
30.2.3.2 CPU/DMA Interface Block

This module handles all transactions with the CPU and DMA. The CPU requests for reads and writes to the SRAM memory for each endpoint. These requests are registered in this interface and are handled by the block. When the DMA is configured, this interface is responsible for all transactions between the DMA and USB. The block supports the DMA request line for each data endpoint. The behavior of the DMA depends on the type of logical transfer mode configured in the configuration register.

30.2.3.3 Memory Interface

The memory interface is used to control the interface between the USB and SRAM memory unit. The maximum memory size supported is 512 bytes organized as 256 × 16-bit memory unit. This is a dedicated memory for the USB. The memory access can be requested by the SIE or by the CPU/DMA. The SIE Interface block and the CPU/DMA interface block handle these requests.

30.2.3.4 Arbiter Logic

This is the main block of the arbiter. It is responsible for arbitrations for all the transactions that happen in the arbiter. It arbitrates the CPU, DMA, and SIE access to the memory unit and the registers. This block also handles memory management, which is either ‘Manual’ or ‘Automatic’. In Manual memory management, the read and write address manipulations are done by the firmware. In Automatic management, all the memory handling is done by the block itself. This block takes care of the buffer size allocation. It also handles common memory area. This block also handles the interrupt requests for each endpoint.

30.3 Operation

30.3.1 Functions of USB PHY

The USB includes the transmitter and receiver (transceiver), which corresponds to the USB PHY. Figure 30-2 shows the PHY architecture. The USB PHY also includes the pull-up resistor on the D+ line to identify the device as full-speed type to the host. The PHY integrates the 22-Ω series termination resistors on the USB line. The signal between the USB device and the host is a differential signal. The receiver receives the differential signal from the host and converts it to a single-ended signal for processing by the SIE. The transmitter converts the single-ended signal from the SIE to the differential signal, and transmits it to the host. The differential signal is given to the upstream devices at a nominal voltage range of 0 V to 3.3 V.

30.3.1.1 Power Scheme

The USB PHY is powered by the VBUS power pad of the PSoC 6 MCU. The VBUS pad can be driven either by the host VBUS (bus-powered) or an external power supply (self-powered).

The USB PHY needs a nominal voltage of 3.3 V for its communication with the host.

Figure 30-2. USB PHY Architecture
30.3.1.2 VBUS Detection

USB devices can either be bus-powered (power sourced from the host) or self-powered (power sourced from an external power supply). The VDD_USB power pad pin powers the USB PHY and USB I/Os (D+ and D– pins). The presence of VBUS can be detected using the following steps:

1. Enable the interrupt on VDD_USB power pad. For this write ‘1’ to the VDDIO_ACTIVE[5] bit of VDD_INTR_MASK register.
2. VDDIO_ACTIVE[5] bit of the supply detection interrupt register (VDD_INTR) is set to ‘1’ whenever a change to supply is detected. Clear the interrupt cause by writing ‘1’ to the bitfield.
3. Check the status of the VDD_ACTIVE[5] bit of the external power supply detection register (VDD_ACTIVE). The bit is set to ‘1’ when there is supply and ‘0’ when there is no supply.

30.3.1.3 USB D+ Pin Pull-up Enable Logic

When a USB device is self-powered, the USB specification warrants that the device enable the pull-up resistor on its D+ pin to identify itself as a full-speed device to the host. When the host VBUS is removed, the device should disable the pull-up resistor on the D+ line to not back power the host. The USB PHY includes an internal 1.5-kΩ pull-up resistor on the D+ line to indicate to the host that the PSoC 6 MCU is a full-speed device. The pull-up resistor can be enabled or disabled by configuring the DP_UP_EN bit in the USBLPM_POWER_CTRL register.

30.3.1.4 Transmitter and Receiver Logic

The transceiver block transmits and receives USB differential signals with an upstream device, and includes the USB D+ pull-up resistor used to maintain an idle state on the bus. Output data is differentially transmitted to upstream devices at a nominal voltage of 3.3 V. The differential inputs received from upstream devices are converted into single-ended data and sent to the core logic at a nominal voltage of 1.8 V. The D+ and D– pins are terminated with 22-Ω resistors to meet the USB impedance specification.

30.3.1.5 GPIO Mode Logic

The D+ and D– pins can be used either as GPIO pins or USB I/O pins. This is controlled by the IOMUX bit of the USBDEV_USBIO_CR1 register. This bit should be set HIGH for GPIO functionality and LOW for USB operation.

30.3.1.6 Link Power Management (LPM)

The USB PHY supports link power management (LPM), which is similar to the suspend mode, but has transitional latencies in tens of microseconds between power states, compared to the greater than 20 ms latency associated with suspend/resume modes. For more details on LPM, refer to the USB 2.0 specification. The following features are supported for LPM:

- The LPM_CTL register should be configured to enable/disable LPM, type of response when LPM is enabled, and the response when a sub PID other than the LPM token is received from the host.
- The LPM_STAT register stores the values of the Best Effort Service Latency (BESL) and the remote wakeup feature as sent by the host. The firmware should read this register on the LPM interrupt event and enter the appropriate low-power mode (Deep Sleep or Sleep) based on the BESL value from the host.

30.3.2 Endpoints

The SIE and arbiter support eight data endpoints (EP1 to EP8) and one control endpoint (EP0). The data endpoints share the SRAM memory area of 512 bytes. The endpoint memory management can be either manual or automatic. The endpoints are configured for direction and other configuration using the SIE and arbiter registers. The endpoint read address and write address registers are accessed through the arbiter.

The endpoints can be individually made active. In the Auto Management mode, the register EP_ACTIVE is written to control the active state of the endpoint. The endpoint activation cannot be dynamically changed during runtime. In Manual Memory Management mode, the firmware decides the memory allocation, so it is not required to specify the active endpoints. The EP_ACTIVE register is ignored during the manual memory management mode. The EP_TYPE register is used to control the transfer direction (IN, OUT) for the endpoints. The control endpoint has separate eight bytes for its data (EP0_DR registers).

30.3.3 Transfer Types

The PSoC 6 MCU USB supports full-speed transfers and is compliant with the USB 2.0 specification. It supports four types of transfers:

- Interrupt Transfer
- Bulk Transfer
- Isochronous Transfer
- Control Transfer

For further details about these transfers, refer to the USB 2.0 specification.

30.3.4 Interrupt Sources

The USB device block generates 14 interrupts to the CPU. These interrupts are mapped to three general-purpose interrupt lines – INTR_LO, INTR_MED, and INTR_HI. Each of these three interrupt lines has an associated status register, which identifies the cause of the interrupt event. These are the USBLPM_INTR_CAUSE_LO, USBLPM_INTR_CAUSE_MED, and USBLPM_INTR_CAUSE_HI registers. The routing of these interrupts is controlled by the USBLPM_INTR_LVL_SEL register fields.

The following events generate an interrupt on one of the three interrupt lines:

- USB start of frame (SOF) event
30.3.4.1 USB Start of Frame (SOF) Event

The SOF interrupt is generated upon receiving an SOF packet from the USB host. The SOF interrupt is enabled using the SOF_INTR_MASK bitfield in the USBLPM_INTR_SIE_MASK register.

- The SOF interrupt status is reflected in the SOF_INTR status bit in the USBLPM_INTR_SIE status register.
- The SOF interrupt status is also available in the SOF_INTR_MASKED bit of the USBLPM_INTR_SIE_MASKED register – this bit is the logical AND of the corresponding SOF bits in the USBLPM_INTR_SIE_MASK register and the USBLPM_INTR_SIE register.
- If there is no SOF interrupt for 3 ms, the USB device goes into SUSPEND state.

30.3.4.2 USB Bus Reset Event

The USB bus reset interrupt is generated when a USB bus reset condition occurs. The bus reset interrupt is enabled by setting the BUS_RESET_INTR_MASK bit in the USBLPM_INTR_SIE_MASK register.

- The bus reset interrupt status is reflected in the BUS_RESET_INTR bit in the USBLPM_INTR_SIE status register.
- The bus reset interrupt status is also available in the BUS_RESET_INTR_MASKED bit of the USBLPM_INTR_SIE_MASKED register – this bit is the logical AND of the corresponding bus reset bits in the USBLPM_INTR_SIE_MASK register and the USBLPM_INTR_SIE register.
- The SIE logic triggers the counter to start running on CLK_PERI when an SE0 condition is detected on the USB bus. When the counter reaches the count value configured in the USBDDEV_BUS_RST_CNT register, the bus reset interrupt is triggered.

30.3.4.3 Data Endpoint Interrupt Events

These are eight interrupt events corresponding to each data endpoint (EP1-EP8). Each of the endpoint interrupt events can be enabled/disabled by using the corresponding bit in the USBDDEV_SIE_EP_INT_EN register. The interrupt status of each endpoint can be known by reading the USBDDEV_SIE_EP_INT_SR status register. An endpoint whose interrupt is enabled can trigger the interrupt on the following events:

- Successful completion of an IN/OUT transfer
- NAK-ed IN/OUT transaction if the corresponding NAK_INT_EN bit in the SIE_EPx_CR0 register is set
- When there is an error in the transaction, the ERR_IN_TXN bit in the SIE_EPx_CR0 register is set and interrupt is generated.
- If the STALL bit in SIE_EPx_CR0 is set, then stall events can generate interrupts. This stall event can occur if an OUT packet is received for an endpoint whose mode bits in SIE_EPx_CR0 are set to ACK_OUT or if an IN packet is received with mode bits set to ACK_IN.

30.3.4.4 Control Endpoint Interrupt Event

The interrupt event corresponding to the control endpoint (EP0) is generated under the following events:

- Successful completion of an IN/OUT transfer
- When a SETUP packet is received on the control endpoint

The EP0 interrupt is setup using the EP0_INTR_SET bit of the USBLPM_INTR_SIE_SET register.

30.3.4.5 Link Power Management (LPM) Event

Generated whenever the LPM token packet is received. The LPM interrupt is enabled by setting the LPM_INTR_MASK bit in the USBLPM_INTR_SIE_MASK register. The LPM interrupt status is reflected in the LPM_INTR status bit in the USBLPM_INTR_SIE status register.

- The LPM interrupt status is also available in the LPM_INTR_MASKED bit of the USBLPM_INTR_SIE_MASKED register; this bit is the logical AND of the corresponding LPM bits in the USBLPM_INTR_SIE_MASK and USBLPM_INTR_SIE registers.
- The firmware needs to read the USBLPM_LPM_STAT register to read the BESL remote wakeup values and appropriately enter the desired low-power mode. Enter the low-power mode in the main code. The exit from LPM is identical to the resume event wakeup in the case of suspend mode.

30.3.4.6 RESUME Interrupt

The RESUME interrupt is asserted by the USB block when it detects '0' on the DP pad. The RESUME interrupt is enabled by setting the RESUME_INTR_MASK bitfield of the USBLPM_INTR_SIE_MASK register.

- The RESUME interrupt status is reflected in the RESUME_INTR status bit in the USBLPM_INTR_SIE status register.
- The RESUME interrupt status is also available in the RESUME_INTR_MASKED bit of the USBLPM_INTR_SIE_MASKED register – this bit is the logical AND of the corresponding RESUME bits in the USBLPM_INTR_SIE_MASK and USBLPM_INTR_SIE registers.
- The RESUME interrupt is an Active mode interrupt and not available in Deep Sleep or Hibernate mode.
30.3.4.7 Arbiter Interrupt Event

The arbiter interrupt can arise from five possible sources. Each interrupt source is logically ANDed with its corresponding ENABLE bit and the results are logically ORed to result in a single arbiter interrupt event.

The arbiter interrupt event can arise under any of the following five scenarios:

- DMA Grant
- IN Buffer Full
- Buffer Overflow
- Buffer Underflow
- DMA Termin

DMA Grant

This event is applicable in Mode 2 or Mode 3. (See Logical Transfer Modes on page 332 for details on DMA modes). This event is triggered when the DMA controller pulses the Burstend signal corresponding to that endpoint, for which a DMA request had been raised to the DMA controller earlier. The request may have been either a manual DMA request or an automatic arbiter DMA request. A common grant status exists for both modes of requests. This grant status indicates completion of the DMA transaction. This status indication can be used by firmware to determine when the next manual DMA request can be raised. Multiple requests raised for the same endpoint before the DMA grant status is set will be dropped by the block. Only the first of multiple requests will be transmitted to DMA controller.

IN Buffer Full

This event status can occur in any of the DMA modes (Mode 1, 2, or 3) and is applicable only for IN endpoints.

- Store and Forward Mode (Modes 1 and 2): This status is set when the entire packet data is transferred to the local memory. The check is that data written for the particular endpoint is equal to the programmed byte count for that endpoint in the USBDEV_SIE_EPx_CNT0 and USBDEV_SIE_EPx_CNT1 registers.
- Cut Through Mode (Mode 3): In this mode, the IN buffer full status is set when the IN endpoint’s dedicated buffer is filled with the packet data. The size of this buffer is determined by the value programmed in bits [3:0] of the USBDEV_BUF_SIZE register. This status indication can be used to determine when the mode value in the USBDEV_SIE_EPx_CR0 register can be programmed to acknowledge an IN token for that endpoint.

Buffer Overflow

This event status is active only in the Cut Through Mode (Mode 3). The following conditions can cause this bit to be set:

- Data overflow on the endpoint dedicated buffer space
  - In an IN endpoint, the dedicated buffer can overflow if the DMA transfer writes a larger number of bytes than the space available in the dedicated buffer. Until an IN token is received for that endpoint, it cannot use the common buffer area, hence resulting in an overflow of data. The possible causes of this buffer overflow can be incorrect programming of either the DMA transfer descriptor transfer size or the USBDEV_BUF_SIZE register.

Buffer Underflow

This event status can occur in any of the DMA modes (Mode 2 or Mode 3). This underflow condition can occur only for an IN endpoint. The underflow condition can occur either in the dedicated buffer space or common buffer space. The underflow condition on the dedicated buffer space can be due to the reduced dedicated IN buffer size or DMA bandwidth constraint. The underflow condition can occur on the common buffer space due to DMA bandwidth constraint and/or lower DMA channel priority.

DMA Termin

This status is set when USBDEV generates a dma_termin signal to indicate the total programmed/received bytes that are written/read by the DMA controller. This status indication can be used by the firmware to reprogram the IN/OUT endpoint for the next transfer. For an OUT endpoint, this indicates that the OUT packet data is available in the system memory for further processing by the application.

30.3.5 DMA Support

Each of the eight data endpoints has one DMA channel available to transfer data between the endpoint buffer and the SRAM memory. The USB generates the DMA request signals (usb.dma_req[7:0]) to the respective DMA channels to initiate the data transfer for the endpoint. This goes to the Trigger Group 13 multiplexer as input triggers that can be routed to one of the trigger inputs of the DMA block. The Burstend signals from the DMA channel to the correspond-
ing endpoint is routed using the Trigger Group 9 multiplexer. For more details, see the DMA Controller chapter on page 72 and Trigger Multiplexer Block chapter on page 197.

### 30.4 Logical Transfer Modes

The USB block in PSoC 6 MCUs supports two types of logical transfers. The logical transfers can be configured using the register setting for each endpoint. Any of the logical transfer methods can be adapted to support the three types of data transfers (Interrupt, Bulk, and Isochronous) mentioned in the USB 2.0 specification. The control transfer is mandatory in any USB device.

The logical transfer mode is a combination of memory management and DMA configurations. The logical transfer modes are related to the data transfer within the USB (to and from the SRAM memory unit for each endpoint). It does not represent the transfer methods between the device and the host (the transfer types specified in the USB 2.0 specification).

The USB supports two basic types of transfer modes:

- **Store and Forward mode**
  - Manual Memory Management with No DMA Access (Mode 1)
  - Manual Memory Management with Manual DMA Access (Mode 2)

- **Cut Through mode**
  - Automatic Memory Management with Automatic DMA Access (Mode 3)

Table 30-1 gives a comparison of the two transfer modes.

<table>
<thead>
<tr>
<th>Feature</th>
<th>Store and Forward Mode</th>
<th>Cut Through Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRAM Memory Usage</td>
<td>Requires more memory</td>
<td>Requires less memory</td>
</tr>
<tr>
<td>SRAM Memory Management</td>
<td>Manual</td>
<td>Auto</td>
</tr>
<tr>
<td>SRAM Memory Sharing</td>
<td>512 bytes of SRAM shared between endpoints. Sharing is done by firmware.</td>
<td>Each endpoint is allocated a lesser share of memory automatically by the block. The remaining memory is available as “common area.” This common area is used during the transfer.</td>
</tr>
<tr>
<td>IN Command</td>
<td>Entire packet present in SRAM memory before the IN command is received.</td>
<td>Memory filled with data only when SRAM IN command is received. Data is given to host when enough data is available (based on DMA configuration). Does not wait for the entire data to be filled.</td>
</tr>
<tr>
<td>OUT Command</td>
<td>Entire packet is written to SRAM memory on OUT command. After entire data is available, it is copied from SRAM memory to the USB device.</td>
<td>Waits only for enough bytes (depends on DMA configuration) to be written in SRAM memory. When enough bytes are present, it is immediately copied from SRAM memory to the USB device.</td>
</tr>
<tr>
<td>Transfer of Data</td>
<td>Data is transferred when all bytes are written to the memory.</td>
<td>Data is transferred when enough bytes are available. It does not wait for the entire data to be filled.</td>
</tr>
<tr>
<td>Types Based on DMA</td>
<td>No DMA mode</td>
<td>Only Auto DMA mode</td>
</tr>
<tr>
<td>Supported Transfer Types</td>
<td>Ideal for interrupt and bulk transfers</td>
<td>Ideal for Isochronous transfer</td>
</tr>
</tbody>
</table>

Every endpoint has a set of registers that need to be handled during the modes of operation, as detailed in Table 30-2.
Universal Serial Bus (USB) Device Mode

Table 30-2. Endpoint Registers

<table>
<thead>
<tr>
<th>Register</th>
<th>Comment</th>
<th>Content</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>USBDEV_ARB_RWx_WA</td>
<td>Endpoint Write Address Register</td>
<td>Address of the SRAM</td>
<td>This register indicates the SRAM location to which the data in the data register is to be written.</td>
</tr>
<tr>
<td>USBDEV_ARB_RWx_RA</td>
<td>Endpoint Read Address Register</td>
<td>Address of the SRAM</td>
<td>This register indicates the SRAM location from which the data must be read and stored to the data register.</td>
</tr>
<tr>
<td>USBDEV_ARB_RWx_DR</td>
<td>Endpoint Data Register</td>
<td>8-Bit Data</td>
<td>Data register is read/written to perform any transaction. IN command: Data written to the data register is copied to the SRAM location specified by the WA register. After write, the WA value is automatically incremented to point to the next memory location. OUT command: Data available in the SRAM location pointed by the RA register is read and stored to the DR. When the DR is read, the value of RA is automatically incremented to point to the next SRAM memory location that must be read.</td>
</tr>
<tr>
<td>USBDEV_SIE_EPx_CNT0 and USBDEV_SIE_EPx_CNT1</td>
<td>Endpoint Byte Count Register</td>
<td>Number of Bytes</td>
<td>Holds the number of bytes that can be transferred. IN command: Holds the number of bytes to be transferred to host. OUT command: Holds the maximum number of bytes that can be received. The firmware programs the maximum number of bytes that can be received for that endpoint. The SIE updates the register with the number of bytes received for the endpoint.</td>
</tr>
<tr>
<td>&quot;Mode&quot; bits in USBDEV_SIE_EPx_CR0</td>
<td>Mode Values</td>
<td>Response to the Host</td>
<td>Controls how the USB device responds to the USB traffic and the USB host. Some examples of modes are ACK, NAK, and STALL.</td>
</tr>
</tbody>
</table>

In Manual memory management, the endpoint read and endpoint write address registers are updated by the firmware. So the memory allocation can be done by the user. The memory allocation decides which endpoints are active; that is, you can decide to share the 512 bytes for all the eight endpoints or a lesser number of endpoints.

In Automatic memory management, the endpoint read and endpoint write address registers are updated by the USB block. The block assigns memory to the endpoints that are activated using the USBDEV_EP_ACTIVE register. The size of memory allocated depends on the value in the USBDEV_BUF_SIZE register. The remaining memory, after allocation, is called the common area memory and is used for data transfer.

In all of these modes, either the 8-bit endpoint data register or the 16-bit endpoint data register can be used to read/write to the endpoint buffer. While transferring data to the 16-bit data registers, ensure that the corresponding SRAM memory address locations are also 16-bit aligned.

In the following text, the algorithm for the IN and OUT transaction for each mode is discussed. An IN transaction is when the data is read by the USB host (for example, PC). An OUT transaction is when the data is written by the USB host to the USB device. The choice of using the DMA and memory management can be configured using the USBDEV_ARB_EPx_CFG register.
30.4.1 Manual Memory Management with No DMA Access

All operations in this mode are controlled by the CPU and works in a store-and-forward operation mode. An entire packet is transferred to the memory and a mode bit (such as ACK IN or ACK OUT) is set by the CPU. The SIE responds appropriately to an IN/OUT token received from the host. All memory space management is handled by the CPU.

Figure 30-3. No DMA Access IN Transaction

Figure 30-4. No DMA Access OUT Transaction

30.4.2 Manual Memory Management with DMA Access

This mode is similar to the No DMA Access except that write/read of packets is performed by the DMA. A DMA request for an endpoint is generated by setting the DMA_CFG bit in the USBDEV_ARB_EPx_CFG register. When the DMA service is granted and is done (DMA_GNT), an arbiter interrupt can be programmed to occur. The transfer is done using a single DMA cycle or multiple DMA cycles. After completion of every DMA cycle, the arbiter interrupt (DMA_GNT) is generated. Similarly, when all the data bytes (programmed in byte count) are written to the memory, the arbiter interrupt occurs and the IN_BUF_FULL bit is set.
Figure 30-5 and Figure 30-6 show the flow charts for manual DMA IN and OUT transactions respectively.

Figure 30-5. Manual DMA IN Transaction

1. Write WA register (based on required memory allocation)
2. Set Packet size in the Endpoint byte count register
3. Set the DMA request in USBDEV_ARB_EPx_CFG register
4. DMA writes data to Endpoint Data Register
   WA++
5. DMA Grant Arbiter interrupt generated
6. Is all data written to SRAM?
   Yes
   Write to RA register (= initial WA register)
   Set mode in CR0 register
   Wait
   No
   Is IN Token Received?
   Yes
   USB block reads data stored at RA and transmit to Host.
   RA++
   Is all data transmitted?
   Yes
   SIE sets Endpoint mode as NAK IN and raises endpoint interrupt for ACKed transaction; DMA Termin Generated
   No
   Responds automatically with ACK
   Interrupt generated
   End
   No
30.4.3 Automatic DMA Mode

This is the Automatic memory management mode with auto DMA access. The CPU programs the initial buffer size requirement for IN/OUT packets and informs the arbiter block of the endpoint configuration details for the particular application. The block then controls memory partitioning and handling of all memory pointers. During memory allocation, each active IN endpoint (set by the USBDEV_EP_ACTIVE and USBDEV_EP_TYPE registers) is allocated a small amount of memory configured using the USBDEV_BUF_SIZE register (32 bytes for each of the eight endpoints). The remaining memory (256 bytes) is left as common area and is common for all endpoints.

In this mode, the memory requirement is less and it is suitable for full-speed isochronous transfers up to 1023 bytes.

When an IN command is sent by the host, the device responds with the data present in the dedicated memory area for that endpoint. It simultaneously issues a DMA request for more data for that EP. This data fills up the common area. The device does not wait for the entire packet of data to be available. It waits only for the (USBDMA_DMA_THRES_MSB, USBDMA_DMA_THRES) number of data available in the SRAM memory and begins the transfer from the common area.

Similarly, when an OUT command is received, the data for the OUT endpoint is written to the common area. When some data (greater than USBDMA_DMA_THRES_MSB, USBDMA_DMA_THRES) is available in the common area, the arbiter block initiates a DMA request and the data is immediately written to the device. The device does not wait for the common area to be filled.

This mode requires the configuration of the USBDMA_DMA_THRES and USBDMA_DMA_THRES_MSB registers to hold the number of bytes that can be transferred in one DMA transfer (32 bytes). Similarly, the burst count of the DMA should always be equal to the value set in the USBDMA_DMA_THRES registers. Apart from the DMA configuration, this mode also needs the configuration of the USBDMA_BUF_SIZE for the IN and the OUT buffers and the USBDEV_EP_ACTIVE and the USBDEV_EP_TYPE registers.

Each DMA channel has two descriptors and both of them are used in this mode. Each descriptor is considered as a data chunk of 32 bytes and it executes according to the trigger mechanism. The descriptors are chained and hence 64 bytes can be transferred without firmware interaction. When both descriptors complete the endpoint DMA done interrupt and the DMA error interrupt triggers (due to the lack of data to transfer). The descriptors are updated to advance the source SRAM (IN endpoint) or destination SRAM (OUT endpoint) pointer locations and then enabled again. This sequence continues till all data is transferred.

The steps for IN and OUT transactions using automatic DMA mode are shown in Figure 30-7 and Figure 30-8.
Figure 30-7. IN Transaction using Automatic DMA Mode

1. Set Packet size in the Endpoint byte count register
2. Set IN_DATA_RDY for the endpoint in ARB_EP1_CFG register
3. Block automatically raises interrupt for DMA
4. DMA writes to Data register
5. Is the endpoint Buffer full?
6. Update mode value in the Mode register
7. Wait
8. Is IN Command received?
9. Is the complete data available in the memory?
10. SIE reads data from SRAM (specified by location RA) and transmits to host
11. RA++
12. Is all data in buffer transmitted?
13. Set the data valid bits
14. End

This memory location is very limited. The memory location is filled initially to make sure the host does not stall when an IN command is sent. When an IN command is received the PHUB initiates the copy of data from device to common area. This initialization takes some time. The data in the end point buffer is transmitted until the data is copied to the common area.

In the mean time, the PHUB initiates the transaction. The data from the device is copied to the common area. The data from the USB is written to the SRAM by the DMA. This initialization takes some time.

The process is continued till all the data is transferred.
30.4.4 Control Endpoint Logical Transfer

The control endpoint has a special logical transfer mode. It does not share the 512 bytes of memory. Instead, it has a dedicated 8-byte register buffer (USBDEV_EP0_DRx registers). The IN and OUT transaction for the control endpoint is detailed in the following figures.
Figure 30-9. Control Endpoint IN Transaction

Set the mode bits to ACK the IN token

Is SETUP token received?
  Yes
  The block ACKs it
  Generates interrupt and sets the bit in EP0_CR register to indicate that SETUP token was received

Read the status bit and data valid bit

Is Data Valid?
  Yes
  Read the EP0_DRx register to find the type of request
  Copy the required data to the EP0_DRx registers
  Set the data valid bit and the mode bits. Also update the byte count value

Is IN Token Received?
  Yes
  The block transmits the data from the EP0_DRx registers
  The block sets the mode value to NAK all further IN tokens
  Block generates interrupt on receiving ACK from host and sets the IN byte received bit

Are all bytes transferred?
  Yes
  End
  No

No

Figure 30-10. Control Endpoint OUT Transaction

Program the mode bits for ACK_OUT

Is SETUP token received?
  Yes
  The block ACKs it
  Generates interrupt and sets the bit in EP0_CR register to indicate that SETUP token was received

Read the data valid bit in EP0_CNT

Is Data Valid?
  Yes
  Read the EP0_DRx register to find the type of request
  Update the mode bits to ACK an OUT token

Is OUT Token Received?
  Yes
  The block stores the received byte to the EP0_DRx registers and ACK the received byte
  Interrupt generated
  Read the status and data valid bits
  Is data Valid?
  Yes
  Set the mode bit to NAK all OUT tokens till all bytes have been received

Are all bytes transferred?
  Yes
  End
  No

No
30.5 USB Power Modes

The USB supports two modes of operation:

- **Active mode**: In this mode, the USB is powered up and clocks are turned on.
- **Low-power (Deep Sleep) mode**: In this mode, all clocks except the low-frequency clock are turned off.

Before entering low-power mode, the firmware should enable the GPIO interrupt (falling edge interrupt) on the D+ pin. The USB suspend mode can be determined by monitoring the SOF interrupt; this means, if there is no SOF interrupt from the USB for more than 3 ms, the USB goes into suspend mode and the block can be put into low-power mode by the firmware.

If there is any activity on the USB bus, D+ will be pulled low, which will cause a CPU interrupt. This interrupt can be used to wake up the USB device.

30.6 USB Device Registers

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>USBDEV_EP0_DR</td>
<td>Control endpoint EP0 data register</td>
</tr>
<tr>
<td>USBDEV_CR0</td>
<td>USB control 0 register</td>
</tr>
<tr>
<td>USBDEV_CR1</td>
<td>USB control 1 register</td>
</tr>
<tr>
<td>USBDEV_SIE_EP_INT_EN</td>
<td>USB SIE data endpoint interrupt enable register</td>
</tr>
<tr>
<td>USBDEV_SIE_EP_INT_SR</td>
<td>USB SIE data endpoint interrupt status</td>
</tr>
<tr>
<td>USBDEV_SIE_EPx_CNT0</td>
<td>Non-control endpoint count register</td>
</tr>
<tr>
<td>USBDEV_SIE_EPx_CNT1</td>
<td>Non-control endpoint count register</td>
</tr>
<tr>
<td>USBDEV_SIE_EPx_CR0</td>
<td>Non-control endpoint's control register</td>
</tr>
<tr>
<td>USBDEV_USBIO_CR0</td>
<td>USBIO control 0 register</td>
</tr>
<tr>
<td>USBDEV_USBIO_CR2</td>
<td>USBIO control 2 register</td>
</tr>
<tr>
<td>USBDEV_USBIO_CR1</td>
<td>USBIO control 1 register</td>
</tr>
<tr>
<td>USBDEV_DYN_RECONFIG</td>
<td>USB dynamic reconfiguration register</td>
</tr>
<tr>
<td>USBDEV_SOF0</td>
<td>Start of frame register</td>
</tr>
<tr>
<td>USBDEV_SOF1</td>
<td>Start of frame register</td>
</tr>
<tr>
<td>USBDEV_OSCLOCK_DR0</td>
<td>Oscillator lock data register 0</td>
</tr>
<tr>
<td>USBDEV_OSCLOCK_DR1</td>
<td>Oscillator lock data register 1</td>
</tr>
<tr>
<td>USBDEV_EP0_CR</td>
<td>Endpoint0 control register</td>
</tr>
<tr>
<td>USBDEV_EP0_CNT</td>
<td>Endpoint0 count register</td>
</tr>
<tr>
<td>USBDEV_ARB_RWx_WA</td>
<td>Endpoint write address value register</td>
</tr>
<tr>
<td>USBDEV_ARB_RWx_WA_MSB</td>
<td>Endpoint write address value register</td>
</tr>
<tr>
<td>USBDEV_ARB_RWx_RA</td>
<td>Endpoint read address value register</td>
</tr>
<tr>
<td>USBDEV_ARB_RWx_RA_MSB</td>
<td>Endpoint read address value register</td>
</tr>
<tr>
<td>USBDEV_ARB_RWx_DR</td>
<td>Endpoint data register</td>
</tr>
<tr>
<td>USBDEV_BUF_SIZE</td>
<td>Dedicated endpoint buffer size register</td>
</tr>
<tr>
<td>USBDEV_EP_ACTIVE</td>
<td>Endpoint active indication register</td>
</tr>
<tr>
<td>USBDEV_EP_TYPE</td>
<td>Endpoint type (IN/OUT) indication register</td>
</tr>
<tr>
<td>USBDEV_ARB_EPx_CFG</td>
<td>Endpoint configuration register</td>
</tr>
<tr>
<td>USBDEV_ARB_EPx_INT_EN</td>
<td>Endpoint interrupt enable register</td>
</tr>
<tr>
<td>USBDEV_ARB_EPx_SR</td>
<td>Endpoint interrupt enable register</td>
</tr>
<tr>
<td>USBDEV_ARB_CFG</td>
<td>Arbiter configuration register</td>
</tr>
<tr>
<td>USBDEV_USB_CLK_EN</td>
<td>USB block clock enable register</td>
</tr>
<tr>
<td>USBDEV_ARB_INT_EN</td>
<td>Arbiter interrupt enable register</td>
</tr>
<tr>
<td>USBDEV_ARB_INT_SR</td>
<td>Arbiter interrupt status register</td>
</tr>
<tr>
<td>Name</td>
<td>Description</td>
</tr>
<tr>
<td>--------------------------</td>
<td>-------------------------------------------------------</td>
</tr>
<tr>
<td>USBDEV_CWA</td>
<td>Common area write address register</td>
</tr>
<tr>
<td>USBDEV_CWA_MSB</td>
<td>Endpoint read address value register</td>
</tr>
<tr>
<td>USBDEV_DMA_THRES</td>
<td>DMA burst / threshold configuration register</td>
</tr>
<tr>
<td>USBDEV_DMA_THRES_MSB</td>
<td>DMA burst / threshold configuration register</td>
</tr>
<tr>
<td>USBDEV_BUS_RST_CNT</td>
<td>Bus reset count register</td>
</tr>
<tr>
<td>USBDEV_MEM_DATA</td>
<td>Data register</td>
</tr>
<tr>
<td>USBDEV_SOF16</td>
<td>Start of frame register</td>
</tr>
<tr>
<td>USBDEV_OSCLK_DR16</td>
<td>Oscillator lock data register</td>
</tr>
<tr>
<td>USBDEV_ARB_RWx_WA16</td>
<td>Endpoint write address value register</td>
</tr>
<tr>
<td>USBDEV_ARB_RWx_RA16</td>
<td>Endpoint read address value register</td>
</tr>
<tr>
<td>USBDEV_ARB_RWx_DR16</td>
<td>Endpoint data register</td>
</tr>
<tr>
<td>USBDEV_DMA_THRES16</td>
<td>DMA burst / threshold configuration register</td>
</tr>
<tr>
<td>USBLPM_POWER_CTL</td>
<td>Power control register</td>
</tr>
<tr>
<td>USBLPM_USBIO_CTL</td>
<td>USB IO control register</td>
</tr>
<tr>
<td>USBLPM_FLOW_CTL</td>
<td>Flow control register</td>
</tr>
<tr>
<td>USBLPM_LPM_CTL</td>
<td>LPM control register</td>
</tr>
<tr>
<td>USBLPM_LPM_STAT</td>
<td>LPM status register</td>
</tr>
<tr>
<td>USBLPM_INTR_SIE</td>
<td>USB SOF, BUS RESET, and EP0 interrupt status register</td>
</tr>
<tr>
<td>USBLPM_INTR_SIE_SET</td>
<td>USB SOF, BUS RESET, and EP0 interrupt set register</td>
</tr>
<tr>
<td>USBLPM_INTR_SIE_MASK</td>
<td>USB SOF, BUS RESET, and EP0 interrupt mask register</td>
</tr>
<tr>
<td>USBLPM_INTR_SIE_MASKED</td>
<td>USB SOF, BUS RESET, and EP0 interrupt masked register</td>
</tr>
<tr>
<td>USBLPM_INTR_LVL_SEL</td>
<td>Select interrupt level for each interrupt source register</td>
</tr>
<tr>
<td>USBLPM_INTR_CAUSE_HI</td>
<td>High-priority interrupt cause register</td>
</tr>
<tr>
<td>USBLPM_INTR_CAUSE_MED</td>
<td>Medium-priority interrupt cause register</td>
</tr>
<tr>
<td>USBLPM_INTR_CAUSE_LO</td>
<td>Low-priority interrupt cause register</td>
</tr>
</tbody>
</table>
The USB subsystem in PSoC 6 MCUs can be configured to function as a USB host. The USB host in the PSoC 6 MCU supports both full-speed (12 Mbps) and low-speed (1.5 Mbps) devices and is designed to be complaint with the USB Specification Revision 2.0. This chapter details the PSoC 6 MCU USB and its operations. For details about the USB specification, refer to the USB Implementers Forum website.

31.1 Features
The USB host in the PSoC 6 MCU has the following features:
- Automatic detection of device connection or disconnection
- Full-speed or low-speed transfer
- Automatic detection of full-speed or low-speed transfer
- Supports USB bus reset sending function
- Supports IN, OUT, SETUP, and SOF tokens
- Supports Bulk, Control, Interrupt, and Isochronous transfer
- Automatic detection of handshake packet for OUT token and automatic sending of handshake packet for IN token (excluding STALL)
- Supports a maximum packet length of up to 256 bytes
- Supports action against errors (CRC error, toggle error, and timeout)

31.2 Architecture

Figure 31-1. USB Host Block Diagram
31.2.1 USB Physical Layer (USB PHY)

The USB includes the transmitter and receiver (transceiver), which corresponds to the USB PHY. This module allows physical layer communication with the USB device through the D+, D−, and VDDUSB pins. It handles differential mode communication with the device. The USB PHY also includes pull-down resistors on the D+ and D− lines. Differential signaling is used between the USB host and the device. The host controller unit receives the differential signal from the device and converts it to a single-ended signal. While transmitting, the host controller unit converts the single-ended signal to the differential signal, and transmits it to the device. The differential signal is at a nominal voltage range of 0 V to 3.3 V.

31.2.2 Clock Control Block

This block controls the gated clocks – system clock and USB clock. The USB host requires a clock frequency of 48 MHz. USB host compliance requires a clock source with an accuracy of ±0.25 percent. One way of doing this is to use Clk_HF[3] sourced from an highly accurate ECO. The PLL can be used to generate the required 48-MHz clock from the ECO. Refer to the Clocking System chapter on page 146 for details on generation of clock required for USB operation.

31.2.3 Interrupt Control Block

This block controls the interrupts associated with USB host operations. The USB host block has three general-purpose interrupt signals: INTR_USBHOST_LO, INTR_USBHOST_MED, and INTR_USBHOST_HI. There are 11 interrupt trigger events associated with USB host operation that can be mapped to any of the three interrupt lines. Each of these three interrupt lines has a status register to identify the interrupt source. These are INTR_USBHOST_CAUSE_LO, INTR_USBHOST_CAUSE_MED, and INTR_USBHOST_CAUSE_HI registers.

31.2.4 Endpoint n (n=1, 2)

The USB host has two endpoints. The maximum buffer size of endpoint 1 is 256 bytes and that of endpoint 2 is 64 bytes. The endpoint buffers are used to send and receive data. If endpoint 1 is used as the transmitter, endpoint 2 must be used as the receiver and vice-versa. The DIR bit of the HOST_EPn_CTL (n=1, 2) register is used to configure the endpoint as an IN buffer (DIR=0) or OUT buffer (DIR=1).

31.2.5 DREQ Control

The USB host supports data transfer through DMA. DMA operation is enabled by configuring the HOST_DMA_ENBL register. There are two DMA transfer modes: Automatic data transfer mode and packet transfer mode. The DMAE bit of the HOST_EPn_CTL (n=1, 2) register is used to set the mode of DMA transfer. The Host Endpoint Block register (HOST_EPn_BLK; n=1, 2) sets the total number of bytes for DMA transfer.

31.3 USB Host Operations

To operate the USB as a host, the following settings are required:

- Enable the pull-down resistors on both D+ and D− pins. To enable the pull-down resistors, set the DP_DOWN_EN bit and DM_DOWN_EN bit of the power control register (POWER_CTL) to ‘1’.
- Set both the HOST and ENABLE bits of the Host Control 0 register (HOST_CTL0) to ‘1’.
- Set the USTP bit of the Host Control 1 register (HOST_CTL1) to ‘0’.
- Supply the operating clock for USB (48 MHz). CLK_HF[3] is the root clock for USB communication. Use FLL as the source clock for CLK_HF[3] to generate the USB clock. Note that the system clock must be set to 13 MHz or more for the USB host mode of operation. Refer to the Clocking System chapter on page 146 for more details on clock generation.

31.3.1 Detecting Device Connection

When an external USB device is not connected, both the D+ and D− pins are set to logic LOW by the pull-down resistors. In the unconnected state, CSTAT bit of the HOST_STATUS register is ‘0’ and the TMODE bit is undefined. If an external USB device is connected, then the CSTAT bit is set to ‘1’.

When a device is detected, the CNNIRQ bit of the Interrupt USB host (INTR_USBHOST) register is set to ‘1’. A device can be detected either by the method of interrupt or by polling. If ‘1’ is set to the CNNIRQM bit of the Interrupt USB host (INTR_USBHOST_MASK) register, a device connection interrupt occurs. To clear this interrupt, write ‘1’ to the CNNIRQ bit of INTR_USBHOST register. When detecting a device connection by polling, set the CNNIRQM bit of the INTR_USBHOST_MASK register to ‘0’ and check when the CNNIRQ bit of INTR_USBHOST changes to ‘1’.

31.3.2 Obtaining Transfer Speed of the USB Device

To obtain the possible transfer speed of the remote USB device after detecting a connection, check the value of the TMODE bit of the HOST_STATUS register. The following shows the relationships between the transfer speed and the value of the TMODE bit of HOST_STATUS.

- If TMODE=1, then the device is a full-speed device
- If TMODE=0, then the device is a low-speed device

Figure 31-2 shows the flow chart for device connection detection and obtaining the transfer speed.
31.3.3 USB Bus Reset

The USB bus is reset by sending SE0 for 10 ms or more if the URST bit of the HOST_STATUS register is set to ‘1’. After the USB bus is reset, the URST bit of HOST_STATUS is set to ‘0’, and the URIRQ bit of INTR_USBHOST is set to ‘1’. If the URIRQM bit of the INTR_USBHOST_MASK register is then set to ‘1’, an interrupt occurs. To clear this interrupt, write ‘1’ to the URIRQ bit of INTR_USBHOST.

Figure 31-3 shows the timing diagram for USB bus reset.
31.3.4 USB Packets

Exchange of information between the host and the device takes place in the form of packets, which are always initiated by the host. There are three types of USB packets:

- **Token**
- **Data**
- **Handshake**

The following sections explain about the settings required to initiate the packets by the PSoC 6 MCU USB host.

31.3.4.1 Token Packet

Endpoint 1 and Endpoint 2 buffers are used to send and receive data. If the DIR bit of the HOST_EP1_CTL register is ‘1’, the Endpoint 1 buffer is an OUT buffer. If the DIR bit of the HOST_EP2_CTL register is ‘0’, then the Endpoint 2 buffer is an IN buffer. Both the endpoints should never be configured as an OUT buffer or IN buffer simultaneously.

When issuing an IN, OUT, or SETUP token, use the following settings to process a token packet:

1. Set the BINI bit of the HOST_EP1_CTL and HOST_EP2_CTL registers to ‘1’.
2. Set the DIR bit of the HOST_EP1_CTL and HOST_EP2_CTL registers to ‘1’ or ‘0’.
3. Set the BINI bit of the HOST_EP1_CTL and HOST_EP2_CTL registers to ‘0’.
4. Specify the target address in the HOST_ADDR register.
5. Specify the maximum number of bytes for the packet in the PKS bitfield.
6. If the target Endpoint n (n=1 or 2) is set to OUT direction (HOST_EPn_CTL.DIR=1), write the data to be sent to the Endpoint n (n=1 or 2) buffer. Use HOST_EPn_WR1_DR for 1-byte data and HOST_EPn_WR2_DR for 2-byte data. Also, set ‘0’ to the EPnDRQ (n=1 or 2) bit of the INTR_HOST_EP register.
7. If the target endpoint is set to IN direction, read the EPnDRQ (n=1 or 2) bit of the INTR_HOST_EP register. A value of ‘1’ indicates that the packet transfer ended normally. Clear the EPnDRQ bit by writing ‘1’.
8. Specify the target endpoint, token, and toggle data in the Host Token Endpoint (HOST_TOKEN) register.

The USB PHY sends a token packet in the order of sync, token, address, endpoint, CRC5, and EOP based on the specified token; however, sync, CRC5, and EOP are sent automatically. After one packet is sent, the CMPIRQ bit of the INTR_USBHOST register is set to ‘1’. The TKNEN bit of the HOST_TOKEN register is set to ‘000’. At this time, if the CMPIRQM bit of INTR_USBHOST_MASK register is ‘1’, an interrupt occurs. To clear this interrupt, write ‘1’ to the CMPIRQ bit of the INTR_USBHOST register. Figure 31-6 shows the flow chart for setting up a SETUP token.
Figure 31-4. IN Token Flow Chart

START

Specify the target address in HOST_ADDR

Configure the transfer direction and packet size for the endpoints using the HOST_EPn_CTL (n=1,2) registers

Set HOST_EPn_CTL.BFINI=0 to clear the send/receive buffer initialization

HOST_TOKEN setting

HOST_TOKEN.TKNEN=setting value

Yes

No

INTR_USBHOST.CMPIRQ=1? Check for token transfer completion

Yes

No

Is SOF Lost

HOST_ERR.LSTSOF=1?

No

Check for Time out error

HOST_ERR.TOUT=1?

No

Check for toggle error

HOST_ERR.TGERR=1?

No

Check for Handshake error

HOST_ERR.HS=00?

No

Yes

Error Processing

No

Yes

Read received data from HOST_EPn_RWn_OR Register (n=1,2)

INTR_HOST_EP.EPnDRQ =1

No

Enable Endpoint Buffers

HOST_EPn_CTL.BFINI=1

END

Figure 31-5. OUT Token Flow Chart

START

Specify the target address in HOST_ADDR

Configure the transfer direction and packet size for the endpoints using the HOST_EPn_CTL (n=1,2) registers

Set HOST_EPn_CTL.BFINI=0 to clear the send/receive buffer initialization

Error Processing

Enumeration?

No

Yes

Write data to HOST_EPn_RWn_DR (n=1,2)

INTR_USBHOST.CMPIRQ=1? Check for token transfer completion

Yes

No

intr_HOST_EP.EPnDRQ=0 (n=1,2) to clear the interrupt cause

HOST_TOKEN setting

HOST_TOKEN.TKNEN=setting value

Yes

No

INTR_USBHOST.CMPIRQ=1? Check for token transfer completion

Yes

No

Is SOF Lost

HOST_ERR.LSTSOF=1?

Yes

Is SOF Lost

HOST_ERR.LSTSOF=1?

Yes

No

Check for Time out error

HOST_ERR.TOUT=1?

Yes

No

Check for toggle error

HOST_ERR.TGERR=1?

Yes

No

Check for Handshake error

HOST_ERR.HS=00?

Yes

No

Enable Endpoint Buffers

HOST_EPn_CTL.BFINI=1

END
Figure 31-6. SETUP Token Flow Chart

START

Specify the target address in HOST_ADDR

Configure the transfer direction and packet size for the endpoints using the HOST_EPn_CTL (n=1,2) registers

Set HOST_EPn_CTL.BFINI=0 to clear the send/receive buffer initialization

HOST_TOKEN setting

HOST_TOKEN.TKNEN =setting value

INTR_USBHOST.CMPIRQ=1? Check for token transfer completion

Is SOF Lost
HOST_ERR.LSTSOF=1?

Check for Time out error
HOST_ERR.TOUT=1?

Check for toggle error
HOST_ERR.TGERR=1?

Check for Handshake error
HOST_ERR.HS=00?

Enable Endpoint Buffers
HOST_EPn_CTL.BFINI=1

Error Processing

END
When issuing an SOF token, specify the EOF time in the Host EOF Setup (HOST_EOF) register and the frame number in the Host Frame Setup (HOST_FRAME) register respectively. Then, specify an SOF token code in the TKNEN bit of the HOST_TOKEN register. After sync, SOF token, frame number, CRC5, and EOP are sent, the SOFBUSY bit of the HOST_STATUS register is set to ‘1’, and the HOST_FRAME register is incremented by one. The CMPIRQ bit of the INTR_USBHOST register is also set to ‘1’, causing the TKNEN bit of the HOST_TOKEN register to be cleared to ‘000'. To clear a token completion interrupt, write ‘1’ to the CMPIRQ bit of the Host Interrupt (HIRQ) register.

An SOF is automatically sent every 1 ms while the SOFBUSY bit of the HOST_STATUS register is ‘1’. Figure 31-7 depicts steps to send an SOF token.

Figure 31-7. SOF Token Flow Chart

The conditions (SOF stop conditions) to set the SOFBUSY bit of the HOST_STATUS register to ‘0’ are as follows:
- Writing 0 to the SOFBUSY bit of HOST_STATUS
- Resetting the USB bus
- Writing 1 to the SUSP bit of HOST_STATUS
- Disconnecting the USB device (when the CSTAT bit of HOST_STATUS is ‘0’)

The HOST_EOF register is used to prevent the SOF from being sent simultaneously with other tokens. If the TKNEN bit of the HOST_TOKEN register is written within the time period specified by the HOST_EOF register, the specified token is placed into the wait state. After the SOF is sent, the token in the wait state is issued. The Host EOF Setup register specifies a 1-bit time as the time unit. For example, if ‘0x10’ is specified in the Host EOF Setup Register, the time is set to $16 \times 1/12 \text{MHz} = 1333.3 \text{ns}$ in the full-speed mode and $16 \times 1/1.5 \text{MHz} = 10666.6 \text{ns}$ in the low-speed mode. When the EOF setting is shorter than the 1-packet time, SOF may be sent doubly during execution of other tokens. In this case, the LSTSOF bit of the Host Error Status (HOST_ERR) register is set to ‘1’ and SOF is not sent. If ‘1’ is set to the LSTSOF bit of the HOST_ERR register, the value of the Host EOF Setup register must be increased.

Figure 31-8. SOF Timing
31.3.4.2 Data Packet

Follow these steps to send or receive a data packet after sending a token packet.

- Transmitting data (host to device)
  - Sync pattern is automatically sent.
  - If the TGGL bit of HOST_TOKEN is 0, DATA0 is sent. If the TGGL bit is 1, DATA1 is sent.
  - If the DIR bit of the HOST_EP1_CTL register is 1 (that is, if EP1 is an OUT endpoint), select the Endpoint 1 buffer; otherwise, select the Endpoint 2 buffer. Then, send all the target data.
  - 16-bit CRC is automatically sent.
  - 2-bit EOP is automatically sent.
  - 1-bit J State is automatically sent.

- Receiving data (device to host)
  - Receive sync.
  - Receive toggle data, and compare it with the value of the TGGL bit of HOST_TOKEN.
  - If the toggle data matches the value of the TGGL bit, check the DIR bit of HOST_EP1_CTL. If the DIR bit is 1, select the Endpoint 2 buffer; otherwise, select the Endpoint 1 buffer. Then, distribute the received data to the respective buffers.
  - Verify the 16-bit CRC when EOF is received.

31.3.4.3 Handshake Packet

A handshake packet is used to notify the remote device of the status of the local device. A handshake packet sends either one of ACK, NAK, and STALL from the receiving side when it is judged that the receiving side is ready to receive data normally. If the USB circuit receives a handshake packet, the type of the received handshake packet is set to the HS bit of the HOST_ERR register.

31.3.5 Retry Function

When a NAK or CRC error occurs at the end of a packet, if ‘1’ is set to the RETRY bit of the Host Control 2 (HOST_CTL2) register, processing is retried repeatedly for the period specified in the Host Retry Timer Setup (HOST_RTIMER) register.

When an error other than STALL or device disconnection occurs, the target token is retried if the RETRY bit of HOST_CTL2 is 1. The conditions to end retry processing are as follows.

- The RETRY bit of HOST_CTL2 is set to 0.
- ‘0’ is detected in the retry timer.
- The interrupt flag is generated by SOF (SOFIRQ of INTR_USBHOST = 1).
- ACK is detected.
- A device disconnection is detected.

The retry timer is activated at the start of a token and counted down by a 1-bit transfer clock. When the retry timer reaches ‘0’, the target token is sent and processing ends. If a token retry occurs in the EOF area, the retry timer is stopped until SOF is sent. After SOF is sent, the retry timer restarts with the value that is set when the timer stopped.

31.3.6 Error Status

The USB host supports detection of the following types of errors:

- Stuffing Error
  - If 1 is written to six successive bits, 0 is inserted into one bit. If 1 is successively detected in seven bits, it is regarded as a Stuffing error, and the STUFF bit of the HOST_ERR register is set to 1. To clear this status, write ‘1’ to the STUFF bit.

- Toggle Error
  - When sending an IN token, the toggle data of a data packet is compared with the value of the TGGL bit of the HOST_TOKEN register. If they do not match, the TGERR bit of the HOST_ERR register is set to 1. To clear the TGERR bit, write ‘1’ to the TGERR bit of HOST_ERR.

- CRC Error
  - When receiving an IN token, the data and CRC of the received data packet are obtained with the CRC polynomial G(X) = X16 + X15 + X2 + 1. If the remainder is not 0x800D, it means that a CRC Error has occurred, and the CRC bit of the HOST_ERR register is set to 1. To clear the CRC bit, write ‘1’ to the CRC bit of HOST_ERR.

- Time Out Error
  - The TOUT bit of the HOST_ERR register is set and time out error is considered under any of the following conditions:
    - A data packet or handshake packet is not input in the specified time
    - SE0 is detected when receiving data
    - Stuffing error is detected
  - To clear the TOUT bit, write 0 to the TOUT bit of the HOST_ERR register.

- Receive Error
  - The PKS bit of Endpoint Control register (HOST_EPn_CTL; n=1, 2) indicates the receiver packet size. When the received data exceeds the specified receive packet size, the RERR bit of the HOST_ERR register is set to 1. To clear the RERR bit, write ‘1’ to the RERR bit of HOST_ERR.

- Lost SOF Error
  - When LSTSOF bit of the HOST_ERR register is set, it means that the SOF token cannot be sent because another token is in process. When this bit is ‘1’, it means that no lost SOF error is detected.
31.3.7 End of Packet (EOP)

If a packet ends in the USB host, the CMPIRQ bit of the INTR_USBHOST register is set to 1. At this time, if the CMPIRQM bit of the INTR_USBHOST_MASK register is 1, an interrupt occurs.

When a packet ends, the interrupt flag is generated when the TKNEN bit of the HOST_TOKEN register is set as ‘001’ (SETUP token), ‘010’ (IN token), ‘011’ (OUT token), or ‘100’ (SOF token).

![Figure 31-9. EOP Interrupt Timing Diagram (for SOF token)](image)

Write data to the TKNEN bit of HTOKEN.

```
CMPIRQ bit (HIRQ)
```

31.3.8 Interrupt Sources

The USB host generates 11 interrupts to the CPU. These interrupts are mapped to three general-purpose interrupt lines: INTR_LO, INTR_MED, and INTR_HI. Each of these three interrupt lines has an associated status register, which identifies the cause of the interrupt event. These are INTR_USBHOST_CAUSE_LO, INTR_USBHOST_CAUSE_MED, INTR_USBHOST_CAUSE_HI, INTR_HOST_EP_CAUSE_LO, INTR_HOST_EP_CAUSE_MED, and INTR_HOST_EP_CAUSE_HI.

![Figure 31-10. USB Host Interrupt Sources](image)
The following events generate an interrupt on one of the three interrupt lines:

- **Start-of-frame (SOF) event**
  SOF interrupt is generated when an SOF token is sent. The SOF interrupt is enabled by setting the SOFIRQM bit of the INTR_USBHOST_MASK register. The status of the SOF interrupt is reflected in the SOFIRQ bit of the INTR_USBHOST register.

- **Device connection and disconnection events**
  The CNNIRQ bit of the INTR_USBHOST register is set to ‘1’ when a device connection is detected. The interrupt can be enabled by setting the CNNIRQM bit of the INTR_USBHOST_MASK register. When a device is disconnected, an interrupt is generated if the DIRQM bitfield of INTR_USBHOST_MASK is set to ‘1’. The status of the device disconnection is reflected in the DIRQ bit of the INTR_USBHOST register.

- **USB bus reset event**
  The URIRQ bit of the INTR_USBHOST register is set when the USB bus reset ends. An interrupt is generated if the URIRQM bit of the INTR_USBHOST_MASK register is set to ‘1’.

- **Token completion event**
  When token (IN, OUT, or SETUP token) processing is complete, the CMPIRQ bit of the INTR_USBHOST_MASK register is set to ‘1’. An interrupt is generated if the CMPIRQM bit is set to ‘1’.

- **Interrupt on resume event**
  The RWKIRQ bit of the INTR_USBHOST register is set when the host enters the resume state from suspend state. The RWKIRQ bit is set under the following conditions:
  - The SUSP bit of the HOST_STATUS register is set to ‘0’.
  - The D+/D– pins are placed in the K-state.
  - A device connection/disconnection is detected.
  An interrupt is generated on a resume event if the RWKIRQM bit of the INTR_USBHOST_MASK register is set to ‘1’.

- **Interrupt on token cancellation**
  An interrupt is generated when a token send is canceled based on the setting of the CANCEL bit in the Host Control 2 register (HOST_CTL2). If the CANCEL bit is set and if the target token is written to the HOST_TOKEN register in the EOF area (specified in the Host EOF Setup register), the token send is canceled.

- **Endpoint interrupts**
  The PSoC 6 MCU USB host has two endpoints: Endpoint1 and Endpoint2. Each endpoint can generate two interrupts. When the packet transfer of an endpoint ends normally, the EPnDRQ (n=1 or 2) bit of the INTR_HOST_EP register is set to ‘1’. An interrupt can be triggered if the EPnDRQM (n=1 or 2) bit of the INTR_HOST_EP_MASK register is set to ‘1’. If the packet size does not match the packet size specified in the PKS bit of the HOST_EPn_CTL (n=1 or 2) register, the EPnSPK (n=1 or 2) bit of the INTR_HOST_EP register is set. An interrupt can be configured by setting the EPnSPKM (n=1 or 2) bit of the INTR_HOST_EP_MASK register.

### 31.3.9 DMA Transfer Function

Data handled by the USB host can be transferred via DMA between the send/receive buffer and the internal RAM. There are two modes of DMA transfer:

- **Packet transfer mode**
- **Automatic data size transfer mode**

#### 31.3.9.1 Packet Transfer Mode

The packet transfer mode transfers each packet according to the configured data size in DMA. This transfer mode can access each buffer of the endpoints.

In the packet transfer mode the OUT direction transfer (host to device) involves the following sequence of steps:

1. After the EPnDRQ bit (n=1 or 2) of the INTR_HOST_EP register is set and the interrupt handling is entered, configure the DMA register settings relevant to the number of transfers and block size corresponding to the data size to be transferred in the next OUT packet; then, enable DMA to start the transfer.

2. After the DMA transfer, clear the EPnDRQ bit (n=1 or 2) of the INTR_HOST_EP register and the interrupt cause flag of DMAC, and return from the interrupt handling.
The data transfer in the IN direction (device to host) involves the following sequence of steps:

1. After the EPnDRQ bit (n=1 or 2) of the INTR_HOST_EP register is set and the interrupt handling is entered, check the transfer data size.
2. Configure the DMA register setting relevant to the number of transfers and block size corresponding to the transfer data size, and then enable DMA to start the transfer.
3. After the transfer, clear the EPnDRQ bit (n=1 or 2) of the INTR_HOST_EP register and the interrupt source flag of DMAC, and return from the interrupt handling.

### 31.3.9.2 Automatic Data Transfer Mode

Automatic data transfer mode is enabled by setting the DMAE bit of the HOST_EPn_CTL register (n=1 or 2). When the EPnDRQ bit (n=1 or 2) of the INTR_HOST_EP register is set while DMAE is enabled, the DMA request is automatically cleared when the data size corresponding to PKS bits of the HOST_EPn_CTL register (n=1 or 2) has been transferred. Later, the same sequence is repeated until the data size configured in the DMA is reached. In this mode, configuration by software is not required. Thus, this mode can transfer data automatically by a single setting. It can also transfer even bytes; to transfer odd bytes, a software transfer sequence is required.
The data transfer in the OUT direction (host to device) must be processed in the following sequence:

1. Configure the DMA register setting relevant to the number of transfers and block size corresponding to the total data size, and then enable DMA to start the transfer.
2. Set the packet size and total number of bytes for DMA transfer to PKS bits of the HOST_EPn_CTL (n=1 or 2) register and BLK_NUM bits of the HOST_EPn_BLK (n=1 or 2) register, respectively.
3. Enable DMAE bit of the HOST_EPn_CTL (n=1 or 2) register and EPnDRQE bit of the Host DMA Enable (HOST_DMA_ENBL) (n=1 or 2) register.
4. After the transfer, reconfigure the DMAC using an interrupt generated by the DMA controller, and clear the flag to return from interrupt handling.

To transfer the odd bytes of data via DMA, write the last byte of data by software transfer.

The data transfer in the IN direction (device to host) must be processed in the following sequence:

1. Configure the DMA register setting relevant to the number of transfers and block size corresponding to the total data size, and then enable DMA to start the transfer.
2. Enable DMAE bit of the HOST_EPn_CTL (n=1 or 2) register and EPnDRQE bit of the HOST_DMA_ENBL (n=1 or 2) register.
3. After the transfer, reconfigure the DMA controller using an interrupt generated by the DMAC and clear the flag to return from interrupt handling.

To transfer the data size corresponding to odd number of bytes via DMA, either of the following methods can be used:
- Use the software transfer only for the last data, and read the low-order byte (HOST_EPn_RW1_DR: n=1 or 2).
- Transfer all the data + 1 byte via DMA, and discard the last data after an endian conversion.
31.3.10 Suspend and Resume Operations

The USB host supports suspend and resume operations.

31.3.10.1 Suspend Operation

If '1' is set to the SUSP bit of the HOST_STATUS register, the following procedure is performed, and the USB circuit is placed in the suspend state.

- The USB bus is placed in the high-impedance state.
- All circuit blocks with no clock required are stopped.

31.3.10.2 Resume Operation

The USB bus changes from the suspend state to the resume state to start processing when one of the following conditions is satisfied.

- 0 is set to the SUSP bit of the HOST_STATUS register.
- The D+ or D– pin is placed in the K-state mode by the device.
- A device disconnection is detected.
- A device connection is detected.

The host can start issuing tokens when RWKIRQ bit of the INTR_USBHOST register is set to ‘1’.

The following timing diagrams illustrate each resume condition.

- '0' is set to the SUSP bit of the HOST_STATUS register.
- '1' is set to the SUSP bit of the HOST_STATUS register.
- The D+ or D– pin is placed in the K-state mode.
- The D+ or D– pin is placed in the K-state mode.

**Figure 31-17. Resume Operation with Register (Full-speed mode)**

**Figure 31-18. Resume Operation by Device (Full-speed mode)**
### 31.3.11 Device Disconnection

The device disconnection timer starts when both the D+ and D– pins are set to LOW. If both D+ and D– remain at LOW for 2.5 µs or more, the device is considered to be disconnected. This then sets the CSTAT bit of the HOST_STATUS register as '0' and the DIRQ bit of the INTR_USBHOST register as '1'. At this time, if the DIRQM bit of the INTR_USBHOST_MASK register is 1, an interrupt occurs. To clear this interrupt, write '1' to the DIRQ bit of the INTR_USBHOST register.

If the USB bus is reset, the device is considered to be disconnected. In this case, the CSTAT bit of the HOST_STATUS register is set to 0, but the DIRQ bit of the INTR_USBHOST register is not set to 1.
# USB Host Registers

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>HOST_CTL0</td>
<td>Host control 0 register</td>
</tr>
<tr>
<td>HOST_CTL1</td>
<td>Host control 1 register</td>
</tr>
<tr>
<td>HOST_CTL2</td>
<td>Host control 2 register</td>
</tr>
<tr>
<td>HOST_ERR</td>
<td>Host error status register</td>
</tr>
<tr>
<td>HOST_STATUS</td>
<td>Host status register</td>
</tr>
<tr>
<td>HOST_FCOMP</td>
<td>Host SOF interrupt frame compare register</td>
</tr>
<tr>
<td>HOST_RTIMER</td>
<td>Host retry timer setup register</td>
</tr>
<tr>
<td>HOST_ADDR</td>
<td>Host address register</td>
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<tr>
<td>HOST_EOF</td>
<td>Host EOF setup register</td>
</tr>
<tr>
<td>HOST_FRAME</td>
<td>Host frame setup register</td>
</tr>
<tr>
<td>HOST_TOKEN</td>
<td>Host token endpoint register</td>
</tr>
<tr>
<td>HOST_EP1_CTL</td>
<td>Host endpoint 1 control register</td>
</tr>
<tr>
<td>HOST_EP1_STATUS</td>
<td>Host endpoint 1 status register</td>
</tr>
<tr>
<td>HOST_EP1_RW1_DR</td>
<td>Host endpoint 1 data 1-byte register</td>
</tr>
<tr>
<td>HOST_EP1_RW2_DR</td>
<td>Host endpoint 1 data 2-byte register</td>
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<tr>
<td>HOST_EP2_CTL</td>
<td>Host endpoint 2 control register</td>
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<td>HOST_EP2_STATUS</td>
<td>Host endpoint 2 status register</td>
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<td>HOST_EP2_RW2_DR</td>
<td>Host endpoint 2 data 2-byte register</td>
</tr>
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<td>Host interrupt level 1 selection register</td>
</tr>
<tr>
<td>HOST_LVL2_SEL</td>
<td>Host interrupt level 2 selection register</td>
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<tr>
<td>INTR_USBHOST_CAUSE_HI</td>
<td>Interrupt USB host cause high register</td>
</tr>
<tr>
<td>INTR_USBHOST_CAUSE_MED</td>
<td>Interrupt USB host cause medium register</td>
</tr>
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<td>Interrupt USB host cause low register</td>
</tr>
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<td>Host endpoint 1 block register</td>
</tr>
<tr>
<td>HOST_EP2_BLK</td>
<td>Host endpoint 2 block register</td>
</tr>
</tbody>
</table>
32. LCD Direct Drive

The PSoC 6 MCU Liquid Crystal Display (LCD) drive system is a highly configurable peripheral that allows the device to directly drive STN and TN segment LCDs.

32.1 Features

The PSoC 6 MCU LCD segment drive block has the following features:

- Supports up to 56 segments and 8 commons
- Supports Type A (standard) and Type B (low-power) drive waveforms
- Any GPIO can be configured as a common or segment
- Supports five drive methods:
  - Digital correlation
  - PWM at 1/2 bias
  - PWM at 1/3 bias
  - PWM at 1/4 bias
- Ability to drive 3-V displays from 1.8 V \( V_{DD} \) in Digital Correlation mode
- Operates in Active, Sleep, and Deep Sleep modes
- Digital contrast control

32.2 Architecture

32.2.1 LCD Segment Drive Overview

A segmented LCD panel has the liquid crystal material between two sets of electrodes and various polarization and reflector layers. The two electrodes of an individual segment are called commons (COM) or backplanes and segment electrodes (SEG). From an electrical perspective, an LCD segment can be considered as a capacitive load; the COM/SEG electrodes can be considered as the rows and columns in a matrix of segments. The opacity of an LCD segment is controlled by varying the root-mean-square (RMS) voltage across the corresponding COM/SEG pair.

The following terms/voltages are used in this chapter to describe LCD drive:

- \( V_{RMSOFF} \): The voltage that the LCD driver can realize on segments that are intended to be off.
- \( V_{RMSON} \): The voltage that the LCD driver can realize on segments that are intended to be on.
- Discrimination Ratio (D): The ratio of \( V_{RMSON} \) and \( V_{RMSOFF} \) that the LCD driver can realize. This depends on the type of waveforms applied to the LCD panel. Higher discrimination ratio results in higher contrast.

Liquid crystal material does not tolerate long term exposure to DC voltage. Therefore, any waveforms applied to the panel must produce a 0-V DC component on every segment (on or off). Typically, LCD drivers apply waveforms to the COM and SEG electrodes that are generated by switching between multiple voltages. The following terms are used to define these waveforms:

- **Duty**: A driver is said to operate in 1/M duty when it drives ‘M’ number of COM electrodes. Each COM electrode is effectively driven 1/M of the time.

- **Bias**: A driver is said to use 1/B bias when its waveforms use voltage steps of \((1/B) \times V_{DRV}\). \(V_{DRV}\) is the highest drive voltage in the system (equals \( V_{DD} \)). The PSoC 6 MCU supports 1/2, 1/3, and 1/4 biases in PWM drive modes.
- **Frame**: A frame is the length of time required to drive all the segments. During a frame, the driver cycles through the commons in sequence. All segments receive 0-V DC (but non-zero RMS voltage) when measured over the entire frame.

The PSoC 6 MCU supports two different types of drive waveforms in all drive modes. These are:

- **Type-A Waveform**: In this type of waveform, the driver structures a frame into M sub-frames. ‘M’ is the number of COM electrodes. Each COM is addressed only once during a frame. For example, COM[i] is addressed in sub-frame i.

- **Type-B Waveform**: The driver structures a frame into 2M sub-frames. The two sub-frames are inverses of each other. Each COM is addressed twice during a frame. For example, COM[i] is addressed in sub-frames i and M+i. Type-B waveforms are slightly more power efficient because it contains fewer transitions per frame.

### 32.2.2 Drive Modes

The PSoC 6 MCU supports the following drive modes.

- PWM drive at 1/2 bias
- PWM drive at 1/3 bias
- PWM drive at 1/4 bias with high-frequency clock input
- Digital correlation

#### 32.2.2.1 PWM Drive

In PWM drive mode, multi-voltage drive signals are generated using a PWM output signal together with the intrinsic resistance and capacitance of the LCD. Figure 32-1 illustrates this.
The output waveform of the drive electronics is a PWM waveform. With the Indium Tin Oxide (ITO) panel resistance and the segment capacitance to filter the PWM, the voltage across the LCD segment is an analog voltage, as shown in Figure 32-1. This figure illustrates the generation of a 1/3 bias waveform (four commons and voltage steps of \( V_{DD}/3 \)). See the Clocking System chapter on page 146 for details.

The PWM is derived from either CLK_LF (32 kHz, low-speed operation) or CLK_PERI (high-speed operation). See the Clocking System chapter on page 146 for more details of peripheral and low-frequency clocks. The filtered analog voltage across the LCD segments typically runs at low frequency for segment LCD driving.

Figure 32-2 and Figure 32-3 illustrate the Type A and Type B waveforms for COM and SEG electrodes for 1/2 bias and 1/4 duty. Only COM0/COM1 and SEG0/SEG1 are drawn for demonstration purpose. Similarly, Figure 32-4 and Figure 32-5 illustrate the Type A and Type B waveforms for COM and SEG electrodes for 1/3 bias and 1/4 duty.
Figure 32-2. PWM1/2 Type-A Waveform Example

One frame of Type A waveform (addresses all segments once)

Resulting voltage across segments ($V_{DC} = 0$)

Discrimination ratio: $D = \frac{0.661}{0.433} = 1.527$
Figure 32-3. PWM1/2 Type-B Waveform Example

One frame of Type B waveform
(addresses all segments twice)

Resulting voltage across segments
($V_{dc} = 0$)

Segment On:
$V_{rms} = 0.661 \times V_{dd}$

Segment Off:
$V_{rms} = 0.433 \times V_{dd}$

Discrimination ratio:
$D = 0.661/0.433 = 1.527$
Figure 32-4. PWM1/3 Type-A Waveform Example

One Frame of Type A Waveform
(addresses all segments once)

COM0
2/3 VDD
1/3 VDD
0

COM1
2/3 VDD
1/3 VDD
0

SEG0
2/3 VDD
1/3 VDD
0

SEG1
2/3 VDD
1/3 VDD
0

Resulting voltage across segments
(VDD = 0)

COM0-SEG0
Segment On:
V_{\text{last}} = 0.577 V_{\text{DD}}

COM0-SEG1
Segment Off:
V_{\text{last}} = 0.333 V_{\text{DD}}

COM1-SEG0
Segment On:
V_{\text{last}} = 0.577 V_{\text{DD}}

COM1-SEG1
Segment Off:
V_{\text{last}} = 0.333 V_{\text{DD}}

Discrimination ratio:
D = \frac{0.577}{0.333} = 1.732

Segment is On
Segment is Off
Figure 32-5. PWM1/3 Type-B Waveform Example

One Frame of Type B Waveform
(addresses all segments twice)

Resulting voltage across segments
($V_{DC} = 0$)

Segment On:
$V_{RMS} = 0.577 V_{DD}$
Segment Off:
$V_{RMS} = 0.333 V_{DD}$

Discrimination ratio:
$D = \frac{0.577}{0.333} = 1.732$
The effective RMS voltage for ON and OFF segments can be calculated easily using these equations:

\[
V_{RMS(ON)} = \frac{B^2 + 2(M-1)Y_{OBS}}{2M} \\
V_{RMS(OFF)} = \frac{B^2}{\sqrt{\frac{2(2-M) + 2(M-1)Y_{OBS}}{B}}} 
\]

**Equation 32-1**

**Equation 32-2**

Where B is the bias and M is the duty (number of COMs).

For example, if the number of COMs is four, the resulting discrimination ratios (D) for 1/2 and 1/3 biases are 1.528 and 1.732, respectively. 1/3 bias offers better discrimination ratio in two and three COM drives also. Therefore, 1/3 bias offers better contrast than 1/2 bias and is recommended for most applications. 1/4 bias is available only in high-speed operation of the LCD. They offer better discrimination ratio especially when used with high COM designs (more than four COMs).

When the low-speed operation of LCD is used, the PWM signal is derived from the 32-kHz CLK_LF. To drive a low-capacitance display with acceptable ripple and rise/fall times using a 32-kHz PWM, additional external series resistances of 100 kΩ - 1 MΩ should be used. External resistors are not required for PWM frequencies greater than ~1 MHz. The ideal PWM frequency depends on the capacitance of the display and the internal ITO resistance of the ITO routing traces.

The 1/2 bias mode has the advantage that PWM is only required on the COM signals; the SEG signals use only logic levels, as shown in Figure 32-2 and Figure 32-3.

### 32.2.2.2 Digital Correlation

The digital correlation mode, instead of generating bias voltages between the rails, takes advantage of the characteristic of LCDs that the contrast of LCD segments is determined by the RMS voltage across the segments. In this approach, the correlation coefficient between any given pair of COM and SEG signals determines whether the corresponding LCD segment is on or off. Thus, by doubling the base drive frequency of the COM signals in their inactive sub-frame intervals, the phase relationship of the COM and SEG drive signals can be varied to turn segments on and off. This is different from varying the DC levels of the signals as in the PWM drive approach. Figure 32-8 and Figure 32-9 are example waveforms that illustrate the principles of operation.
Figure 32-6. Digital Correlation Type-A Waveform

One Frame of Type A Waveform
(addresses all segments once)

Segment On:
VRMS = 0.791 VDD
(VDC = 0)

Segment Off:
VRMS = 0.612 VDD

Discrimination ratio:
D = 0.791/0.612 = 1.291

Resulting voltage across segments
(VDC = 0)

Segment On:
V_{res} = 0.791 V_{DD}

Segment Off:
V_{res} = 0.612 V_{DD}

Discrimination ratio:
D = 0.791/0.612 = 1.291
Figure 32-7. Digital Correlation Type-B Waveform

One Frame of Type B Waveform
(addresses all segments twice)

Resulting voltage across segments
($V_{DC} = 0$)

Segment On:
$V_{rms} = 0.791 V_{DD}$

Segment Off:
$V_{rms} = 0.612 V_{DD}$

Segment is On

Segment is Off

Discrimination ratio:
$D = \frac{0.791}{0.612} = 1.291$
The RMS voltage applied to on and off segments can be calculated as follows:

\[
V_{RMS(\text{OFF})} = \frac{(M-1)}{2M} \times V_{DD}
\]

\[
V_{RMS(\text{ON})} = \frac{2 + (M-1)}{2M} \times V_{DD}
\]

Where B is the bias and M is the duty (number of COMs). This leads to a discrimination ratio (D) of 1.291 for four COMs. Digital correlation mode also has the ability to drive 3-V displays from 1.8-V \( V_{DD} \).

### 32.2.3 Recommended Usage of Drive Modes

The PWM drive mode has higher discrimination ratios compared to the digital correlation mode, as explained in 32.2.2.1 PWM Drive and 32.2.2.2 Digital Correlation. Therefore, the contrast in digital correlation method is lower than PWM method but digital correlation has lower power consumption because its waveforms toggle at low frequencies.

The digital correlation mode creates reduced, but acceptable contrast on TN displays, but no noticeable difference in contrast or viewing angle on higher contrast STN displays. Because each mode has strengths and weaknesses, recommended usage is as follows.

#### Table 32-1. Recommended Usage of Drive Modes

<table>
<thead>
<tr>
<th>Display Type</th>
<th>Deep Sleep Mode</th>
<th>Sleep/Active Mode</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Four COM TN Glass</td>
<td>Digital correlation</td>
<td>PWM 1/3 bias</td>
<td>Firmware must switch between LCD drive modes before going to deep sleep or waking up.</td>
</tr>
<tr>
<td>Four COM STN Glass</td>
<td>Digital correlation</td>
<td>No contrast advantage for PWM drive with STN glass.</td>
<td></td>
</tr>
<tr>
<td>Eight COM, STN</td>
<td>Not supported</td>
<td>PWM 1/4 bias</td>
<td>Supported only in the high-speed LCD mode. The low-speed clock is not fast enough to make the PWM work at high multiplex ratios.</td>
</tr>
</tbody>
</table>

### 32.2.4 Digital Contrast Control

In all drive modes, digital contrast control can be used to change the contrast level of the segments. This method reduces contrast by reducing the driving time of the segments. This is done by inserting a ‘Dead-Time’ interval after each frame. During dead time, all COM and SEG signals are driven to a logic 1 state. The dead time can be controlled in fine resolution. Figure 32-8 illustrates the dead-time contrast control method for 1/3 bias and 1/4 duty implementation.
Figure 32-8. Dead-Time Contrast Control

Two Frames of Type A Waveform with Deadtime
(Example for 1/4th Duty and 1/3rd bias)
32.3 PSoC 6 MCU Segment LCD Direct Drive

The LCD controller block contains two generators; one with a high-speed clock source CLK_PERI and the other with a low-speed clock source (32 kHz) derived from the CLK_LF. These are called high-speed LCD master generator and low-speed LCD master generator, respectively. Both the generators support PWM and digital correlation drive modes. PWM drive mode with low-speed generator requires external resistors, as explained in PWM Drive on page 359.

The multiplexer selects one of these two generator outputs to drive LCD, as configured by the firmware. The LCD pin logic block routes the COM and SEG outputs from the generators to the corresponding I/O matrices. Any GPIO can be used as either COM or SEG. This configurable pin assignment for COM or SEG is implemented in GPIO and I/O matrix; see High-Speed I/O Matrix. These two generators share the same configuration registers. These memory mapped I/O registers are connected to the system bus (AHB) using an AHB interface.

The LCD controller works in three device power modes: Active, Sleep, and Deep Sleep. High-speed operation is supported in Active and Sleep modes. Low-speed operation is supported in Active, Sleep, and Deep Sleep modes. The LCD controller is unpowered in Hibernate mode.

32.3.1 High-Speed and Low-Speed Master Generators

The high-speed and low-speed master generators are similar to each other. The only exception is that the high-speed version has larger frequency dividers to generate the frame and sub-frame periods. The high-speed generator is in the active power domain and the low-speed generator is in the Deep Sleep power domain. A single set of configuration registers is provided to control both high-speed and low-speed blocks. Each master generator has the following features and characteristics:
Register bit configuring the block for either Type A or Type B drive waveforms (LCD_MODE bit in LCD_CONTROL register).

- Register bits to select the number of COMs (COM_NUM field in LCD_CONTROL register).
- Operating mode configuration bits enabled to select one of the following:
  - Digital correlation
  - PWM 1/2 bias
  - PWM 1/3 bias
  - PWM 1/4 bias (not supported in low-speed generator)
  - Off/disabled. Typically, one of the two generators will be configured to be Off

OP_MODE and BIAS fields in LCD_CONTROL bits select the drive mode.

- A counter to generate the sub-frame timing. The SUBFR_DIV field in the LCD_DIVIDER register determines the duration of each sub-frame. If the divide value written into this counter is C, the sub-frame period is 4 × (C+1). The low-speed generator has an 8-bit counter. This counter generates a maximum half sub-frame period of 8 ms from the 32-kHz CLK_LF. The high-speed generator has a 16-bit counter.

- A counter to generate the dead time period. These counters have the same number of bits as the sub-frame period counters and use the same clocks. DEAD_DIV field in the LCD_DIVIDER register controls the dead time period.

### 32.3.2 Multiplexer and LCD Pin Logic

The multiplexer selects the output signals of either high-speed or low-speed master generator blocks and feeds it to the LCD pin logic. This selection is controlled by the configuration and control register. The LCD pin logic uses the sub-frame signal from the multiplexer to choose the display data. This pin logic will be replicated for each LCD pin.

### 32.3.3 Display Data Registers

Each LCD segment pin is part of an LCD port with its own display data register, LCD_DATAx. The device has eight such LCD ports. Note that these ports are not real pin ports but the ports/connections available in the LCD hardware for mapping the segments to commons. Each LCD segment configured is considered as a pin in these LCD ports. The LCD_DATAx registers are 32-bit wide and store the ON/OFF data for all SEG-COM combination enabled in the design. For example, LCD_DATA0 holds SEG-COM data for COM0 to COM3 and LCD_DATA1 holds SEG-COM data for COM4 to COM7. The bits [4+i:3] (where 'i' is the pin number) of each LCD_DATA0 register represent the ON/OFF data for Pin[i] in Port[x] and COM[3,2,1,0] combinations, as shown in Table 32-2. The LCD_DATAx register should be programmed according to the display data of each frame. The display data registers are Memory Mapped I/O (MMIO) and accessed through the AHB slave interface. See the device datasheet for the pin connections.

### 32.4 Register List

#### Table 32-2. SEG-COM Mapping Example of LCD_DATA0 Register (each SEG is a pin of the LCD port)

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>PIN_7-COM3</td>
<td>PIN_7-COM2</td>
</tr>
<tr>
<td>PIN_5-COM3</td>
<td>PIN_5-COM2</td>
</tr>
<tr>
<td>PIN_3-COM3</td>
<td>PIN_3-COM2</td>
</tr>
<tr>
<td>PIN_1-COM3</td>
<td>PIN_1-COM2</td>
</tr>
</tbody>
</table>

#### Table 32-3. LCD Direct Drive Register List

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCD_ID</td>
<td>This register includes the information of LCD controller ID and revision number</td>
</tr>
<tr>
<td>LCD_DIVIDER</td>
<td>This register controls the sub-frame and dead-time period</td>
</tr>
<tr>
<td>LCD_CONTROL</td>
<td>This register is used to configure high-speed and low-speed generators</td>
</tr>
<tr>
<td>LCD_DATA0</td>
<td>LCD port pin data register for COM0 to COM3</td>
</tr>
<tr>
<td>LCD_DATA1</td>
<td>LCD port pin data register for COM4 to COM7</td>
</tr>
</tbody>
</table>
33. Universal Digital Blocks (UDB)

This chapter shows the design details of the PSoC 6 MCU universal digital blocks (UDBs). The UDB architecture implements a balanced approach between configuration granularity and efficiency; UDBs have a combination of programmable logic devices (PLDs), structured logic (datapaths), and a flexible routing scheme.

33.1 Features

- PSoC 6 MCUs contain an array of twelve UDBs
- For optimal flexibility, each UDB contains several components:
  - An ALU-based 8-bit datapath (DP) with multiple registers, FIFOs, and an 8-word instruction store
  - Two PLDs, each with 12 inputs, eight product terms, and four macrocell outputs
  - Control and status modules
  - Clock and reset modules
- Flexible routing through the UDB array
- Portions of UDBs can be shared or chained to enable larger functions
- Flexible implementations of multiple digital functions, including timers, counters, PWM (with dead band generator), UART, SPI, and CRC generation/checking
- Register-based interface to CPU

33.2 Architecture

Figure 33-1 shows the components of a single UDB: two PLDs, a datapath, and control, status, clock and reset functions.

Figure 33-1. Single UDB Block Diagram
Figure 33-2 shows how the array of four UDBs interfaces with the rest of the PSoC 6 MCU.

The major components of a UDB are:

- **PLDs (2)** – These blocks take inputs from the routing channel and form registered or combinational sum-of-products logic to implement state machines, control for datapath operations, conditioning inputs, and driving outputs.

- **Datapath** – This block contains a dynamically programmable ALU, four registers, two FIFOs, comparators, and condition generation.

- **Control and Status** – These modules provide a way for CPU firmware to interact and synchronize with UDB operation.

- **Reset and Clock Control** – These modules provide clock selection and enabling, and reset selection, for the other blocks in the UDB.

- **Chaining Signals** – The PLDs and datapath have chaining signals that enable neighboring UDBs to be linked, to create higher precision functions.

- **Routing Channel** – UDBs are connected to the routing channel through a programmable switch matrix for connections between blocks in one UDB, and to all other UDBs in the array.

- **System Bus Interface** – All registers and RAM in each UDB are mapped into the system address space and are accessible by the CPU as 8, 16 and 32-bit accesses.

### 33.2.1 Programmable Logic Device (PLD)

Each UDB has two “12C4” PLDs. The PLD blocks, shown in Figure 33-3, can be used to implement state machines, perform input or output data conditioning, and to create lookup tables (LUTs). PLDs may also be configured to perform arithmetic functions, sequence the datapath, and generate status. General-purpose RTL can be synthesized and mapped to the PLD blocks. This section presents an overview of the PLD design.
33.2.1.1 PLD Macrocells

Figure 33-4 shows the macrocell architecture. The output drives the routing array and can be registered or combinational. The registered modes are D Flip-Flop (DFF) with true or inverted input and Toggle Flip-Flop (TFF) on input high or low. The output register can be set or reset for purposes of initialization, or asynchronously during operation under control of a routed signal.
PLD Macrocell Read-Only Registers

The outputs of the eight macrocells in the two PLDs can be accessed by the CPU as an 8-bit read-only register. Macrocells across multiple UDBs can be accessed as 16 or 32-bit read-only registers. See “UDB Addressing” on page 409.

33.2.1.2 PLD Carry Chain

PLDs are chained together in UDB address order. As shown in Figure 33-5, the carry chain input “selin” is routed from the previous UDB in the chain through each macrocell in both PLDs, and then to the next UDB as the carry chain out “selout”. To support the efficient mapping of arithmetic functions, special product terms are generated and used in the macrocell in conjunction with the carry chain.

Figure 33-5. PLD Carry Chain and Special Product Term Inputs

33.2.1.3 PLD Configuration

The PLDs can be configured by accessing a set of 16 or 32-bit registers; see “UDB Addressing” on page 409.

33.2.2 Datapath

The datapath, shown in Figure 33-6, contains an 8-bit single-cycle ALU, with associated compare and condition generation circuits. A datapath may be chained with datapaths in neighboring UDBs to achieve higher precision functions. The datapath includes a small dynamic configuration RAM, which can dynamically select the operation to perform in a given cycle. The datapath is optimized to implement typical embedded functions such as timers, counters, PWMs, PRS, CRC, shifters, and dead band generators. The add and subtract functions allow support for digital delta-sigma operations.
33.2.2.1 Overview

The following are key datapath features:

Dynamic Configuration

Dynamic configuration is the ability to change the datapath function and interconnect on a cycle-by-cycle basis, under sequencer control. This is implemented using the configuration RAM, which stores eight unique configurations. The address input to this RAM can be routed from any block connected to the routing fabric, typically PLD logic, I/O pins, or other datapaths.

ALU

The ALU can perform eight general-purpose functions: increment, decrement, add, subtract, AND, OR, XOR, and PASS. Function selection is controlled by the configuration RAM on a cycle-by-cycle basis. Independent shift (left, right, nibble swap) and masking operations are available at the output of the ALU.

Conditionals

Each datapath has two comparators with bit masking options, which can be configured to select a variety of datapath register inputs for comparison. Other detectable conditions include all zeros, all ones, and overflow. These conditions form the primary datapath output selects to be routed to the digital routing fabric as inputs to other functions.

Built-in CRC/PRS

The datapath has built-in support for single-cycle cyclic redundancy check (CRC) computation and pseudo random sequence (PRS) generation of arbitrary width and arbitrary polynomial specification. To achieve longer than 8-bit CRC/PRS widths, signals may be chained between datapaths. This feature is controlled dynamically and therefore, can be interleaved with other functions.

Variable MSb

The most significant bit of an arithmetic and shift function can be programatically specified. This supports variable width CRC/PRS functions and, in conjunction with ALU output masking, can implement arbitrary width timers, counters, and shift blocks.

Input/Output FIFOs

Each datapath contains two 4-byte FIFOs, which can be individually configured for direction as an input buffer (CPU
writes to the FIFO, datapath internals read the FIFO), or an output buffer (datapath internals write to the FIFO, the CPU reads from the FIFO). These FIFOs generate full or empty status signals that can be routed to interact with sequencers or interrupts.

**Chaining**

The datapath can be configured to chain conditions and signals with neighboring datapaths. Shift, carry, capture, and other conditional signals can be chained to form higher precision arithmetic, shift, and CRC/PRS functions.

**Time Multiplexing**

In applications that are oversampled or do not need the highest clock rates, the single ALU in the datapath can be efficiently shared between two sets of registers and condition generators. ALU and shift outputs are registered and can be used as inputs in subsequent cycles. Usage examples include support for 16-bit functions in one (8-bit) datapath, or interleaving a CRC generation operation with a data shift operation.

**Datapath Inputs**

The datapath has three types of inputs: configuration, control, and serial and parallel data. The configuration inputs select the dynamic configuration RAM address. The control inputs load the data registers from the FIFOs and capture accumulator outputs into the FIFOs. Serial data inputs include shift in and carry in. A parallel data input port allows up to eight bits of data to be brought in from routing.

**Datapath Outputs**

A total of 16 signals are generated in the datapath. Some of these signals are conditional signals (for example, compares), some are status signals (for example, FIFO status), and the rest are data signals (for example, shift out). These 16 signals are multiplexed into the six datapath outputs and then driven to the routing matrix. By default, the outputs are single synchronized (pipelined). A combinational output option is also available for these outputs.

**Datapath Working Registers**

Each datapath module has six 8-bit working registers. All registers are readable and writable by CPU.

### Table 33-1. Datapath Working Registers

<table>
<thead>
<tr>
<th>Type</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Accumulator</td>
<td>A0, A1</td>
<td>The accumulators may be both a source and a destination for the ALU. They may also be loaded from a data register or a FIFO. The accumulators typically contain the current value of a function, such as a count, CRC, or shift. These registers are non-retention; they lose their values in Sleep mode and are reset to 0x00 on wakeup.</td>
</tr>
<tr>
<td>Data</td>
<td>D0, D1</td>
<td>The data registers typically contain constant data for a function, such as a PWM compare value, timer period, or CRC polynomial. These registers retain their values across sleep intervals.</td>
</tr>
<tr>
<td>FIFOs</td>
<td>F0, F1</td>
<td>The two 4-byte FIFOs provide both a source and a destination for buffered data. The FIFOs can be configured as both input buffers, both output buffers, or as one input buffer and one output buffer. Status signals indicate the full/empty status of these registers. Usage examples include buffered Tx and Rx data in the SPI or UART and buffered PWM compare and buffered timer period data. These registers are non-retention; they lose their values in Sleep mode and are reset to 0x00 on wakeup.</td>
</tr>
</tbody>
</table>

### 33.2.2.2 Datapath FIFOs

**FIFO Modes and Configurations**

Each FIFO has a variety of operation modes and configurations.

### Table 33-2. FIFO Modes and Configurations

<table>
<thead>
<tr>
<th>Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input/Output</td>
<td>In input mode, the CPU writes to the FIFO and the data is read and consumed by the datapath internals. In output mode, the FIFO is written to by the datapath internals and is read and consumed by the CPU.</td>
</tr>
<tr>
<td>Single Buffer</td>
<td>The FIFO operates as a single-byte buffer with no status. Data written to the FIFO is immediately available for reading, and can be overwritten at anytime.</td>
</tr>
<tr>
<td>Level/Edge</td>
<td>The control to load the FIFO from the datapath internals can be either level or edge triggered.</td>
</tr>
</tbody>
</table>
Figure 33-7 shows the possible FIFO configurations controlled by the input/output modes. The Tx/Rx mode has one FIFO in input mode and the other in output mode. The primary example of this configuration is SPI. The dual capture configuration provides independent capture of A0 and A1, or two separately controlled captures of either A0 or A1. Finally, the dual buffer mode can provide buffered periods and compares, or two independent periods/compares.

Table 33-2. FIFO Modes and Configurations (continued)

<table>
<thead>
<tr>
<th>Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal/Fast</td>
<td>The control to load the FIFO from the datapath source is sampled on the currently selected datapath clock (normal) or the HFCLK (fast). This allows captures to occur at the highest rate in the system (HFCLK), independent of the datapath clock.</td>
</tr>
<tr>
<td>Software Capture</td>
<td>When this mode is enabled and the FIFO is in output mode, a read by the CPU of the associated accumulator (A0 for F0, A1 for F1) initiates a synchronous transfer of the accumulator value into the FIFO. The captured value may then be immediately read from the FIFO. If chaining is enabled, the operation follows the chain to the MS block for atomic reads by datapaths of multi-byte values.</td>
</tr>
<tr>
<td>Asynch</td>
<td>When the datapath is being clocked asynchronously to the HFCLK, the FIFO status signals can be routed to the rest of the datapath either directly, single sampled to the datapath clock, or double sampled in the case of an asynchronous datapath clock.</td>
</tr>
<tr>
<td>Independent Clock Polarity</td>
<td>Each FIFO has a control bit to invert polarity of the FIFO clock with respect to the datapath clock.</td>
</tr>
</tbody>
</table>

![Figure 33-7. FIFO Configurations](image-url)
Figure 33-8 shows a detailed view of FIFO sources and sinks.

![FIFO Sources and Sinks](image)

When the FIFO is in input mode, the source is the system bus and the sinks are the Dx and Ax registers. When in output mode, the sources include the Ax registers and the ALU, and the sink is the system bus. The multiplexer selection is statically set in UDB configuration register CFG15, as shown in Table 33-3 for the F0_INSEL[1:0] or F1_INSEL[1:0].

### Table 33-3. FIFO Multiplexer Set in UDB CFG15 Register

<table>
<thead>
<tr>
<th>Fx_INSEL[1:0]</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Input mode - System bus writes the FIFO, FIFO output destination is Ax or Dx.</td>
</tr>
<tr>
<td>01</td>
<td>Output A0 Mode - FIFO input source is A0, FIFO output destination is the system bus.</td>
</tr>
<tr>
<td>10</td>
<td>Output A1 Mode - FIFO input source is A1, FIFO output destination is the system bus.</td>
</tr>
<tr>
<td>11</td>
<td>Output ALU Mode - FIFO input source is the ALU output, FIFO output destination is the system bus.</td>
</tr>
</tbody>
</table>

### FIFO Status

Each FIFO generates two status signals, “bus” and “block,” which are sent to the UDB routing through the datapath output multiplexer. The “bus” status can be used to assert an interrupt request to read/write the FIFO. The “block” status is primarily intended to provide the FIFO state to the UDB internals. The meanings of the status bits depend on the configured direction (Fx_INSEL[1:0] in the UDB CFG15 register) and the FIFO level bits. The FIFO level bits (Fx_LVL) are set in the Auxiliary Control (ACTL) register in working register space. Table 33-4 shows the options.

### Table 33-4. FIFO Status Options

<table>
<thead>
<tr>
<th>Fx_INSEL[1:0]</th>
<th>Fx_LVL</th>
<th>FIFO Status</th>
<th>FIFO Status</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input</td>
<td>0</td>
<td>Not Full</td>
<td>Bus Status</td>
<td>Asserted when there is room for at least 1 byte in the FIFO.</td>
</tr>
<tr>
<td>Input</td>
<td>1</td>
<td>At Least Half Empty</td>
<td>Bus Status</td>
<td>Asserted when there is room for at least 2 bytes in the FIFO.</td>
</tr>
</tbody>
</table>
Table 33-4. FIFO Status Options

<table>
<thead>
<tr>
<th>Fx_INSEL[1:0]</th>
<th>Fx_LVL</th>
<th>FIFO Status</th>
<th>FIFO Status Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input</td>
<td>NA</td>
<td>Empty</td>
<td>Block Status</td>
<td>Asserted when there are no bytes left in the FIFO. When not empty, the datapath internals may consume bytes. When empty the datapath may idle or generate an underrun condition.</td>
</tr>
<tr>
<td>Output</td>
<td>0</td>
<td>Not Empty</td>
<td>Bus Status</td>
<td>Asserted when there is at least 1 byte available to be read from the FIFO.</td>
</tr>
<tr>
<td>Output</td>
<td>1</td>
<td>At Least Half Empty</td>
<td>Bus Status</td>
<td>Asserted when there are at least 2 bytes available to be read from the FIFO.</td>
</tr>
<tr>
<td>Output</td>
<td>NA</td>
<td>Full</td>
<td>Block Status</td>
<td>Asserted when the FIFO is full. When not full, the datapath internals may write bytes to the FIFO. When full, the datapath may idle or generate an overrun condition.</td>
</tr>
</tbody>
</table>

**FIFO Operation**

Figure 33-9 illustrates a typical sequence of reads and writes and the associated status generation. Although the figure shows reads and writes occurring at different times, a read and write can also occur simultaneously.

**FIFO Fast Mode (FIFO FAST)**

When the FIFO is configured for output, the FIFO load operation normally uses the currently selected datapath clock for sampling the write signal. As shown in Figure 33-10, with the FIFO fast mode set, the HFCLK can be optionally selected for this operation. Used in conjunction with edge sensitive mode, this operation reduces the latency of accumulator-to-FIFO transfer from the resolution of the datapath clock to the resolution of the HFCLK, which can be much higher. This allows the CPU to read the captured result in the FIFO with minimal latency.
Figure 33-10 illustrates that the fast load operation is independent of the currently selected datapath clock; however, using the HFCLK may cause higher power consumption. Note that the incoming fx_id signal must be able to meet HFCLK timing, which can require local resynchronization.

![FIFO Fast Configuration Sinks](image)

**FIFO Level/Edge Write Mode**

Two modes are available for writing the FIFO from the datapath. In the first mode, data is synchronously transferred from the accumulators to the FIFOs. The control for that write (fx_id) is typically generated from a state machine or condition that is synchronous to the datapath clock. The FIFO is written in any cycle where the input load control is a ‘1’.

In the second mode, the FIFO is used to capture the value of the accumulator in response to a positive edge of the fx_id signal. In this mode the duty cycle of the waveform is arbitrary (however, it must be at least one datapath clock cycle in width). An example of this mode is capturing the value of the accumulator using an external pin input as a trigger. The limitation of this mode is that the input control must revert to ‘0’ for at least one cycle before another positive edge is detected.

Figure 33-11 shows the edge detect option on the fx_id control input. One bit for this option sets the mode for both FIFOs in a UDB. Note that edge detection is sampled at the rate of the selected FIFO clock.

![Edge Detect Option for Internal FIFO Write](image)

**FIFO Software Capture Mode**

A common and important requirement is to allow the CPU the ability to reliably read the contents of an accumulator during normal operation. This is done with software capture and is enabled by setting the FIFO Cap configuration bit (FIFO_CAP bit in the UDB CFG16 register). This bit applies to both FIFOs in a UDB, but is operational only when a FIFO is in output mode. When using software capture, F0 should be set to load from A0 and F1 from A1.

As shown in Figure 33-12, reading the accumulator triggers a write to the FIFO from that accumulator. This signal is chained so that a read of a given byte simultaneously captures accumulators in all chained UDBs. This allows the CPU to reliably read 16 bits or more simultaneously. The data returned in the read of the accumulator should be ignored; the captured value may be read from the FIFOs immediately.

The fx_id signal, which generates a FIFO load, is ORed with the software capture signal; the results can be unpredictable when both hardware and software capture are used at the same time. As a general rule, these functions should be mutually exclusive; however, hardware and software capture can be used simultaneously with the following settings:

- FIFO capture clocking mode is set to FIFO FAST
- FIFO write mode is set to FIFO EDGE

With these settings, hardware and software capture work essentially the same and in any given HFCLK cycle, either signal asserted initiates a capture.
Clear the target FIFO in firmware (UDB ACTL register) before initiating a software capture. This initializes the FIFO read and write pointers to a known state.

Figure 33-12. Software Capture Configuration

**FIFO Control Bits**

The Auxiliary Control (ACTL) register has four bits that may be used by the CPU firmware to control the FIFO during normal operation.

The FIFO0 CLR and FIFO1 CLR bits are used to reset or flush the FIFO. When a ‘1’ is written to one of these bits, the associated FIFO is reset. The bit must be written back to ‘0’ for FIFO operation to continue. If the bit is left asserted, the given FIFO is disabled and operates as a one byte buffer without status. Data can be written to the FIFO; the data is immediately available for reading and can be overwritten at anytime. Data direction using the Fx INSEL[1:0] (UDB CFG15 register) configuration bits is still valid.

The FIFO0 LVL and FIFO1 LVL bits control the level at which the 4-byte FIFO asserts bus status (when the bus is either reading or writing to the FIFO) to be asserted. The meaning of FIFO bus status depends on the configured direction, as shown in Table 33-5.

Table 33-5. FIFO Level Control Bits in UDB ACTL Register

<table>
<thead>
<tr>
<th>FIFOxLVL</th>
<th>Input Mode (Bus is Writing FIFO)</th>
<th>Output Mode (Bus is Reading FIFO)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Not Full</td>
<td>Not Empty</td>
</tr>
<tr>
<td></td>
<td>At least 1 byte can be written</td>
<td>At least 1 byte can be read</td>
</tr>
<tr>
<td>1</td>
<td>At least Half Empty</td>
<td>At least 2 bytes can be written</td>
</tr>
<tr>
<td></td>
<td>At least 2 bytes can be written</td>
<td>At least 2 bytes can be read</td>
</tr>
</tbody>
</table>

**FIFO Asynchronous Operation**

Figure 33-13 illustrates the concept of asynchronous FIFO operation. As an example, assume F0 is set for input mode and F1 is set for output mode, which is a typical configuration for Tx and Rx registers.

On the Tx side, the datapath state machine uses “empty” to determine if there are any bytes available to consume. Empty is set synchronously to the DP state machine, but is cleared asynchronously due to a bus write. When cleared, the status is synchronized back to the DP state machine.

On the Rx side, the datapath state machine uses “full” to determine whether there is a space left to write to the FIFO. Full is set synchronously to the DP state machine, but is cleared asynchronously due to a bus read. When cleared, the status is synchronized back to the DP state machine.

A single FIFO ASYNCH bit of the UDB CFG16 register is used to enable this synchronization method; when set it applies to both FIFOs. It is applied only to the block status, as it is assumed that bus status is naturally synchronized by the interrupt process.
FIFO Overflow Operation

Use FIFO status signaling to safely implement both internal (datapath) and external (CPU) reads and writes. There is no built-in protection from underflow and overflow conditions. If the FIFO is full and subsequent writes occur (overflow), the new data overwrites the front of the FIFO (the data currently being output, the next data to read). If the FIFO is empty and subsequent reads occur (underflow), the read value is undefined. FIFO pointers remain accurate regardless of underflow and overflow.

FIFO Clock Inversion Option

Each FIFO has a control bit called FX CK INV in the UDB CFG16 register that controls the polarity of the FIFO clock, with respect to the polarity of the DP clock. By default, the FIFO operates at the same polarity as the DP clock. When this bit is set, the FIFO operates at the opposite polarity as the DP clock. This provides support for "both clock edge" communication protocols, such as SPI.

FIFO Dynamic Control

Normally, the FIFOs are configured statically in either input or output mode. As an alternative, each FIFO can be configured into a mode where the direction is controlled dynamically, that is, by routed signals. One configuration bit per FIFO (FX DYN bit in the UDB CFG17 register) enables the mode. Figure 33-14 shows the configurations available in dynamic FIFO mode.

In internal access mode, the datapath can read and write the FIFO. In this configuration, the FX INSEL bits must be configured to select the source for the FIFO writes. FX INSEL = 00 (CPU bus source) is invalid in this mode; they can only be 01, 10, or 11 (A0, A1, or ALU). Note that the only read access is to the associated accumulator; the data register destination is not available in this mode.

In external access mode, the CPU can both read and write the FIFO. The configuration between internal and external access is dynamically switchable using datapath routing signals. The datapath input signals D0_LOAD and D1_LOAD are used for this control. Note that in the dynamic control mode, D0_LOAD and D1_LOAD are not available for their normal use in loading the D0/D1 registers from F0/F1. The dx_LOAD signals can be driven by any routed signal, including constants.

In one usage example, starting with external access (dx_LOAD == 1), the CPU can write one or more bytes of data to the FIFO. Then toggling to internal access (dx_LOAD == 0), the datapath can perform operations on the data. Then tog-
gling back to external access, the CPU can read the result of the computation.

Because the Fx INSEL must always be set to 01, 10, or 11 (A0, A1, or ALU), which is "output mode" in normal operation, the FIFO status signals have the following definitions (also dependent on Fx LVL control).

Table 33-6. FIFO Status

<table>
<thead>
<tr>
<th>Status Signal</th>
<th>Meaning</th>
<th>Fx LVL = 0</th>
<th>Fx LVL = 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>fx_blk_stat</td>
<td>Write Status</td>
<td>FIFO full</td>
<td>FIFO full</td>
</tr>
<tr>
<td>fx_bus_stat</td>
<td>Read Status</td>
<td>FIFO not empty</td>
<td>At least half full</td>
</tr>
</tbody>
</table>

Because the datapath and CPU may both write and read the FIFO, these signals are no longer considered "block" and "bus" status. The blk_stat signal is used for write status and the bus_stat signal is used for read status.

33.2.2.3 FIFO Status

There are four FIFO status signals, two for each FIFO: fifo0_bus_stat, fifo0_blk_stat, fifo1_bus_stat, and fifo1_blk_stat. The meaning of these signals depends on the direction of the given FIFO, which is determined by static configuration.

33.2.2.4 Datapath ALU

The ALU core consists of three independent 8-bit programmable functions, which include an arithmetic/logic unit, a shifter unit, and a mask unit. See the UDB datapath architecture block diagram (Figure 33-6) for more details.

Arithmetic and Logic Operation

The ALU functions, which are configured dynamically by the configuration RAM, are shown in Table 33-7.

Table 33-7. ALU Functions in UDB DCFG Register

<table>
<thead>
<tr>
<th>Func[2:0]</th>
<th>Function</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>PASS</td>
<td>srca</td>
</tr>
<tr>
<td>001</td>
<td>INC</td>
<td>++srca</td>
</tr>
<tr>
<td>010</td>
<td>DEC</td>
<td>--srca</td>
</tr>
<tr>
<td>011</td>
<td>ADD</td>
<td>srca + srb</td>
</tr>
<tr>
<td>100</td>
<td>SUB</td>
<td>srca – srb</td>
</tr>
<tr>
<td>101</td>
<td>XOR</td>
<td>srca ^ srb</td>
</tr>
<tr>
<td>110</td>
<td>AND</td>
<td>srca and srb</td>
</tr>
<tr>
<td>111</td>
<td>OR</td>
<td>srca</td>
</tr>
</tbody>
</table>

srca = ‘A’ input source to the ALU, srb = ‘B’ input source to the ALU. See Figure 33-6.

Carry In

The carry in is used in arithmetic operations. Table 33-8 shows the default carry in value for certain functions.

Table 33-8. Carry In Functions

<table>
<thead>
<tr>
<th>Function</th>
<th>Operation</th>
<th>Default Carry In Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>INC</td>
<td>++srca</td>
<td>srca + 00h + ci, where ci is forced to 1</td>
</tr>
<tr>
<td>DEC</td>
<td>--srca</td>
<td>srca + ffh + ci, where ci is forced to 0</td>
</tr>
<tr>
<td>ADD</td>
<td>srca + srb</td>
<td>srca + srb + ci, where ci is forced to 0</td>
</tr>
<tr>
<td>SUB</td>
<td>srca – srb</td>
<td>srca + ~srb + ci, where ci is forced to 1</td>
</tr>
</tbody>
</table>

In addition to this default arithmetic mode for carry operation, there are three additional carry options. The CI SELA and CI SELB configuration bits in the CFG13 register determine the carry in for a given cycle. Dynamic configuration RAM selects either the A or B configuration on a cycle-by-cycle basis. The options are defined in Table 33-9.

Table 33-9. Additional Carry In Functions in UDB CFG13

<table>
<thead>
<tr>
<th>CI SEL A</th>
<th>CI SEL B</th>
<th>Carry Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Default</td>
<td>Default arithmetic mode as described in Table 33-8.</td>
<td></td>
</tr>
<tr>
<td>01</td>
<td>Registered</td>
<td>Carry Flag, result of the carry from the previous cycle. This mode is used to implement add with carry and subtract with borrow operations. It can be used in successive cycles to emulate a double precision operation.</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>Routed</td>
<td>Carry is generated elsewhere and routed to this input. This mode can be used to implement controllable counters.</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Chained</td>
<td>Carry is chained from the previous datapath. This mode can be used to implement single cycle operations of higher precision involving two or more datapaths.</td>
<td></td>
</tr>
</tbody>
</table>

When a routed carry is used, the meaning with respect to each arithmetic function is shown in Table 33-10. Note that in the case of the decrement and subtract functions, the carry is active low (inverted).

Table 33-10. Routed Carry In Functions

<table>
<thead>
<tr>
<th>Function</th>
<th>Carry In Polarity</th>
<th>Carry In Active</th>
<th>Carry In Inactive</th>
</tr>
</thead>
<tbody>
<tr>
<td>INC</td>
<td>True</td>
<td>++srca</td>
<td>srca</td>
</tr>
<tr>
<td>DEC</td>
<td>Inverted</td>
<td>--srca</td>
<td>srca</td>
</tr>
<tr>
<td>ADD</td>
<td>True</td>
<td>(srca + srb) + 1</td>
<td>srca + srb</td>
</tr>
<tr>
<td>SUB</td>
<td>Inverted</td>
<td>(srca – srb) – 1</td>
<td>(srca – srb)</td>
</tr>
</tbody>
</table>

Carry Out

The carry out is a selectable datapath output and is derived from the currently defined MSb position, which is statically programmable. This value is also chained to the next most significant block as an optional carry in. Note that in the case of decrement and subtract functions, the carry out is inverted.
Table 33-11. Carry Out Functions

<table>
<thead>
<tr>
<th>Function</th>
<th>Carry Out Polarity</th>
<th>Carry Out Active</th>
<th>Carry Out Inactive</th>
</tr>
</thead>
<tbody>
<tr>
<td>INC</td>
<td>True</td>
<td>++srca == 0</td>
<td>srca</td>
</tr>
<tr>
<td>DEC</td>
<td>Inverted</td>
<td>--srca == –1</td>
<td>srca</td>
</tr>
<tr>
<td>ADD</td>
<td>True</td>
<td>srca + srcb &gt; 255</td>
<td>srca + srcb</td>
</tr>
<tr>
<td>SUB</td>
<td>Inverted</td>
<td>srca – srcb &lt; 0</td>
<td>(srca – srcb)</td>
</tr>
</tbody>
</table>

**Carry Structure**

Figure 33-15 shows the options for carry in, and for MSb selection for carry out generation. The registered carry out value may be selected as the carry in for a subsequent arithmetic operation. This feature can be used to implement higher precision functions in multiple cycles.

**Shift Operation**

The shift operation occurs independent of the ALU operation, according to Table 33-12.

Table 33-12. Shift Operation Functions in UDB DCFG Register

<table>
<thead>
<tr>
<th>Shift[1:0]</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Pass</td>
</tr>
<tr>
<td>01</td>
<td>Shift Left</td>
</tr>
<tr>
<td>10</td>
<td>Shift Right</td>
</tr>
<tr>
<td>11</td>
<td>Nibble Swap</td>
</tr>
</tbody>
</table>

A shift out value is available as a datapath output. Both shift out right (sor) and shift out left (sol_msb) share that output selection. A static configuration bit (SHIFT SEL in the UDB CFG15 register) determines which shift output is used as a datapath output. When no shift is occurring, the sor and sol_msb signal is defined as the LSB or MSb of the ALU function, respectively.

The SI SELA and SI SELB configuration bits determine the shift in data for a given operation. Dynamic configuration RAM selects the A or B configuration on a cycle-by-cycle basis. Shift in data is valid only for left and right shift; it is not used for pass and nibble swap. Table 33-13 shows the selections and usage that apply to both left and right shift directions.
The shift out left data comes from the currently defined MSb position (MSB_EN and MSB_SEL bits in the CFG14 register), and the data that is shifted in from the left (in a shift right operation) goes into the currently defined MSb position. Both shift out data (left or right) are registered and can be used in a subsequent cycle. This feature can be used to implement a higher precision shift in multiple cycles.

**Table 33-13. Shift In Functions in UDB CFG15 Register**

<table>
<thead>
<tr>
<th>SI SEL A/ SI SEL B</th>
<th>Shift In Source</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Default/Arithmetic</td>
<td>The default input is the value of the DEF SI configuration bit (fixed 1 or 0). However, if the MSb SI bit is set, then the default input is the currently defined MSb (for right shift only).</td>
</tr>
<tr>
<td>01</td>
<td>Registered</td>
<td>The shift in value is driven by the current registered shift out value (from the previous cycle). The shift left operation uses the last shift out left value. The shift right operation uses the last shift out right value.</td>
</tr>
<tr>
<td>10</td>
<td>Routed</td>
<td>Shift in is selected from the routing channel (the SI input).</td>
</tr>
<tr>
<td>11</td>
<td>Chained</td>
<td>Shift in left is routed from the right datapath neighbor and shift in right is routed from the left datapath neighbor.</td>
</tr>
</tbody>
</table>

The shift out left data comes from the currently defined MSb position (MSB_EN and MSB_SEL bits in the CFG14 register), and the data that is shifted in from the left (in a shift right operation) goes into the currently defined MSb position. Both shift out data (left or right) are registered and can be used in a subsequent cycle. This feature can be used to implement a higher precision shift in multiple cycles.

**Figure 33-16. Shift Operation**

Note that the bits that are isolated by the MSb selection are still shifted. In the example shown, bit 7 still shifts in the sil value on a right shift and bit 5 shifts in bit 4 on a left shift. The shift out either right or left from the isolated bits is lost.

**ALU Masking Operation**

An 8-bit mask register (AMASK) in the UDB static configuration register space (CFG9) defines the masking operation. In this operation, the output of the ALU is masked (ANDed) with the value in the mask register. A typical use for the ALU mask function is to implement free-running timers and counters in power of two resolutions.
33.2.2.5 Datapath Inputs and Multiplexing

The datapath has a total of nine inputs, as shown in Table 33-14, including six inputs from the channel routing. These consist of the configuration RAM address, FIFO and data register load control signals, and the data inputs shift in and carry in.

Table 33-14. Datapath Inputs

<table>
<thead>
<tr>
<th>Input</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAD2</td>
<td>Asynchronous dynamic configuration RAM address. There are eight 16-bit words, which are user-programmable. Each word contains the datapath control bits for the current cycle. Sequences of instructions can be controlled by these address inputs.</td>
</tr>
<tr>
<td>RAD1</td>
<td></td>
</tr>
<tr>
<td>RAD0</td>
<td></td>
</tr>
<tr>
<td>F0 LD</td>
<td>When asserted in a given cycle, the selected FIFO is loaded with data from one of the A0 or A1 accumulators or from the output of the ALU. The source is selected by the Fx INSEL[1:0] configuration bits. This input is edge sensitive. It is sampled at the datapath clock; when a ‘0’ to ‘1’ transition is detected, a load occurs at the subsequent clock edge.</td>
</tr>
<tr>
<td>F1 LD</td>
<td></td>
</tr>
<tr>
<td>D0 LD</td>
<td>When asserted in a given cycle, the Dx register is loaded from associated FIFO Fx. This input is edge sensitive. It is sampled at the datapath clock; when a ‘0’ to ‘1’ transition is detected, a load occurs at the subsequent clock edge.</td>
</tr>
<tr>
<td>D1 LD</td>
<td></td>
</tr>
<tr>
<td>SI</td>
<td>This is a data input value that can be used for either shift in left or shift in right.</td>
</tr>
<tr>
<td>CI</td>
<td>This is the carry in value used when the carry in select control is set to “routed carry.”</td>
</tr>
</tbody>
</table>

As shown in Figure 33-17, each input has a 6-to-1 multiplexer, therefore, all inputs are permutable. Inputs are handled in one of two ways, either level sensitive or edge sensitive. RAM address, shift in and data in values are level sensitive; FIFO and data register load signals are edge sensitive.

33.2.2.6 CRC/PRS Support

The datapath can support cyclic redundancy checking (CRC) and pseudo random sequence (PRS) generation. Chaining signals are routed between datapath blocks to support CRC/PRS bit lengths of longer than eight bits.

The most significant bit (MSb) of the most significant block in the CRC/PRS computation is selected and routed (and chained across blocks) to the least significant block. The MSb is then XORed with the data input (SI data) to provide the feedback (FB) signal. The FB signal is then routed (and chained across blocks) to the most significant block. This feedback value is used in all blocks to gate the XOR of the polynomial (from the DATA0 or DATA1 register) with the current accumulator value.

Figure 33-18 shows the structural configuration for the CRC operation. The PRS configuration is identical except that the shift in (SI) is tied to ‘0’. In the PRS configuration, D0 or D1 contain the polynomial value, while A0 or A1 contain the initial (seed) value and the CRC residual value at the end of the computation.

To enable CRC operation, the CFB_EN bit in the dynamic configuration RAM must be set to ‘1’. This enables the AND of SRCB ALU input with the CRC feedback signal. When set to zero, the feedback signal is driven to ‘1’, which allows for normal arithmetic operation. Dynamic control of this bit on a cycle-by-cycle basis gives the capability to interleave a CRC/PRS operation with other arithmetic operations.
**CRC/PRS Chaining**

Figure 33-19 illustrates an example of CRC/PRS chaining across three UDBs. This scenario can support a 17- to 24-bit operation. The chaining control bits are set according to the position of the datapath in the chain as shown in the figure.

The CRC/PRS feedback signal (cfbo, cfbi) is chained as follows:

- If a given block is the least significant block, then the feedback signal is generated in that block from the built-in logic that takes the shift in from the right (sir) and XORs it with the MSb signal. (For PRS, the “sir” signal is tied to ‘0’.)
- If a given block is not the least significant block, the CHAIN FB configuration bit must be set and the feedback is chained from the previous block in the chain.

The CRC/PRS MSb signal (cmsbo, cmsbi) is chained as follows:

- If a given block is not the most significant block, the CHAIN C MSB configuration bit in the UDB CFG14 register must be set and the MSb signal is chained from the next block in the chain.
- If a given block is the most significant block, the MSb (according to the polynomial selected) is configured using the MSB_SEL configuration bits in the UDB CFG14 register.

**CRC/PRS Polynomial Specification**

As an example of how to configure the polynomial for programming into the associated D0/D1 register, consider the CCITT CRC-16 polynomial, which is defined as \( x^{16} + x^{12} + x^5 + 1 \). The method for deriving the data format from the polynomial is shown in Figure 33-20.

The \( x^0 \) term is inherently always ‘1’ and therefore does not need to be programmed. For each of the remaining terms in the polynomial, a ‘1’ is set in the appropriate position in the alignment shown.

**Note:** This polynomial format is slightly different from the format normally specified in Hex. For example, the CCITT CRC16 polynomial is typically denoted as 1021H. To convert to the format required for datapath operation, shift right by one and add a ‘1’ in the MSb. In this case, the correct polynomial value to load into the D0 or D1 register is 8810H.

---

**Figure 33-18. CRC Functional Structure**

**Figure 33-19. CRC/PRS Chaining Configuration**
Example CRC/PRS Configuration

The following is a summary of CRC/PRS configuration requirements, assuming that D0 is the polynomial and the CRC/PRS is computed in A0:

1. Select a suitable polynomial and write it into D0.
2. Select a suitable seed value (for example, all zeros for CRC, all ones for PRS) and write it into A0.
3. Configure chaining if necessary.
4. Select the MSb position as defined in the polynomial from the MSB_SEL static configuration register bits and set the MSB_EN register bit in the UDB CFG14 register.
5. Configure the dynamic configuration RAM word fields:
   a. Select D0 as the ALU SRCB (ALU B input source).
   b. Select A0 as the ALU SRCA (ALU A input source).
   c. Select XOR for the ALU function.
   d. Select SHIFT LEFT for the SHIFT function.
   e. Select CFB_EN to enable the support for CRC/PRS.
   f. Select ALU as the A0 write source.

If a CRC operation, configure “shift in right” for input data from routing and supply input on each clock. If a PRS operation, tie “shift in right” to '0'.

Clocking the UDB with this configuration generates the required CRC or outputs the MSb, which may be output to the routing for the PRS sequence.

External CRC/PRS Mode

A static configuration bit may be set (EXT CRCPRS in the UDB CFG16 register) to enable support for external computation of a CRC or PRS. As shown in Figure 33-21, computation of the CRC feedback is done in a PLD block. When the bit is set, the CRC feedback signal is driven directly from the Carry In (CI) datapath input selection mux, bypassing the internal computation. The figure shows a simple configuration that supports up to an 8-bit CRC or PRS. Normally the built-in circuitry is used, but this feature gives the capability for more elaborate configurations, such as up to a 16-bit CRC/PRS function in one UDB using time division multiplexing.

In this mode, the dynamic configuration RAM bit CFB_EN in the UDB DCFG0 register still controls whether the CRC feedback signal is ANDed with the SRCB ALU input. Therefore, as with the built-in CRC/PRS operation, the function can be interleaved with other functions if required.
33.2.2.7 Datapath Outputs and Multiplexing

Conditions are generated from the registered accumulator values, ALU outputs, and FIFO status. These conditions can be driven to the digital routing for use in other UDB blocks, for use as interrupts, or to I/O pins. The 16 possible conditions are shown in Table 33-15.

Table 33-15. Datapath Condition Generation

<table>
<thead>
<tr>
<th>Name</th>
<th>Condition</th>
<th>Chain</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ce0</td>
<td>Compare Equal</td>
<td>Y</td>
<td>A0 == D0</td>
</tr>
<tr>
<td>cl0</td>
<td>Compare Less Than</td>
<td>Y</td>
<td>A0 &lt; D0</td>
</tr>
<tr>
<td>z0</td>
<td>Zero Detect</td>
<td>Y</td>
<td>A0 == 00h</td>
</tr>
<tr>
<td>ff0</td>
<td>Ones Detect</td>
<td>Y</td>
<td>A0 == FFh</td>
</tr>
<tr>
<td>ce1</td>
<td>Compare Equal</td>
<td>Y</td>
<td>A1 or A0 == D1 or A0 (dynamic selection)</td>
</tr>
<tr>
<td>cl1</td>
<td>Compare Less Than</td>
<td>Y</td>
<td>A1 or A0 &lt; D1 or A0 (dynamic selection)</td>
</tr>
<tr>
<td>z1</td>
<td>Zero Detect</td>
<td>Y</td>
<td>A1 == 00h</td>
</tr>
<tr>
<td>ff1</td>
<td>Ones Detect</td>
<td>Y</td>
<td>A1 == FFh</td>
</tr>
<tr>
<td>ov_msb</td>
<td>Overflow</td>
<td>N</td>
<td>Carry (MSb) ^ Carry (MSb–1)</td>
</tr>
<tr>
<td>co_msb</td>
<td>Carry Out</td>
<td>Y</td>
<td>Carry out of MSb defined bit</td>
</tr>
<tr>
<td>cmsb</td>
<td>CRC MSb</td>
<td>Y</td>
<td>MSb of CRC/PRS function</td>
</tr>
<tr>
<td>So</td>
<td>Shift Out</td>
<td>Y</td>
<td>Selection of shift output</td>
</tr>
<tr>
<td>f0_blk_stat</td>
<td>FIFO0 Block Status</td>
<td>N</td>
<td>Definition depends on FIFO configuration</td>
</tr>
<tr>
<td>f1_blk_stat</td>
<td>FIFO1 Block Status</td>
<td>N</td>
<td>Definition depends on FIFO configuration</td>
</tr>
<tr>
<td>f0_bus_stat</td>
<td>FIFO0 Bus Status</td>
<td>N</td>
<td>Definition depends on FIFO configuration</td>
</tr>
<tr>
<td>f1_bus_stat</td>
<td>FIFO1 Bus Status</td>
<td>N</td>
<td>Definition depends on FIFO configuration</td>
</tr>
</tbody>
</table>

There are a total of six datapath outputs. As shown in Figure 33-22, each output has a 16-1 multiplexer that allows any of these 16 signals to be routed to any of the datapath outputs.
Compares

There are two compares, one of which has fixed sources (Compare 0) and the other has dynamically selectable sources (Compare 1). Each compare has an 8-bit statically programmed mask register, which enables the compare to occur in a specified bitfield. By default, the masking is off (all bits are compared) and must be enabled.

Comparator 1 inputs are dynamically configurable. As shown in Table 33-16, there are four options for Comparator 1, which applies to both the "less than" and the "equal" conditions. The CMP SELA and CMP SELB configuration bits in the UDB CFG12 register determine the possible compare configurations. A dynamic configuration RAM bit CMP SEL in the UDB DCFG0 register selects one of the A or B configurations on a cycle-by-cycle basis.

Table 33-16. Compare Configuration

<table>
<thead>
<tr>
<th>CMP SEL A CMP SEL B</th>
<th>Comparator 1 Compare Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>A1 Compare to D1</td>
</tr>
<tr>
<td>01</td>
<td>A1 Compare to A0</td>
</tr>
<tr>
<td>10</td>
<td>A0 Compare to D1</td>
</tr>
<tr>
<td>11</td>
<td>A0 Compare to A0</td>
</tr>
</tbody>
</table>

Compare 0 and Compare 1 are independently chainable to the conditions generated in the previous datapath (in addressing order). The decision to chain compares is statically specified by CHAIN0 and CHAIN1 bits of the UDB CFG14 registers. Figure 33-23 illustrates compare equal chaining, which is just an ANDing of the compare equal in this block with the chained input from the previous block.

Figure 33-24 illustrates compare less than chaining. In this case, the "less than" is formed by the compare less than output in this block, which is unconditional. This is ORed with the condition where this block is equal, and the chained input from the previous block is asserted as less than.

All Zeros and All Ones Detect

Each accumulator has dedicated all zeros detect and all ones detect. These conditions are statically chainable as specified in the UDB configuration registers. The decision to chain these conditions is statically specified in the UDB configuration registers. Chaining of zero detect is the same concept as the compare equal. Successive chained data is ANDed if the chaining is enabled.

Overflow

Overflow is defined as the XOR of the carry into the MSb and the carry out of the MSb. The computation is done on the currently defined MSb as specified by the MSB_SEL bits. This condition is not chainable, however the computation is valid when done in the most significant datapath of a multi-precision function as long as the carry is chained between blocks.

33.2.2.8 Datapath Parallel Inputs and Outputs

As shown in Figure 33-25, the datapath Parallel In (PI) and Parallel Out (PO) signals give limited capability to bring routed data directly into and out of the datapath. Parallel Out
signals are always available for routing as the ALU asrc selection between A0 and A1.

Parallel In needs to be selected for input to the ALU. The two options available are static operation or dynamic operation. For static operation, the PI SEL bit of the UDB CFG15 register forces the ALU asrc to be PI. The PI DYN bit of the UDB CFG15 register is used to enable the PI dynamic operation. When it is enabled, and assuming the PI SEL is 0, the PI multiplexer may then be controlled by the CFB_EN (UDB DCFG10 register) dynamic control bit. The primary function of CFB_EN is to enable PRS/CRC functionality.

### 33.2.2.9 Datapath Chaining

Each datapath block contains an 8-bit ALU, which is designed to chain carries, shifted data, capture triggers, and conditional signals to the nearest neighbor datapaths, to create higher precision arithmetic functions and shifters. These chaining signals, which are dedicated signals, allow single-cycle 16-, 24- and 32-bit functions to be efficiently implemented without the timing uncertainty of channel routing resources. In addition, the capture chaining supports the ability to perform an atomic read of the accumulators in chained blocks. As shown in Figure 33-26, all generated conditional and capture signals chain in the direction of least significant to most significant blocks. Shift left also chains from least to most significant. Shift right chains from most to least significant. The CRC/PRS chaining signal for feedback chains least to most significant; the MSb output chains from most to least significant.
33.2.2.10 Dynamic Configuration RAM

Each datapath contains a 16 bit-by-8 word dynamic configuration RAM, which is shown in Figure 33-27. The purpose of this RAM is to control the datapath configuration bits on a cycle-by-cycle basis, based on the clock selected for that datapath. This RAM has synchronous read and write ports for purposes of loading the configuration via the system bus.

An additional asynchronous read port is provided as a fast path to output these 16-bit words as control bits to the datapath. The asynchronous address inputs are selected from datapath inputs and can be generated from any of the possible signals on the channel routing, including I/O pins, PLD outputs, control block outputs, or other datapath outputs. The primary purpose of the asynchronous read path is to provide a fast single-cycle decode of datapath control bits.

![Figure 33-27. Configuration RAM I/O](image)

The fields of this dynamic configuration RAM word are shown here. A description of the usage of each field follows.

<table>
<thead>
<tr>
<th>Register</th>
<th>Address</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>CFGRAM</td>
<td>61h - 6Fh (odd)</td>
<td>FUNC[2:0]</td>
<td>SRCA</td>
<td>SRCB[1:0]</td>
<td>SHIF[1:0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Register</th>
<th>Address</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CFGRAM</td>
<td>60h - 6Eh (even)</td>
<td>A0 WR SRC[1:0]</td>
<td>A1 WR SRC[1:0]</td>
<td>CFB EN</td>
<td>CI SEL</td>
<td>SI SEL</td>
<td>CMP_SEL</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### 33.2.3 Status and Control Module

**Figure 33-28** shows a high-level view of the Status and Control module. The control register drives into the routing to provide firmware control inputs to UDB operation. The status register read from routing provides firmware a method of monitoring the state of UDB operation.

**Figure 33-29** shows a more detailed view of the Status and Control module. The primary purpose of this block is to coordinate CPU firmware interaction with internal UDB operation. However, due to its rich connectivity to the routing matrix, this block may be configured to perform other functions.

<table>
<thead>
<tr>
<th>Field</th>
<th>Bits</th>
<th>Parameter</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>FUNC[2:0]</td>
<td>3</td>
<td>ALU Function</td>
<td>000 PASS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>001 INC SRCA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>010 DEC SRCA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>011 ADD</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100 SUB</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>101 XOR</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>110 AND</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>111 OR</td>
</tr>
<tr>
<td>SRCA</td>
<td>1</td>
<td>ALU A Input Source</td>
<td>0 A0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 A1</td>
</tr>
<tr>
<td>SRCB</td>
<td>2</td>
<td>ALU B Input Source</td>
<td>00 D0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01 D1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10 A0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11 A1</td>
</tr>
<tr>
<td>SHIFT[1:0]</td>
<td>2</td>
<td>SHIFT Function</td>
<td>00 PASS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01 Left Shift</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10 Right Shift</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11 Nibble Swap</td>
</tr>
<tr>
<td>A0 WR SRC[1:0]</td>
<td>2</td>
<td>A0 Write Source</td>
<td>00 None</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01 ALU</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10 D0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11 F0</td>
</tr>
<tr>
<td>A1 WR SRC[1:0]</td>
<td>2</td>
<td>A1 Write Source</td>
<td>00 None</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01 ALU</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10 D1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11 F1</td>
</tr>
<tr>
<td>CFB EN</td>
<td>1</td>
<td>CRC Feedback Enable</td>
<td>0 Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 Disable</td>
</tr>
<tr>
<td>CI SEL</td>
<td>1</td>
<td>Carry In Configuration Select</td>
<td>0 ConfigA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 ConfigB</td>
</tr>
<tr>
<td>SI SEL</td>
<td>1</td>
<td>Shift In Configuration Select</td>
<td>0 ConfigA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 ConfigB</td>
</tr>
<tr>
<td>CMP SEL</td>
<td>1</td>
<td>Compare Configuration Select</td>
<td>0 ConfigA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 ConfigB</td>
</tr>
</tbody>
</table>

* For CI, SI, and CMP, the RAM fields select between two predefined static settings; see Table 33-9, Table 33-13, and Table 33-16, respectively.
Modes of operation include:

- **Status Input** – The state of routing signals can be input and captured as status and read by the CPU.
- **Control Output** – The CPU can write to the control register to drive the state of the routing.
- **Parallel Input** – To datapath parallel input.
- **Parallel Output** – From datapath parallel output.
- **Counter Mode** – In this mode, the control register operates as a 7-bit down counter with programmable period and automatic reload. Routing inputs can be configured to control both the enable and reload of the counter. When this mode is enabled, control register operation is not available.
- **Sync Mode** – In this mode, the status register operates as a 4-bit double synchronizer. When this mode is enabled, status register operation is not available.
33.2.3.1 Status and Control Mode

When operating in status and control mode, this module functions as a status register, interrupt mask register, and control register in the configuration shown in Figure 33-30.

Figure 33-30. Status and Control Operation

Status Register Operation

One 8-bit, read-only status register is available for each UDB. Inputs to this register come from any signal in the digital routing fabric. The status register is nonretention; it loses its state across sleep intervals and is reset to 0x00 on wakeup. Each bit can be independently programmed to operate in one of two ways, as shown in Table 33-18.

Table 33-18. Status Register Mode Selection in UDB CFG20 Register

<table>
<thead>
<tr>
<th>STAT MD</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Transparent read. A read returns the current value of the routed signal</td>
</tr>
<tr>
<td>1</td>
<td>Sticky, clear on read. A high on the input is sampled and captured. It is cleared when the register is read.</td>
</tr>
</tbody>
</table>

An important feature of the status register clearing operation is to note that the clear of status is applied only to the bits that are set. This allows other bits that are not set to continue to capture status, so that a coherent view of the process can be maintained.

Transparent Status Read

By default, a CPU read of this register transparently reads the state of the associated routing. This mode can be used for a transient state that is computed and registered internally in the UDB.

Sticky Status, with Clear on Read

In this mode, the status register inputs are sampled on each cycle of the status and control clock. If the signal is high in a given sample, it is captured in the status bit and remains high, regardless of the subsequent state of the input. When the CPU reads the status register the bit is cleared. The status register clearing is independent of mode and occurs even if the UDB clock is disabled; it is based on the HFCLK and occurs as part of the read operation.

Status Latching During Read

Figure 33-31 shows the structure of the status read logic. The sticky status register is followed by a latch, which latches the status register data and holds it stable during the duration of the read cycle, regardless of the number of wait states in a given read.
Interrupt Generation

In most functions, interrupt generation is tied to the setting of status bits. As shown in Figure 33-31, this feature is built into the status register logic as the masking and OR reduction of status. Only the lower seven bits of status input can be used with the built-in interrupt generation circuitry. The most significant bit is typically used as the interrupt output and may be routed to the interrupt controller through the digital routing. In this configuration, the MSb of the status register is read as the state of the interrupt bit.

33.2.3.2 Control Register Operation

One 8-bit control register is available for each UDB. This operates as a standard read/write register on the system bus, where the output of these register bits are selectable as drivers into the digital routing fabric.

The Control register is nonretention; it loses its contents across sleep intervals and is reset to 0x00 on wakeup.

Control Register Operating Modes

Three modes are available that may be configured on a bit-by-bit basis. The configuration is controlled by the concatenation of the bits of the two 8-bit registers CTL_MD1[7:0] and CTL_MD0[7:0] of the UDB CFG18 and CFG19 registers. For example, {CTL_MD1[0],CTL_MD0[0]} controls the mode for Control Register bit 0, as shown in Table 33-19.

Table 33-19. Mode for Control Register Bit 0 in the UDB CFG18 and CFG19 Registers

<table>
<thead>
<tr>
<th>CTL MD</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Direct mode</td>
</tr>
<tr>
<td>01</td>
<td>Sync mode</td>
</tr>
<tr>
<td>10</td>
<td>Double Sync mode</td>
</tr>
<tr>
<td>11</td>
<td>Pulse mode</td>
</tr>
</tbody>
</table>

Control Register Direct Mode

The default mode is Direct mode. As shown in Figure 33-32, when the Control Register is written by the CPU the output of the control register is driven directly to the routing on that write cycle.

Control Register Sync Mode

In Sync mode, as shown in Figure 33-33, the control register output is driven by a re-sampling register clocked by the currently selected Status and Control (SC) clock. This allows the timing of the output to be controlled by the selected SC clock, rather than the HFCLK.

Control Register Double Sync Mode

In Double Sync mode, as shown in Figure 33-34, a second register clocked by the selected SC clock is added after the re-sampling register. This allows the circuit to perform robustly when the HFCLK and SC clock are asynchronous.
**Control Register Pulse Mode**

Pulse mode is similar to Sync mode in that the control bit is re-sampled by the SC clock; the pulse starts on the first SC clock cycle following the bus write cycle. The output of the control bit is asserted for one full SC clock cycle. At the end of this clock cycle, the control bit is automatically reset.

With this mode of operation, firmware can write a ‘1’ to a control register bit to generate a pulse. After it is written as a ‘1’, it is read back by firmware as a ‘1’ until the completion of the pulse, after which it is read back as a ‘0’. The firmware can then write another ‘1’ to start another pulse. A new pulse cannot be generated until the previous one is completed. Therefore, the maximum frequency of pulse generation is every other SC clock cycle.

**Control Register Reset**

The control register has two reset modes, controlled by the EXT RES configuration bit, as shown in Figure 33-35. When EXT RES is 0 (the default) then in sync or pulse mode the routed reset input resets the synced output but not the actual control bit. When EXT RES is 1 then the routed reset input resets both the control bit and the synced output.

**Parallel Input/Output Mode**

In this mode, as Figure 33-36 shows, the status and control routing is connected to the datapath parallel in and parallel out signals. To enable this mode, the SC OUT configuration bits in the UDB CFG22 registers are set to select datapath parallel out. The parallel input connection is always available, but these routing connections are shared with the status register inputs, counter control inputs, and the interrupt output.
33.2.3.4 Counter Mode

As shown in Figure 33-37, when the block is in counter mode, a 7-bit down counter is exposed for use by UDB internal operation or firmware applications. This counter has the following features:

- A 7-bit read/write period register.
- A 7-bit read/write count register. It can be accessed only when the counter is disabled.
- Automatic reload of the period to the count register on terminal count (0).
- A firmware control bit in the Auxiliary Control (ACTL0) working register called CNT START, to start and stop the counter. (This is an overriding enable and must be set for optional routed enable to be operational.)

- Selectable bits from the routing for optional dynamic control of the counter enable and load functions:
  - EN, routed enable to start or stop counting.
  - LD, routed load signal to force the reload of period. When this signal is asserted, it overrides a pending terminal count. It is level sensitive and continues to load the period while asserted.

- The 7-bit count may be driven to the routing fabric as sc_out[6:0].
- The terminal count may be driven to the routing fabric as sc_out[7].
- In default mode, the terminal count is registered. In alternate mode the terminal count is combinational.
- In default mode, the routed enable, if used, must be asserted for routed load to operate. In alternate mode the routed enable and routed load signals operate independently.

To enable the counter mode, the SC_OUT_CTL[1:0] bits of the UDB CFG22 register must be set to counter output. In this mode the normal operation of the control register is not available. The status register can still be used for read operations, but should not be used to generate an interrupt because the mask register is reused as the counter period register. The Period register is implemented as a retention register and maintains its state across sleep intervals. For a period of N clocks, the period value of N–1 should be loaded. N = 1 (period of 0) is not supported as a clock divide value, and results in the terminal count output of a constant 1. The use of SYNC mode depends on whether the dynamic control inputs (LD/EN) are used. If they are not used, SYNC mode is unaffected. If they are used, SYNC mode is unavailable.

![Figure 33-37. Counter Mode](image-url)
33.2.3.5 Sync Mode

As shown in Figure 33-38, the status register can operate as a 4-bit double synchronizer, clocked by the current SC_CLK, when the SYNC MD bit in the UDB CFG22 register is set. This mode may be used to implement local synchronization of asynchronous signals, such as GPIO inputs. When enabled, the signals to be synchronized are selected from SC_IN[3:0], the outputs are driven to the SC_IO_OUT[3:0] pins, and SYNC MD automatically puts the SC_IO pins into output mode. When in this mode, the normal operation of the status register is not available, and the status sticky bit mode is forced off, regardless of the control settings for this mode. The control register is not affected by the mode. The counter can still be used with limitations. No dynamic inputs (LD/EN) to the counter can be enabled in this mode.

Figure 33-38. Sync Mode

33.2.3.6 Status and Control Clocking

The status and control registers require a clock selection for any of the following operating modes:

- Status register with any bit set to sticky, clear on read mode.
- Control register in counter mode.
- Sync mode.

The clock for this is allocated in the reset and clock control module. See "Reset and Clock Control Module" on page 401.

33.2.3.7 Auxiliary Control Register

The read-write Auxiliary Control register is a special register that controls fixed function hardware in the UDB. This register allows CPU to dynamically control the interrupt, FIFO, and counter operation. The register bits and descriptions are as follows.

<table>
<thead>
<tr>
<th>Auxiliary Control Registers</th>
</tr>
</thead>
<tbody>
<tr>
<td>CNT START</td>
</tr>
</tbody>
</table>

### FIFO0 Clear, FIFO1 Clear

The FIFO0 CLR and FIFO1 CLR bits are used to reset the state of the associated FIFO. When a ‘1’ is written to these bits, the state of the associated FIFO is cleared. These bits must be written back to ‘0’ to allow FIFO operation to continue. When these bits are left asserted, the FIFOs operate as simple one-byte buffers, without status.

### FIFO0 Level, FIFO1 Level

The FIFO0 LVL and FIFO1 LVL bits control the level at which the 4-byte FIFO asserts bus status (when the bus is either reading or writing to the FIFO) to be asserted. The meaning of FIFO bus status depends on the configured direction, as shown in Table 33-20.

<table>
<thead>
<tr>
<th>FIFOx LVL</th>
<th>Input Mode (Bus is Writing FIFO)</th>
<th>Output Mode (Bus is Reading FIFO)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Not Full</td>
<td>Not Empty</td>
</tr>
<tr>
<td></td>
<td>At least 1 byte can be written</td>
<td>At least 1 byte can be read</td>
</tr>
<tr>
<td>1</td>
<td>At Least Half Empty</td>
<td>At Least Half Full</td>
</tr>
<tr>
<td></td>
<td>At least 2 bytes can be written</td>
<td>At least 2 bytes can be read</td>
</tr>
</tbody>
</table>

### Interrupt Enable

When the status register’s interrupt generation logic is enabled, the INT EN bit gates the resulting interrupt signal.

### Count Start

The CNT START bit may be used to enable and disable the counter (valid only when the SC_OUT_CTL[1:0] bits are configured for counter output mode).
33.2.3.8 Status and Control Register Summary

Table 33-21 summarizes the function of the status and control registers. Note that the control and mask registers are shared with the count and period registers and the meaning of these registers is mode dependent.

Table 33-21. Status, Control Register Function Summary

<table>
<thead>
<tr>
<th>Mode</th>
<th>Control/Count</th>
<th>Status/SYNC</th>
<th>Mask/Period</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control</td>
<td>Control Out</td>
<td>Status In or</td>
<td>Status Mask</td>
</tr>
<tr>
<td>Count</td>
<td>Count Out</td>
<td>SYNC</td>
<td>Count Period</td>
</tr>
<tr>
<td>Status</td>
<td>Control Out or Count Out</td>
<td>Status In</td>
<td>Status Mask</td>
</tr>
<tr>
<td>SYNC</td>
<td>SYNC</td>
<td>NA(^b)</td>
<td></td>
</tr>
</tbody>
</table>

- Note that in counter mode, the mask register is operating as a period register and cannot function as a mask register. Therefore, interrupt output is not available when counter mode is enabled.
- Note that in SYNC mode, the status register function is not available, and therefore, the mask register is unusable. However, it can be used as a period register for count mode.

33.2.4 Reset and Clock Control Module

The primary function of the reset and clock block is to select a clock from the available global system clocks or HFCLK for each of the PLDs, the datapath, and the status and control block. It also supplies dynamic and firmware-based resets to the UDB blocks. As shown in Figure 33-39, there are four clock control blocks, and one reset block. Four inputs are available for use from the routing matrix (RC_IN[3:0]). Each clock control block can select a clock enable source from these routing inputs, and there is also a multiplexer to select one of the routing inputs to be used as an external clock source. As shown, the external clock source selection can be optionally synchronized. There are a total of six clocks that can be selected for each UDB component: four UDB peripheral clocks, HFCLK, and the selected external clock (ext clk). Any of the routed input signals (rc_in) can be used as either a level sensitive or edge sensitive enable. The reset function of this block provides a routed reset for the PLD blocks and SC counter, and a firmware reset capability to each block to support reconfiguration.

The HFCLK input to the reset and clock control is distinct from the system HFCLK. This clock is called “hf_clk_app” because it is gated similar to the other UDB peripheral clocks and used for UDB applications. The system HFCLK is used only for I/O access and is automatically gated, per access. The datapath clock generator produces three clocks: one for the datapath in general, and one for each of the FIFOs.
Figure 33-39. Reset and Clock Control
33.2.4.1 Clock Control

Figure 33-40 illustrates one instance of the clock selection and enable circuit. Each UDB has four of these circuits: one for each of the PLD blocks, one for the datapath, and one for the status and control block. The main components of this circuit are a global clock selection multiplexer, clock inversion, clock enable selection multiplexer, clock enable inversion, and edge detect logic.

**Clock Selection**

Four UDB peripheral clocks (see Clocking System chapter on page 146), gclk[0] to gclk[3], are routed to all UDBs; the remaining four clock configurations, gclk[4] to gclk[7], are not supported in the PSoC 6 MCU. Any of these clocks may be selected. UDB peripheral clocks are the output of user-selectable clock dividers. Another selection is HFCLK, which is the highest frequency in the system. Called “hf_clk_app,” this signal is routed separately from the system HFCLK. In addition, an external routing signal can be selected as a clock input to support direct-clocked functions such as SPI. Because application functions are mapped to arbitrary boundaries across UDBs, individual clock selection for each UDB subcomponent block supports a fine granularity of programming.

**Clock Inversion**

The selected clock may be optionally inverted. This limits the maximum frequency of operation due to the existence of one half cycle timing paths. Simultaneous bus writes and internal writes (for example writing a new count value while a counter is counting) are not supported when the internal clock is inverted and the same frequency as HFCLK. This limitation affects A0, A1, D0, D1, and the Control register in counter mode.

**Clock Enable Selection**

The clock enable signal may be routed to any synchronous signal and can be selected from any of the four inputs from the routing matrix that are available to this block.

**Clock Enable Inversion**

The clock enable signal may be optionally inverted. This feature allows the clock enable to be generated in any polarity.

**Clock Enable Mode**

By default, the clock enable is OFF. After configuring the target block operation, software can set the mode to one of the following using the EN MODE[1:0] bits of the UDB CFG24 register shown in Figure 33-40.

<table>
<thead>
<tr>
<th>Clock Enable Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00: off</td>
<td></td>
</tr>
<tr>
<td>01: on</td>
<td></td>
</tr>
<tr>
<td>10: positive edge</td>
<td></td>
</tr>
<tr>
<td>11: level</td>
<td></td>
</tr>
</tbody>
</table>

Table 33-22. Clock Enable Mode in UDB CFG24 Register
Clock Enable Usage

The two general usage scenarios for the clock enable are:

**Firmware Enable** – It is assumed that most functions require a firmware clock enable to start and stop the function. Because the boundary of a function mapped into the UDB array is arbitrary—it may span multiple UDBs and/or portions of UDBs—there must be a way to enable a given function atomically. This is typically implemented from a bit in a control register routed to one or more clock enable inputs. This scenario also supports the case where applications require multiple, unrelated blocks to be enabled simultaneously.

**Emulated Local Clock Generation** – This feature allows local clocks to be generated by UDBs, and distributed to other UDBs in the array by using a synchronous clock enable implementation scheme, rather than directly clocking from one UDB to another. Using the positive edge feature of the clock enable mode eliminates restrictions on the duty cycle of the clock enable waveform.

### Special FIFO Clocking

The datapath FIFOs have special clocking considerations. By default, the FIFO clocks follow the same configuration as the datapath clock. However, the FIFOs have special control bits that alter the clock configuration:

- Each FIFO clock can be inverted with respect to the selected datapath clock polarity.
- When FIFO FAST mode is set in the UDB CFG16 register, the HFCLK overrides the datapath clock selection normally in use by the FIFO.

#### 33.2.4.2 Reset Control

The two modes of reset control are: compatible mode and alternate mode. The modes are controlled by the ALT RES bit in each UDB CFG31 register. When this bit is ‘0’, the compatible scheme is implemented. When this bit is ‘1’, the alternate scheme is implemented.

##### Compatible Reset Scheme

This scheme features a routed reset, for dynamically resetting the embedded state of block, which can be applied to each PLD macrocell and the SC counter.

##### Compatible PLD Reset Control

Figure 33-41 shows the compatible PLD reset system, using routed dynamic resets.
**Compatible Datapath Reset Control**

*Figure 33-42* shows the compatible datapath reset system, using firmware reset. The firmware reset asynchronously clears the DP output registers, the carry and shift out flags, the FIFO state, accumulators, and data registers. Note that the D0 and D1 registers are implemented as retention registers that maintain their state across sleep intervals. The FIFO data is unknown because it is RAM-based.

*Figure 33-42. Compatible Datapath Reset Structure*
Compatible Status and Control Reset Control

Figure 33-43 shows the compatible status and control block reset. The mask/period and auxiliary control registers are retention registers.

Alternate Reset Scheme

Table 33-23 shows a summary of the differences between the compatible reset scheme and the alternate reset scheme.

<table>
<thead>
<tr>
<th>Feature</th>
<th>Compatible</th>
<th>Alternate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Granularity</td>
<td>One routed reset is shared by all blocks in the UDB</td>
<td>Each UDB component block can select an individual reset</td>
</tr>
<tr>
<td>Status register</td>
<td>No routed reset capability</td>
<td>Optionally can use the selected SC routed reset</td>
</tr>
<tr>
<td>Datapath</td>
<td>No routed reset capability</td>
<td>Optionally can use the selected DP routed reset</td>
</tr>
</tbody>
</table>
Alternate PLD Reset Control

Figure 33-44 shows the alternate PLD reset system. Although there are provisions for individual resets for each PLD, this is not supported in the PLD block. Therefore, in the alternate reset scheme, the PLD0 reset control settings applies to both PLDs.

![Diagram showing alternate PLD reset structure](image)

Note: The current PLD only supports 1 routed reset. Both are controlled by PLD0 routed reset.
Alternate Datapath Reset Control

Figure 33-45 shows the alternate datapath reset system. The datapath routed reset applies to all datapath states, except the data registers, which are implemented as retention registers.

Figure 33-45. Alternate Datapath Reset Structure
Alternate Status and Control Reset Control

Figure 33-46 shows the alternate status and control block reset. The mask/period and auxiliary control registers are retention registers.

![Figure 33-46. Alternate Status and Control Reset Control](image)

33.2.4.3 UDB POR Initialization

Register and State Initialization

Table 33-24. UDB POR State Initialization

<table>
<thead>
<tr>
<th>State Element</th>
<th>State Element</th>
<th>POR State</th>
</tr>
</thead>
<tbody>
<tr>
<td>Configuration Latches</td>
<td>CFG 0 – 31</td>
<td>0</td>
</tr>
<tr>
<td>Ax, Dx, CTL, ACTL, MASK</td>
<td>Accumulators, data registers, auxiliary control register, mask register</td>
<td>0</td>
</tr>
<tr>
<td>ST, Macrocell</td>
<td>Status and macrocell read only registers</td>
<td>0</td>
</tr>
<tr>
<td>DP CFG RAM and Fx (FIFOs)</td>
<td>Datapath configuration RAM and FIFO RAM</td>
<td>Unknown</td>
</tr>
<tr>
<td>PLD RAM</td>
<td>PLD configuration RAM</td>
<td>Unknown</td>
</tr>
</tbody>
</table>

Routing Initialization

On POR, the state of input and output routing is as follows:

- All outputs from the UDB that drive into the routing matrix are held at ‘0’.
- All drivers out of the routing and into UDB inputs are initially gated to ‘0’.

As a result of this initialization, conflicting drive states on the routing are avoided and initial configuration occurs in an order-independent sequence.

33.2.5 UDB Addressing

The UDBs can be accessed through a number of address spaces, for 8, 16, and 32-bit accesses of both the working registers (A0, A1, D0, D1, FIFOs, and so on) and the configuration registers.

- 8-bit working registers – This address space allows access to individual working registers in a single UDB.
- 16-bit working registers consecutive – This address space allows access to the same working register in two consecutive UDBs, for example D0 of UDB n and D0 of UDB n + 1
- 16-bit working registers paired – This address space allows access to two working registers, for example A0 and A1, from the same UDB.
32-bit working registers – This address space allows access to the same working register, for example A1, in all four UDBs.

8-, 16-, or 32-bit configuration registers – This address space allows access to the configuration registers for a single UDB.

33.2.6 System Bus Access Coherency

UDB registers have dual access modes:

- System bus access, where the CPU is reading or writing a UDB register.
- UDB internal access, where the UDB function is updating or using the contents of a register.

### 33.2.6.1 Simultaneous System Bus Access

Table 33-25 lists the possible simultaneous access events and required behavior:

<table>
<thead>
<tr>
<th>Register</th>
<th>UDB Write Bus Write</th>
<th>UDB Write Bus Read</th>
<th>UDB Read Bus Write</th>
<th>UDB Read Bus Read</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ax</td>
<td>Undefined result</td>
<td>Not allowed directly&lt;sup&gt;a, b&lt;/sup&gt;</td>
<td>UDB reads previous value</td>
<td>Current value is read by both</td>
</tr>
<tr>
<td>Dx</td>
<td>Not supported (UDB and bus must be opposite access)</td>
<td>If FIFO status flags are used, no simultaneous read/write at the same location is possible</td>
<td>Not supported (UDB and bus must be opposite access)</td>
<td></td>
</tr>
<tr>
<td>Fx</td>
<td>NA, bus does not write</td>
<td>Bus reads previous value</td>
<td>NA, UDB does not read</td>
<td></td>
</tr>
<tr>
<td>ST</td>
<td>NA, UDB does not write</td>
<td>Bus reads previous value</td>
<td>NA, UDB does not read</td>
<td></td>
</tr>
<tr>
<td>CTL</td>
<td>Undefined result</td>
<td>Not allowed directly&lt;sup&gt;c&lt;/sup&gt;</td>
<td>UDB reads previous value</td>
<td>Current value is read by both</td>
</tr>
<tr>
<td>CNT</td>
<td>NA, UDB does not write</td>
<td>NA, UDB does not write</td>
<td>UDB reads previous value</td>
<td>Current value is read by both</td>
</tr>
<tr>
<td>ACTL</td>
<td>NA, UDB does not write</td>
<td>NA, UDB does not write</td>
<td>UDB reads previous value</td>
<td>Current value is read by both</td>
</tr>
<tr>
<td>MASK</td>
<td>NA, UDB does not write</td>
<td>NA, UDB does not write</td>
<td>UDB reads previous value</td>
<td>Current value is read by both</td>
</tr>
<tr>
<td>PER</td>
<td>NA, UDB does not write</td>
<td>NA, UDB does not write</td>
<td>UDB reads previous value</td>
<td>Current value is read by both</td>
</tr>
</tbody>
</table>

<sup>a</sup> The Ax registers can be safely read by using the software capture feature of the FIFOs.

<sup>b</sup> The Dx registers can only be written dynamically by the FIFOs. When this mode is programmed, direct read of the Dx registers is not allowed.

<sup>c</sup> The CNT register can only be safely read when it is disabled. An alternative for dynamically reading the CNT value is to route the output to the SC register (in transparent mode).

<sup>d</sup> Macrocell register bits can also be routed to the status register (in transparent mode) inputs for safe reading.

### 33.2.6.2 Coherent Accumulator Access (Atomic Reads and Writes)

The UDB accumulators are the primary target of data computation. Therefore, reading these registers directly during normal operation gives an undefined result, as indicated in Table 33-25. However, there is built-in support for atomic reads in the form of software capture, which is implemented across chained blocks. In this usage model, a read of the least significant accumulator transfers the data from all chained blocks to their associated FIFOs. Atomic writes to the accumulator can be implemented programmatically. Individual writes can be performed to the input FIFOs, and then the status signal of the last FIFO written can be routed to all associated blocks and simultaneously transfer the FIFO data into the Dx or Ax registers.
33.3 Port Adapter Block

The Port Adaptor block extends the UDBs to provide an interface to the GPIOs through the High-Speed I/O Matrix (HSIOM), described in "High-Speed I/O Matrix" on page 170. The HSIOM places registers for faster routing of DSI signals to GPIO outputs and output enables. The HSIOM also allows GPIOs to be shared amongst multiple blocks, for example port data registers and peripherals such as I2C. Figure 33-47 shows a high-level view.

![Figure 33-47. Port Adapter Block Diagram](image)

Each 8-bit GPIO port has one port adaptor (PA). There are eight inputs from the GPIO data in, eight outputs to the GPIO data out, and eight output enable (OE) connections. The registers in the PA are used for synchronizing inputs, outputs, and output enables. Another feature is the port input clock multiplexer. This multiplexer selects one of the port inputs to be used as a clock. The clock can be used locally in the PA and routed to the global clocks (see Clocking System chapter on page 146).

Two programmable clock selectors are available, to supply separate clocks for the input and output synchronization registers. The OE register uses the same clock as the output register. Also, two programmable reset selectors are available, in the same manner as for the clock selectors.

33.3.1 PA Data Input Logic

Figure 33-48 shows the structure for the data input logic. Inputs are from each pin of an I/O port. The signal can be either single synchronized or double synchronized, or synchronization can be bypassed for asynchronous inputs. Synchronization is to the selected port input clock. The output of this circuit connects to the DSI routing.

![Figure 33-48. Detail of GPIO Input Logic](image)
33.3.2 PA Port Pin Clock Multiplexer Logic

Figure 33-49 shows the port pin multiplexer. Each port has eight data input signals, one of which is selected for use as a clock. This selection is routed for use as:

- Programmable clock in the port adapter
- Source for the UDB clock tree
- Programmable reset in the port adapter
- For use as a clock enable in the port adapter.

Note that the selected signal does not pass through synchronizers and is asynchronous to other clock domains within the block. It should be used carefully for selected functions.

![Figure 33-49. Detail of GPIO Pin Selection](image)

33.3.3 PA Data Output Logic

Figure 33-50 shows the structure for the data output logic. Outputs go to each pin of an I/O port (through HSIOM). The signal can be single synchronized or synchronization can be bypassed for asynchronous outputs. Other options include the ability to output either the selected clock or an inverted version of the clock.

![Figure 33-50. Detail of GPIO Output Data Logic](image)
33.3.4 PA Output Enable Logic

Figure 33-51 shows the output enable (OE) logic. This circuit shares the clock and reset associated with data output. This connection is unique in that there are four DSI outputs associated with the OE, but these are muxed to a total of four OE connections to the I/O port pins, as Figure 33-52 shows.

Note that due to the active low sense of the OE signals at the ports, there is an additional inversion in the path between the OE sync logic and the OE multiplexers.
33.3.5 PA Clock Multiplexer

Figure 33-53 shows the structure of the PA clock multiplexer. As noted previously, each PA has two programmable clock selectors, to supply separate clocks for port inputs and outputs and output enables (OEs).

![Figure 33-53. PA Clock Multiplexer Detail](image)

33.3.6 PA Reset Multiplexer

The structure of the PA reset multiplexer is shown in Figure 33-54.

![Figure 33-54. PA Reset Multiplexer Detail](image)

As shown in Figure 33-55, the reset selection logic is duplicated, one for input, and one that serves both output and output enable. Each of these resets has an individual enable, which applies to all eight bits in the associated category.

![Figure 33-55. PA Reset System](image)
Section E: Analog Subsystem

This section encompasses the following chapters:
- Analog Reference Block chapter on page 416
- Low-Power Comparator chapter on page 419
- Continuous Time Block mini (CTBm) chapter on page 424
- Continuous Time DAC chapter on page 430
- SAR ADC chapter on page 439
- Temperature Sensor chapter on page 460
- Analog Routing chapter on page 463
- CapSense chapter on page 466

Top Level Architecture

Analog System Block Diagram
34. Analog Reference Block

The Analog Reference block (AREF) generates highly accurate reference voltage and currents needed by the programmable analog subsystem (PASS) and CapSense (CSD) blocks.

34.1 Features

- Provides accurate bandgap references for PASS and CSD subsystems
- 1.2-V voltage reference ($V_{REF}$) generator
- Option to output alternate voltage references routed from SRSS or from an external pin
- Proportional to absolute temperature (IPTAT) current reference generation
- Zero dependency to absolute temperature (IZTAT) flat current reference generation, which is independent of temperature variations
- Option to generate IZTAT from SRSS generated current reference
- Option to enable or disable references in Deep Sleep mode
34.2 Architecture

Figure 34-1 shows the architecture of the AREF block. AREF contains a precise bandgap reference, which generates a 1.2-V $V_{\text{REF}}$ and a PTAT current that is 1 $\mu$A at room temperature (23 °C). It also generates a current reference, which is stable over temperature (IZTAT).
34.2.1 Bandgap Reference Block

The AREF block contains a local bandgap reference generator, which has tighter accuracy, temperature stability, and lower noise than the SRSS bandgap reference. The bandgap reference block provides a temperature stable voltage and current reference \( V_{\text{REF}} \) and an additional current that tracks temperature. All AREF output currents are sinking.

Table 34-1. Bandgap References in AREF

<table>
<thead>
<tr>
<th>Bandgap Reference Outputs</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>VREF</td>
<td>1.2 V</td>
</tr>
<tr>
<td>IPTAT</td>
<td>1 µA</td>
</tr>
</tbody>
</table>

34.2.2 Zero Dependency To Absolute Temperature Current Generator (IZTAT)

The IZTAT current generator uses the output of the bandgap reference block to generates a precise current reference, which has a low variation over temperature.

Table 34-2. IZTAT Reference

<table>
<thead>
<tr>
<th>IZTAT Reference Outputs</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>IZTAT</td>
<td>1 µA</td>
</tr>
</tbody>
</table>

34.2.3 Reference Selection Multiplexers

AREF has two multiplexers to select the sources for the output references.

34.2.3.1 \( V_{\text{REF}} \) Selection Multiplexer Options

- SRSS – routes the \( V_{\text{REF}} \) from SRSS (0.8 V)
  
  Note: SRSS references are not available in Deep Sleep power mode. This option should not be used when the device is in Deep Sleep mode.

- Local – routes the locally generated bandgap reference (1.2 V)

- External – routes the reference from the external \( V_{\text{REF}} \) pin

34.2.3.2 IZTAT Selection Multiplexer Options

- SRSS - uses the SRSS current reference (250 nA) to generate IZTAT.

  Note: SRSS references are not available in Deep Sleep power mode. This option should not be used when the device is in Deep Sleep mode.

- Local - internally generates IZTAT

34.2.4 Startup Modes

AREF supports two startup modes, which provide a trade-off between wakeup time and noise performance when transitioning from the Deep Sleep to Active power mode. This is selected using the AREF_MODE bit of the AREF_CTRL register. The FAST_START mode enables faster wakeup, but with higher noise levels. Firmware can switch to NORMAL mode after the FAST_START settling time to achieve better noise performance.

Table 34-3. Startup Modes

<table>
<thead>
<tr>
<th>AREF_MODE</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 (NORMAL)</td>
<td>Normal startup mode</td>
</tr>
<tr>
<td>1 (FAST_START)</td>
<td>Fast startup mode</td>
</tr>
</tbody>
</table>

34.2.5 Low-Power Modes

AREF’s voltage and current references can be made available during the Deep Sleep power mode. This is configured using the DEEPSLEEP_ON bit in the AREF_CTRL register. Individual references can be active by configuring DEEPSLEEP_MODE as shown in Table 34-4.

Note: These options are applicable only when DEEPSLEEP_ON = 1.

Table 34-4. Deep Sleep Mode

<table>
<thead>
<tr>
<th>DEEPSLEEP_MODE[1:0]</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00 (OFF)</td>
<td>All references are OFF during Deep Sleep</td>
</tr>
<tr>
<td>01 (IPTAT)</td>
<td>IPTAT is ON during Deep Sleep. This mode enables fast wakeup from Deep Sleep.</td>
</tr>
<tr>
<td>10 (IPTAT_IZTAT)</td>
<td>IPTAT and IZTAT are ON during Deep Sleep and available to CTBm</td>
</tr>
<tr>
<td>11 (IPTAT_IZTAT_VREF)</td>
<td>IPTAT, IZTAT, and VREF are ON during Deep Sleep</td>
</tr>
</tbody>
</table>

34.3 Registers

Table 34-5. List of AREF Registers

<table>
<thead>
<tr>
<th>Register</th>
<th>Comment</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>AREF_CTRL</td>
<td>AREF control register</td>
<td>Reference selection, startup time, and low-power mode.</td>
</tr>
</tbody>
</table>
35. Low-Power Comparator

PSOC 6 MCUs have two low-power comparators, which can perform fast analog signal comparison of internal and external analog signals in all system power modes. Low-power comparator output can be inspected by the CPU, used as an interrupt/wakeup source to the CPU when in low-power mode (Sleep, LPSLEEP, or Deep Sleep), used as a wakeup source to system resources when in Hibernate mode, or fed to DSI as an asynchronous or synchronous signal (level or pulse).

35.1 Features

The PSoC 6 MCU comparators have the following features:
- Configurable input pins
- Programmable power and speed
- Ultra low-power mode support
- Each comparator features a one-sided hysteresis option
- Rising edge, falling edge, combined rising and falling edge detection at the comparator output
- Local reference voltage generation
- Wakeup source from low-power modes

35.2 Architecture

Figure 35-1 shows the block diagram for the low-power comparator.
The following sections describe the operation of the PSoC 6 MCU low-power comparator, including input configuration, power and speed modes, output and interrupt configuration, hysteresis, and wakeup from low-power modes.

### 35.2.1 Input Configuration

Low-power comparators can operate with the following input modes:

- Compare two voltages from external pins
- Compare a voltage from an external pin against an internally generated analog-signal (through AMUXBUS).
- Compare two internal voltages through AMUXBUS A/AMUXBUS B
- Compare internal/external signals with a locally generated reference voltage. Note that this voltage is not a precision reference and can vary from 0.4 V–0.8 V.

See the device datasheet for detailed specifications of the low-power comparator.

Note that AMUXBUS connections are not available in Deep Sleep and Hibernate modes. If Deep Sleep or Hibernate operation is required, the low-power comparator must be connected to the dedicated pins. This restriction also includes routing of any internally-generated signal, which uses the AMUXBUS for the connection. See the I/O System chapter on page 164 for more details on connecting the GPIO to AMUXBUS A/B or setting up the GPIO for comparator input. See the Analog Routing chapter on page 463 for detailed, device-level analog routing information.

Refer to the LPCOMP_CMP0_SW, LPCOMP_CMP1_SW, LPCOMP_CMP0_SW_CLEAR, and LPCOMP_CMP1_SW_CLEAR registers in the PSoC 63 with BLE Registers TRM to understand how to control the internal routing switches shown in Figure 35-1.

If the inverting input of a comparator is routed to a local voltage reference, the LPREF_EN bit in the LPCOMP_CONFIG register must be set to enable the voltage reference.

### 35.2.2 Output and Interrupt Configuration

Both Comparator0 and Comparator1 have hardware outputs available at dedicated pins. See the device datasheet for the location of comparator output pins. In addition, comparator outputs can be routed through DSI to the programmable digital logic (UDBs) or any GPIO that supports DSI.

Firmware readout of Comparator0 and Comparator1 outputs are available at the OUT0 and OUT1 bits of the LPCOMP_STATUS register (Table 35-1). The output of each comparator is connected to a corresponding edge detector block. This block determines the edge that triggers the interrupt. The edge selection and interrupt enable is configured using the INTTYPE0 and INTTYPE1 bitfields in the LPCOMP_CMP0_CTRL and LPCOMP_CMP1_CTRL registers for Comparator0 and Comparator1, respectively.
Using the INTTYPE0 and INTTYPE1 bits, the interrupt type can be selected to disabled, rising edge, falling edge, or both edges, as described in Table 35-1.

Each comparator's output can also be routed directly to a GPIO pin through the HSIOM. See the I/O System chapter on page 164 for more details.

During an edge event, the comparator will trigger an interrupt. The interrupt request is registered in the COMP0 bit and COMP1 bit of the LPCOMP_INTR register for Comparator0 and Comparator1, respectively. Both Comparator0 and Comparator1 share a common interrupt signal output (see Figure 35-1), which is a logical OR of the two interrupts and mapped as the low-power comparator block’s interrupt in the CPU NVIC. Refer to the Interrupts chapter on page 47 for details. If both the comparators are used in a design, the COMP0 and COMP1 bits of the LPCOMP_INTR register must be read in the interrupt service routine to know which one triggered the interrupt. Alternatively, COMP0_MASK bit and COMP1_MASK bit of the LPCOMP_INTR_MASK register can be used to mask the Comparator0 and Comparator1 interrupts to the CPU. Only the masked interrupts will be serviced by the CPU. After the interrupt is processed, the interrupt should be cleared by writing a ‘1’ to the COMP0 and COMP1 bits of the LPCOMP_INTR register in firmware. If the interrupt to the CPU is not cleared, it stays active regardless of the next compare events. This can interrupt the CPU continuously. Refer to the Interrupts chapter on page 47 for details.

LPCOMP_INTR_SET register bits [1:0] can be used to assert an interrupt for firmware debugging.

In Deep Sleep mode, the wakeup interrupt controller (WIC) can be activated by a comparator edge event, which then wakes up the CPU. Similarly in Hibernate mode, the LPCOMP can wake up the system resources sub-system. Thus, the LPCOMP has the capability to monitor a specified signal in low-power modes. See the Power Supply and Monitoring chapter on page 120 and the Device Power Modes chapter on page 128 for more details.

### Table 35-1. Output and Interrupt Configuration

<table>
<thead>
<tr>
<th>Register[Bit_Pos]</th>
<th>Bit_Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPCOMP_STATUS[0]</td>
<td>OUT0</td>
<td>Current/instantaneous output value of Comparator0</td>
</tr>
<tr>
<td>LPCOMP_STATUS[16]</td>
<td>OUT1</td>
<td>Current/instantaneous output value of Comparator1</td>
</tr>
<tr>
<td>LPCOMP_CMP0_CTRL[7:6]</td>
<td>INTTYPE0</td>
<td>Sets on which edge Comparator0 will trigger an IRQ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00: Disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01: Rising Edge</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10: Falling Edge</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11: Both rising and falling edges</td>
</tr>
<tr>
<td>LPCOMP_CMP1_CTRL[7:6]</td>
<td>INTTYPE1</td>
<td>Sets on which edge Comparator1 will trigger an IRQ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00: Disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01: Rising Edge</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10: Falling Edge</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11: Both rising and falling edges</td>
</tr>
<tr>
<td>LPCOMP_INTR[0]</td>
<td>COMP0</td>
<td>Comparator0 Interrupt: hardware sets this interrupt when Comparator0 triggers. Write a ‘1’ to clear the interrupt</td>
</tr>
<tr>
<td>LPCOMP_INTR[1]</td>
<td>COMP1</td>
<td>Comparator1 Interrupt: hardware sets this interrupt when Comparator1 triggers. Write a ‘1’ to clear the interrupt</td>
</tr>
<tr>
<td>LPCOMP_INTR_SET[0]</td>
<td>COMP0</td>
<td>Write a ‘1’ to trigger the software interrupt for Comparator0</td>
</tr>
<tr>
<td>LPCOMP_INTR_SET[1]</td>
<td>COMP1</td>
<td>Write a 1 to trigger the software interrupt for Comparator1</td>
</tr>
</tbody>
</table>

#### 35.2.3 Power Mode and Speed Configuration

The low-power comparators can operate in three power modes:
- Normal
- Low-power
- Ultra low-power

The power or speed setting for Comparator0 is configured using the MODE0 bitfield of the LPCOMP_CMP0_CTRL register. Similarly, the power or speed setting for Comparator1 is configured using the MODE1 bitfield of the LPCOMP_CMP1_CTRL register. The power consumption and response time vary depending on the selected power mode; power consumption is highest in fast mode and lowest in ultra-low-power mode, response time is fastest in fast mode and slowest in ultra-low-power mode.
mode. Refer to the device datasheet for specifications for the response time and power consumption for various power settings.

The comparators can also be enabled or disabled using these bitfields, as described in Table 35-2.

Note: The output of the comparator may glitch when the power mode is changed while comparator is enabled. To avoid this, disable the comparator before changing the power mode.

### Table 35-2. Comparator Power Mode Selection Bits

<table>
<thead>
<tr>
<th>Register[Bit_Pos]</th>
<th>Bit_Name</th>
<th>Description</th>
</tr>
</thead>
</table>
| LPCOMP_CMP0_CTRL[1:0] | MODE0 | Comparator0 power mode selection  
00: Off  
01: Ultra low-power operating mode. This mode must be used when the device is in Deep Sleep or Hibernate mode.  
10: Low-power operating mode  
11: Normal, full-speed, full-power operating mode  
See the device datasheet for electrical specifications in each power mode. |
| LPCOMP_CMP1_CTRL[1:0] | MODE1 | Comparator1 power mode selection  
00: Off  
01: Ultra low-power operating mode. This mode must be used when the device is in Deep Sleep or Hibernate mode.  
10: Low-power operating mode  
11: Normal, full-speed, full-power operating mode  
See the device datasheet for electrical specifications in each power mode. |

Additionally, the entire low-power comparator system can be enabled or disabled globally using the LPCOMP_CONFIG[31] bit. See the PSoC 63 with BLE Registers TRM for details of these bitfields.

#### 35.2.4 Hysteresis

For applications that compare signals close to each other and slow changing signals, hysteresis helps to avoid oscillations at the comparator output when the signals are noisy. For such applications, a fixed hysteresis may be enabled in the comparator block. See the device datasheet for the hysteresis voltage range.

The 30-mV hysteresis level is enabled/disabled by using the HYST0 and HYST1 bitfields in the LPCOMP_CMP0_CTRL and LPCOMP_CMP1_CTRL registers for Comparator0 and Comparator1, as described in Table 35-3.

### Table 35-3. Hysteresis Control Bits

<table>
<thead>
<tr>
<th>Register[Bit_Pos]</th>
<th>Bit_Name</th>
<th>Description</th>
</tr>
</thead>
</table>
| LPCOMP_CMP0_CTRL[5] | HYST0 | Enable/Disable hysteresis to Comparator0  
1: Enable Hysteresis  
0: Disable Hysteresis  
See the device datasheet for hysteresis voltage range. |
| LPCOMP_CMP1_CTRL[5] | HYST1 | Enable/Disable hysteresis to Comparator1  
1: Enable Hysteresis  
0: Disable Hysteresis  
See the device datasheet for hysteresis voltage range. |

#### 35.2.5 Wakeup from Low-Power Modes

The comparator is operational in the device’s low-power modes, including Sleep, Deep Sleep, and Hibernate modes. The comparator output can wake the device from Sleep and Deep Sleep modes. The comparator output can generate interrupts in Deep Sleep mode when enabled in the LPCOMP_CONFIG register, the INTTYPEEx bits in the LPCOMP_CMPx_CTRL register should not be set to disabled, and the INTR_MASKx bit should be set in the LPCOMP_INTR_MASK register for the corresponding comparator to wake the device from low-power modes. Comparisons involving AMUXBUS connections are not available in Deep Sleep and Hibernate modes. Moreover, if
the comparator is required in Deep Sleep or Hibernate modes, then it must be configured into Ultra Low-Power mode before the device is put into Deep Sleep or Hibernate mode.

In the Deep Sleep and Hibernate power modes, a compare event on either Comparator0 or Comparator1 output will generate a wakeup interrupt. The INTTYPEEx bits in the LPCOMP_CONFIG register should be properly configured. The mask bits in the LPCOMP_INTR_MASK register is used to select whether one or both of the comparator's interrupt is serviced by the CPU. See the Device Power Modes chapter on page 128 for more details.

35.2.6 Comparator Clock

The comparator uses the system main clock SYSCLK as the clock for interrupt synchronization. See the Clocking System chapter on page 146 for more details.

35.3 Register List

Table 35-4. Low-Power Comparator Register Summary

<table>
<thead>
<tr>
<th>Register</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPCOMP_CONFIG</td>
<td>LPCOMP global configuration register</td>
</tr>
<tr>
<td>LPCOMP_INTR</td>
<td>LPCOMP interrupt register</td>
</tr>
<tr>
<td>LPCOMP_INTR_SET</td>
<td>LPCOMP interrupt set register</td>
</tr>
<tr>
<td>LPCOMP_INTR_MASK</td>
<td>LPCOMP interrupt request mask register</td>
</tr>
<tr>
<td>LPCOMP_INTR_MASKED</td>
<td>LPCOMP masked interrupt output register</td>
</tr>
<tr>
<td>LPCOMP_STATUS</td>
<td>Output status register</td>
</tr>
<tr>
<td>LPCOMP_CMP0_CTRL</td>
<td>Comparator0 configuration register</td>
</tr>
<tr>
<td>LPCOMP_CMP1_CTRL</td>
<td>Comparator1 configuration</td>
</tr>
<tr>
<td>LPCOMP_CMP0_SW</td>
<td>Comparator0 switch control</td>
</tr>
<tr>
<td>LPCOMP_CMP1_SW</td>
<td>Comparator1 switch control</td>
</tr>
<tr>
<td>LPCOMP_CMP0_SW_CLEAR</td>
<td>Comparator0 switch control clear</td>
</tr>
<tr>
<td>LPCOMP_CMP1_SW_CLEAR</td>
<td>Comparator1 switch control clear</td>
</tr>
</tbody>
</table>
36. Continuous Time Block mini (CTBm)

The Continuous Time Block mini (CTBm) provides on-chip operational amplifiers (opamps) for creating continuous-time signal chains. Each CTBm includes a switch matrix for input/output configuration, two identical opamps, which are also configurable as two comparators, a charge pump inside each opamp, a sample-and-hold circuit, and a digital interface for comparator output routing, switch controls, and interrupts.

36.1 Features

The PSoC 6 MCU CTBm has the following features:
- Discrete, high-performance, and highly configurable on-chip operational amplifiers
- Programmable power, bandwidth, compensation, and output drive strength
- Flexible input and output routing
- Support for opamp voltage-follower mode using internal connections
- Comparator mode with optional 10-mV hysteresis
- Works as buffer/pre-amplifier for SAR inputs
- Works as buffer/amplifier/sample-and-hold for CTDAC outputs
- Operates in Deep Sleep power mode
36.2 Architecture

Figure 36-1. CTBm Block Diagram

Legend
- Firmware Controlled Switch
- Firmware and DSI Controlled Switch
- Firmware, DSI and SARSEQ Controlled Switch

Note: CTDAC is not a part of the CTBm. See the Continuous Time DAC chapter on page 430 for more details.

As the block diagram shows, the CTBm has two identical opamps, a switch routing matrix and a sample and hold circuit. Each opamp has one input and three output stages, all of which share the common input stage, as shown in Figure 36-1. Note that only one output stage can be selected at a time. The output stage can be operated as a low-drive strength internal buffer (1X), a high-drive strength external buffer (10X), or a comparator. The other configurable features are power and speed, compensation, sample and hold, and switch routing control.

Note that analog references required for CTBm must be enabled using the PASS_AREF_CTRL register. See the Analog Reference Block chapter on page 416 for more details.

Using the switching matrix, the opamp inputs and outputs can be connected to dedicated I/Os or other internal analog blocks. See the device datasheet for the location of CTBm port for the dedicated I/Os.

To use the CTBm, the first step is to set up external components (such as resistors), if required. Then, enable the block by setting the ENABLE bit in the CTBM_CTB_CTRL register. To have almost rail-to-rail input range and minimal distortion common mode input, there is one charge pump inside each opamp. The charge pump can be enabled by setting the OA0_PUMP_EN bit in the CTBM_OA_RES0_CTRL register for Opamp0 and OA1_PUMP_EN bitfield in the CTBM_OA_RES1_CTRL register for Opamp1. See the PSoC 63 with BLE Registers TRM for details of these registers.

After enabling the opamps and charge pumps, follow these steps to set up the amplifier:
1. Configure power mode
2. Configure output strength
3. Configure compensation
4. Configure input switch
5. Configure output switch, especially when opamp output must be connected to SAR ADC

Follow these steps to set up a comparator:
1. Configure the power mode
2. Configure the input switch
3. Configure the comparator output circuitry, as required - interrupt generation, DSI output, and so on.
4. Configure hysteresis and enable the comparator.

36.2.1 Power Mode and Output Strength Configuration

The opamp can operate in three power modes - low, medium, and high. Power modes are configured using the PWR_MODE bitfield in the respective CTBM_OA_RESx_CTRL register. The slew rate and gain-bandwidth product (GBW) are maximum in highest power mode and minimum in lowest power mode.

In addition, the output driver of each opamp can be configured to the internal driver low-drive strength (1X driver) or low-drive strength external driver (10X driver). 1X and 10X drivers are mutually exclusive - they cannot be active at the same time. 1X output driver is suited to drive smaller on-chip capacitive and resistive loads at higher speeds. The 10X output driver is useful for driving large off-chip capacitive and resistive loads. See the device datasheet for gain bandwidth, slew rate, and maximum output drive capability (IOUT specifications in various power modes and output strength configurations. Table 36-1 summarizes the bits used to configure the opamp output drive strength and power modes.

<table>
<thead>
<tr>
<th>Register[Bit_Pos]</th>
<th>Bit_Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTBM_CTB_CTRL[31]</td>
<td>ENABLE</td>
<td>CTBM power mode selection</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: CTBM is disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: CTBM is enabled</td>
</tr>
<tr>
<td>CTBM_OA_RES0_CTRL[11]</td>
<td>OA0_PUMP_EN</td>
<td>Opamp0 pump enable bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Opamp0 pump is disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Opamp0 pump is enabled</td>
</tr>
<tr>
<td>CTBM_OA_RES1_CTRL[11]</td>
<td>OA1_PUMP_EN</td>
<td>Opamp1 pump enable bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Opamp1 pump is disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Opamp1 pump is enabled</td>
</tr>
<tr>
<td>CTBM_OA_RES0_CTRL[1:0]</td>
<td>OA0_PWR_MODE</td>
<td>Opamp0 power mode select bits</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00: Opamp0 is OFF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01: Opamp0 is in low-power mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10: Opamp0 is in medium-power mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11: Opamp0 is in high-power mode</td>
</tr>
<tr>
<td>CTBM_OA_RES1_CTRL[1:0]</td>
<td>OA1_PWR_MODE</td>
<td>Opamp1 power mode select bits</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00: Opamp1 is OFF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01: Opamp1 is in low-power mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10: Opamp1 is in medium-power mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11: Opamp1 is in high-power mode</td>
</tr>
<tr>
<td>CTBM_OA_RES0_CTRL[2]</td>
<td>OA0_DRIVE_STR_SEL</td>
<td>Opamp0 output drive strength select bits</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Opamp0 output drive strength is 1X</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Opamp0 output drive strength is 10X</td>
</tr>
<tr>
<td>CTBM_OA_RES1_CTRL[2]</td>
<td>OA1_DRIVE_STR_SEL</td>
<td>Opamp1 output drive strength select bits</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Opamp1 output drive strength is 1X</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Opamp1 output drive strength is 10X</td>
</tr>
</tbody>
</table>

36.2.2 Compensation

Each opamp also has a programmable compensation capacitor block, which allows optimizing the stability of the opamp performance based on output load. The compensation of each opamp is controlled by the respective CTBM_OAx_COMP_TRIM register, as explained in Table 36-2. Note that all the GBW and slew rate specifications in the
device datasheet are applied for all compensation trims.

Table 36-2. Opamp Compensation Bits

<table>
<thead>
<tr>
<th>Register[Bit_Pos]</th>
<th>Bit_Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTBM_OAx_COMP_TRIM[1:0]</td>
<td>OAx_COMP_TRIM</td>
<td>Opamp compensation trim bits</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00: No compensation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01: Minimum compensation, high speed, and low stability</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10: Medium compensation, balanced speed, and stability</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11: Maximum compensation, low speed, and high stability</td>
</tr>
</tbody>
</table>

36.2.3 Switching Matrix

The CTBm has many switches to configure input and output routing of the opamps, as shown in Figure 36-1. Table 36-3 lists the switches and the respective control bits to open/close the switches.

Table 36-3. Switches and their Control Bits

<table>
<thead>
<tr>
<th>Switch</th>
<th>Description</th>
<th>Register</th>
<th>Bitfield</th>
</tr>
</thead>
<tbody>
<tr>
<td>A00</td>
<td>Opamp0 non-inverting input to AMUXBUS A</td>
<td>CTBM_OA0_SW</td>
<td>OA0P_A00</td>
</tr>
<tr>
<td>A20</td>
<td>Opamp0 non-inverting input to Px.0</td>
<td>CTBM_OA0_SW</td>
<td>OA0P_A00</td>
</tr>
<tr>
<td>A30</td>
<td>Opamp0 non-inverting input to Px.6 (and C6H)</td>
<td>CTBM_OA0_SW</td>
<td>OA0P_A30</td>
</tr>
<tr>
<td>A11</td>
<td>Opamp0 inverting input to Px.1</td>
<td>CTBM_OA0_SW</td>
<td>OA0M_A11</td>
</tr>
<tr>
<td>A81</td>
<td>Opamp0 inverting input to output</td>
<td>CTBM_OA0_SW</td>
<td>OA0M_A81</td>
</tr>
<tr>
<td>D51</td>
<td>Opamp0 output to sarbus0</td>
<td>CTBM_OA0_SW</td>
<td>OA0O_D51</td>
</tr>
<tr>
<td>D81</td>
<td>Opamp0 - shorts 1X, 10X outputs</td>
<td>CTBM_OA0_SW</td>
<td>OA0O_D81</td>
</tr>
<tr>
<td>A03</td>
<td>Opamp1 non-inverting input to AMUXBUS B</td>
<td>CTBM_OA1_SW</td>
<td>OA1P_A03</td>
</tr>
<tr>
<td>A13</td>
<td>Opamp1 non-inverting input to Px.5</td>
<td>CTBM_OA1_SW</td>
<td>OA1P_A13</td>
</tr>
<tr>
<td>A43</td>
<td>Opamp1 non-inverting input to Px.7</td>
<td>CTBM_OA1_SW</td>
<td>OA1P_A43</td>
</tr>
<tr>
<td>A73</td>
<td>Opamp1 non-inverting input to V_REF</td>
<td>CTBM_OA1_SW</td>
<td>OA1P_A73</td>
</tr>
<tr>
<td>A22</td>
<td>Opamp1 inverting input to Px.4</td>
<td>CTBM_OA1_SW</td>
<td>OA1M_A22</td>
</tr>
<tr>
<td>A82</td>
<td>Opamp1 inverting input to output</td>
<td>CTBM_OA1_SW</td>
<td>OA1M_A82</td>
</tr>
<tr>
<td>D52</td>
<td>Opamp1 output to sarbus0</td>
<td>CTBM_OA1_SW</td>
<td>OA1O_D52</td>
</tr>
<tr>
<td>D62</td>
<td>Opamp1 output to sarbus1</td>
<td>CTBM_OA1_SW</td>
<td>OA1O_D62</td>
</tr>
<tr>
<td>D82</td>
<td>Opamp1 - shorts 1X, 10X outputs</td>
<td>CTBM_OA1_SW</td>
<td>OA1O_D82</td>
</tr>
<tr>
<td>CIS</td>
<td>Opamp0 non-inverting input isolation (for C_HOLD)</td>
<td>CTBM_CTD_SW</td>
<td>CTDH_CIS</td>
</tr>
<tr>
<td>ILR</td>
<td>C_HOLD leakage reduction (drives far side of isolation switch CIS)</td>
<td>CTBM_CTD_SW</td>
<td>CTDH_ILR</td>
</tr>
<tr>
<td>CA0</td>
<td>C_HOLD to Opamp0 non-inverting input</td>
<td>CTBM_CTD_SW</td>
<td>CTDH_CA0</td>
</tr>
<tr>
<td>COS</td>
<td>CTDAC output to C_HOLD (degltitch capable)</td>
<td>CTBM_CTD_SW</td>
<td>CTDO_COS</td>
</tr>
<tr>
<td>CHD</td>
<td>C_HOLD disconnect</td>
<td>CTBM_CTD_SW</td>
<td>CTDH_CHD</td>
</tr>
<tr>
<td>C6H</td>
<td>CTDAC output to Px.6</td>
<td>CTBM_CTD_SW</td>
<td>CTDO_C6H</td>
</tr>
<tr>
<td>CRD</td>
<td>Opamp1 output to CTDAC Ref</td>
<td>CTBM_CTD_SW</td>
<td>CTD_DCRD</td>
</tr>
<tr>
<td>COR</td>
<td>CTDAC output to Opamp1 inverting input</td>
<td>CTBM_CTD_SW</td>
<td>CTD_S_COR</td>
</tr>
<tr>
<td>CRS</td>
<td>CTDAC Ref sense to Opamp1 inverting input</td>
<td>CTBM_CTD_SW</td>
<td>CTD_S_CRS</td>
</tr>
</tbody>
</table>

Note: GPIO switches are not covered in this table. For a detailed description of GPIO switches and AMUXBUS connections, see the I/O System chapter on page 164.

Switches D51/D52/D62 shown in Figure 36-1 can be hardware controlled by the SAR sequencer (SARSEQ) as well as DSI signals, in addition to being firmware controllable. For more details of the SAR sequencer, see the SAR ADC chapter on page 439.

The CTBm switches will also work in the Deep Sleep power mode. The firmware control will keep values from Active to...
Deep Sleep mode. The hardware control signals will be latched during Deep Sleep.

Using the switching matrix, the opamps in CTBm can be configured to have inputs from:
- Dedicated pins
- CTDAC
- AMUXBUS A/B

Similarly, the output of the opamps can be connected to:
- Dedicated pins
- SAR ADC input (sarbuss0 / sarbus1)
- AMUXBUS A/B

See the device datasheet for the location of dedicated CTBm pins. See the Continuous Time DAC chapter on page 430 for details of CTDAC-CTBm connections. For more details of AMUXBUS connections to other analog blocks in the PSoC 6 MCU, see Analog Routing chapter on page 463.

### 36.2.4 Sample and Hold

CTBm has a sample and hold (SH) at the CTBm amplifier input, connected to the CTDAC output. This sampling is controlled by firmware. Switches also exist to route the CTDAC output to a pin without buffering, and to drive a buffered reference voltage to the CTDAC through a CTBm amplifier. The Continuous Time DAC chapter on page 430 contains detailed explanation of CTBm and sample and hold operating together with the CTDAC.

### 36.2.5 Comparator Mode

Each opamp can be configured as a comparator by setting the respective OAx_COMP_EN bit in the CTBM_OA_REx_CTRL register. Note that enabling the comparator disables the compensation capacitors and shuts down the 1X and 10X output drivers. The comparator has the following features:
- Optional 10-mV input hysteresis
- Configurable power/speed
- Optional output synchronization
- Configurable edge detection (rising/falling/both/disable)

#### 36.2.5.1 Comparator Configuration

A hysteresis of 10 mV can be enabled in one direction (low to high). Input hysteresis can be enabled by setting OAx_HYST_EN bit in the CTBM_OA_RESx_CTRL register. The two comparators also have three power modes: low, medium, and high, controlled by OAx_PWR_MODE bitfield in the CTBM_OA_RESx_CTRL register. Power modes differ in response time and power consumption; power consumption is maximum in fast mode and minimum in ultra-low-power mode. Exact specifications for power consumption and response time are provided in the device datasheet.

The output state of Comparator0 and Comparator1 can be monitored by the firmware using OAx_COMP bits in the CTBM_COMP_STAT register.

Table 36-4 summarizes various bits used to configure the comparator mode in the CTBm.

<table>
<thead>
<tr>
<th>Register[Bit_Pos]</th>
<th>Bit_Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTBM_OA_RESx_CTRL[4]</td>
<td>OA_COMP_EN</td>
<td>Opamp comparator enable bit</td>
</tr>
<tr>
<td>CTBM_OA_RES_CTRL[5]</td>
<td>OA_HYST_EN</td>
<td>Opamp comparator hysteresis enable bit</td>
</tr>
<tr>
<td>CTBM_OA_RES_CTRL[6]</td>
<td>O_BYPASS_DSI_SYNC</td>
<td>Opamp bypass comparator output synchronization for DSI (trigger) output</td>
</tr>
<tr>
<td>CTBM_OA_RES_CTRL[7]</td>
<td>O_DSI_LEVEL</td>
<td>Opamp comparator DSI (trigger) output synchronization level</td>
</tr>
</tbody>
</table>

#### 36.2.5.2 Comparator Interrupt

The comparator output is connected to an edge detector block, which is used to detect the edge (disable/rising/falling/both) that generates interrupt. It can be configured using OAx_COMPINT bitfields in the CTBM_OA_RESx_CTRL register. Each interrupt has an interrupt mask bit in the CTBM_INTR_MASK register. By setting the interrupt mask low, the corresponding interrupt source is ignored. The CTBm comparator interrupt to the CPUSS will be raised if logic AND of the interrupt flags in INTR registers and the corresponding interrupt masks in the CTBM_INTR_MASK register is logic 1.
Writing a ‘1’ to the COMPx bits in the CTBM_INTR register clears the corresponding interrupt.

For firmware convenience, the logic AND of the interrupt flags and the interrupt masks is also made available in the CTBM_INTR_MASKED register.

For verification and debug purposes, a set bit is provided for each interrupt in the CTBM_INTR_SET register. This bit allows the firmware to raise the interrupt without a real comparator switch event.

**Note:** The Programmable Analog Subsystem (PASS) in the PSoC 6 MCU generates a combined interrupt to the CPUSS. To understand which block generated the interrupt, firmware must read the PASS_INTR_CAUSE register. For more details on the PSoC 6 MCU interrupt architecture, see the Interrupts chapter on page 47.

### 36.2.6 Deep Sleep Operation

CTBm opamps can operate in the Deep Sleep power mode with reduced GBW and output drive capability. The CTBm switches will also work in the Deep Sleep mode. The firmware control will keep values from Active to Deep Sleep mode. The hardware control signals will be latched during Deep Sleep.

The Deep Sleep operation can be enabled using the DEEPSLEEP_ON bit in the CTBM_CTB_CTRL register. Note that analog references required for CTBm must be enabled and configured for Deep Sleep operation using the PASS_AREF_CTRL register. See the Analog Reference Block chapter on page 416 for more details.

### 36.3 Register List

Table 36-5. Register Summary

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTBM_CTB_CTRL</td>
<td>Global CTBm enable and power control register</td>
</tr>
<tr>
<td>PASS_AREF_CTRL</td>
<td>Global AREF control for PASS register</td>
</tr>
<tr>
<td>CTBM_OA0_RES0_CTRL</td>
<td>Opamp0 control register</td>
</tr>
<tr>
<td>CTBM_OA0_RES1_CTRL</td>
<td>Opamp1 control register</td>
</tr>
<tr>
<td>CTBM_COMP_STAT</td>
<td>Comparator status register</td>
</tr>
<tr>
<td>PASS_INTR_CAUSE</td>
<td>Global interrupt cause register for PASS</td>
</tr>
<tr>
<td>CTBM_INTR</td>
<td>Interrupt request register</td>
</tr>
<tr>
<td>CTBM_INTR_SET</td>
<td>Interrupt request set register</td>
</tr>
<tr>
<td>CTBM_INTR_MASK</td>
<td>Interrupt request mask register</td>
</tr>
<tr>
<td>CTBM_INTR_MASKED</td>
<td>Interrupt request masked register</td>
</tr>
<tr>
<td>CTBM_OA0_SW</td>
<td>Opamp0 switch control register</td>
</tr>
<tr>
<td>CTBM_OA0_SW_CLEAR</td>
<td>Opamp0 switch control clear register</td>
</tr>
<tr>
<td>CTBM_OA1_SW</td>
<td>Opamp1 switch control register</td>
</tr>
<tr>
<td>CTBM_OA1_SW_CLEAR</td>
<td>Opamp1 switch control clear register</td>
</tr>
<tr>
<td>CTBM_CTD_SW</td>
<td>CTDAC connection switch control register</td>
</tr>
<tr>
<td>CTBM_CTD_SW_CLEAR</td>
<td>CTDAC connection switch control clear register</td>
</tr>
<tr>
<td>CTBM_CTB_SW_DS_CTRL</td>
<td>CTBm bus switch control register</td>
</tr>
<tr>
<td>CTBM_CTB_SW_SQ_CTRL</td>
<td>CTBm bus switch SAR sequencer control enable/disable register</td>
</tr>
<tr>
<td>CTBM_CTB_SW_STATUS</td>
<td>CTBm bus switch control status register</td>
</tr>
<tr>
<td>CTBM_OA0_OFFSET_TRIM</td>
<td>Opamp0 offset trim control register</td>
</tr>
<tr>
<td>CTBM_OA0_SLOPE_OFFSET_TRIM</td>
<td>Opamp0 offset slope trim control register</td>
</tr>
<tr>
<td>CTBM_OA0_COMP_TRIM</td>
<td>Opamp0 comparator trim control register</td>
</tr>
<tr>
<td>CTBM_OA1_OFFSET_TRIM</td>
<td>Opamp1 offset trim control register</td>
</tr>
<tr>
<td>CTBM_OA1_SLOPE_OFFSET_TRIM</td>
<td>Opamp1 offset slope trim control register</td>
</tr>
<tr>
<td>CTBM_OA1_COMP_TRIM</td>
<td>Opamp1 comparator trim control register</td>
</tr>
</tbody>
</table>
37. Continuous Time DAC

The PSoC 6 MCU analog subsystem supports a 12-bit continuous time digital-to-analog converter (CTDAC). The 12-bit DAC provides continuous time output without the need for an external sample and hold (S/H) circuit. The CTDAC block can be used in applications that require voltage references, bias, or analog waveform output. It consists of the following blocks:

- CTDAC core
- CTDAC control interface

The CTDAC core includes a combination of 8-bit R-2R ladder DAC and 4-bit thermometer decoded resistors to generate the 12-bit DAC output voltage from the reference. VDDA or any signal buffered through Opamp1 of the CTBm provides the reference voltage to the DAC. The core is closely integrated with the CTBm, which provides easy buffering of the DAC output voltage in addition to providing buffered input reference voltage and sample/hold feature for the DAC output.

The CTDAC control interface provides an option to control the DAC output through CPU and DMA. This includes a double-buffered DAC voltage control register, clock input for programmable update rate, interrupt on DAC buffer empty to CPU, and trigger to DMA.

37.1 Features

The CTDAC has the following features:

- 12-bit continuous time output – no external S/H required
- 2-µs settling time for a 25 pF load
- Support in Deep Sleep power mode
- Selectable voltage reference:
  - VDDA
  - Internal VREF buffered through Opamp1 of CTBm
  - External VREF buffered through Opamp1 of CTBm
- Selectable output paths:
  - Direct DAC output to a pin
  - Buffered DAC output through Opamp0 of CTBm
  - Sample and hold output path through Opamp0 or to a pin directly
- Selectable input modes:
  - Unsigned 12-bit mode
  - Virtual signed 12-bit mode
- Configurable update rate using clock and DSI strobe signal
- Double-buffered DAC voltage control register
- Interrupt and DMA trigger on DAC buffer empty
- Configurable as PGA along with Opamp1 of CTBm
37.2 Architecture

Figure 37-1. CTDAC Block Diagram

Figure 37-2 shows the internal architecture of the DAC along with the CTBm connections. CTDAC core, CTBm routes, and the CTDAC control interface are covered in detail in this section.

Figure 37-2. CTDAC with CTBm Registers

Switch types
- Large switch – Low resistance
- Small switch – High resistance
- Tiny switch – Very high resistance
- Very large switch – Very low resistance

CTBm switches to other peripherals (I/Os, SAR ADC, AMUX)
37.2.1 CTDAC Core

The CTDAC core includes the following components:
- R-2R architecture with switches
- Input reference selection
- Output path selection
- Flip-flops to register input from the control interface

Figure 37-3. CTDAC Core Architecture

37.2.1.1 CTDAC Architecture

Figure 37-3 shows the CTDAC core components. The CTDAC includes a binary coded R-2R structure for the lower eight bits (B[0:7]) and a thermometer decoded resistor structure for the upper four bits (S[1:15]). The lower eight bits [7:0] of the CTDAC_VAL register control the B[7:0] signals directly. The upper four bits [11:8] of the CTDAC_VAL register control the thermometer resistors selection signals S[15:1]. The signals S[15:1] are generated using a binary to thermometer decode logic, which means the number of 1s (from LSB) set in the signal S[15:1] depends on the upper storage logic.
Continuous Time DAC

37.2.1.2 Input Voltage Reference

The CTDAC can have one of the following sources as the input voltage reference:
- \( V_{DDA} \)
- Internal \( V_{REF} \)
- External voltage

Closing the CVD switch (CTDD_CVD bit [0] of CTDAC_SW register) selects \( V_{DDA} \) as the CTDAC voltage reference. Figure 37-4 shows the signal path. Note that CVD is a very low-resistance switch and provides good current drive capability for the direct CTDAC output (P9.6) from \( V_{DDA} \).

Figure 37-4. \( V_{DDA} \) Voltage Reference

Figure 37-5 shows the signal path to select the internal \( V_{REF} \) as the CTDAC reference. As seen, this signal path includes various switches from the CTBm along with Opamp1 (OA1). Internal reference \( (V_{REF}) \) is buffered through OA1 and then is routed through CRD switch in CTBm to the CTDAC reference. The internal reference can be used when the DAC output needs to be accurate and supply independent. Note that for the CTDAC to operate properly in this configuration, CTBm should be enabled and OA1 should be configured in voltage follower mode with all the switches configured properly.

Figure 37-5. Internal \( V_{REF} \) as Voltage Reference
Figure 37-6 shows the signal path to connect an external signal as CTDAC reference. The signal path appears similar to the internal reference signal path. Instead of routing the internal $V_{\text{REF}}$, the OA1 positive terminal connections can be used to route an external signal.

37.2.1.3 Output Paths

The CTDAC output can be routed in three different paths:

- Direct output path
- Buffered output path through Opamp0
- Sample and hold path using Opamp0 and $C_{\text{HOLD}}$ capacitor

Figure 37-7 shows the direct and buffered output path from the DAC. As seen, the direct path does not involve any switches from the CTBm and is completely controlled by the CTDAC switches. However, the direct path has a slower settling time for a given load (see the device datasheet for details). The buffered path on the other hand makes use of the CTBm Opamp0 as voltage buffer and routes the CTDAC output. This path provides a better settling time for the DAC output at the pin.
CTBm includes a $C_{\text{HOLD}}$ capacitor, which can be used to implement a Sample and Hold circuit for the CTDAC output. Figure 37-8 shows the Sample and Hold path for the CTDAC output. In this mode, the CHD switch is closed. The DAC output is sampled onto the $C_{\text{HOLD}}$ capacitor. When sampled, DAC can be powered off or disconnected to save power and the Opamp0, configured as buffer, holds the voltage at the output. This is useful when a low-power, occasional update voltage reference is required.

![Sample Mode using DAC](image)

![Hold Mode using DAC](image)

37.2.1.4 Other Configurations

The CTDAC with the Opamp1 can be used to implement a PGA (see Figure 37-10). In this configuration, the COR switch feeds back the Opamp1 output through the R-2R divider. The CTDAC VAL register controls the gain of the amplifier. The gain is given by $(4096/\text{CTDAC VAL})$. Note that this configuration should be used only for very low frequency signals and is not guaranteed to work for fast-switching signals. This is because of significant destabilizing capacitance introduced by the DAC in the amplifier feedback loop, which can result in oscillations.
37.2.2 CTDAC Control Interface

The CTDAC control interface provides a digital interface to control and use the CTDAC. It offers the following features:

- Support for unsigned and virtual-signed numbers
- Double buffered DAC data register
- Programmable update rate using clock and DSI
- CPU interrupts and DMA triggers on data register empty event

37.2.2.1 CTDAC Modes

The CTDAC supports two modes in which the DAC output value from the CTDAC_VAL register is interpreted. The content of the register can be either an unsigned or a virtual signed value. In the unsigned mode, the DAC output value is simply proportional to the register value; this means, 0x0 gives the lowest value and 0xFFF gives the maximum value. In the virtual signed mode, the MSb of the 12-bit value is inverted. This implies the lowest output value is at 0x800 (0x000 after MSb inversion). The output corresponding to 0x000 (translated to 0x800) is VDACREF/2. This value can be considered as analog ground (AGND).

The mode in which CTDAC operates is selected by the CTDAC_MODE bits [25:24] of the CTDAC_CTRL register. Setting the bits to 00b selects unsigned mode of operation. The other two combinations are reserved for future use.

37.2.2.2 Update Rate and Double Buffering

The CTDAC is capable of generating a fixed voltage or a waveform at the output. Generating a fixed voltage is simple. However, to generate a waveform, the DAC output should be updated at a desired sample rate. The CTDAC supports a clock input (CLK signal in Figure 37-2) for this purpose. The DAC output is refreshed on every rising edge of the clock.

In addition to the clock, the update can be further controlled by a DSI signal. When used, the DAC value is updated on the rising edge of the clock only after a valid DSI strobe signal is received. DSI_STROBE_EN bit [28] and DSI_STROBE_LEVEL bit [29] of the CTDAC_CTRL register configure how the DSI signal affects the DAC update rate. The DSI_STORBE_EN bit decides whether the DSI strobe control is enabled (DSI_STROBE_EN = 1). The DSI_STROBE_LEVEL bit decides whether to use DSI signal as a pulse-triggered or level-triggered signal. In pulse-triggered, the DAC value is updated on the next rising clock edge after a positive edge on the DSI signal is detected. In level-triggered, the DAC value is updated on the rising edge of every clock as long as the DSI signal is high.

When the CTDAC is used for a fixed output, the desired value can be written directly to the CTDAC_VAL register. However, this does not work in creating a waveform using a fixed sample rate because the writes from the DMA or CPU cannot be cycle (sample rate) accurate. The CTDAC control interface provides a double buffer (CTDAC_VAL_NXT register) to address the problem. The next sample value of the waveform is written to the CTDAC_VAL_NXT register ahead of time and the next rising edge of the clock transfers the CTDAC_VAL_NXT contents to the CTDAC_VAL register.

37.2.2.3 Interrupts and DMA Triggers

The CTDAC supports a generation of interrupts on the CTDAC_VAL_NXT register empty event (VDAC_EMPTY). This interrupt can be used by the CPU to transfer the next value to the CTDAC_VAL_NXT register. In addition to the interrupt, the same event can generate a DMA trigger for initiating a DMA transfer to the CTDAC_VAL_NXT register.
VDAC_EMPTY bit [0] of the CTDAC_INTR register provides the status of the CTDAC interrupt. VDAC_EMPTY_MASK bit [0] of the CTDAC_INTR_MASK register enables the interrupt to be serviced by CPU.

### 37.2.2.4 Other Control Configurations

The CTDAC_SW and CTDAC_SW_CLEAR registers are used to close or open the CVD and CO6 switches (Figure 37-2). The CTDAC_SW register is used to close the switches – CTDD_CVD bit [0] for CVD switch and CTDD_CO6 bit [8] for CO6 switch. Setting the bits closes the corresponding switch. To open the switch, the corresponding bits in the CTDAC_SW_CLEAR register should be set. Clearing the bit in the CTDAC_SW register does not have any effect. Controls for other switches shown in Figure 37-2 is present in the CTBm. Refer to the Continuous Time Block mini (CTBm) chapter on page 424 for details.

The CTDAC also provides an option to debounce or deglitch the output value every time it is updated. This prevents small glitches in the DAC output during an update to propagate to the pin or opamp input. The DEGLITCH_COS bit [9] in the CTDAC_CTRL register enables the deglitch functionality on the opamp input. When set, the COS switch in CTBm is forced open for (DEGLITCH_CNT+1) CLK_PERI clock cycles. DEGLITCH_CO6 bit [8] of the CTDAC_CTRL register does the same with the CO6 switch in CTDAC, which connects to the pin.

The output of the DAC can be enabled or disabled using the OUT_EN bit [22] of the CTDAC_CTRL register. If the bit is set, the output of the CTDAC is enabled. If the bit is cleared, output is disabled. The DISABLED_MODE bit [27] and CTDAC_RANGE bit [23] of the CTDAC_CTRL register decide the disabled output state – Tristate (DISABLED_MODE = 0), VSSA (DISABLED_MODE = 1, CTDAC_RANGE = 0), or VREF (DISABLED_MODE = 1, CTDAC_RANGE = 1).

The CTDAC supports two output ranges:
- VSSA to (VDACREF × 4095/4096)
- VDACREF/4096 to VDACREF

The two ranges are almost the same except that the second range is lifted by one LSb. The CTDAC_RANGE bit [23] of the CTDAC_CTRL register decides the range. Setting the bit provides one LSb lifted range.


### 37.2.3 Using CTDAC

Follow these steps to use the CTDAC:
1. Configure various switches in CTDAC and CTBm according to the input reference voltage and output path selection.
2. Configure deglitch, CTDAC mode, range, Deep Sleep operation capability, and DSI control in the CTDAC_CTRL register according to your requirements.
3. Enable VDAC_EMPTY interrupt if used.
4. Configure and enable DMA with VDAC_EMPTY as trigger and CTDAC_VAL_NXT register as destination (see the DMA Controller chapter on page 72), if used.
5. Configure and enable the clock for CTDAC (see the Clocking System chapter on page 146).
6. Configure and enable the DSI strobe signal, if used.
7. Enable the CTBm and opamps based on the configuration in step 1.
   a. Enable the CTBm if any of the switches from the CTBm is used in the input reference and output path.
   b. Enable Opamp1 if an internal reference is used.
   c. Enable and configure the Opamp1 positive input if an external reference is used.
   d. Enable Opamp0 if the DAC output is buffered.
8. Enable the CTDAC block by setting the ENABLED bit in the CTDAC_CTRL register.
9. Enable the DAC output by setting the OUT_EN bit in the CTDAC_CTRL register.
10. Update the CTDAC_VAL register for fixed output and the CTDAC_VAL_NXT register for clocked output.
11. Additional updates can happen in VDAC_EMPTY ISR or through DMA transfers.
12. The DAC output can be enabled/disabled at any time using the OUT_EN bit.
### Register List

Table 37-1. List of CTDAC Registers

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTDAC_CTRL</td>
<td>Global CTDAC control register</td>
</tr>
<tr>
<td>CTDAC_INTR</td>
<td>CTDAC interrupt request register</td>
</tr>
<tr>
<td>CTDAC_INTR_SET</td>
<td>CTDAC interrupt request set register</td>
</tr>
<tr>
<td>CTDAC_INTR_MASK</td>
<td>CTDAC interrupt request mask</td>
</tr>
<tr>
<td>CTDAC_INTR_MASKED</td>
<td>CTDAC interrupt request masked</td>
</tr>
<tr>
<td>CTDAC_CTDAC_SW</td>
<td>CTDAC switch control register</td>
</tr>
<tr>
<td>CTDAC_CTDAC_SW_CLEAR</td>
<td>CTDAC switch control clear register</td>
</tr>
<tr>
<td>CTDAC_CTDAC_VAL</td>
<td>Current DAC value register</td>
</tr>
<tr>
<td>CTDAC_CTDAC_VAL_NXT</td>
<td>Next DAC value (double buffering) register</td>
</tr>
<tr>
<td>CTDAC_TRIM</td>
<td>CTDAC trim register</td>
</tr>
</tbody>
</table>
38. SAR ADC

The PSoC 6 MCU has a successive approximation register analog-to-digital converter (SAR ADC). The SAR ADC is designed for applications that require moderate resolution and high data rate. It consists of the following blocks:

- SARMUX
- SAR ADC core
- SARREF
- SARSEQ

Figure 38-1 shows the simplified block diagram of PSoC 6 MCU SAR ADC. The SAR ADC core is a fast 12-bit ADC with sampling rate of 1 Msps. Preceding the SAR ADC is the SARMUX, which can route external pins and internal signals (AMUXBUS A/AMUXBUS B, CTBm, temperature sensor output) to the internal channels of SAR ADC. The sequencer controller (SARSEQ) is used to control SARMUX and SAR ADC to do an automatic scan on all enabled channels without CPU intervention. SARSEQ also performs pre-processing such as averaging and accumulating the output data.

The seventeenth channel is an injection channel that is used by firmware for infrequent and incidental sampling of pins and signals, for example, the internal temperature sensor.

The result from each channel is double-buffered and a complete scan may be configured to generate an interrupt at the end of the scan. Alternatively, the data can be routed to programmable digital blocks (UDBs) for further processing without CPU intervention. The sequencer may also be configured to flag overflow, collision, and saturation errors that can be configured to assert an interrupt.

For more flexibility, it is also possible to control most analog switches, including those in the SARMUX with the UDBs or firmware. This makes it possible to implement an alternative sequencer with the UDBs or firmware.

38.1 Features

- Maximum sample rate of 1 Msps
- Sixteen individually configurable channels and one injection channel
- Result may be left- or right-aligned
- Each channel has the following features:
  - Input from external pin (only for eight channels in single-ended mode and four channels in differential mode) or internal signals (AMUXBUS/CTBm/temperature sensor)
  - Each channel may choose one of the four programmable acquisition times to allow high-impedance signals to settle
  - Single-ended or differential measurement
  - Averaging and accumulation
  - Results are double-buffered
- Scan can be triggered by firmware, trigger from other peripherals, pin, or UDB
  - One-shot – periodic or continuous mode
- Hardware averaging support
  - First order accumulate
  - Supports 2 to 256 samples (powers of 2)
- Results can be represented in 16-bit sign extended values
- Selectable voltage references
- Internal $V_{DDA}$ and $V_{DDA}/2$ references
- Internal 1.2-V reference with buffer
- External reference

- Interrupt generation
  - Finished scan conversion
  - Saturation detect and over-range (configurable) detect for every channel
  - Scan results overflow
  - Collision detect

- Configurable injection channel
  - Triggered by firmware
  - Can be interleaved between two scan sequences (tailgating)
  - Selectable sample time, single-ended or differential, averaging

- Low-power modes
  - ADC core and reference voltage have dedicated low power modes

### 38.2 Architecture

![Block Diagram](image)

This section includes the following contents:
- Introduction of each block: SAR ADC core, SARMUX, SARREF, and SARSEQ
- SAR ADC system resource: Interrupt, low-power mode, and SAR ADC status
- System operation modes
  - Register mode
  - DSI mode
- Configuration examples

### 38.2.1 SAR ADC Core

The PSoC 6 MCU SAR ADC core is a 12-bit SAR ADC. The maximum sample rate for this ADC is 1 Msp. The SAR ADC core has the following features:
- Fully differential architecture; also supports single-ended mode
- 12-bit resolution
- Four programmable acquisition times
- Seven programmable power levels
- Supports single and continuous conversion mode
SAR_CTRL register contains the bitfields that control the operation of SAR ADC core. See the PSoC 63 with BLE Registers TRM for more details of this register.

38.2.1.1 Single-ended and Differential Modes

The PSoC 6 MCU SAR ADC can operate in single-ended and differential modes. Differential or single-ended mode can be configured using the DIFFERENTIAL_EN bitfield in the channel configuration register, SAR_CHAN_CONFIGx, where x is the channel number (0–15).

SAR ADC gives full range output (0 to 4095) for differential inputs in the range of –VREF to +VREF.

Note: The precise value of the input range in the differential mode is –VREF to (+VREF – (VREF/2047)). The positive input range is limited by the resolution of the ADC.

The single-ended mode options of negative input include VSSA, VREF, or an external input from P1, P3, P5, or P7 pins of SARMUX. See the device datasheet for the exact location of SARMUX pins. This mode is configured by the NEG_SEL bitfield in the global configuration register SAR_CTRL. When VMINUS is connected to these SARMUX pins, the single-ended mode is equivalent to differential mode. However, when the odd pin of each differential pair is connected to the common alternate ground, these conversions are 11-bit because measured signal value cannot go below ground.

To get a single-ended conversion with 12 bits, you must connect VREF to the negative input of the SAR ADC; then, the input range can be from 0 to 2 × VREF.

Note that temperature sensor can only be used in single-ended mode.

38.2.1.2 Input Range

All inputs should be in the range of VSSA to VDDA. Input voltage range is also limited by VREF. If voltage on negative input is Vn and the ADC reference is VREF, the range on the positive input is Vn ± VREF. This criterion applies for both single-ended and differential modes. In single-ended mode, Vn is connected to VSSA, VREF or an external input.

Note that Vn ± VREF should be in the range of VSSA to VDDA. For example, if negative input is connected to VSSA, the range on the positive input is 0 to VREF, not –VREF to VREF. This is because the signal cannot go below VSSA. Only half of the ADC range is usable because the positive input signal cannot swing below VSS, which effectively only generates an 11-bit result.

38.2.1.3 Result Data Format

Result data format is configurable from two aspects:

- Signed/unsigned
- Left/right alignment

When the result is considered signed, the most significant bit of the conversion is used for sign extension to 16 bits with MSb. For an unsigned conversion, the result is zero extended to 16-bits. The sample value can be either right-aligned or left-aligned within the 16 bits of the result register. By default, data is right-aligned in data[11:0], with sign extension to 16 bits, if required. Left-alignment will cause lower significant bits to be made zero.

Result data format can be controlled by DIFFERENTIAL_SIGNED, SINGLE_ENDED_SIGNED, and LEFT_ALIGN bitfields in the SAR_SAMPLE_CTRL register.

The result data format can be shown as follows.

<table>
<thead>
<tr>
<th>Alignment</th>
<th>Signed/Unsigned</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Right</td>
<td>Unsigned</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Right</td>
<td>Signed</td>
<td>11</td>
<td>11</td>
<td>11</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Left</td>
<td>–</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
</tbody>
</table>
38.2.1.4 Negative Input Selection

The negative input connection choice affects the voltage range and effective resolution (Table 38-2). In single-ended mode, negative input of the SAR ADC can be connected to VSSA, VREF, or P1, P3, P5, or P7 pins of SARMUX.

Table 38-2. Negative Input Selection Comparison

<table>
<thead>
<tr>
<th>Single-ended/Differential</th>
<th>Signed/Unsigned</th>
<th>SARMUX VMINUS</th>
<th>SARMUX VPLUS Range</th>
<th>Result Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single-ended</td>
<td>N/A</td>
<td>VSSA</td>
<td>+VREF</td>
<td>0x7FF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>VSSA = 0</td>
<td>0x000</td>
</tr>
<tr>
<td>Single-ended</td>
<td>Unsigned</td>
<td>VREF</td>
<td>+2 × VREF</td>
<td>0xFF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>VREF</td>
<td>0x800</td>
</tr>
<tr>
<td></td>
<td>Signed</td>
<td>VREF</td>
<td>+2 × VREF</td>
<td>0x7FF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>VREF</td>
<td>0x000</td>
</tr>
<tr>
<td></td>
<td>Unsigned</td>
<td>Vx</td>
<td>Vx + VREF</td>
<td>0xFFF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Vx</td>
<td>0x800</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Vx – VREF</td>
<td>0</td>
</tr>
<tr>
<td>Single-ended</td>
<td>Signed</td>
<td>Vx</td>
<td>Vx + VREF</td>
<td>0x7FF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Vx</td>
<td>0x000</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Vx – VREF</td>
<td>0x800</td>
</tr>
<tr>
<td>Differential</td>
<td>Unsigned</td>
<td>Vx</td>
<td>Vx + VREF</td>
<td>0xFFF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Vx</td>
<td>0x800</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Vx – VREF</td>
<td>0</td>
</tr>
<tr>
<td>Differential</td>
<td>Signed</td>
<td>Vx</td>
<td>Vx + VREF</td>
<td>0x7FF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Vx</td>
<td>0x000</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Vx – VREF</td>
<td>0x800</td>
</tr>
</tbody>
</table>

a. For single-ended mode with VMINUS connected to VSSA, conversions are effectively 11-bit because voltages cannot swing below VSSA on any PSoC 6 MCU pin. Because of this, the global configuration bit SINGLE_ENDED_SIGNED (SAR_SAMPLE_CTRL[2]) will be ignored and the result is always (0x000-0x7FF).

b. Vx is the differential input common mode voltage.

Note that single-ended conversions with VMINUS connected to the pins with SARMUX connectivity are electrically equivalent to differential mode. However, when the odd pin of each differential pair is connected to the common alternate ground, these conversions are 11-bit because measured signal value (SARMUX.vplus) cannot go below ground.

38.2.1.5 Acquisition Time

Acquisition time is the time taken by sample and hold (S/H) circuit inside SAR ADC to settle. After acquisition time, the input signal source is disconnected from the SARADC core, and the output of the S/H circuit will be used for conversion. Each channel can select one from four acquisition time options, from 4 to 1023 SAR clock cycles defined in global configuration registers SAR_SAMPLE_TIME01 and SAR_SAMPLE_TIME23. These two registers contain four programmable sample times ST0, ST1, ST2, and ST3. One of these four sample times can be selected for a particular channel by configuring the SAMPLE_TIME_SEL bitfield in the respective SAR_CHAN_CONFIGx register.
The acquisition time should be sufficient to charge the internal hold capacitor of the ADC through the resistance of the routing path, as shown in Figure 38-2. The recommended value of acquisition time is:

\[ t_{ACQ} \geq 9 \times (R_{SRC} + R_{SW2} + R_{SW1}) \times C_{SHOLD} \]

Where:

- \( C_{SHOLD} \approx 10 \text{ pF} \)
- \( R_{SW2} + R_{SW1} = \sim 500 \text{ to } 1000 \Omega \), depending on the routing path (See Analog Routing on page 445 for details).
- \( R_{SRC} \) = series resistance of the signal source

### 38.2.1.6 SAR ADC Clock

SAR ADC clock frequency must be between 1.8 MHz and 36 MHz, which comes from the peripheral clock (CLK_PERI) in the system resources subsystem (SRSS). See the Clocking System chapter on page 146 to know how to configure the peripheral clock.

### 38.2.1.7 SAR ADC Timing

As Figure 38-3 shows, an ADC conversion with the minimum acquisition time of four clocks requires 18 clocks to complete. Note that the minimum acquisition time of four clock cycles at 36 MHz is based on the minimum acquisition time supported by the SAR block (\( R_{SW1} \) and \( C_{SHOLD} \) in Figure 38-2 on page 443), which is 97 ns.

Total clock cycles for valid output are equal to:

- 4 clock cycles for sampling input (minimum acquisition time set by SAR_SAMPLE_TIME01 or SAR_SAMPLE_TIME23)
- + 12 clock cycle conversions (with 12-bit resolution)
- + 1 clock for EOF output signal
- + 1 clock for continuous conversion mode and Auto-zero
- =18 clock cycles.
Figure 38-3. SAR ADC Timing

SARADC CLK

trigger

SOC

sample

18 clock cycles

State

EOC

Next

Data_out

Data

Data
38.2.2 SARMUX

SARMUX is an analog dedicated programmable multiplexer. The main features of SARMUX are:

- Controlled by sequencer controller block (SARSEQ), firmware, or UDBs
- Internal temperature sensor
- Multiple inputs:
  - Analog signals from pins (port 2)
  - Temperature sensor output (settling time for the temperature sensor is about 1 µs)
  - CTBm output via sarbus0/1
  - AMUXBUS A/AMUXBUS B

38.2.2.1 Analog Routing

SARMUX has many switches that may be controlled by SARSEQ block (sequencer controller), firmware, or the DSI. Different control methods have different control capability on the switches. Figure 38-4 shows the SARMUX switches. See the device datasheet for the exact location of SARMUX pins.

Figure 38-4. SARMUX Switches and Control Capability

**Sequencer control:** In the sequencer control mode, the SARMUX switches are controlled by the SARSEQ block. After configuring each channel’s analog routing, it enables multi-channel, automatic scan in a round-robin fashion, without CPU intervention. Not every switch in analog routing can be controlled by the sequencer, as Figure 38-4 shows. SAR_MUX Switch SQ_CTRL register can be used to enable/disable SARSEQ control of SARMUX switches. See section 19.3.4 SARSEQ for more details of sequencer control.

**Firmware control:** In firmware control, registers are written by the firmware to connect required signals to VPLUS/VMINUS terminals before starting the scan. Firmware can control every switch in SARMUX, as Figure 38-4 shows. However, firmware control needs continuous CPU intervention for multi-channel scans. The SAR_MUX SWITCH0 register can be used by the
firmware to control SARMUX switches. Note that additional register writes may be required to connect blocks outside the SARMUX. See the Analog Routing chapter on page 463 for more details.

**DSI control:** Switches are controlled by DSI signals from the UDB, which can act as a secondary sequencer with a customized logic design. DSI can control most SARMUX switches. The SAR_MUX_SWITCH_DCTRL register can be used to enable or disable DSI control of SARMUX switches.

### 38.2.2.2 Analog Interconnection

The PSoC 6 MCU analog interconnection is very flexible. SAR ADC can be connected to multiple inputs via SARMUX, including both external pins and internal signals. For example, it can connect to a neighboring block such as CTBm. It can also connect to non-SARMUX ports through AMUXBUS A/AMUXBUS B, at the expense of scanning performance (more parasitic coupling, longer RC time to settle).

This section discusses several routing cases to provide a better understanding of analog interconnections. See the Analog Routing chapter on page 463 for details of all available analog routing options in PSoC 6 MCUs.

**Input from SARMUX Port**

Figure 38-5 shows how two GPIOs that support SARMUX are connected to SAR ADC as a differential pair ($V_{PLUS}/V_{MINUS}$) via switches. In this mode, sequencer control, firmware control, and DSI control are possible. In addition to SARMUX switch configuration, the GPIOs must be configured properly to connect to SARMUX. See the I/O System chapter on page 164 for more details.
Figure 38-5. Input from External Pins

Legend
- Unused or Open Switches
- Used SARMUX Switches
- Unused Pin
- Used Pin
- Unused Analog Route
- Used Analog Route

Note: Pins and blocks shown in Figure 38-5 may not be available in all PSoC 6 MCUs. See the specific device datasheet for more details.
Input from Other Pins through AMUXBUS

Figure 38-6 shows how two pins that do not support SARMUX connectivity are connected to SAR ADC as a differential pair. Additional switches are required to connect these two pins to AMUXBUS A and AMUXBUS B, and then connect AMUXBUS A and AMUXBUS B to the SAR ADC. See the I/O System chapter on page 164 and Analog Routing chapter on page 463 for details of AMUXBUS connections.

The additional switches reduce the scanning performance (more parasitic coupling, longer RC time to settle). This is not recommended for external signals; the dedicated SARMUX port should be used, if possible. Moreover, sequencer control may not be available if more than one AMUXBUS channel is required.

AMUXBUS A and B can be also used to connect other analog peripherals in the PSoC 6 MCU to the SAR ADC. See the Analog Routing chapter on page 463 for more details.
Input from CTBm Output via sarbus

SAR ADC can be connected to CTBm output via sarbus 0/1. Figure 38-7 shows how to connect an opamp (configured as a follower) output to a single-ended SAR ADC. Figure 38-8 shows how to connect two opamp outputs to SAR ADC as a differential pair. Note that external components of the opamp circuit are not shown (for example, resistors used to create differential amplifier front end). Because additional switches are used for signal routing. However, the on-chip opamps add value for many applications. In this mode, sequencer control, firmware control, and DSI control are possible. See the Continuous Time Block mini (CTBm) chapter on page 424 for more details of CTBm opamps, routing, and switches.
Figure 38-8. Inputs from CTBm Output via sarbus0 and sarbus1

Legend
- Unused or Open Switches
- Used SARMUX Switches
- Used CTBm Switches
- Unused Pin
- Used Pin
- Unused Analog Route
- Used Analog Route
Input from Temperature Sensor

On-chip temperature sensor can be used to measure the device temperature. See the Temperature Sensor chapter on page 460 for more details of this block. For temperature sensors, differential conversions are not available (conversion result is undefined), thus always use it in single-ended mode. As Figure 38-9 shows, temperature sensor can be routed to positive input of SAR ADC using a switch that can be controlled by the sequencer, firmware, or DSI. Setting the MUX_FW_TEMP_VPLUS bit in the SAR_MUX_SWITCH0 register can enable the temperature sensor and connect its output to VPLUS of SAR ADC; clearing this bit will disable temperature sensor by cutting off its bias current.

Figure 38-9. Inputs from Temperature Sensor
38.2.3 SARREF

The main features of the SAR reference block (SARREF) are:
- Reference options: \( V_{DDA}, V_{DDA}/2, 1.2\)-V bandgap, and external reference
- Reference buffer and bypass capacitor to enhance internal reference drive capability

38.2.3.1 Reference Options

SARREF generates \( V_{DDA} \) and \( V_{DDA}/2 \) voltages. In addition, it can take in a 1.2-V bandgap reference from AREF (see the Analog Reference Block chapter on page 416 for details) or an external \( V_{REF} \) connected to a dedicated pin (see the device datasheet for details). External \( V_{REF} \) value should be between 1-V and \( V_{DDA} \).

The external \( V_{REF} \) pin is also used to bypass the internal references. The \( V_{REF\_SEL} \) bitfield in the SAR_CTRL register can be used to select which one of these references is connected to the SAR ADC.

38.2.3.2 Reference Buffer and Bypass Capacitors

The internal references, 1.2 V from bandgap and \( V_{DDA}/2 \), are buffered with the reference buffer. This reference may be routed to the external \( V_{REF} \) pin where a capacitor can be used to filter noise that may exist on the reference.

The \( V_{REF\_BYP\_CAP\_EN} \) bitfield in the SAR_CTRL register can be used to enable the bypass capacitor. \( \text{REFBUF\_EN} \) and \( PWR\_CTRL\_VREF \) bitfields in the same register can be used to enable the buffer, and select one of seven available power levels of the reference buffer respectively.

SAR performance varies with the mode of reference and the \( V_{DDA} \) supply.

Table 38-3. Reference Modes

<table>
<thead>
<tr>
<th>Reference Mode</th>
<th>( V_{DDA} )</th>
<th>Maximum SAR ADC Frequency</th>
<th>Maximum Sample Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>External Reference</td>
<td>1.7 V–3.6 V</td>
<td>18 MHz</td>
<td>1 Msps</td>
</tr>
<tr>
<td></td>
<td>2.7 V–3.6 V</td>
<td>36 MHz</td>
<td>1 Msps</td>
</tr>
<tr>
<td>Internal reference without bypass capacitor</td>
<td>1.7 V–3.6 V</td>
<td>1.8 MHz</td>
<td>100 ksps</td>
</tr>
<tr>
<td>Internal reference with bypass capacitor</td>
<td>1.7 V–3.6 V</td>
<td>18 MHz</td>
<td>1 Msps</td>
</tr>
<tr>
<td></td>
<td>2.7 V–3.6 V</td>
<td>36 MHz</td>
<td>1 Msps</td>
</tr>
<tr>
<td>( V_{DDA} ) as reference</td>
<td>1.7 V–2.7 V</td>
<td>18 MHz</td>
<td>1 Msps</td>
</tr>
<tr>
<td></td>
<td>2.7 V–3.6 V</td>
<td>36 MHz</td>
<td>1 Msps</td>
</tr>
</tbody>
</table>

Reference buffer startup time varies with different bypass capacitor size. Table 38-4 lists two common values for the bypass capacitor and its startup time specification. If reference selection is changed between scans or when scanning after device low-power modes in which the ADC is not active (see the Device Power Modes chapter on page 128), make sure the reference buffer is settled before the SAR ADC starts sampling.

Table 38-4. Bypass Capacitor Values vs Startup Time

<table>
<thead>
<tr>
<th>Capacitor Value</th>
<th>Startup Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Internal reference with bypass capacitor (50 nF)</td>
<td>120 ( \mu )s</td>
</tr>
<tr>
<td>Internal reference with bypass capacitor (100 nF)</td>
<td>210 ( \mu )s</td>
</tr>
<tr>
<td>Internal reference without bypass capacitor</td>
<td>10 ( \mu )s</td>
</tr>
</tbody>
</table>

38.2.3.3 Input Range versus Reference

All inputs should be between \( V_{SSA} \) and \( V_{DDA} \). The ADCs input range is limited by \( V_{REF} \) selection. If negative input is \( V_n \) and the ADC reference is \( V_{REF} \), the range on the positive input is \( V_n \pm V_{REF} \). This criteria applies for both single-ended and differential modes as long as both negative and positive inputs stay within \( V_{SSA} \) to \( V_{DDA} \).
38.2.4 SARSEQ

SARSEQ is a dedicated control block that automatically sequences the input mux from one channel to the next while placing the result in an array of registers, one per channel. SARSEQ has the following functions:

- Controls SARMUX analog routing automatically without CPU intervention
- Controls SAR ADC core such as selecting acquisition times
- Receives data from SAR ADC and pre-process (average, range detect)
- Results are double-buffered; therefore, the CPU can safely read the results of the last scan while the next scan is in progress.

The features of SARSEQ are:

- Sixteen channels can be individually enabled as an automatic scan without CPU intervention
- A seventeenth channel (injection channel) for infrequent signal to insert in an automatic scan
- Each channel has the following features:
  - Single-ended or differential mode
  - Input from external pin or internal signal (AMUXBUS/CTBm/temperature sensor)
  - Four programmable acquisition times
  - Result averaging and accumulation
  - Scan triggering
  - One-shot, periodic, or continuous mode
  - Triggered by any digital signal or input from GPIO pin
  - Triggered by internal UDB of fixed-function block
  - Software triggered
  - Hardware averaging support
  - First order accumulate
  - From 2 to 256 samples averaging (powers of 2)
  - Results in 16-bit representation
  - Double buffering of output data
  - Left or right adjusted results
  - Results in working register and result register
  - Interrupt generation
    - Finished scan conversion
    - Channel saturation detection
    - Range (configurable) detection
    - Scan results overflow
    - Collision detect
  - Configurable injection channel
  - Triggered by firmware
  - Can be interleaved between two scan sequences (tailgating)

Figure 38-10. SARSEQ Block Diagram
38.2.4.1 Channel Configuration

The SAR_CHAN_CONFIGx register contains the following bitfields, which control the behavior of respective channels during a SARSEQ scan:

- **POS_PORT_ADDR** and **POS_PIN_ADDR** select the connection to VPLUS terminal of the ADC
- **NEG_ADDR_EN**, **NEG_PORT_ADDR**, and **NEG_PIN_ADDR** select the connection to VMINUS terminal of the ADC
- **SAMPLE_TIME_SEL** selects the acquisition time for the channel
- **AVG_EN** enables the hardware averaging feature
- **DIFFERENTIAL_EN** selects single-ended/differential mode

SAR_CHAN_EN contains the enable bits that can be used to include or exclude a channel for the next SARSEQ scan.

38.2.4.2 Averaging

The SARSEQ block has a 20-bit accumulator and shift register to implement averaging. Averaging is performed after sign extension. The SAR_SAMPLE_CTRL register controls the global averaging settings.

Each channel configuration register (SAR_CHAN_CONFIG) has an enable bit (AVG_EN) to enable averaging.

The AVG_CNT bitfield in the SAR_SAMPLE_CTRL register specifies the number of accumulated samples (N) according to the formula:

\[ N = 2^{(AVG\_CNT+1)} \]  
N range = [2..256]

For example, if AVG_CNT = 3, then N = 16.

Because the conversion result is 12-bit and the maximum value of N is 256 (left shift 8 bits), the 20-bit accumulator will never overflow.

The AVG_SHIFT bitfield in the SAR_SAMPLE_CTRL register is used to shift the accumulated result to get the averaged value. If this bit is set, the SAR sequencer performs sign extension and then accumulation. The accumulated result is then shifted right AVG_CNT + 1 bits to get the averaged result.

The AVG_MODE bitfield in the SAR_SAMPLE_CTRL can be used to select between accumulate-and-dump and interleaved averaging modes. If a channel is configured for accumulate-and-dump averaging, the SARSEQ will take N consecutive samples of the specified channel before moving to the next channel. In the interleaved mode, one sample is taken per channel and averaged over several scans.

38.2.4.3 Range Detection

The SARSEQ supports range detection to allow automatic detection of result values compared to two programmable thresholds without CPU involvement. Range detection is defined by the SAR_RANGE_THRES register. The RANGE_LOW field in the SAR_RANGE_THRES register defines the lower threshold and RANGE_HIGH field defines the upper threshold of the range.

The RANGE_COND bitfield in the SAR_RANGE_COND register define the condition that triggers a channel maskable range detect interrupt (RANGE_INTR). The following conditions can be selected:

0: result < RANGE_LOW (below the range)

1: RANGE_LOW \leq \text{result} < RANGE_HIGH (inside the range)

2: RANGE_HIGH \leq \text{result} (above the range)

3: result < RANGE_LOW || RANGE_HIGH \leq \text{result} (outside range)

See Range Detection Interrupts on page 457 for details.

38.2.4.4 Double Buffer

Double buffering is used so that firmware can read the results of a complete scan while the next scan is in progress. The SAR ADC results are written to a set of working registers until the scan is complete, at which time the data is copied to a second set of registers where the data can be read by your application. This action allows sufficient time for the firmware to read the previous scan before the present scan is completed. All input channels are double buffered with 16 registers, except the injection channel. The injection channel is not required to be doubled buffered because it is not normally part of a normal channel scan.

SAR_CHAN_WORKx registers contain the working data and SAR_CHAN_RESULTx contain the buffered results of the channels. The SAR_CHAN_WORK_UPDATED and SAR_CHAN_RESULT_UPDATED registers can be used to track if the working data and the result value of a channel is updated.

38.2.4.5 Injection Channel

The injection channel is similar to the other channels, with the exception that it is not part of a regular scan. The injection channel is used for incidental or rare conversions; for example, sampling the temperature sensor every two seconds. Note that if SAR is operating in continuous mode, enabling the injection channel will change the sample rate.

The injection channel can be controlled only by the firmware with a firmware trigger (one-shot). This means the injection channel does not support continuous or DSI trigger. Because the only trigger is one-shot, there is no need for double buffering or an overflow interrupt.
The conversions for the injection channel can be configured in the same way as the regular channels by setting SAR_INJ_CHAN_CONFIG register, it supports:

- Pin or signal selection
- Single-ended or differential selection
- Sample time select from one of the four globally specified sample times
- Averaging select

It supports the same interrupts as the regular channel except the overflow interrupt.

- Maskable end-of-conversion interrupt INJ_EOC_INTR
- Maskable range detect interrupt INJ_RANGE_INTR
- Maskable saturation detect interrupt INJ_SATURATE_INTR
- Maskable collision interrupt INJ_COLLISION_INTR

SAR_INTR, SAR_INTR_MASK, SAR_INTR_MASKED, and SAR_INTR_SET are the corresponding registers.

**Tailgating**

The injection channel conversion can be triggered by setting the start or enable the INJ_START_EN bitfield in the SAR_INJ_CHAN_CONFIG register. Select tailgating by setting INJ_TAILGATING=1. The injection channel will be scanned at the end of the ongoing scan of regular channels without any collision. However, if there is no ongoing scan or the SAR ADC is idle, and tailgating is selected, INJ_START_EN will enable the injection channel to be scanned at the end of the next scan of regular channels.

If tailgating is not selected, setting the INJ_START_EN bit immediately starts the conversion of the injection channel provided there is no ongoing scan or SAR ADC is idle. If a scan of the regular channels is ongoing, then the injection channel will be scanned at the end of the ongoing scan, but it will cause a collision and generate a collision interrupt (INJ_COLLISION_INTR). Another potential problem without tailgating is that it can cause the next scan of the regular channels to collide with the injection channel conversion (FW/DSI_COLLISION_INTR is raised). As a result, the next scan of regular channels is postponed until the injection scan is finished, thus causing jitter on a regular scan. Note that continuous trigger and DSI trigger level mode will never trigger a collision interrupt.

Figure 38-11. Injection Channel Flow Chart

\[ ^\text{1 scan here means scan of ALL the regular channels} \]
The disadvantage of tailgating is that it may be a long time before the next trigger occurs. If there is no risk of colliding or causing jitter on the regular channels, the injection channel can be used safely without tailgating.

After completing the conversion for the injection channel, the end-of-conversion interrupt (INJ_EOC_INTR) is set and the INJ_START_EN bit is cleared. The conversion data of the injection is put in the SAR_INJ_RESULT register. Similar to the SAR_CHAN_RESULT, the registers contain mirror bits for “valid” (=INJ_EOC_INTR), range detect, saturation detect interrupt, and a mirror bit of the collision interrupt (INJ_COLLISION_INTR).

Figure 38-12 is an example of when injection channel is enabled during a continuous scan (channel 1, 3, 5, and 7 are enabled), and tailgating is enabled. Note that the INJ_START_EN bit is immediately cleared when the SAR is disabled (but only if it was enabled before).

**38.2.5 SAR Interrupts**

SAR ADC can generate interrupts on these events:
- **End of Scan** – When scanning is complete for all the enabled channels.
- **Overflow** – When the result register is updated before the previous result is read.
- **Collision** – When a new trigger is received while the SAR ADC is still processing the previous trigger.
- **Injection End of Conversion** – When the injection channel is converted.
- **Range Detection** – When the channel result meets the threshold value.
- **Saturation Detection** – When the channel result is equal to the minimum or maximum value.

This section describes each interrupt in detail. These interrupts have an interrupt mask in the SAR_INTR_MASK register. By making the interrupt mask low, the corresponding interrupt source is ignored. The SAR interrupt is generated if the interrupt mask bit is high and the corresponding interrupt source is pending.

When servicing an interrupt, the interrupt service routine (ISR) can clear the interrupt source by writing a ‘1’ to the corresponding interrupt bit in the SAR_RANGE_INTR register, after reading the data.

The SAR_INTR_MASKED register is the logical AND between the interrupts sources and the interrupt mask. This register provides a convenient way for the firmware to determine the source of the interrupt.

For verification and debug purposes, a set bit (such as EOS_SET in the SAR_INTR_SET register) is used to trigger each interrupt. This action allows the firmware to generate an interrupt without the actual event occurring.

**38.2.5.1 End-of-Scan Interrupt (EOS_INTR)**

After completing a scan, the end-of-scan interrupt (EOS_INTR) is raised. Firmware should clear this interrupt after picking up the data from the RESULT registers.

Optionally, the EOS_INTR can also be sent out on the DSI bus by setting the EOS_DSI_OUT_EN bit in the SAR_SAMPLE_CTRL register. The EOS_INTR signal is maintained on the DSI bus for two system clock cycles. These cycles coincide with the data_valid signal for the last channel of the scan (if selected).

EOS_INTR can be masked by making the EOS_MASK bit 0 in the SAR_INTR_MASK register. EOS_MASKED bit of the SAR_INTR_MASKED register is the logic AND of the interrupt flags and the interrupt masks, which are for firmware convenience. Writing a ‘1’ to EOS_SET bit in SAR_INTR_SET register can set the EOS_INTR, which is intended for debug and verification.

**38.2.5.2 Overflow Interrupt**

If a new scan completes and the hardware tries to set the EOS_INTR and EOS_INTR is still high (firmware does not clear it fast enough), then an overflow interrupt (OVERFLOW_INTR) is generated by the hardware. This usually means that the firmware is unable to read the previous results before the current scan completes. In this case, the old data is overwritten.

OVERFLOW_INTR can be masked by making the OVERFLOW_MASK bit 0 in the SAR_INTR_MASK register. OVERFLOW_MASKED bit of the SAR_INTR_MASKED register is the logic AND of the interrupt flags and the interrupt masks, which are for firmware convenience. Writing a ‘1’ to the OVERFLOW_SET bit in SAR_INTR_SET register can set OVERFLOW_INTR, which is intended for debug and verification.
38.2.5.3 Collision Interrupt

It is possible that a new trigger is generated while the SARSEQ is still busy with the scan started by the previous trigger. Therefore, the scan for the new trigger is delayed until after the ongoing scan is completed. It is important to notify the firmware that the new sample is invalid. This is done through the collision interrupt, which is raised any time a new trigger, other than the continuous trigger, is received.

There are three collision interrupts: for the firmware trigger (FW_COLLISION_INTR), for the DSI trigger (DSI_COLLISION_INTR), and for the injection channel (INJ_COLLISION_INTR). These interrupts allow the firmware to identify which trigger collided with an ongoing scan.

When the DSI trigger is used in level mode, the DSI_COLLISION_INTR will never be set.

The three collision interrupts can be masked by making the corresponding bit ‘0’ in the SAR_INTR_MASK register. The corresponding bit in the SAR_INTR_MASKED register is the logic AND of the interrupt flags and the interrupt masks. Writing a ‘1’ to the corresponding bit in the SAR_INTR_SET register can set the collision interrupt, which is intended for debug and verification.

38.2.5.4 Injection End-of-Conversion Interrupt (INJ_EOC_INTR)

After completing a conversion for the injection channel, the injection end-of-conversion interrupt is raised (INJ_EOC_INTR). The firmware clears this interrupt after picking up the data from the INJ_RESULT register.

Note that if the injection channel is tailgating a scan, the EOS_INTR is raised in parallel to starting the injection channel conversion. The injection channel is not considered part of the scan.

INJ_EOC_INTR can be masked by making the INJ_EOC_MASK bit ‘0’ in the SAR_INTR_MASK register. The INJ_EOC_MASKED bit of SAR_INTR_MASKED register is the logic AND of the interrupt flags and the interrupt masks. Writing a ‘1’ to the INJ_EOC_SET bit in SAR_INTR_SET register can set INJ_EOC_INTR, which is intended for debug and verification.

38.2.5.5 Range Detection Interrupts

Range detection interrupt flag can be set after averaging, alignment, and sign extension (if applicable). This means it is not required to wait for the entire scan to complete to determine whether a channel conversion is over-range. The threshold values need to have the same data format as the result data.

Range detection interrupt for a specified channel can be masked by setting the SAR_RANGE_INTR_MASK register specified bit to ‘0’. Register SAR_RANGE_INTR_MASKED reflects a bitwise AND between the interrupt request and mask registers. If the value is not zero, then the SAR interrupt signal to the NVIC is high.

SAR_RANGE_INTR_SET can be used for debug/verification. Write a ‘1’ to set the corresponding bit in the interrupt request register; when read, this register reflects the interrupt request register.

There is a range detect interrupt for each channel (RANGE_INTR and INJ_RANGE_INTR).

38.2.5.6 Saturate Detection Interrupts

The saturation detection is always applied to every conversion. This feature detects if a sample value is equal to the minimum or maximum value and sets a maskable interrupt flag for the corresponding channel. This action allows the firmware to take action, such as discarding the result, when the SAR ADC saturates. The sample value is tested right after conversion, before averaging. This means that the interrupt is set while the averaged result in the data register is not equal to the minimum or maximum.

Saturation interrupt flag is set immediately to enable a fast response to saturation, before the full scan and averaging. Saturation detection interrupt for specified channel can be masked by setting the SAR_SATURATE_INTR_MASK register specified bit to ‘0’. SAR_SATURATE_INTR_MASK register reflects a bit-wise AND between the interrupt request and mask registers. If the value is not zero, then the SAR interrupt signal to the NVIC is high.

SAR_SARTURATE_INTR_SET can be used for debug/verification. Write a ‘1’ to set the corresponding bit in the interrupt request register; when read, this register reflects the interrupt request register.

38.2.5.7 Interrupt Cause Overview

INTR_CAUSE register contains an overview of all the pending SAR interrupts. It allows the ISR to determine the cause of the interrupt. The register consists of a mirror copy of SAR_INTR_MASKED. In addition, it has two bits that aggregate the range and saturate detection interrupts of all channels. It includes a logical OR of all the bits in RANGE_INTR_MASKED and SATURATE_INTR_MASKED registers (does not include INJ_RANGE_INTR and INJ_SATURATE_INTR).

38.2.6 Trigger

A scan can be triggered in the following ways:

- A firmware or one-shot trigger is generated when the firmware writes to the FW_TRIGGER bit of the SAR_START_CTRL register. After the scan is completed, the SARSEQ clears the FW_TRIGGER bit and goes back to idle mode waiting for the next trigger. The FW_TRIGGER bit is cleared immediately after the SAR is disabled.
- A periodic trigger comes in through the DSI connections (dsi_trigger).
- Trigger from other peripherals through the trigger multiplexer (see the Trigger Multiplexer Block chapter on page 197 for more details).
- A continuous trigger is activated by setting the CONTINUOUS bit in SAR_SAMPLE_CTRL register. In this mode, after completing a scan the SARSEQ starts the next scan immediately; therefore, the SARSEQ is always BUSY. As a result, all other triggers are essentially ignored. Note that FW_TRIGGER will still get cleared by hardware on the next completion.

These triggers are mutually exclusive. If a DSI trigger coincides with a firmware trigger, the DSI trigger is handled first and a separate scan is done for the firmware trigger (and a collision interrupt is set). When a DSI trigger coincides with a continuous trigger, both triggers are effectively handled at the same time (a collision interrupt may be set for the DSI trigger).

For firmware continuous trigger, it takes only one SAR ADC clock cycle before the sequencer tells the SAR ADC to start sampling (provided the sequencer is idle). For the DSI trigger, it depends on the trigger configuration setting.

38.2.7 SAR ADC Status

The current SAR status can be observed through the BUSY and CUR_CHAN fields in the SAR_STATUS register. The BUSY bit is high whenever the SAR is busy sampling or converting a channel; the CUR_CHAN bits indicate the number of the current channel being sampled (channel 16 indicates the injection channel). SW_VREF_NEG bit indicates the current switch status, including DSI and register controls, of the switch in the SAR ADC that shorts NEG with VREF input.

The CUR_AVG_ACCU and CUR_AVG_CNT fields in the SAR_AVG_STAT register indicate the current averaging accumulator contents and the current sample counter value for averaging (counts down).

The SAR_MUX_SWITCH_STATUS register gives the current switch status of MUX SWITCH0 register. These status registers help to debug SAR behavior.
## 38.3 Registers

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SAR_CTRL</td>
<td>Global configuration register. Analog control register</td>
</tr>
<tr>
<td>SAR_SAMPLE_CTRL</td>
<td>Global configuration register. Sample control register</td>
</tr>
<tr>
<td>SAR_SAMPLE_TIME01</td>
<td>Global configuration register. Sample time specification ST0 and ST1</td>
</tr>
<tr>
<td>SAR_SAMPLE_TIME23</td>
<td>Global configuration register. Sample time specification ST2 and ST3</td>
</tr>
<tr>
<td>SAR_RANGE_THRES</td>
<td>Global range detect threshold register</td>
</tr>
<tr>
<td>SAR_RANGE_COND</td>
<td>Global range detect mode register</td>
</tr>
<tr>
<td>SAR_CHAN_EN</td>
<td>Enable bits for the channels</td>
</tr>
<tr>
<td>SAR_START_CTRL</td>
<td>Start control register (firmware trigger)</td>
</tr>
<tr>
<td>SAR_CHAN_CONFIGx</td>
<td>Channel configuration register. There are 16 such registers with x = 0 to 15</td>
</tr>
<tr>
<td>SAR_CHAN_WORKx</td>
<td>Channel working data register. There are 16 such registers with x = 0 to 15</td>
</tr>
<tr>
<td>SAR_CHAN_RESULTx</td>
<td>Channel result data register. There are 16 such registers with x = 0 to 15</td>
</tr>
<tr>
<td>SAR_CHAN_WORK_UPDATED</td>
<td>Channel working data register: updated bits</td>
</tr>
<tr>
<td>SAR_CHAN_RESULT_UPDATED</td>
<td>Channel result data register: updated bits</td>
</tr>
<tr>
<td>SAR_STATUS</td>
<td>Current status of internal SAR registers (for debug)</td>
</tr>
<tr>
<td>SAR_AVG_STAT</td>
<td>Current averaging status (for debug)</td>
</tr>
<tr>
<td>SAR_INTR</td>
<td>Interrupt request register</td>
</tr>
<tr>
<td>SAR_INTR_SET</td>
<td>Interrupt set request register</td>
</tr>
<tr>
<td>SAR_INTR_MASK</td>
<td>Interrupt mask register</td>
</tr>
<tr>
<td>SAR_INTR_MASKED</td>
<td>Interrupt masked request register</td>
</tr>
<tr>
<td>SAR_SATURATE_INTR</td>
<td>Saturate interrupt request register</td>
</tr>
<tr>
<td>SAR_SATURATE_INTR_SET</td>
<td>Saturate interrupt set request register</td>
</tr>
<tr>
<td>SAR_SATURATE_INTR_MASK</td>
<td>Saturate interrupt mask register</td>
</tr>
<tr>
<td>SAR_SATURATE_INTR_MASKED</td>
<td>Saturate interrupt masked request register</td>
</tr>
<tr>
<td>SAR_RANGE_INTR</td>
<td>Range detect interrupt request register</td>
</tr>
<tr>
<td>SAR_RANGE_INTR_SET</td>
<td>Range detect interrupt set request register</td>
</tr>
<tr>
<td>SAR_RANGE_INTR_MASK</td>
<td>Range detect interrupt mask register</td>
</tr>
<tr>
<td>SAR_RANGE_INTR_MASKED</td>
<td>Range detect interrupt masked request register</td>
</tr>
<tr>
<td>SASR_INTR_CAUSE</td>
<td>Interrupt cause register</td>
</tr>
<tr>
<td>SAR_INJ_CHAN_CONFIG</td>
<td>Injection channel configuration register</td>
</tr>
<tr>
<td>SAR_INJ_RESULT</td>
<td>Injection channel result register</td>
</tr>
<tr>
<td>SAR_MUX_SWITCH0</td>
<td>SARMUX firmware switch controls</td>
</tr>
<tr>
<td>SAR_MUX_SWITCH_CLEAR0</td>
<td>SARMUX firmware switch control clear</td>
</tr>
<tr>
<td>SAR_MUX_SWITCH_DS_CTRL</td>
<td>SARMUX switch DSI control</td>
</tr>
<tr>
<td>SAR_MUX_SWITCH_SQ_CTRL</td>
<td>SARMUX switch sequencer control</td>
</tr>
<tr>
<td>SAR_MUX_SWITCH_STATUS</td>
<td>SARMUX switch status</td>
</tr>
</tbody>
</table>
39. Temperature Sensor

PSoc 6 MCUs have an on-chip temperature sensor that is used to measure the internal die temperature. The sensor consists of a transistor connected in diode configuration.

39.1 Features

- Measures device temperature
- Voltage output can be internally connected to SAR ADC for digital readout
- Factory calibrated parameters

39.2 Architecture

The temperature sensor consists of a single bipolar junction transistor (BJT) in the form of a diode. The transistor is biased using a reference current \( I_{REF} \) from the analog reference block (see the Analog Reference Block chapter on page 416 for more details). Its base-to-emitter voltage (\( V_{BE} \)) has a strong dependence on temperature at a constant collector current and zero collector-base voltage. This property is used to calculate the die temperature by measuring the \( V_{BE} \) of the transistor using SAR ADC, as shown in Figure 39-1.

The analog output from the sensor (\( V_{BE} \)) is measured using the SAR ADC. Die temperature in °C can be calculated from the ADC results as given in the following equation:

\[
\text{T}_{\text{Temp}} = (A \times \text{SAR}_{\text{out}} + 2^{10} \times B) + T_{\text{adjust}}
\]

- \( T_{\text{Temp}} \) is the slope compensated temperature in °C represented as Q16.16 fixed point number format.
- ‘A’ is the 16-bit multiplier constant. The value of A is determined using the PSoC 6 MCU characterization data of two point slope calculation. It is calculated as given in the following equation.
Temperature Sensor

Equation 39-2

\[ A = (\text{signed int}) \left( 2^{16} \left( \frac{100^\circ C - (-40^\circ C)}{\text{SAR}_{100^\circ C} - \text{SAR}_{-40^\circ C}} \right) \right) \]

Where,
\( \text{SAR}_{100^\circ C} = \text{ADC counts at } 100^\circ C \)
\( \text{SAR}_{-40^\circ C} = \text{ADC counts at } -40^\circ C \)

Constant 'A' is stored in a register SFLASH_SAR_TEMP_MULTIPLIER. See the PSoC 63 with BLE Registers TRM for more details.

- 'B' is the 16-bit offset value. The value of B is determined on a per die basis by taking care of all the process variations and the actual bias current (IREF) present in the chip. It is calculated as given in the following equation.

Equation 39-3

\[ B = (\text{unsigned int}) \left( 2^{26} \times 100^\circ C - \left( \frac{A \times \text{SAR}_{100^\circ C}}{2^{10}} \right) \right) \]

Where,
\( \text{SAR}_{100^\circ C} = \text{ADC counts at } 100^\circ C \)

Constant 'B' is stored in a register SFLASH_SAR_TEMP_OFFSET. See the PSoC 63 with BLE Registers TRM for more details.

- \( T_{\text{adjust}} \) is the slope correction factor in °C. The temperature sensor is corrected for dual slopes using the slope correction factor. It is evaluated based on the result obtained without slope correction, which is given by the following equation:

Equation 39-4

\[ T_{\text{initial}} = (A \times \text{SAR}_{\text{OUT}} + 2^{10} \times B) \]

If \( T_{\text{initial}} \) is greater than the center value (15 °C), then \( T_{\text{adjust}} \) is given by the following equation.

Equation 39-5

\[ T_{\text{adjust}} = \left( \frac{0.5^\circ C}{100^\circ C - 15^\circ C} \times (100^\circ C \times 2^{16} - T_{\text{initial}}) \right) \]

If \( T_{\text{initial}} \) is less than center value, then \( T_{\text{adjust}} \) is given by the following equation.

Equation 39-6

\[ T_{\text{adjust}} = \left( \frac{0.5^\circ C}{40^\circ C + 15^\circ C} \times (40^\circ C \times 2^{16} - T_{\text{initial}}) \right) \]

Figure 39-2. Temperature Error Compensation

Note: A and B are 16-bit constants stored in flash during factory calibration. These constants are valid only when the SAR ADC is running at 12-bit resolution with a 1.2-V reference.
39.3 Temperature Sensor Configuration

The temperature sensor output is routed to the positive input of SAR ADC via dedicated switches, which can be controlled by sequencer, firmware, or digital system interconnect (DSI). See the SAR ADC chapter on page 439 for details on how to read the temperature sensor output using the ADC. The temperature sensor is switched ON only when it is connected to the positive input of the SAR ADC.

39.4 Algorithm

1. Configure SAR ADC in single-ended mode with $V_{NEG} = V_{SS}$, $V_{REF} = 1.2$ V, 12-bit resolution, and right-aligned result. See the SAR ADC chapter on page 439 for more details.
2. Enable the SARMUX and SAR ADC. See the SAR ADC chapter on page 439 for more details.
3. Enable the temperature sensor.
4. Trigger a SAR ADC conversion and get the digital output from the SAR ADC. See the SAR ADC chapter on page 439 for more details.
5. Fetch ‘A’ from SFLASH_SAR_TEMP_MULTIPLIER and ‘B’ from SFLASH_SAR_TEMP_OFFSET.
6. Calculate the die temperature using the equations given in 39.2 Architecture.

39.5 Registers

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SAR_MUX_SWITCH0</td>
<td>This register has the SAR_MUX_FW_TEMP_VPLUS field to connect the temperature sensor to the SAR MUX terminal.</td>
</tr>
<tr>
<td>SAR_MUX_SWITCH_STATUS</td>
<td>This register provides the status of the temperature sensor switch connection to SAR MUX.</td>
</tr>
<tr>
<td>SFLASH_SAR_TEMP_MULTIPLIER</td>
<td>Multiplier constant ‘A’ as defined in Equation 39-1.</td>
</tr>
<tr>
<td>SFLASH_SAR_TEMP_OFFSET</td>
<td>Constant ‘B’ as defined in Equation 39-1.</td>
</tr>
</tbody>
</table>
40. Analog Routing

The PSoC 6 MCU has a flexible analog routing system that interconnects programmable analog blocks and GPIOs. Analog routing in the PSoC 6 MCU reduces external connections, allows last-minute feature changes, and eliminates delays caused by PCB spins by reconfiguring interconnection between analog blocks.

40.1 Features

The PSoC 6 MCU analog routing has the following features:

- Flexible connections between different analog blocks and GPIOs
- Two system-wide analog mux buses (AMUXBUS) that interconnect all analog capable GPIOs
- Switches in the analog routing can be used to create analog multiplexers
40.2 Architecture

Figure 40-1 shows the analog routing available in PSoC 6 MCUs.
Notes:
- The analog features and GPIOs shown in Figure 40-1 may not be available in all PSoC 6 MCUs. See the respective device datasheets for available analog features and ports in a device.
- Certain analog blocks such as CapSense and LPCOMP have additional internal routing, which is not shown in Figure 40-1. See the respective chapters of these blocks in this document for details.

Analog routing in the PSoC 6 MCU consists of several on-chip analog buses and analog switches. Table 40-1 gives a summary of connections available between analog blocks.

Table 40-1. Available Connections between PSoC 6 MCU Analog Blocks

<table>
<thead>
<tr>
<th>From GPIOS</th>
<th>To GPIOs</th>
<th>To SAR ADC</th>
<th>To CTBm (OA0, OA1)</th>
<th>To CTDAC</th>
<th>To LPCOMP</th>
<th>To CapSense IDACs</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMUXBUS A</td>
<td>AMUXBUS A B</td>
<td>Dedicated SARSEQ port</td>
<td>Dedicated CTBm pins</td>
<td>N/A⁸</td>
<td>Dedicated LPCOMP pins</td>
<td>N/A³</td>
</tr>
<tr>
<td>AMUXBUS B</td>
<td>AMUXBUS A B</td>
<td>AMUXBUS A B</td>
<td>AMUXBUS A B</td>
<td>AMUXBUS A B</td>
<td>AMUXBUS A B</td>
<td>AMUXBUS A B</td>
</tr>
<tr>
<td>From SAR ADC</td>
<td>N/A⁶</td>
<td>N/A⁶</td>
<td>N/A³</td>
<td>N/A³</td>
<td>N/A³</td>
<td>N/A³</td>
</tr>
<tr>
<td>From CTBm (OA0, OA1)</td>
<td>Dedicated CTBm pins</td>
<td>AMUXBUS A</td>
<td>AMUXBUS A</td>
<td>AMUXBUS B</td>
<td>N/A⁴</td>
<td>AMUXBUS A</td>
</tr>
<tr>
<td>AMUXBUS A</td>
<td>AMUXBUS B</td>
<td>Internal bus</td>
<td>AMUXBUS A</td>
<td>AMUXBUS A</td>
<td>AMUXBUS B</td>
<td>AMUXBUS A</td>
</tr>
<tr>
<td>From CTDAC</td>
<td>Dedicated CTDAC pin</td>
<td>Through CTBm</td>
<td>Through CTBm</td>
<td>Internal bus</td>
<td>N/A⁴</td>
<td>AMUXBUS A</td>
</tr>
<tr>
<td>AMUXBUS A</td>
<td>AMUXBUS B</td>
<td>AMUXBUS A</td>
<td>AMUXBUS A</td>
<td>AMUXBUS B</td>
<td>AMUXBUS A</td>
<td>AMUXBUS B</td>
</tr>
<tr>
<td>From LPCOMP</td>
<td>N/A⁸</td>
<td>N/A⁵</td>
<td>N/A⁵</td>
<td>N/A⁴</td>
<td>N/A⁵</td>
<td>N/A⁵</td>
</tr>
<tr>
<td>From CapSense IDACs</td>
<td>AMUXBUS A</td>
<td>AMUXBUS A B</td>
<td>AMUXBUS A B</td>
<td>AMUXBUS A B</td>
<td>N/A⁴</td>
<td>AMUXBUS A B</td>
</tr>
<tr>
<td>AMUXBUS B</td>
<td>AMUXBUS A B</td>
<td>AMUXBUS A B</td>
<td>AMUXBUS A B</td>
<td>AMUXBUS A B</td>
<td>AMUXBUS A B</td>
<td>AMUXBUS A B</td>
</tr>
</tbody>
</table>

Notes:
- For detailed routing and switch-control information of a block, click on the respective block name.
- CapSense block connections used for touch sensing are not shown in Table 40-1 because CapSense is not expected to be connected to any other analog blocks during touch sensing.
- AMUXBUS routing is not available in Deep Sleep and Hibernate power modes of PSoC 6 MCUs.

Most analog blocks have dedicated connections to certain pins, which, when used, provide the best possible performance. However, these blocks can be also connected to other GPIOs using AMUXBUS in case the dedicated pin is not available or is used by another resource.

40.2.1 AMUXBUS Splitting

AMUXBUS A and AMUXBUS B are system-wide analog buses that can connect to almost all analog blocks and GPIOs in the PSoC 6 MCU. However, the PSoC 6 MCU has only two of these buses. Each AMUXBUS can be split into multiple segments using the HSIOM_AMUX_SPLIT_CTL register. For more information on AMUXBUS connections, see the I/O System chapter on page 164.

40.3 Register List

Table 40-2. Register Summary

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>HSIOM_AMUX_SPLIT_CTL</td>
<td>This register controls the breaking of AMUX buses A and B into multiple segments.</td>
</tr>
</tbody>
</table>
41. CapSense

The CapSense system can measure the self-capacitance of an electrode or the mutual capacitance between a pair of electrodes. In addition to capacitive sensing, the CapSense system can function as an ADC to measure voltage on any GPIO pin that supports the CapSense functionality.

The CapSense touch sensing method in PSoC 6 MCUs, which senses self-capacitance, is known as CapSense Sigma Delta (CSD). Similarly, the mutual-capacitance sensing method is known as CapSense Cross-point (CSX). The CSD and CSX touch sensing methods provide the industry's best-in-class signal-to-noise ratio (SNR), high touch sensitivity, low-power operation, and superior EMI performance.

CapSense touch sensing is a combination of hardware and firmware techniques. Therefore, use the CapSense component provided by the PSoC Creator IDE to implement CapSense designs. See the PSoC 4 and PSoC 6 MCU CapSense Design Guide for more details,
Section F: BLE Subsystem (BLESS)

This section has the following chapter:
- Bluetooth Low Energy Subsystem (BLESS) chapter on page 468

Top Level Architecture

![BLE Subsystem Block Diagram]

- Bluetooth Low Energy Subsystem
  - BLE 4.2 Programmable Link Layer
  - Digital Interface
  - BLE 2 Mbps Radio
42. Bluetooth Low Energy Subsystem (BLESS)

The Bluetooth Low Energy (BLE) subsystem (BLESS) implements the Bluetooth LE Link Layer and Physical Layer as specified in Volume 6 of the Bluetooth 4.2 specification. This subsystem is capable of multiple simultaneous procedures allowed by the Bluetooth 4.2 specification and maintaining a single connection in conjunction with firmware. This subsystem also supports 2 Mbps data rate, according to BLE 5.0 specification. This chapter explains the features, implementation, and operational modes of the BLESS.

42.1 Features

The BLESS subsystem has the following features:

- **Link Layer**
  - All mandatory and optional LE link layer features of Bluetooth v4.0 specifications and multiple optional LE link layer features of Bluetooth v4.1 and v4.2 specifications
  - Both master and slave roles
  - Support for all packet types and control PDUs
  - Duplicate and whitelist filtering
  - Advanced Encryption Standard (AES) 128 encryption/decryption using CCM (Counter with Cipher Block Chaining (CBC) - Message Authentication Code (MAC)) mode
  - Support for Bluetooth v4.1/v4.2 features including low-duty cycle advertising, LE ping mechanism for secure pairing, and L2CAP connection oriented channels
  - Support for single and multiple connections (up to four connections)
  - Support for 2 Mbps transmit/receive

- **Radio/Modem Interface**
  - LDO that can deliver up to 20 mA load current radio
  - Radio control bus (RCB) interface to communicate with the radio

42.2 Architecture

Figure 42-1. BLE Subsystem Block Diagram
The BLESS includes the following major blocks:

- **Link Layer (LL) Controller**: The Link Layer Controller implements the state machines for various Bluetooth LE procedures (advertiser, scanner, initiator, and connection), roles (master and slave), timing critical functions (packet framing/de-framing, CRC generation/checking, encryption/decryption, packet transmission, and protocol time reference keeping), and direct test mode.

- **System Control**: This block consists of the AHB bus interface logic, the interrupt control logic, and the subsystem controller, which controls the BLE subsystem clocks, reset, and power modes.

- **Radio Controller**: This block contains the mode transition FSM that controls the LDO and power supply switches of the radio and PHY.

### 42.2.1 Link Layer Controller

This section provides details about the high-level functional modes and configuration of the link layer.

#### 42.2.1.1 Firmware Reset

The link layer can be reset using a link layer firmware soft reset request. This resets all registers and state machines to their default values and states respectively. The soft reset does not modify the FIFO content; instead, the content becomes invalid and the FIFOs need to be reinitialized.

#### 42.2.1.2 BLE Functional Modes and Configuration

This section details the various modes of BLE functions. The operation of the link layer is defined using a state machine with the following main modes:

- **Standby**
- **Advertising**
- **Scanning (Active or Passive)**
- **Initiating**
- **Connection (Master or Slave)**
- **Direct Test Mode (DTM)**
- **Encryption/Decryption**

#### Standby State

This state is the default functional state. The link layer in this state does not transmit or receive any packet. It is possible to move from this state to Advertising, Scanning, or other states based on the relevant functional requirement. This state can be entered from any of the other states.

#### Advertising State

This state allows the link layer to transmit advertising packets and optionally respond to peer devices’ responses. A device in this state is termed as an advertiser and can be entered from the Standby state. A device moves to this state to either be discoverable or connectable. This mode also enables the device to broadcast data to other devices in the area.

#### Scanning State

The link layer in this state facilitates the device to listen for advertising packets from the peer devices. This state can perform either of the following kinds of scanning:

- **Active scanning**
- **Passive scanning**

Passive scanning is used to listen for the presence of other devices. Active scanning permits the device to respond with scan requests to the advertising device. This can be used to obtain more data about the peer device and potentially move further to engage in connection.

The device in this state is known as scanner and can be entered from the Standby state.

#### Initiating State

The link layer in the Initiating state listens for advertising packets from a specific peer device and responds to initiate a connection with the peer device. A device in this state is known as an initiator and this state can be entered from the Standby state.

#### Connection State

The final procedural state in the link layer protocol is the Connection state. This is entered from either the Advertising or Initiating state. The device in this state is termed as being in connection. This state has two roles: master and slave.

If this state is entered from the Advertising state, then the device is qualified as a slave; if it is entered from the Initiating state, it is known as a master.

#### 2 Mbps

The upcoming BLE 5.0 specification supports 2 Mbps data rate for packet transfers. The feature includes support for asymmetric links (independent rate for transmit and receive), new control procedures in the link layer to allow transition between 1 Mbps and 2 Mbps, and updates to DTM for 2 Mbps PHY testing.

#### Direct-Test Mode

This mode provides the ability to test the physical layer (radio digital/RF). It allows a tester to command a controller’s physical layer to either transmit or receive a sequence of predefined test packets. The tester can then analyze the packets received to determine if the physical layer is working according to the specification. The tester can also measure various RF parameters from the received packets to determine the compliance of the physical layer to RF Specifications.
**Encryption/Decryption**

This mode provides the ability to encrypt a plain text data or decrypt encrypted data. Bluetooth LE uses AES-128 encryption/decryption using CCM. This module also supports encryption using ECB mode.

### 42.2.2 Clocks

This subsystem has three primary clocks.

- **CLK_AHB**: This clock feeds to the System Control block and all logic interfacing the CPU.
- **CLK_ECO**: This clock is a high-accuracy high-frequency clock, which feeds the link layer controller and the radio Phy. This clock is also an input to the system resources subsystem as an alternative high-frequency clock source.
- **CLK_LF**: This clock is a high-accuracy low-frequency clock, which feeds the link layer controller timer logic that is functioning during the low-power operation modes.

### 42.2.3 Power States

BLESS supports four power states. Table 42-1 lists the state transitions and the corresponding trigger events.

<table>
<thead>
<tr>
<th>Current State</th>
<th>Next State</th>
<th>Trigger Event</th>
</tr>
</thead>
<tbody>
<tr>
<td>BLE.OFF</td>
<td>BLE.RST</td>
<td>PSoC power-up to move to RESET state</td>
</tr>
<tr>
<td>BLE.RST</td>
<td>BLE.DPLSP</td>
<td>PSoC moves from RESET to Active state</td>
</tr>
<tr>
<td>BLE.DPSLP</td>
<td>BLE.ACTIVE</td>
<td>Firmware or hardware can trigger DPSLP exit An interrupt is raised to indicate exit so PSoC can exit Deep Sleep state</td>
</tr>
<tr>
<td>BLE.DPSLP</td>
<td>BLE.OFF</td>
<td>1) PSoC power-down or brownout 2) PSoC moves to Hibernate state 3) PSoC moves to OFF state 4) XRES assertion</td>
</tr>
<tr>
<td>BLE.ACTIVE</td>
<td>BLE.OFF</td>
<td>Power Down Event</td>
</tr>
<tr>
<td>BLE.RST</td>
<td>BLE.DPLSP</td>
<td>System reset asserted</td>
</tr>
<tr>
<td>BLE.ACTIVE</td>
<td>BLE.DPLSP</td>
<td>Firmware triggers DPSLP entry</td>
</tr>
</tbody>
</table>

#### 42.2.3.1 BLE.OFF

No power supply to logic.

#### 42.2.3.2 BLE.RST

Power is supplied to logic, but logic is in reset with all resets to the block asserted.
42.2.3.3 BLE.DPSLP

Power is supplied to logic and logic is out of reset. CLK_ECO is absent, CLK_LF is present, and CLK_AHB may be present depending on the PSoC power state. This is the lowest power functional mode. This mode is entered for maximum power saving during advertising/connection interval after packets transmission/reception is completed. The block maintains all the configurations in this state.

42.2.3.4 BLE.ACTIVE

Link layer is active and CLK_ECO is enabled in the link layer. Both CLK_LF and CLK_AHB are present. The link layer may be in preprocessing, transmit, receive, or post-processing state.

42.2.4 Bluetooth LE 4.2 Feature – Data Length Extension

Data length extension is a BLE 4.2 feature that increases the maximum supported length of the LL data PDU from 27 to 251 octets. With this feature enabled, the transmit and receive packet lengths during connection are increased to 251 bytes. The encryption module also supports 251-byte packet encryption and decryption.

42.2.5 Bluetooth LE 4.2 Feature – Privacy 1.2

Privacy 1.2 is a BLE 4.2 feature in which private address generation and resolution is implemented in the BLE link layer. The functionality is partitioned between the BLESS hardware and link layer firmware.

This feature is enabled in the subsystem by setting the PRIV_1_2 bit in BLE_BLELL_LL_CONTROL register. The hardware resolving list can store up to 16 entries and the firmware can extend this list to add more entries by setting the HW_RSLV_LIST_FULL in BLE_BLELL_LL_CONTROL register.

42.2.5.1 Resolving List

The link layer maintains a set of records called resolving list for local and peer IRK value pairs. The resolving list contains the following fields:

- Peer Identity Address: A peer device’s Public or Static address.
- Local Identity Resolution Key (IRK): A key shared with the associated peer device and used to generate a self-resolvable private address (RPA).
- Peer IRK: A key shared by the associated peer device and used to resolve a peer RPA.

The resolving list is implemented between firmware and hardware. The firmware maintains the resolving list as exposed and used by the host layer but works with the hardware resolving list for list operations and management.

42.2.6 Multiple Connections

BLE 4.2 allows a BLE device to maintain multiple connections simultaneously in both master and slave roles. This subsystem can support up to four simultaneous connections. Multiple connections are achieved using both hardware and firmware. This subsystem uses a firmware scalable architecture to support multiple connections. The core connection engine is used for radio transmit/receive during the connection event. Firmware does a context switch at the end of each connection event and schedules different connection events. The BLE link layer functions for window-widening, connection-arbitration, conflict-resolution, control procedures for channel map and connection updates, scheduling for the advertisement/scanner and initiator, and scheduling radio time events are implemented in firmware.

The firmware programs the connection context in parameter memory, BLE_BLELL_CONN_n_PARAM_MEM_BASE_ADDR and the time instant in the Next Instant (NI) timer register, BLE_BLELL_NI_TIMER. When the timer expires, the connection event is started and the link layer core connection engine uses the parameters for radio transmit/receive. When the connection event is closed, firmware reads the status of the current connection and switches the context to the next connection in the queue.

42.2.6.1 Context Switching

The firmware programs parameters of a particular connection in the connection parameter memory and the event instant in the NI timer. When the timer expires, the connection event is started and the core connection engine loads the parameters from connection memory, using the parameters for radio transmit/receive. When the connection event is closed, firmware reads the status of the current connection and switches the context to the next connection in the queue.

The inputs required by the connection engine for radio transmit/receive fall under two categories:

- Parameters that do not change every connection event (such as access address and connection interval). Link layer hardware loads the connection parameters at the start of the connection event. Firmware programs these parameters if there is a connection or channel map update.
- Connection variables that are modified during every connection event (such as SN/NESN and next connection instant).

The instant programmed into the NI timer must be at least 1.25 ms before the actual instant to allow successful arbitration between the various procedures (advertiser, scanner, initiator, connection).
42.2.6.2 Master Role: HW-FW Interaction

When an initiator creates a master connection, it should schedule the first connection event within the transmit window. The hardware-firmware interaction sequence for a master connection creation and establishment is as follows:

- The connection parameters are stored in the connection parameter memory before the initiator scans for advertisement packets.
- On a master connection creation, an interrupt is raised to indicate to the CPU.
- The firmware calculates the transmit window, based on which it calculates the instant for first connection event and configures the NI timer with this instant.
- When the timer expiry is triggered, the connection event in started by the hardware. The connection FSM schedules the radio Tx and Rx during the event and on event close, triggers a connection event close interrupt.
- The firmware reads the status of the current connection and switches the context to the next connection in the queue.

42.2.6.3 Slave Role: HW-FW Interaction

When an advertiser transmitting a connectable advertisement receives a CONNECT_REQ PDU, a slave connection is created and an interrupt is raised. The slave should then listen for the first connection packet from the master to establish the connection. The hardware-firmware interaction sequence for a slave connection creation and establishment is as follows.

- On a slave connection creation, the connection parameters received in the CONNECT_REQ PDU are stored by the hardware in the connection parameter memory and an interrupt is raised to indicate to the CPU.
- The firmware reads the connection parameters. It calculates the instant and offset for the first connection event and configures the NI timer with these values.
- When the timer expiry is triggered, the connection event is started by the hardware. The connection FSM schedules the Rx and Tx during the event.
- If no packet is received, the radio is disabled. If a packet is received, the connection is established and the Bluetooth timer slot value and offset are captured to schedule subsequent connection events. On event close, the firmware triggers a connection event close interrupt.
- The firmware reads the status of the current connection and switches the context to the next connection in the queue.

42.2.6.4 Arbitration

BLE 4.2 states that multiple procedures can be enabled together and the radio must be arbitrated among the procedures. The priority for the arbitration logic is as follows:

- Connection
- Initiator Tx
- Advertisement
- Scanner Tx
- Initiator Rx
- Scanner Rx

Note that the connection can correspond to multiple active connections, which are arbitrated in firmware.

42.2.6.5 Data Buffer Management

Transmit

The connection engine uses SENT/ACK handshake between the link layer and the firmware for data packet transmission. The packets are queued in the transmit data memory by firmware and the link layer processes it in FIFO mode. Four transmit buffers (maximum) are available for each connection, which are indexed by firmware (0–3). Each transmit buffer maintains the sent/ack status.

The transmit buffers and memory descriptors are shared between multiple connections. Each transmit buffer is of 256 bytes depth and can support data length extension packets of maximum 251 bytes payload. The connection engine frames the transmit packet with the header and payload; the LLID and packet length are in the BLE_BLELL_MMMS_DATA_MEM_DESCRIPTOR register. The transmit buffer number associated with the SENT/ACK index is part of the BLE_BLELL_DATA_LIST_SENT register.

Receive

The receive data memory works in FIFO mode for both firmware read and link layer hardware write. The first dword of the packet stored will have the connection index and number of dwords in the packet (including header, payload data, and RSSI). The receive buffer size is 2 KB, this can store up to seven data length extension (DLE) packets of maximum 251 bytes payload. If the received packet crosses the memory boundary and the FIFO is full, the packet is flushed by the hardware logic and is not ACK’ed.
42.2.7 External PA/LNA Support

RF front ends come in a variety of combinations. The most popular and comprehensive RF front ends come with a built-in power amplifier (PA) in the transmit path, a low-noise amplifier (LNA) in the receive path, a transmit/receive bypass path to bypass both the PA and LNA, and RF switches to select between transmit, receive, and bypass paths. Some front ends support multiple antennas. Some front ends have a built-in low-pass filter after the power amplifier. The discrete front ends also have almost the same configuration.

The following control signals are present to support an external PA.

The ENABLE_EXT_PA_LNA bit in the BLE_BLESS_EXT_PA_LNA_CTRL register is the master control for external PA/LNA control.

- **Tx ENABLE**
  This signal will be ON during transmission and OFF when not transmitting. This signal will be active before the actual start of transmission to allow the power amplifier to ramp up. The ramp-up time of the commonly used power amplifiers is typically less than 1 µs. In most front ends, the receive path is automatically chosen when this signal is inactive. The polarity of this signal will be configurable through the PA_CTRL_POL bit in the BLE_BLESS_EXT_PA_LNA_CTRL register.

- **Rx ENABLE**
  This signal is needed to choose between the bypass path and LNA path. This signal will be ON during reception and OFF when the receiver is OFF. The polarity of this signal will be configurable through the LNA_CTRL_POL bit in the BLE_BLESS_EXT_PA_LNA_CTRL register.

- **Chip Enable Signal**
  This signal is needed to put the front end to sleep or standby when the radio is not active. The signal should be ON if either PA control or LNA control is ON. The polarity of this signal will be configurable through the CHIP_EN_POL bit in the BLE_BLESS_EXT_PA_LNA_CTRL register.

![Figure 42-3. EXT PA/LNA Control](image)
## 42.3 Register Summary

Table 42-2 gives the details of all register fields discussed in this chapter. For more details, see *PSoc 63 with BLE Registers TRM*.

Table 42-2. Register List

<table>
<thead>
<tr>
<th>Register</th>
<th>Bits</th>
<th>Field Name</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BLE_BLELL_COMMAND_REGISTER</td>
<td>7:00</td>
<td>COMMAND</td>
<td>The 8-bit command from firmware to the link layer controller. See the <em>PSoc 63 with BLE Registers TRM</em> for the list of instructions and their opcodes. The instruction results in the link layer hardware starting or stopping an operation.</td>
</tr>
<tr>
<td>LL_CONTROL (4.2)</td>
<td>0</td>
<td>PRIV_1_2</td>
<td>Enables Privacy 1.2 feature.</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>DLE</td>
<td>Enables data length extension feature in DTM, connection, and encryption modules.</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>HW_RSLV_LIST_FULL</td>
<td>This bit indicates that the resolving list in the hardware is full and the list is extended in the firmware. This will affect the behavior of address resolution.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 - The resolving list in the hardware is not fully filled. When the whitelist is disabled and a peer identity address not in the resolving list is received, the packet is responded to by the hardware.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 - The resolving list in the hardware is fully filled. All address comparisons must be extended to the firmware list as well. Any match in the firmware list should be followed by copying the matching entry into the hardware resolving list.</td>
</tr>
<tr>
<td>BLE_BLELL_DATA_LIST_SENT_UPDATE_STATUS</td>
<td>3:0</td>
<td>LIST_INDEX_TX_SENT_3_0</td>
<td>Write: Indicates the buffer index for which the SENT bit is updated by firmware. Read: Reads TX_SENT[3:0]. The bits in this field indicate the status of the SENT bit in the hardware for each packet buffer.</td>
</tr>
<tr>
<td></td>
<td>7</td>
<td>SET_CLEAR</td>
<td>Write: Used to set the SENT bit in hardware for the selected packet buffer.</td>
</tr>
<tr>
<td>BLE_BLELL_DATA_LIST_ACK_UPDATE_STATUS</td>
<td>3:0</td>
<td>LIST_INDEX_TX_ACK_3_0</td>
<td>Write: Indicates the buffer index for which the ACK bit is updated by firmware. Read: Reads TX_ACK[3:0]. If a particular bit is set, then the packet in the selected buffer is transmitted (at least once) by the hardware and hardware is waiting for acknowledgement.</td>
</tr>
<tr>
<td></td>
<td>7</td>
<td>SET_CLEAR</td>
<td>Write: Firmware uses the field to clear an ACK bit in the hardware to indicate that the acknowledgement for the transmit packet has been received and processed by firmware.</td>
</tr>
<tr>
<td>BLE_BLELL_NI_TIMER</td>
<td>15:0</td>
<td>NI_TIMER</td>
<td>BT slot at which the next connection should be serviced; granularity is 625 µs. The NI timer should be programmed 1.25 ms before the connection event.</td>
</tr>
</tbody>
</table>
### BLE_BLELL_CONN_n_PARAM_MEM_BASE_ADDR

<table>
<thead>
<tr>
<th>Register</th>
<th>Bits</th>
<th>Field Name</th>
<th>Bit Description</th>
</tr>
</thead>
</table>
| BLE_BLELL_CONN_n_PARAM_MEM_BASE_ADDR | 15:0 | CONN_n_PARAM | Data values are written as 16-bit wide data. This memory is valid only if MMMS is enabled. The layout is as follows:

00 - AA[15:0]
04 - AA[31:16]
08 - CRC_init[15:0]
0C - WINDOW_SIZE[7:0], CRC_init[23:16]
10 - TX_WINDOW_OFFSET
14 - CI[15:0]
18 - SLV_LATENCY[15:0]
1C - SUPERVISORY_TIMEOUT_VAL[15:0]
20 - CHAN_MAP[15:0]
24 - CHAN_MAP[31:16]
28 - SCA[2:0], CHAN_HOP_INCR[4:0], CHAN_MAP[39:32]
2C - Reserved[1:0], RX_DATA_RATE_1M_2M, TX_DATA_RATE_1M_2M, WINDOW_WIDEN_INTERVAL[11:0]
30 - CE_LENGTH[15:0]
34 - NEXT_SUPER_TO[15:0]
38 - Reserved[1:0], LAST_UNMAPPED_CHANNEL[5:0], Reserved[3:0], SN, NESN, Reserved[1:0]
3C - ACCU_WINDOW_WIDEN[15:0]
40 - BT_SLOT_CAPTURE[15:0]
44 - Reserved[15:10], US_CAPTURE[9:0]
48 - Next Connection Instant
4C - Reserved[5:0], US_OFFSET[9:0]

**Note:** The n in the register/field can vary from 1 to 4.

### BLE_BLELL_MMMS_DATA_MEM_DESCRIPTOR

<table>
<thead>
<tr>
<th>Register</th>
<th>Bits</th>
<th>Field Name</th>
<th>Bit Description</th>
</tr>
</thead>
</table>
| BLE_BLELL_MMMS_DATA_MEM_DESCRIPTOR | 1:0 | LLID_C1 | The LLID indicates whether the packet is an LL Data PDU or an LL Control PDU.

00b = Reserved.
01b = LL Data PDU: Continuation fragment of an L2CAP message or an Empty PDU.
10b = LL Data PDU: Start of an L2CAP message or a complete L2CAP message with no fragmentation.
11b = LL Control PDU.

### BLE_BLESS_EXT_PA_LNA_CTRL

<table>
<thead>
<tr>
<th>Register</th>
<th>Bits</th>
<th>Field Name</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BLE_BLESS_EXT_PA_LNA_CTRL</td>
<td>9:2</td>
<td>DATA_LENGTH_C1</td>
<td>This field indicates the length of the data packet. Bits [9:7] are valid only if DLE is set. Range 0x00 to 0xFF.</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>ENABLE_EXT_PA_LNA</td>
<td>When set to 1, enables the external PA and LNA</td>
</tr>
</tbody>
</table>
| | 1 | CHIP_EN_POL | Controls the polarity of the chip enable control signal. 
0 - High enable, low disable 
1 - Low enable, high disable |
| | 2 | PA_CTRL_POL | Controls the polarity of the PA control signal. 
0 - High enable, low disable 
1 - Low enable, high disable |
| | 3 | LNA_CTRL_POL | Controls the polarity of the LNA control signal. 
0 - High enable, low disable 
1 - Low enable, high disable |