

Managing Power Brownout Recovery with Infineon 65-nm NOR Flash

About this document

Scope and purpose

This application note reviews the methods that can be used to ensure that Infineon 65-nm NOR Flash and 63-nm HyperRAM™ devices are initialized correctly.

Intended audience

This is intended for users who manage power brownout recovery with Infineon 65-nm NOR flash.

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Introduction

1 Introduction

The primary method for ensuring that Infineon 65-nm NOR Flash devices and 63-nm HyperRAM devices are correctly initialized is for the system to apply a valid Power-On Reset (POR).

- When the flash device powers up from zero volts, a valid POR is achieved whereby the flash device always attains the Standby state—i.e., the state whereby the flash device can accept commands from the system and respond to those commands.
- However, if a flash device that has been initialized by a valid POR subsequently experiences a drop in supply voltage below the minimum operating voltage, where the flash device does not then undergo a valid POR (i.e., it undergoes a brownout), then the flash device may not repower to the Standby state. In this case, the flash device may be unresponsive to commands from the system.

For systems where the flash device supply voltage cannot be guaranteed to always apply a correct POR, the flash brownout scenario introduces a power failure vulnerability into the system that must be managed to achieve power-fault-tolerant system operation. This application note shows how to manage this power failure vulnerability, and how to test the system to prove that the vulnerability is managed.

Device Scope

2 Device Scope

The following two tables show the flash and RAM devices that are within the scope of this application note:

Table 1 Flash Devices where POR is the Only Valid Initialization Method

Family	Feature Size (nm)	Technology	POR	RESET#	DPD	Software Reset	Init Options after Power Event
S29GL-S	65	MirrorBit Eclipse	<VRST for t _{PD} POR fully resets flash	Partially resets flash	N/A	Partially resets flash	POR-Only
S25FL-S	65	MirrorBit Eclipse	<VRST for t _{PD} POR fully resets flash	Partially resets flash	N/A	Partially resets flash	POR-Only
S25FS-S	65	MirrorBit Eclipse	<VRST for t _{PD} POR fully resets flash	Partially resets flash	Partially resets flash	Partially resets flash	POR-Only
S29GL064S	65	MirrorBit	<VRST for t _{PD} POR fully resets flash	Partially resets flash	N/A	Partially resets flash	POR-Only
S25FL-L	65	Floating Gate	<VRST for t _{PD} POR fully resets flash	Partially resets flash	Partially resets flash	Partially resets flash	POR-Only

Table 2 Flash/RAM Devices where POR or Deep Power Down (DPD) Entry/Exit can be Used to Initialize the Device

Family	Feature Size (nm)	Technology	POR	RESET#	DPD	Software Reset	Init Options after Power Event
S26KL-S	65	MirrorBit	<VRST for t _{PD} POR fully resets flash	Partially resets flash	Fully resets flash	Partially resets flash	POR Plus Orderly Shutdown and Recovery
S26KS-S	65	MirrorBit	<VRST for t _{PD} POR fully resets flash	Partially resets flash	Fully resets flash	Partially resets flash	POR Plus Orderly Shutdown and Recovery
S27KL-1	63	DRAM	<VRST for t _{PD} POR fully resets flash	Partially resets RAM	Fully resets flash	N/A	POR Plus Orderly Shutdown and Recovery
S27KS-1	63	DRAM	<VRST for t _{PD} POR fully resets flash	Partially resets RAM	Fully resets flash	N/A	POR Plus Orderly Shutdown and Recovery

Device Scope

These tables show two classes of flash and RAM parts, all of which can be reinitialized via a datasheet-compliant POR, and some of which can also be reinitialized by the DPD-based Orderly Shutdown and Recovery methods described later in this application note. For these devices, neither the RESET# signal nor the software reset command are sufficient to fully reinitialize these devices.

These tables also mention a “power event”. Supposing that there is a memory device from the table that is correctly initialized by a power-up from zero volts, a power event is simply an excursion below the nominal supply voltage to some value between zero volts and nominal V_{CC} that ultimately returns to the nominal V_{CC} range. In some cases, a power event requires a full reinitialization of the device, and sometimes it does not. This application note describes the requirements and methods for achieving correct reinitialization following a power event.

State Transitions

3 State Transitions

Devices listed in the previous section have a tiered reset scheme whereby:

- POR fully initializes the device
- RESET# returns a correctly initialized device at the nominal voltage to the POR state
- The Software Reset command clears some states in a correctly initialized device at the nominal voltage

In other words, the reset power of these three methods looks like this:

POR > RESET# > Software Reset

Here, the precondition for the correct operation of RESET# and Software Reset is *a correctly initialized device at nominal voltage*. In other words, neither RESET# or Software Reset can reinitialize the device by themselves—only a datasheet-compliant POR can do that.

Table 3 shows the reset precedence in more detail:

Table 3 Flash State Transition

Flash State	Wait Until Done	Software Reset	Program Resume	Erase Resume	RESET#	POR
Busy	Standby	–	–	–	Standby	Standby
Status Error	–	Standby	–	–	Standby	Standby
ASO Mode	–	Standby	–	–	Standby	Standby
Program Suspend	–	–	Busy	–	Standby	Standby
Erase Suspend	–	–	–	Busy	Standby	Standby

There are three ways to cause a Busy state to return to the Standby state:

1. Wait until the operation completes.
2. Drive RESET# LOW.
3. Drive V_{CC} through a datasheet-compliant POR.

This table also shows the limited effect of a Software Reset—it only clears ASO Modes and Status Errors in a properly initialized device running at nominal conditions. The effect of RESET# is somewhat more powerful in that it has the effect of Software Reset, plus it can terminate the Busy state and any Suspend states. POR can do everything that Software Reset and RESET# can do, plus this action can fully reinitialize the device after an arbitrary power event.

Power-On Reset Versus Brownout

4 Power-On Reset Versus Brownout

Each of the datasheets within the scope for this application note contains a diagram like this one, which defines various specifications for how to manage POR:

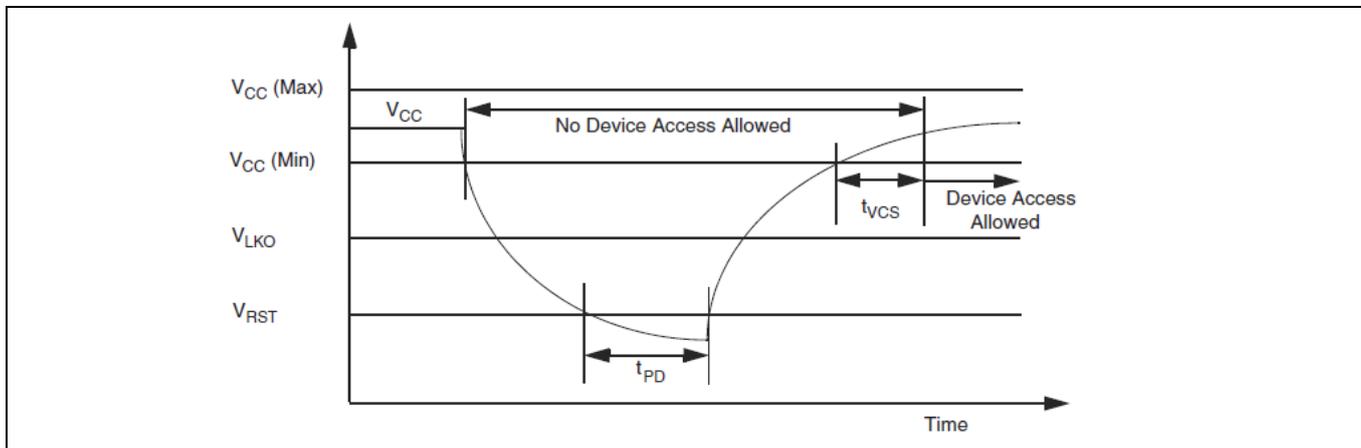


Figure 1 Power Drop Figure from the S26KL-S/S26KS-S Datasheet (Figure 22 from 001-99198 Rev. *H):

For the in-scope devices, here is a table summarizing the POR parameters defined in [Figure 1](#). Datasheets may change over time, so be sure to check the latest datasheet revision for current values.

Table 4 POR Parameters for Flash/RAM Devices Covered in This Application Note

Memory Type	Datasheet Revision	VCC(MIN) to VCC(MAX) (V)	VLKO (V)	VRST (V)	tPD (μs)	tVCS (μs)
MirrorBit Eclipse	001-98285 Rev *K	2.7-3.6	2.25	1.0	15	300
MirrorBit Eclipse	001-98283 Rev *M	2.7-3.6	2.4	1.6	15	300
MirrorBit Eclipse	002-00368 Rev *J	1.7-1.95	1.5	0.7	10	300
MirrorBit	001-98286 Rev *E	2.7-3.6	2.5	1.0	15	50
Floating Gate	002-00124 Rev *E	2.7-3.6	2.7	1.0	10	300
MirrorBit	001-99198 Rev *H	2.7-3.6	2.4	0.7	10	300
MirrorBit	001-99198 Rev *H	1.7-1.95	1.5	0.5	10	300
DRAM	001-97964 Rev *J	2.7-3.6	2.7	0.8	50	150
DRAM	001-97964 Rev *J	1.7-1.95	1.7	0.8	30	150

Let’s define “nominal voltage” to be when $V_{CC(MAX)} > V_{CC} > V_{CC(MIN)}$; by definition, any voltage variation within this range is not a power event.

Per the in-scope datasheets, the lockout voltage, V_{LKO} is the voltage below which the device is powered OFF, at which point POR must be initiated to ensure the flash is properly reinitialized.

The critical factors for a power event to be POR are:

- $V_{CC} < V_{RST}$ for t_{PD} before V_{CC} can rise to nominal voltage (this includes $V_{CC} = 0$ for $t \gg t_{PD}$)

Power-On Reset Versus Brownout

- After V_{CC} is rising, while $V_{CC} > V_{CC(MIN)}$, the first falling edge for CE# can happen after t_{VCS}
- No device access (CE# goes LOW) while $V_{CC} < V_{CC(MIN)}$ and while t_{VCS} has not expired

The ending state of the flash device after POR is the Standby state, so the flash device is correctly initialized and ready to accept and respond to commands. This result is shown in **Figure 2**.

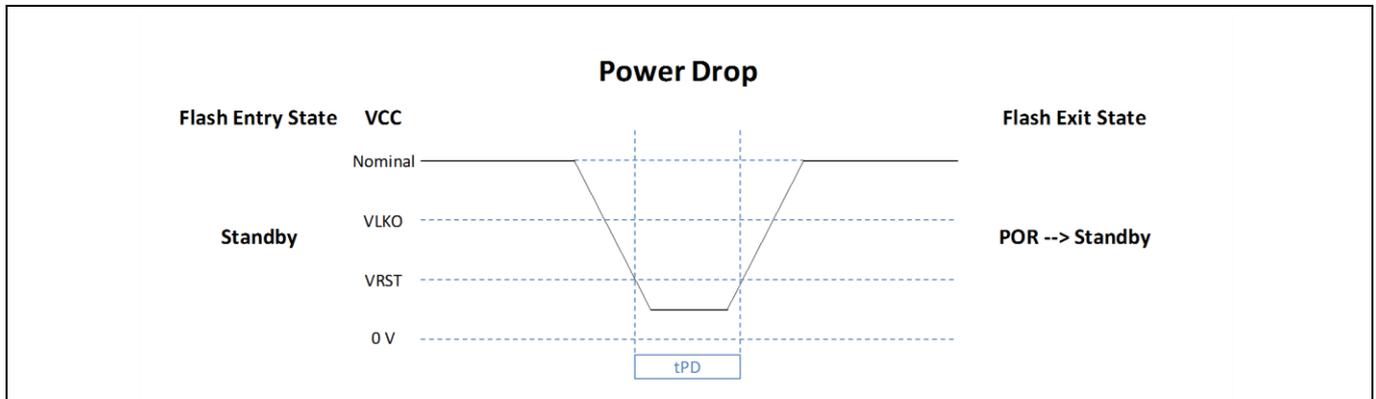


Figure 2 Flash/RAM Exit State After POR

For any power event where $V_{CC(MIN)} > V_{CC} > V_{LKO}$ while CE# stays HIGH, the device is “powered ON” and the power event has no effect on the flash device, either during the power event or once power returns to nominal; and reinitialization by POR is not required. Let’s call this a “safe power event”. As for POR, the ending state of the flash after a safe power event is the Standby state, so the flash device is correctly initialized and ready to accept and respond to commands. This result is shown in **Figure 3**.

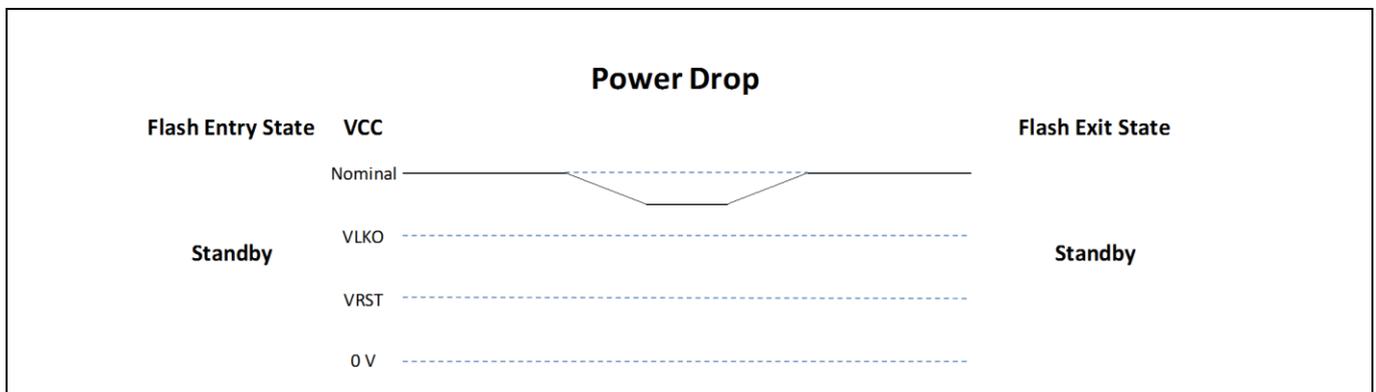


Figure 3 Flash/RAM Exit State After Safe Power Event

Any power event that is not within the boundaries of a safe power event, and that is not within the boundaries of POR is a “brownout” event. Because of the way brownout is defined, power events that stay in the higher voltage range of brownout may be safe, and power events in the lower voltage range of brownout may be POR. Nonetheless, there exists a voltage range within the brownout region where the power event will cause the flash device to partially initialize to an indeterminate state, wherein the flash may not respond to commands.

- It is relatively easy to put the flash device into an unresponsive state via intentional brownout tests—this fact is the root cause of the power failure vulnerability, as well as the basis for testing that the power failure vulnerability is managed.
- It is more difficult to put the HyperRAM device into a nonresponsive state (focused brownout stress tests at Infineon have not been able to make any HyperRAM device enter an unresponsive state).

Power-On Reset Versus Brownout

This result is shown in [Figure 3](#) (presuming an indeterminate ending state can be achieved for RAM):

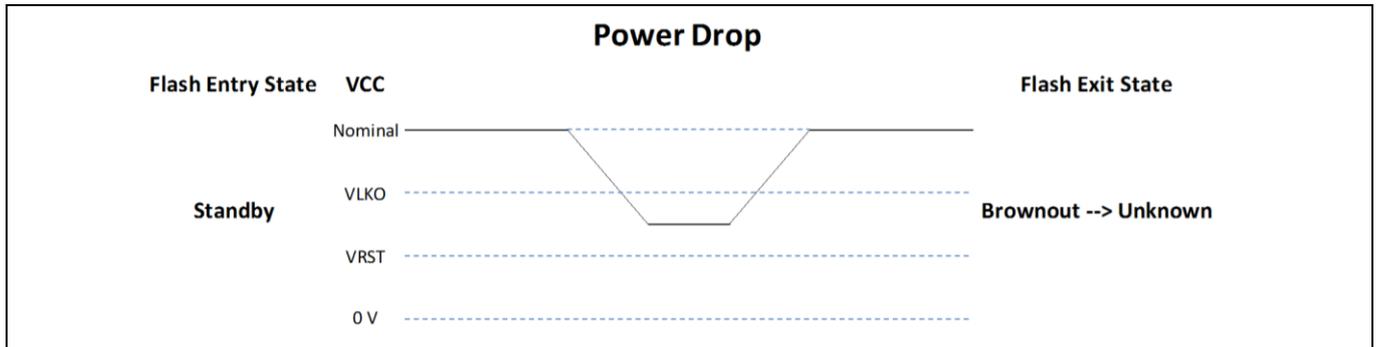


Figure 4 Flash/RAM Exit State after Brownout

One guaranteed recovery—called Recovery 1 in this application note—for an indeterminate exit state after brownout is datasheet-compliant POR. Recovery 1 applies to all flash/RAM devices within scope of this application note.

As shown next for the group of devices in [Table 2](#), there are additional recovery methods based on the Deep Power-Down Mode.

Deep Power-Down (DPD) Mode – Internal POR

5 Deep Power-Down (DPD) Mode – Internal POR

The DPD mode in HyperFlash and HyperRAM devices is a command-based method that can be used to induce “internal POR”. As shown in [Figure 5](#), the DPD logic provides for a system-controllable high-impedance between internal and external V_{CC} lines that can be used to disable all device circuits except the minimal set that is required to monitor CS# and RESET# for DPD Exit requests.

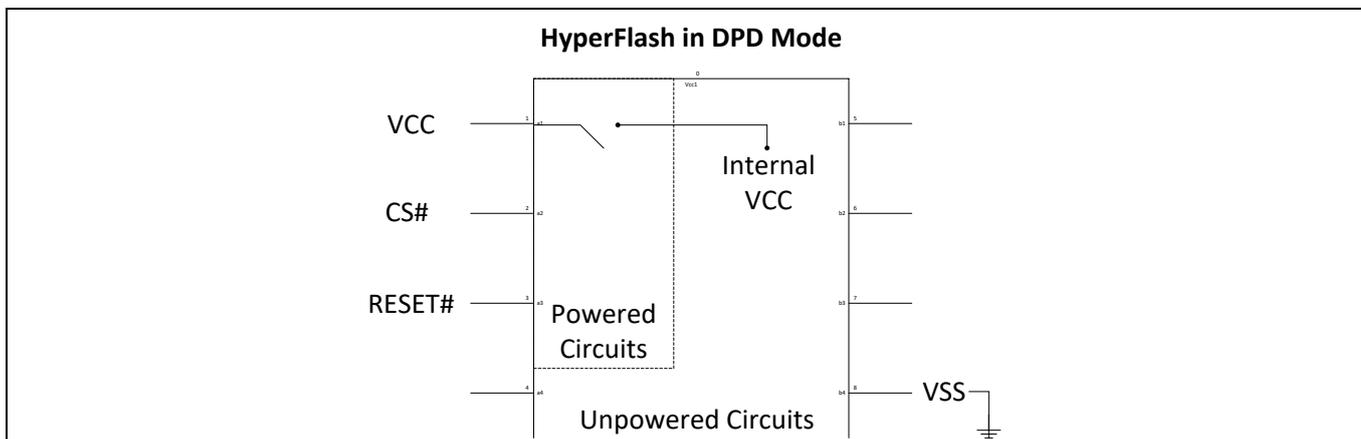


Figure 5 Schematic of the Internal/External VCC Control Logic for the DPD Feature

Once DPD mode is entered and the device is disconnected from the external V_{CC}, the charge drains to zero volts via ground. [Table 5](#) shows the DPD Entry and Exit times for the HyperFlash and HyperRAM devices with the DPD feature:

Table 5 DPD Entry and Exit Times for HyperFlash and HyperRAM

Device Family	Memory Type	Datasheet Revision	t _{DPDIN} (μs)	t _{DPDOUT} (μs)
S26KL-S	MirrorBit	001-99198 Rev *H	10	300
S26KS-S	MirrorBit	001-99198 Rev *H	10	300
S27KL-1	DRAM	001-97964 Rev *J	10	150
S27KS-1	DRAM	001-97964 Rev *J	10	150

Notice that the DPD Entry time, t_{DPDIN}, is quite fast at 10 μs. This is much faster than board-level power decay times which typically range from milliseconds to seconds.

Also, notice that the DPD Exit time, t_{DPDOUT}, is the same as t_{VCS} for POR. This is because the initialization process that takes place during DPD Exit is the same as the initialization process that takes place during POR.

Orderly Shutdown using DPD Mode

6 Orderly Shutdown using DPD Mode

For HyperFlash or HyperRAM devices in Standby mode at the nominal voltage, where the system has advance warning of an impending power drop, entering DPD mode before the power drop always enables datasheet-compliant POR after the power event; that is, this method completely eliminates the power failure vulnerability due to brownout.

Here is the method:

Given a warning of an impending power event:

1. Enter DPD Mode and wait t_{DPDIN} .
2. Wait for the power event to pass
3. After the power event, exit DPD mode and wait t_{DPDOUT} .

There are two cases to consider:

1. DPD mode survives the power event and internal POR is triggered by DPD Exit.
2. DPD mode is released by the power event, automatically initiating internal POR; any subsequent DPD Exit does not trigger another internal POR.

Case 1 is shown in **Figure 6**. In this case, the external V_{CC} never drops low enough to release the DPD mode, so internal V_{CC} stays at zero volts until the system sends the DPD Exit command. Note that the completion of DPD Exit (internal POR) is signaled via RSTO#.

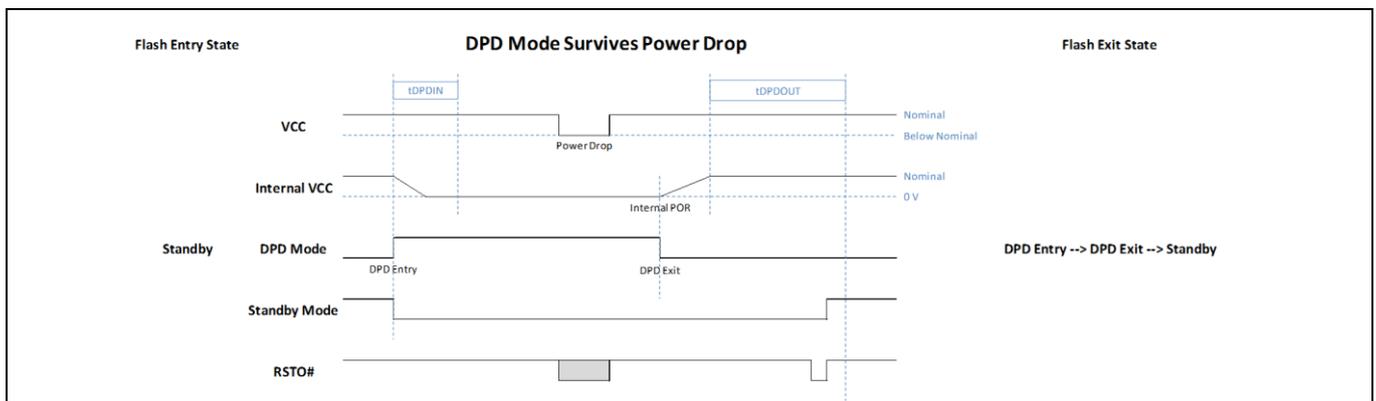


Figure 6 DPD Mode Survives the Power Event

Case 2 is shown in **Figure 7**. In this case, the external V_{CC} drops low enough to release the DPD Mode, at which point the internal V_{CC} rises from zero volts to external V_{CC} , which ultimately continues to rise to nominal. Again, the completion of the internal POR is signaled via RSTO#. It's fine if the system blindly runs the orderly shutdown method and sends the DPD Exit command/signal—this does not cause another internal POR because DPD mode is already released.

Orderly Shutdown using DPD Mode

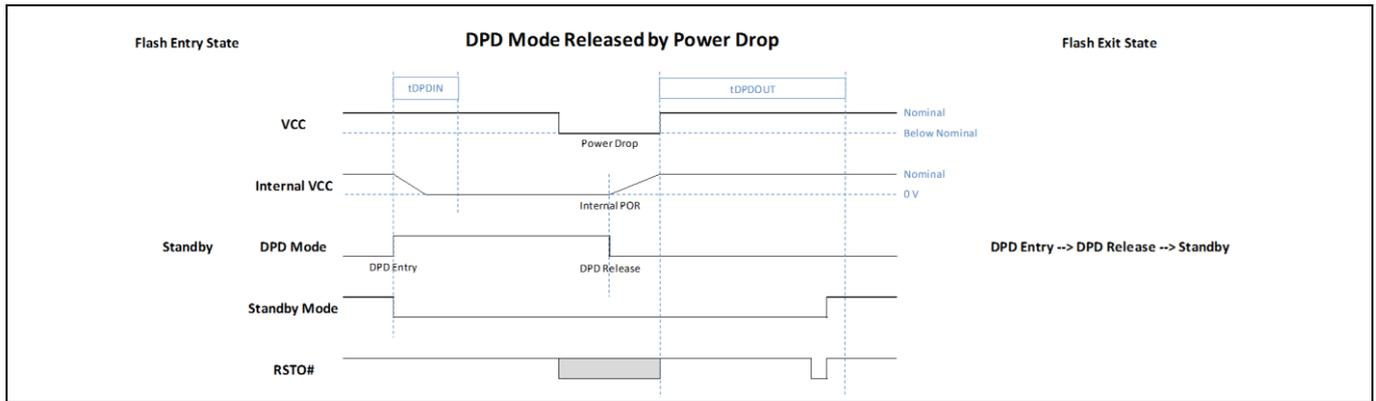


Figure 7 DPD Mode is released by the power event

This method transforms the three exit states enumerated in [Power-On Reset Versus Brownout](#), to only two exit cases, both of which are equivalent to POR. Therefore, the Orderly Shutdown method eliminates the power failure vulnerability due to brownout.

Recovery Using RESET# and DPD Mode

7 Recovery Using RESET# and DPD Mode

For HyperFlash or HyperRAM devices in standby mode at nominal voltage, where the system knows that a power event has happened, or where the system knows the flash (RAM) is unresponsive, asserting RESET# followed by DPD Entry and DPD Exit can recover the devices.

Here is the method for Recovery 2:

Given that a power event has happened, or that the system detects that the flash/RAM is unresponsive; while voltage is nominal:

1. Assert RESET# and wait t_{RPH} from the falling edge of RESET#.
 - This operation ensures that the command decoder can accept the DPD Entry command.
2. Enter DPD and wait t_{DPDIN} .
 - This operation causes an internal power drop to zero volts.
3. Exit DPD mode (normally assert RESET# and wait t_{RPH}) and wait t_{DPDOUT} .
 - This operation causes an internal POR from zero volts to nominal; RSTO# toggles when POR is complete.

There is only one case to show in **Figure 8**. In this figure, the power event has already happened and VCC is nominal; then steps #1, #2 and #3 of the recovery 2 method are performed, where RESET# is used as the DPD Exit method since it works for both flash and RAM (check the datasheets for alternate DPD Exit methods).

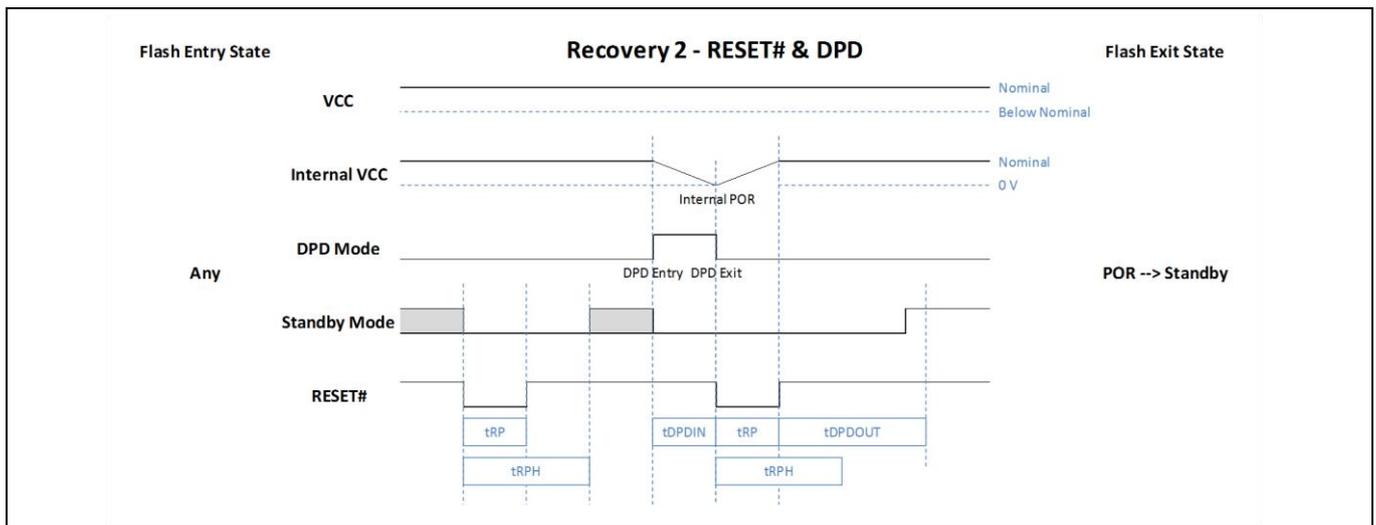


Figure 8 Recovery 2 by RESET# and DPD Entry/Exit

Flash Responsiveness Tests

8 Flash Responsiveness Tests

A flash responsiveness test tenders a flash command that gives a known response; a correct response constitutes “responsiveness” which can be taken as a proxy for correct initialization. Failure of such a test constitutes “non-responsiveness”, which calls for either Recovery 1 or Recovery 2.

Examples of responsiveness tests are:

- Enter CFI mode and read CFI data; if correct CFI data is returned the flash is responsive.
- Read a known data pattern from a specific location in flash; if the returned pattern matches the known pattern, the flash is responsive. All zero or all FFh patterns are not good choices for this test; the best case is a pattern of ~50% 1s and 50% 0s that spans multiple words.

This list is not exhaustive, so any command/response sequence that can be tested to prove responsiveness is fine.

Case 1: POR-Only

9 Case 1: POR-Only

Recovery 1—POR—may be used for any device within scope of this application note; but it must be used for all devices in [Table 1](#). When the system boots from internal flash, the best case is to ensure the system can induce POR in the external flash at will to recover from power events that may be brownouts, or to recover an unresponsive external flash. Datasheet-compliant POR must be managed correctly for any system that boots from external flash—there is no other option for this case.

Case 2: POR and DPD Mode; No RESET#

10 Case 2: POR and DPD Mode; No RESET#

For the HyperBus devices in [Table 2](#) that support the DPD mode, and where the system boots from internal flash: if the system does not have flash/RAM RESET#, then it must have the ability to initiate Recovery 1—POR—by software.

For the Orderly Shutdown method, the flash device may approach the impending power event in the standby state (the DPD Entry command can work) or the busy state (the DPD Entry command is ignored). Given that the busy state due to an in-progress programming command may take 100s of microseconds to complete, and that an in-progress erase may take milliseconds to seconds to complete, the preconditioning logic may run out of time to issue the DPD Entry command before the power event occurs. In this case, a brownout may leave the flash unresponsive after the power event, so without RESET# Recovery 2 is not possible, leaving system-induced Recovery 1 as the only option.

Case 3: DPD Mode and RESET#

11 Case 3: DPD Mode and RESET#

For the HyperBus devices in [Table 2](#) that support the DPD mode, and where the system boots from internal flash: if the system cannot initiate Recovery 1—POR—by software, then the system must have RESET# connected to initiate Recovery 2 to recover from possible brownout.

Case 4: HyperFlash/HyperRAM Multi-Chip Package

12 Case 4: HyperFlash/HyperRAM Multi-Chip Package

This multichip package (MCP) contains one flash die and one RAM die. To enable safe Infineon factory testing, the RESET# signal is connected to the flash die, but it is not connected to the RAM die. Thus, for systems that boot from internal flash, the RAM cannot be recovered by Recovery 2 since RESET# is not available. Therefore, the system must be able to induce Recovery 1—POR if RAM operation is to be power-fault tolerant.

Testing for Power Fault Tolerance

13 Testing for Power Fault Tolerance

The brownout case for in-scope flash devices is known to happen, so your test plan should include test cases for inducing unresponsive flash. The range for brownout conditions is expressed in voltage, but typically system software cannot control power events by voltage.

In this case, the proxy for the minimum voltage of the power event is the power-OFF time or voltage decay time; normally this is much easier to control by software. Therefore, the test case involves varying the power-OFF time in order to focus the minimum in the power-OFF/power-ON curve to happen within the brownout range. Not all focused power events will induce unresponsive flash, but some will; these are your test cases. Be sure to connect an oscilloscope so that power-OFF/power-ON curves for any failure can be proven to be datasheet-compliant or not.

The test plan involves two stages:

1. Demonstrating that your focused power events can induce unresponsive flash with a vulnerable system software design
2. Measuring the survival time for all software candidates that are designed to be invulnerable to power events.

Vulnerable software is expected to see very short survival times. As the power-failure tolerance of the design improves, survival time increases. For robust designs, the survival time is expected to exceed your tolerance for the cost of the test—at this point, you can declare success. There is no way for such a test to prove power failure tolerance by lack of a failure. However, the existence of one failure proves power failure vulnerability—your job is to eliminate these before releasing the product.

The brownout case for in-scope RAM devices has not been confirmed so far, so you can presume that system software that is shown to be power-fault tolerant for flash should also be power-fault tolerant for RAM.

Summary

14 Summary

For systems that boot from an external flash, the board must manage a datasheet-compliant POR every time to correctly initialize in-scope flash/RAM devices.

For systems that boot from internal flash, there are more options. However, the best case when the DPD feature is available is to ensure RESET# is connected to the flash/RAM device and is controllable by software; and to ensure software controlled POR is available.

Finally, focused power failure testing is the only way to confirm that you have eliminated all vulnerabilities to brownout.

References

References

- [1] [S29GL01GS, S29GL512S, S29GL256S, S29GL128S, 1 Gbit \(128 Mbyte\), 512 Mbit \(64 Mbyte\), 256 Mbit \(32 Mbyte\), 128 Mbit \(16 Mbyte\), 3.0V GL-S Flash Memory](#)
- [2] [S25FL512S, 512 Mbit \(64 Mbyte\) 3.0V SPI Flash Memory](#)
- [3] [S25FS128S, S25FS256S 1.8 V, Serial Peripheral Interface with Multi-I/O, MirrorBit® Non-Volatile Flash](#)
- [4] [3.0V GL-S Flash Memory, S29GL064S 64 Mbit Datasheet](#)
- [5] [S25FL256L/S25FL128L, 256 Mbit \(32 Mbyte\)/128 Mbit \(16 Mbyte\), 3.0 V FL-L Flash Memory](#)
- [6] [512 MBIT, 256 MBIT, 128 MBIT HyperFlash™ Family Datasheet](#)
- [7] [S27KL0641/S27KS0641/S70KL1281/S70KS1281, 3.0 V/1.8 V, 64 MBIT \(8 MBYTE\)/128 MBIT \(16 MBYTE\), HYPERRAM™ SELF-REFRESH DRAM](#)
- [8] [512 MBIT HYPERFLASH™ + 64 MBIT HYPERRAM™ 3V Multi-Chip Package \(MCP\) Datasheet](#)



Revision history

Revision history

Document version	Date of release	Description of changes
**	2017-08-30	New Spec
*A	2018-10-04	Sunset Review Fixed column 1 in Table 5 Fixed cross-references Updated Sales and Copyright information
*B	2021-05-06	Updated to Infineon template

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